BG952A-GL QuecOpen Hardware Design

LPWA Module Series

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The device could be used with a separation distance of 20cm to the human body.

Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or

metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-04-30	Arvin WU/ Ben JIANG	Creation of the document
1.0.0	2022-04-30	Arvin WU/ Ben JIANG	Preliminary

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1 Introduction

QuecOpen® is an application solution where the module acts as a main processor. With the development of communication technology and the ever-changing market demands, more and more customers have realized the advantages of QuecOpen® solution, especially the advantage in reducing product cost. With QuecOpen® solution, development flow for wireless applications and hardware designs will be simplified. Main features of QuecOpen® solution are listed below:

- Simplify the development of embedded applications, and shorten the product development cycle
- Simplify circuit design, and reduce product cost
- Decrease the size of terminal products
- Reduce power consumption
- Support firmware update via DFOTA, and provide a mechanism for APP binary image update
- Improve cost-performance ratio of products, and enhance product competitiveness

BG952A-GL QuecOpen® is based on the processor core is ARM Cortex-M4, the maximum frequency is up to 80 MHz, and the RAM size is 128K byte. You can use this module as the basis for developing QuecOpen® applications.

This document, describing BG952A-GL QuecOpen module and its air interface and hardware interfaces connected to your applications, provides you with the interface specifications, electrical and mechanical details, as well as other related information of the module.

With the application notes and user guides provided separately, you can easily use the module to design and set up mobile applications.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	When an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin name, AT command, or argument is under development and currently not supported, unless otherwise specified.

2 Product Concept

2.1. General Description

As an embedded IoT (LTE Cat M1, LTE Cat NB2 and EGPRS) wireless communication module, it provides data connectivity on LTE-FDD and GPRS/EGPRS networks, and supports half-duplex operation in LTE network. It also provides GNSS function to meet your specific application demands.

The module is based on an architecture in which WWAN (LTE) and GNSS Rx chains share certain hardware blocks. However, the module does not support concurrent operation of WWAN and GNSS. The solution adopted in the module is a form of coarse time-division multiplexing (TDM) between WWAN and GNSS Rx chains. Given the relaxed latency requirements of most LPWA applications, time-division sharing of resources can be made largely transparent to applications. For more details, see ***document [1]***.

BG952A-GL QuecOpen is an industrial-grade module for industrial and commercial applications only.

The following table shows the frequency bands of BG952A-GL QuecOpen module.

Table 2: Frequency Bands and GNSS Types of BG952A-GL QuecOpen

Supported Bands Supported Bands	LTE Bands Power Class	GNSS
Cat M1: LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/B20/B25/ B26/B27/B28/B66 Cat NB1/NB2* [1]: LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B17/B18/B19/B20/ B25/B28/B66	Power Class 3 (23 dBm ± 2.7 dB)	GPS, GLONASS.

BG952A-GL QuecOpen, an SMD type module, can be embedded into applications through its 102 LGA

[1] LTE Cat NB2* is backward compatible with LTE Cat NB1.

pins. With a compact profile of 23.6 mm × 19.9 mm × 2.2 mm, it can meet almost all requirements for M2M applications such as security, smart metering, tracking system, and wireless POS.

2.2. Key Features

Table 3: Key Features of BG952A-GL QuecOpen

Features	Details
Power Supply	● Supply voltage: 2.2–4.35 [1] V ● Typical supply voltage: 3.3 V
Transmitting Power	Class 3 (23 dBm ±2.7 dB) for LTE HD-FDD bands
LTE Features	● Supports 3GPP Rel-13/Rel-14* ● Supports LTE Cat M1, NB1/NB2* ● Supports 1.4 MHz RF bandwidth for LTE Cat M1 ● Supports 200 kHz RF bandwidth for LTE Cat NB1/NB2* ● Rel-13: Cat M1: 300 kbps (DL)/375 kbps (UL) Cat NB1: 27.2 kbps (DL)/62.5 kbps (UL) ● Rel-14*: Cat M1: 588 kbps (DL)/1119 kbps (UL) ● Cat NB2*: 127 kbps (DL)/158 kbps (UL)
Internet Protocol Features	● PPP/TCP/UDP/SSL/MQTT/FTP(S)/HTTP(S)/LwM2M/IPv4/IPv6/ TLS/DTLS/PING/CoAP/NITZ protocols ● Supports PAP and CHAP for PPP connections
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interface	Supports 1.8 V external (U)SIM/eSIM card only
USB Interface	● Compliant with USB 2.0 specifications ● Supports full speed mode only ● Used for AT command communication, data transmission, software debugging and firmware upgrade* ● USB serial driver: - Windows 7/8/8.1/10 ● Linux 2.6–5.15
UART Interfaces	**Main UART:** ● Used to connect with external peripherals of the module for customer configuration.

	● 115200 bps baud rate by default ● The default frame format is 8N1 (8 data bits, no parity, 1 stop bit)115200 bps baud rate by default **CLI UART [2]:** ● Used for firmware upgrade, software debugging, log output, GNSS data and NMEA sentence output ● Supports RTS and CTS hardware flow control ● Default frame format: 8N1 (8 data bits, no parity, 1 stop bit) ● Supports RTS and CTS hardware flow control
SPI Interfaces	Supports 3 SPI interfaces, 2 SPI master and 1 SPI slave, which can be multiplexed from GPIOs. **MCU SPIM0:** ● Supports master mode only ● Up to 25 MHz **MCU SPIM1:** ● Supports master mode only ● Up to 25 MHz **MCU SPIS:** ● Supports slave mode only ● Up to 25 MHz
I2C Interface	● Supports 2 channels of MCU I2C interfaces
GNSS	● GPS, GLONASS
AT Commands	● *3GPP TS 27.007* and *3GPP TS 27.005* AT commands ● Quectel enhanced AT commands
Network Indication	One NET_STATUS pin for network connectivity status indication
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● GNSS antenna interface (ANT_GNSS)
Physical Characteristics	● Dimensions: (23.6 ±0.2) mm × (19.9 ±0.2) mm × (2.2 ±0.2) mm ● Weight: approx. 2.15 g
Temperature Range	● Operating temperature range: -35 °C to +75 °C [2)] ● Extended temperature range: -40 °C to +85 °C [3)] ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	● CLI UART interface ● USB interface* ● DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

[2] BG952A-GL supports two CLI UART interfaces, more precisely, pin 27 (CLI_TXD1) and pin 28 (CLI_RXD1) are connected to pin 95 (CLI_TXD2) and pin 94 (CLI_RXD2) respectively inside the module.

1. [1] When the module starts up normally, to ensure full functionality, the minimum supply voltage should be higher than 2.2 V. For every VBAT transition/re-insertion from 0 V, VBAT slew rate < 25 mV/μs. To ensure normal module startup, pulling down PWRKEY to turn on the module after VBAT remains stable for 100 ms.
2. [2] Within the operating temperature range, the module meets 3GPP specifications.
3. [3] Within the extended temperature range, the module remains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

2.3. Functional Diagram

The following figures show the block diagram of the modules and illustrates the major functional parts.

- Power management
- Baseband
- Radio frequency
- Peripheral interfaces

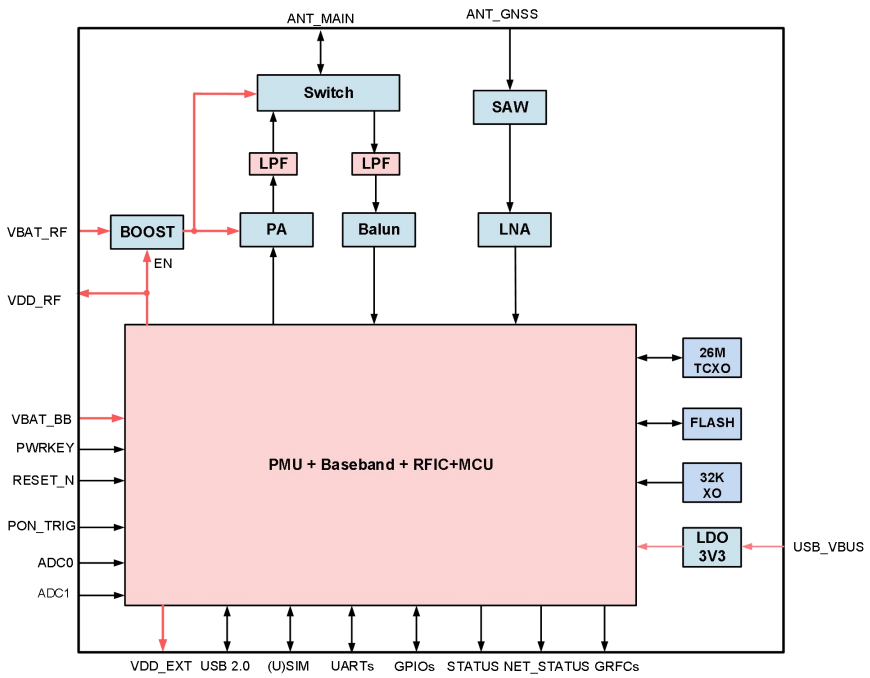


Figure 1: Functional Diagram of BG952A-GL

2.4. Evaluation Board

To facilitate application design with the module conveniently, Quectel supplies the evaluation board (LTE OPEN EVB), a USB to RS-232 converter cable, a micro-USB cable, an earphone, antennas and other peripherals to control or test the module. For more details, see ***document [2]***.

3 Application Interfaces

3.1. General Description

BG952A-GL QuecOpen is equipped with 102 LGA pins. The subsequent chapters provide detailed descriptions of the following interfaces:

- Power supply
- PON_TRIG interface
- (U)SIM interface
- USB interface
- UART interfaces
- PCM and I2C interfaces*
- SPI interfaces*
- ADC interfaces*
- Status indication interfaces
- GRFC interfaces

3.2. Pin Assignment

The following figure shows the pin assignment of the module.

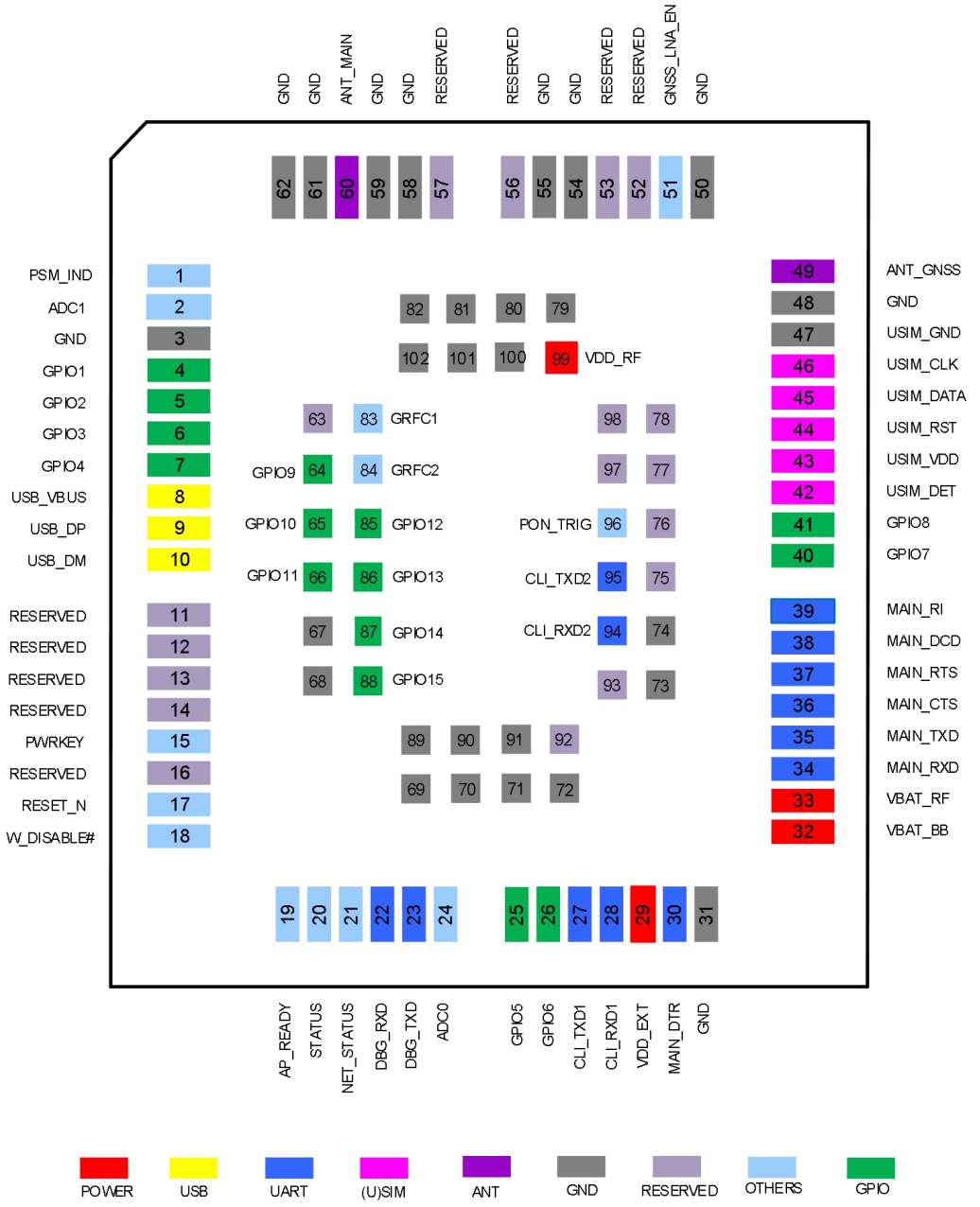


Figure 2: Pin Assignment (Top View)

NOTES

1. ADC input voltage must not exceed 1.8 V.
2. Keep all RESERVED pins and unused pins unconnected.
3. GND pins should be connected to ground in the design.
4. On BG952A-GL, pin 27 (CLI_TXD1) and pin 28 (CLI_RXD1) are connected to pin 95 (CLI_TXD2) and pin 94 (CLI_RXD2) respectively inside the module.
5. The LNA is integrated inside the module. It is not recommended to use an external LNA. It is strongly recommended to keep GNSS_LNA_EN (pin 51) and VDD_RF (pin 99) unconnected.

3.3. Pin Description

The following tables show the pin definition, alternate functions and GPIO pull up/down resistance of the module.

Table 4: Definition of I/O Parameters

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PI	Power Input
PO	Power Output
PD	Pull down
PU	Pull up

Table 5: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32	PI	Power supply for the module's baseband part	Vmax = 4.35 V Vmin = 2.2 V Vnom = 3.3 V	See NOTE 1.
VBAT_RF	33	PI	Power supply for the module's RF part		See NOTE 1
VDD_EXT	29	PO	Provide 1.8 V for external circuits	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. If unused, keep these pins open.
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102				
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turn on/off the module	V_{IL}max = 0.3 V V_{IH}min = 1.0 V	Internally pulled up with a 470 kΩ resistor.
RESET_N	17	DI	Reset the module	V_{IL}max = 0.3 V V_{IH}min = 1.3 V	
Status Indication Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PSM_IND	1	DO	Indicate the module's power saving mode	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	1.8 V power domain. If unused, keep these pins open. Can be configured as GPIOs.
STATUS	20	DO	Indicate the module's operation status		1.8 V power domain. If unused, keep these pins open.
NET_STATUS	21	DO	Indicate the module's network activity status		
PON_TRIG Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

PON_TRIG*	96	DI	Used to wake up the MCU in low power mode	V_{IL}min = -0.2 V V_{IL}max = 0.3 V V_{IH}min = 1 V V_{IH}max = 1.98 V	1.8 V power domain. If unused, keep these pins open.
USB Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	8	AI	USB connection detect	Vnom = 5.0 V	Typical 5.0 V
USB_DP	9	AIO	USB differential data (+)	Vmax = 4.1 V Vmin = -0.2 V	Compliant with USB 2.0 standard specification. Require differential impedance of 90 Ω.
USB_DM	10	AIO	USB differential data (-)		
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_DET	42	DI	(U)SIM card hot-plug detect	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep these pins open.
USIM_VDD	43	PO	(U)SIM card power supply	Vmax = 1.9 V Vmin = 1.7 V	Only 1.8 V (U)SIM card is supported.
USIM_RST	44	DO	(U)SIM card reset	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	1.8 V power domain.
USIM_DATA	45	DIO	(U)SIM card data	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V V_{OL}max = 0.36 V V_{OH}min = 1.44 V	
USIM_CLK	46	DO	(U)SIM card clock	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	
USIM_GND	47		Specified ground for (U)SIM card		
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_DTR	30	DI	Main UART data terminal ready	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep these pins open.
MAIN_RXD	34	DI	Main UART receive		

MAIN_TXD	35	DO	Main UART transmit	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	Can be configured as GPIOs.
MAIN_CTS	36	DO	DTE clear to send signal from DCE (Connect to DTE's CTS)		
MAIN_RTS	37	DI	DTE request to send signal from DCE (Connect to DTE's RTS)	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
MAIN_DCD	38	DO	Main UART data carrier detect	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	
MAIN_RI	39	DO	Main UART ring indication		
CLI UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CLI_RXD2	94	DI	CLI UART2 receive	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. It is recommended to reserve one set of test points.
CLI_TXD2	94	DO	CLI UART2 transmit	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	
CLI_TXD1	27	DO	CLI UART1 transmit		
CLI_RXD1	28	DI	CLI UART1 receive	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
Debug UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	22	DI	Debug UART receive	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep these pins open. Can be configured as GPIOs.
DBG_TXD	23	DO	Debug UART transmit	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

ADC1	2	AI	General-purpose ADC interface	Voltage range: 0.1–1.8 V	If unused, keep these pins open. Can be configured as GPIOs.
ADC0	24	AI	General-purpose ADC interface	Voltage range: 0.1–1.8 V	
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
W_DISABLE#	18	DI	Airplane mode control	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Pulled up by default. When this pin is at low level, the module enters airplane mode. If this pin is unused, keep it open. Can be configured as GPIOs.
AP_READY*	19	DI	Application processor ready		1.8 V power domain. If this pin is unused, keep it open. Can be configured as GPIOs.
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	60	AIO	Main antenna interface	-	50 Ω impedance.
ANT_GNSS	49	AI	GNSS antenna interface	-	50 Ω impedance. If unused, keep this pin unconnected.
External GNSS LNA Interface [3]					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GNSS_LNA_EN	51	DO	External GNSS LNA enable	V_{OL}max = 0.38 V V_{OH}min = 1.36 V	1.8 V power domain. If unused, keep this pin open.
VDD_RF	99	PO	Can be used for external GNSS LNA.	Vnom = 1.9 V I_{OUT}max = 50 mA	If unused, keep this pin open.

[3] The LNA is integrated inside the module. It is recommended to use an external LNA. It is strongly recommended to keep GNSS_LNA_EN (pin 51) and VDD_RF (pin 99) unconnected.

			LNA power supply		
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	11–14, 16, 52,53, 56,57, 63, 75–78, 92,93,97,98				Keep these pins open.
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	4	DIO	General-purpose input/output	V_{OL}max = 0.36 V V_{OH}min = 1.44 V V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep these pins open.
GPIO2	5	DIO			
GPIO3	6	DIO			
GPIO4	7	DIO			
GPIO5	25	DIO			
GPIO6	26	DIO			
GPIO7	40	DIO			
GPIO8	41	DIO			
GPIO9	64	DIO			
GPIO10	65	DIO			
GPIO11	66	DIO			
GPIO12	85	DIO			
GPIO13	86	DIO			
GPIO14	87	DIO			
GPIO15	88	DIO			
GRFC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	83	DO	Generic RF controller	V_{OL}max = 0.38 V V_{OH}min = 1.36 V	1.8 V power domain. If unused, keep this pin unconnected.
GRFC2	84	DO			

NOTES

1. [1)] When the module starts up normally, to ensure full functionality, the minimum supply voltage should be higher than 2.2 V. For every VBAT transition/re-insertion from 0 V, VBAT slew rate < 25 mV/μs. To ensure normal module startup, pulling down PWRKEY to turn on the module after VBAT remains stable for 100 ms.
2. On BG950A-GL/BG951A-GL, PWRKEY is pulled up to an internal voltage of the baseband chipset inside the module, and the minimum high-level output voltage is 1.0 V.
3. Keep all RESERVED pins and unused pins unconnected.
4. Connect GND to ground in the design.

3.4. Pins Multiplexing

See ***document [7]*** for details about pin multiplexing of the module.

3.5. Operating Modes

The operating mode of the module is combined with internal Modem Application Processor (MAP) mode and MCU mode.

Table 6: Overview of MAP Operating Modes

Mode	Details	
Normal Operation	Connected	The module remains registered on the network and is ready to send and receive data. In this mode, the software is active.
	Idle	The module is connected to the network. Its current consumption varies with the network setting and data transfer rate.
Extended Idle Mode DRX (e-I-DRX)	The module and the network may negotiate over non-access stratum signaling the use of e-I-DRX for reducing power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.	
Airplane Mode	In this mode where the RF function is invalid.	
Minimum Functionality Mode	In this mode, both RF function and (U)SIM card are invalid.	

Sleep Mode	The module remains the ability to receive paging message, SMS and TCP/UDP data from the network normally. In this mode, the current consumption is reduced to a low level.
Power OFF Mode	The module's power supply is shut down by its power management unit. In this mode, the software is inactive, the serial interfaces are inaccessible, while the operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.
Power Saving Mode (PSM)	PSM is similar to power-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections. The current consumption is reduced to a minimized level.
Recovery Mode	The module can burn firmware with an empty serial flash, or recover from firmware malfunction. For more details, see ***Chapter 3.5.1.***

NOTE

In e-I-DRX mode, it is recommended to use the main UART interface for data communication, as the use of USB interface will increase power consumption.

Table 7: Overview of MCU Operating Modes

Mode	Details	
Normal	Run	MCU performs user tasks.
Stop	Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers.	
Standby	The standby mode can achieve the lowest power consumption with some data retention (up to 128 KB). and I/Os are latched.	
Shutdown	The shutdown mode can achieve the lowest power consumption. The internal regulator is switched off. The RTC can remain active. SRAM, registers and retention data are lost, except for registers in the RTC domain.	

3.5.1. Recovery Mode

BG952A-GL QuecOpen provides the recovery mode for firmware upgrade in emergency cases. Recovery mode can force the module to boot via CLI UART interface for firmware upgrade.

The following preconditions can set the module into recovery mode.

1. Short-circuit CLI_TXD2 and CLI_RXD2 pins.
2. Drive PWRKEY low to turn on the module. In this case the module will enter recovery mode.
3. After the module enters recovery mode successfully, disconnect the connection between CLI_TXD2 and CLI_RXD2.

4. Upgrade firmware via CLI UART interface.

NOTE

1. In recovery mode, pin 25 functions as CLI_RTS and pin 26 functions as CLI_CTS, while in other modes they are GPIO pins.
2. Since the baud rate of the serial port required to download firmware to the baseband chip is 3 Mbps, the flow control pins of the CLI serial port need to be reserved. Otherwise, you can only download with a 921600 baud rate, which is very slow. It is recommended to reserve the test points of the CLI UART interface, including pin 25, pin 26, pin 94 and pin 95, and keep pin 94 close to pin 95.
3. Ensure that VBAT remains stable for at least 100 ms before pulling down PWRKEY.

3.6. Power Saving Mode*

With different power modes configured in MAP and MCU, power management processor (PMP) selects the proper system modes accordingly. The table below shows the maximum device sleep level per different MAP-MCU power mode combinations.

Table 8: Maximum Device Sleep Level of MAP-MCU Mode Combinations

-		MCU			
		Nomal	Stop	Standby	Shutdown
MAP	Normal	MCU active	MAP normal	MAP sleep	MAP sleep
	Sleep	MCU active	MAP normal	MAP sleep	MAP sleep
	PSM	MCU active	MAP normal	MAP sleep	MAP PSM

3.7. Power Supply

3.7.1. Power Supply Pins

The module provides two VBAT pins for connection with an external power supply. The following table shows the details of VBAT_BB and VBAT_RF pins and ground pins.

Table 9: Power Supply Pin Definition

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_BB	32	Power supply for the module's baseband part	2.2	3.3	4.35	V
VBAT_RF	33	Power supply for the module's RF part	2.2	3.3	4.35	V
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102		-	-	-	-

NOTE

For every VBAT transition/re-insertion from 0 V, VBAT slew rate < 25 mV/μs. After the module starts up normally, in order to ensure full functionality, the minimum supply voltage should be higher than 2.2 V.

3.7.2. Voltage Stability Requirements

The power supply range of the module is from 2.2 V to 4.35 V. Make sure that the input voltage never drops below 2.2 V.

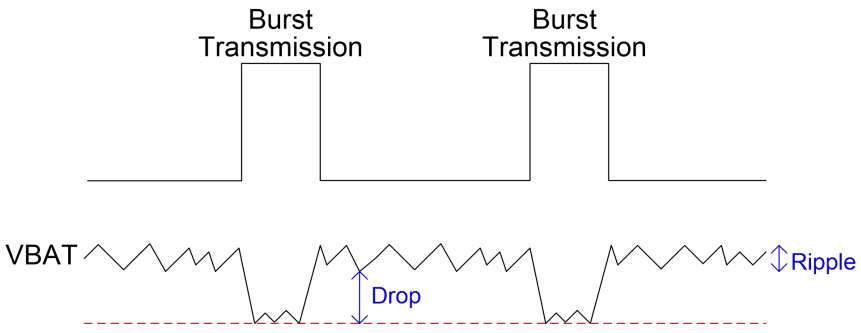


Figure 3: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100 μF with low ESR should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be reserved due to its low ESR. It is

recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 0.6 mm, and the width of VBAT_RF trace should be no less than 2 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to get a stable power source, it is suggested to use two TVSs with low leakage current and suitable reverse stand-off voltage, and also it is recommended to place them as close to the VBAT pins as possible. The following figure shows the star structure of the power supply.

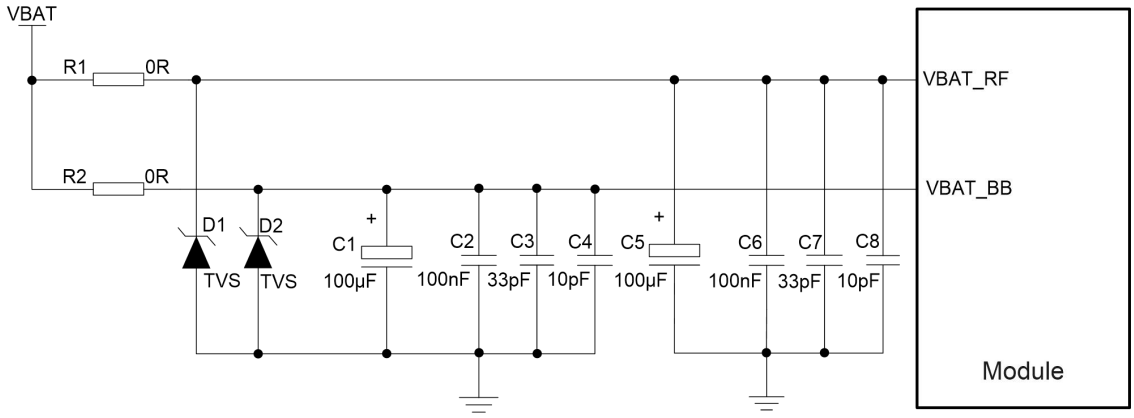


Figure 4: Star Structure of the Power Supply

Power design for a module is critical to its performance. The power supply of the module should be able to provide a sufficient current of at least 0.8 A, so it is recommended to select a DC-DC converter chip or an LDO chip with ultra-low leakage current and current output of at least 1.0 A for the power supply design.

3.7.3. Power Supply Monitoring

AT+CBC can be used to monitor the VBAT_BB voltage value. For more details, see ***document [3]***.

3.8. Turn on

3.8.1. Turn on Module with PWRKEY

The following table shows the pin definition of PWRKEY.

Table 10: PWRKEY Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turn on/off the module	Internally pulled up with a 470 kΩ resistor.

When the module is in power-off mode, it can be turned on by driving PWRKEY low for 500–1000 ms. It is recommended to use an auto power-on circuit to control PWRKEY, as shown below.

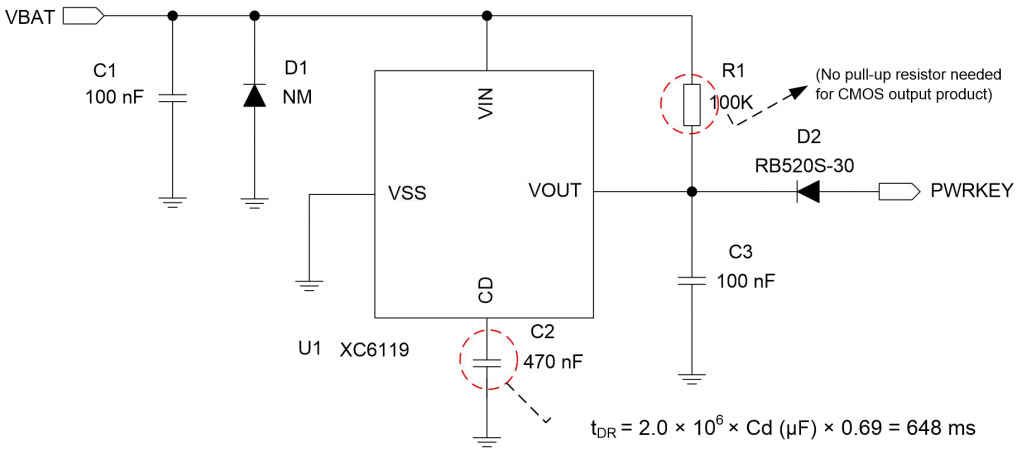


Figure 5: Auto Power-on Circuit

Visit https://www.torexsemi.com for more information on the XC6119 voltage detector.

NOTE

With the above circuit, the module automatically powers on when the power supply is switched on, and keeps PWRKEY at a high level after successful power-on. With this design, if you intend to power on the module again after you power it off with an API or AT command, switch off the power supply of the module and remain in switch-off state for at least 200 ms before you switch on the power supply to enable automatic power-on of the module.

If the device has an extra MCU, it is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

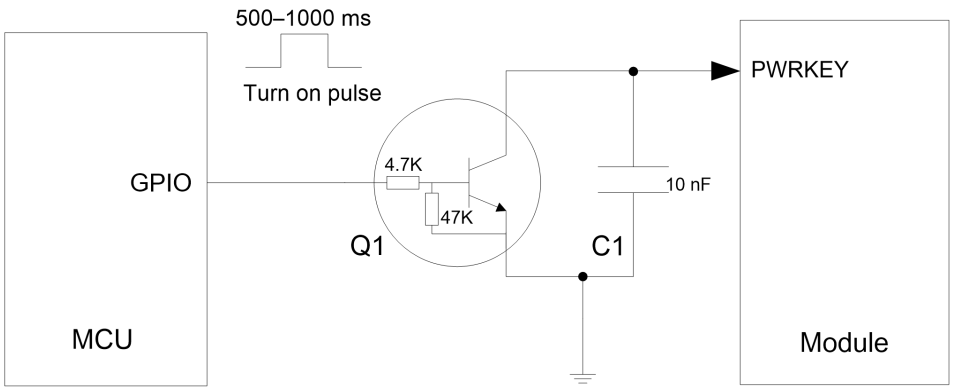


Figure 6: Turn on the Module with a Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the button, electrostatic strike may generate from the finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

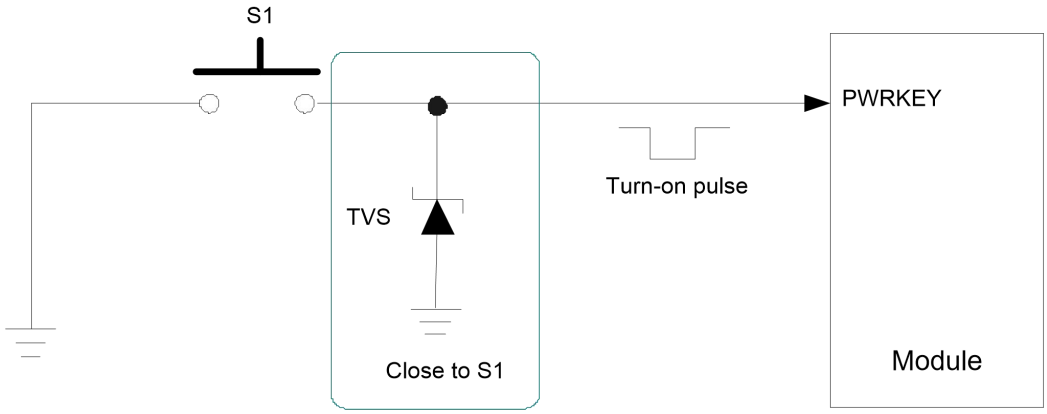


Figure 7: Turn on the Module with a Button

The power-up scenario is illustrated in the following figure.

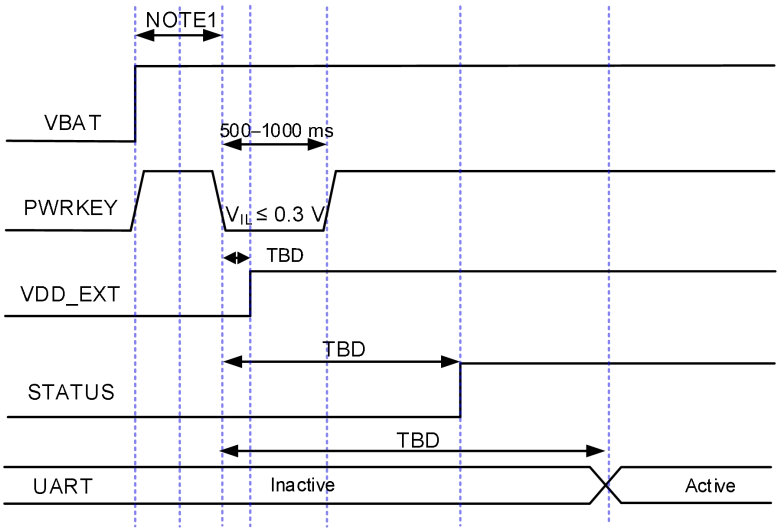


Figure 8: Power-up Timing

NOTES

Ensure that VBAT is stable before pulling down PWRKEY and keep the interval no less than 100 ms.

3.8.2. Turn off Module

After the module is turned off or enters PSM, do not pull up any I/O pin of the module. Otherwise, the module will have additional power consumption and may have damaged pins.

3.8.2.1. Turn off Module with PWRKEY

When the module is powered on, drive PWRKEY low for 650–1500 ms before you release it, and then module will execute power-down procedure.

The power-down timing is illustrated in the following figure.

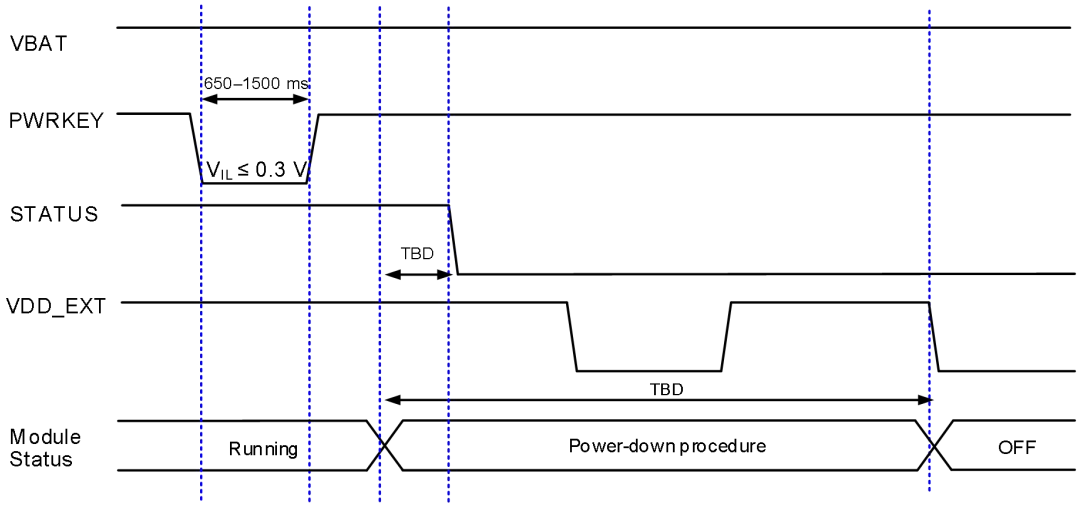


Figure 9: Power-down Timing (PWRKEY)

3.9. Reset the Module

The module can be reset by driving RESET_N low for at least 100 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 11: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description
RESET_N	45	DI	Reset the module. Internally pulled up with a 470 kΩ resistor.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control RESET_N.

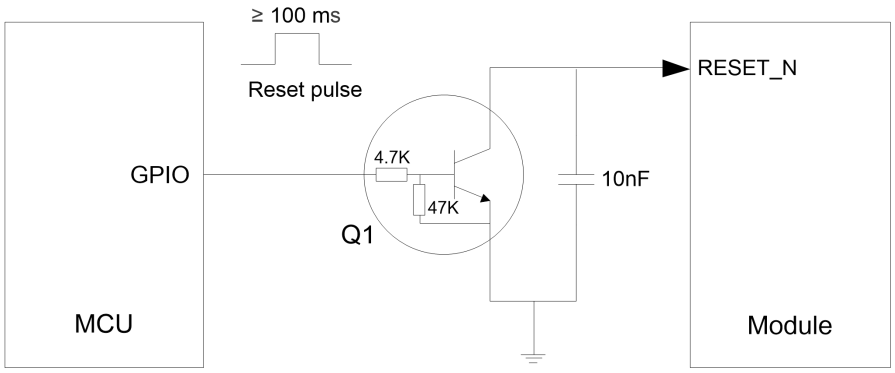


Figure 10: Reference Circuit of RESET_N with a Driving Circuit

Another way to control the RESET_N is by using a button directly.

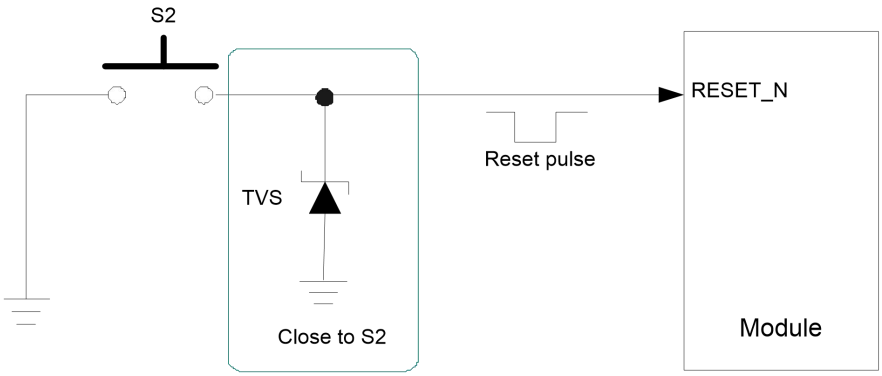


Figure 11: Reference Circuit of RESET_N with a Button

The reset scenario is illustrated in the following figure.

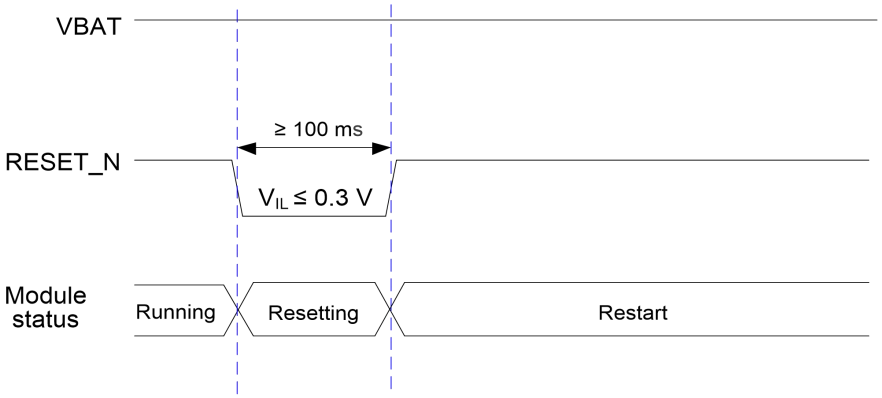


Figure 12: Reset Timing

NOTE

Make sure that there is no large capacitance on RESET_N.

3.10. PON_TRIG Interface

BG952A-GL QuecOpen provides one PON_TRIG pin. Drive PON_TRIG is used to wake up the internal MCU. PON_TRIG is not pulled up/down internally by default.

Table 12: Pin Definition of PON_TRIG Interface

Pin Name	Pin No.	I/O	Description	Comment
PON_TRIG	96	DI	Used to wake up the MCU in low power mode	1.8 V power domain. Pulled down by default.

PON_TRIG is used to wake up the internal MCU. If the low power consumption mode of the MCU is not required, it is strongly recommended to reserve a PON_TRIG test point. A reference design is shown in the following figure.

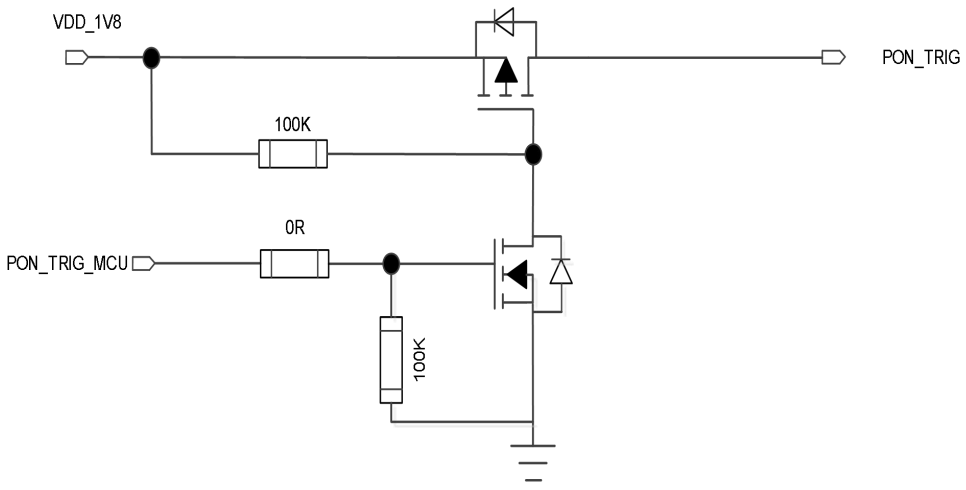


Figure 13: Reference Circuit of PON_TRIG

NOTE

VDD_1V8 is powered by an external LDO.

3.11. (U)SIM Interface

The module supports 1.8 V (U)SIM card only. The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements.

Table 13: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_DET	42	DI	(U)SIM card hot-plug detect	1.8 V power domain.
USIM_VDD	43	PO	(U)SIM card power supply	Only 1.8 V (U)SIM card is supported.
USIM_RST	44	DO	(U)SIM card reset	1.8 V power domain.
USIM_DATA	45	DIO	(U)SIM card data	1.8 V power domain.
USIM_CLK	46	DO	(U)SIM card clock	1.8 V power domain.
USIM_GND	47		Specified ground for (U)SIM card	

The module supports (U)SIM card hot-plug via USIM_DET, and both high and low level detections are supported. The function is disabled by default, and see **AT+QSIMDET** in ***document [3]*** for more details.

The following figure shows a reference design of (U)SIM interface with an 8-pin (U)SIM card connector.

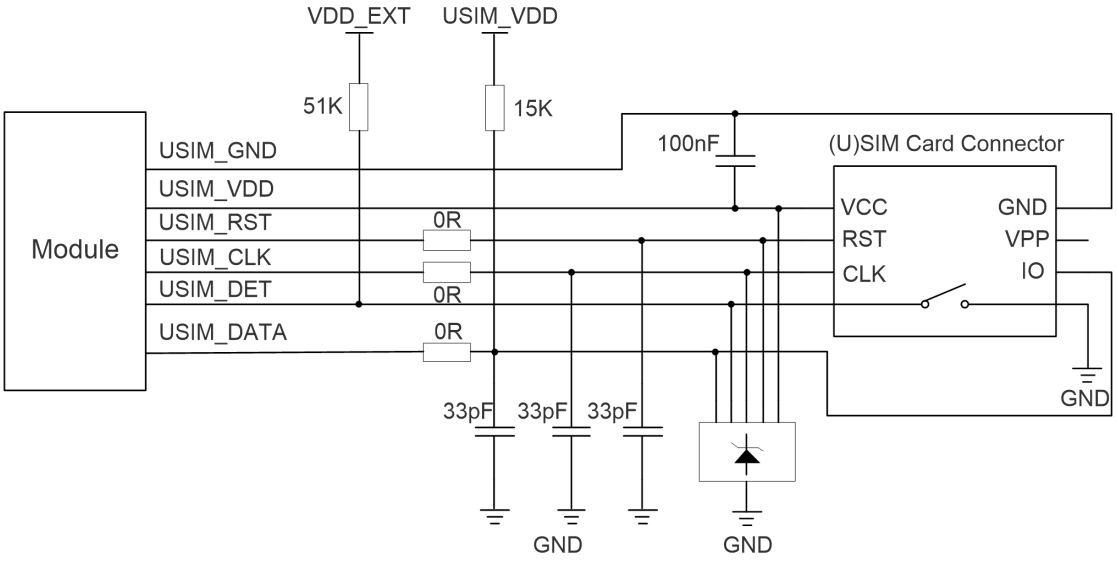


Figure 14: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

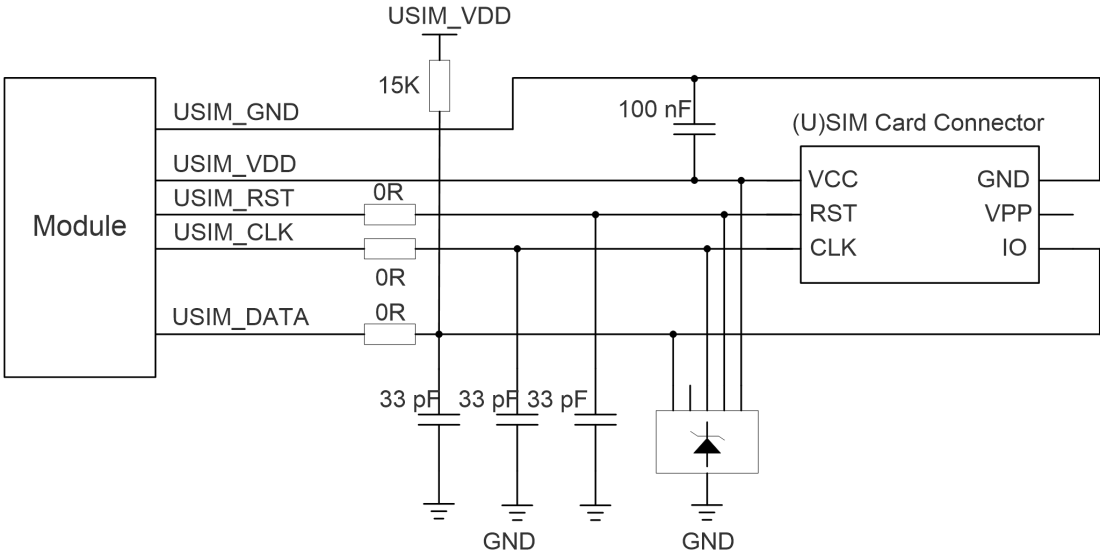


Figure 15: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in (U)SIM circuit design:

- Keep the placement of (U)SIM card connector as close to the module as possible. Keep the trace length less than 200 mm.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground trace between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5 mm to maintain the same electric potential. Make sure the bypass capacitor between USIM_VDD and USIM_GND is less than 1 μF, and place it as close to (U)SIM card connector as possible. If the system ground plane is complete, USIM_GND can be connected to the system ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground. USIM_RST should also be surrounded with ground.
- To offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 15 pF. to facilitate debugging, it is recommended to reserve series resistors for the (U)SIM signals of the module. The 33 pF capacitors are used for filtering interference of EGSM900. Note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

3.12. USB Interface*

BG952A-GL QuecOpen provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports full speed mode only.

The following table shows the pin definition of USB interface.

Table 14: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	Typical 5.0 V
USB_DP	9	AIO	USB differential data (+)	Require differential impedance of 90 Ω
USB_DM	10	AIO	USB differential data (-)	

For more details about USB 2.0 specification, visit http://www.usb.org/home.

It is recommended to reserve test points for debugging and firmware upgrading* in your designs.

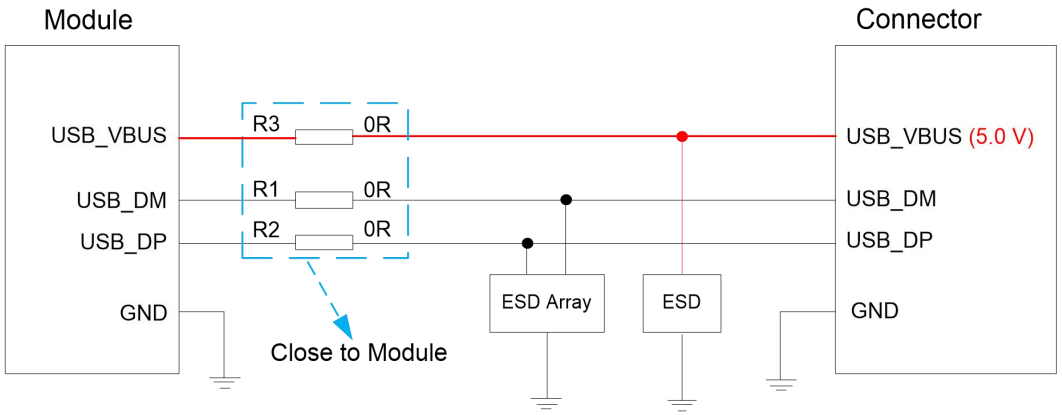


Figure 16: Reference Design of USB Interface

To ensure USB data signal integrity, if possible, reserve a 0 Ω resistor on USB_DP and USB_DM traces, respectively. Resistors R1 and R2 should be placed close to the module and to each other. The extra trace stubs must be as short as possible.

To meet USB 2.0 specification, comply with the following principles while designing the USB interface.

- It is important to route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.

- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection device might cause influences on USB data lines, so pay attention to the selection of the device. Typically, the stray capacitance should be less than 2 pF.
- Keep the ESD protection devices as close to the USB connector as possible.

NOTE

1. After the module is turned off or enters PSM, do not pull up any USB interface pin lest it cause additional power consumption and potentially damage pins on the module.
2. When using the UMTS&LTE EVB board to test the USB interface function of the module, please refer to ***document [8].***

3.13. UART Interfaces

The module provides two UART interfaces: main UART and CLI UART interfacethe. The following are the features of the UART interfaces.

- The main UART interface is used to communicate with peripherals, which can be multiplexed as GPIOs.
- The CLI UART interface supports 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 and 3000000 bps baud rates, and the default is 115200 bps. It is used for firmware upgrade, software debugging, log and GNSS NMEA sentences output, and supports RTS and CTS hardware flow control. The default frame format is 8N1 (8 data bits, no parity, 1 stop bit).

The GPIO pins configuration is determined by compilation time and it cannot be changed dynamically. The following tables show the pin definition of the four UART interfaces.

Table 15: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_DTR	30	DI	Main UART data terminal ready	1.8 V power domain. If these pins are unused, keep them open. Can be configured as GPIOs.
MAIN_RXD	34	DI	Main UART receive	
MAIN_TXD	35	DO	Main UART transmit	
MAIN_CTS	36	DO	Main UART clear to send	
MAIN_RTS	37	DI	Main UART request to send	
MAIN_DCD	38	DO	Main UART data carrier detect	

MAIN_RI*	39	DO	Main UART ring indication

Table 16: Pin Definition of CLI UART Interface

Pin Name	Pin No.	I/O	Description	Comment
CLI_TXD2	95	DO	CLI UART2 transmission	1.8 V power domain. If unused, keep them open.
CLI_RXD2	94	DI	CLI UART2 reception	
CLI_TXD1	27	DO	CLI UART1 transmission	1.8 V power domain. If unused, keep them open.
CLI_RXD1	28	DI	CLI UART1 reception	

The module provides 1.8 V UART interfaces. A voltage-level translator should be used if your application is equipped with a 3.3 V UART interface. It is recommended to use a level conversion chip without internal pull-up. The voltage-level translator TXB0108PWR provided by *Texas Instruments* is recommended. The following figure shows a reference design of the main UART interface:

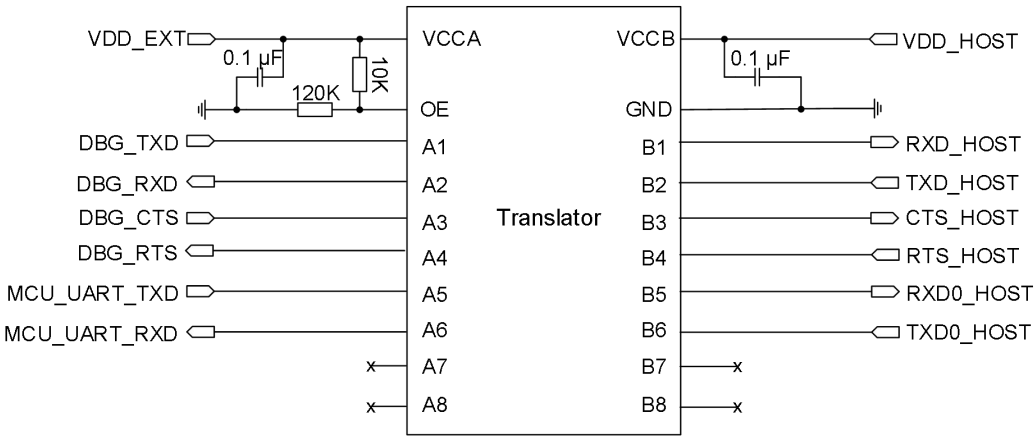


Figure 17: Main UART Reference Design (Translator Chip)

Visit http://www.ti.com for more information on the translator chip.

Another example with transistor circuit is shown as below. For the design of circuits in dotted lines, refer to that of circuits in solid lines, but pay attention to the direction of connection.

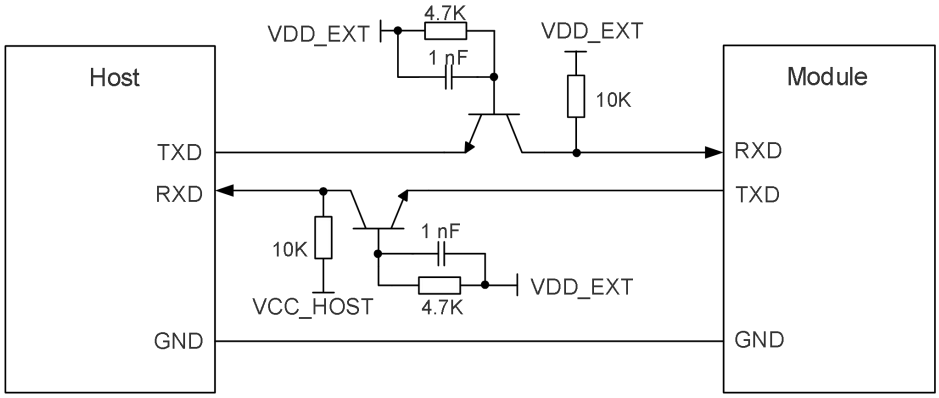


Figure 18: Main UART Reference Design (Transistor Circuit)

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. The UART interface should be disconnected in PSM and power off modes. Otherwise, the module will have additional power consumption and may have damaged pins.
3. It is recommended to use a level-shifting chip without internal pull-up, such as TXB0108PWR, for voltage level translation.

3.14. I2C Interface*

The module provides two Inter-Integrated Circuit (I2C) interface for data communication. The interface supports fast-mode plus and master mode only.

The pins of I2C interface are open drain and are multiplexed from GPIOs. The pull-up resistors should be provided externally.

NOTES

The pins of I2C interface are open drain that must be pulled up to 1.8 V. The pull-up resistors should be provided externally.

The following figure shows a reference design of I2C interface with an external I2C interface sensor.

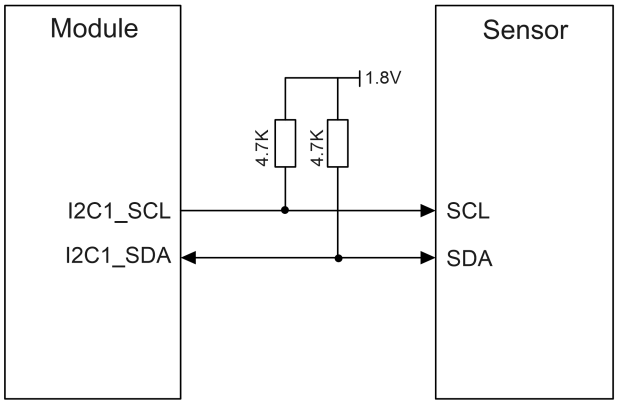


Figure 19: Reference Design of I2C Interface with an External I2C Interface Sensor

3.15. SPI Interfaces*

The module provides three SPI interfaces. 2 SPI interfaces for master mode, 1 SPI interface for slave mode. The SPI interfaces function is multiplexed from GPIOs.

- SPIM0 and SPIM1 interfaces in master mode up to 25 MHz.
- SPIS interface supports slave mode only, up to 25 MHz.

NOTE

The power domain of the SPI interface is 1.8 V. A voltage-level translator should be used between the module and the host if your application is equipped with a 3.3 V processor or device interface.

3.16. ADC Interfaces*

The module provides two analog-to-digital converter (ADC) interfaces by default. The other two ADC interfaces can be multiplexed from GPIOs.

To improve the accuracy of ADC voltage values, the traces of ADC should be surrounded with ground.

Table 17: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment

ADC0	24	AI	General-purpose ADC interface	If unused, keep these pins open. Can be configured as GPIOs.
ADC1	2	AI	General-purpose ADC interface	

The following table describes characteristics of ADC interfaces.

Table 18: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
Voltage Range	0	-	1.8	V
Resolution	6	-	12	bit

NOTES

1. ADC input voltage must not exceed 1.8 V.
2. It is prohibited to supply any voltage to ADC pin when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application, and the divider resistor accuracy should be no less than 1 %.
4. After the module is turned off or enters PSM, do not pull up any pin of ADC interfaces. Otherwise the module will have additional power consumption and may have damaged pins.

3.17. Network Status Indication

The module provides one network status indication pin: NET_STATUS. The pin is used to drive a network status indication LED. The following tables describe the pin definition and logic level changes of NET_STATUS in different network activity status.

Table 19: Pin Definition of NET_STATUS

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	21	DO	Indicate the module's network activity status	1.8 V power domain. If the pin is unused, keep it open.

Table 20: Operating Status of NET_STATUS

Pin Name	Indicator Status (Logic Level Changes)	Network Status
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transfer is ongoing
	Always High	Voice calling

A reference design is shown in the following figure.

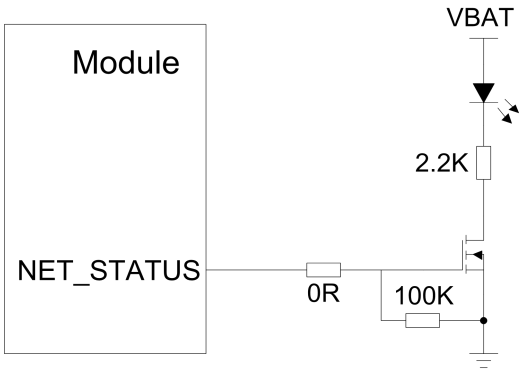


Figure 20: Reference Design of NET_STATUS

3.18. STATUS

The STATUS pin is used to indicate the operation status of the module. It outputs high level when the module powers on.

Table 21: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module's operation status	1.8 V power domain

The following figure shows a reference circuit of STATUS.

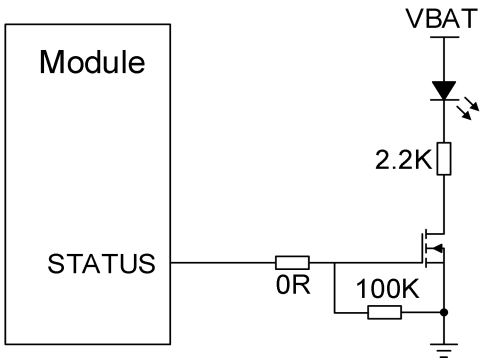


Figure 21: Reference Design of STATUS

3.19. GRFC Interfaces*

The module provides two generic RF control interfaces for the control of external antenna tuners.

Table 22: Pin Definition of GRFC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GRFC1	83	DO	Generic RF controller	1.8 V power domain. If unused, keep these pins open.
GRFC2	84	DO	Generic RF controller	

Table 23: Truth Table of GRFC Interfaces

GRFC1 Level	GRFC2 Level	Frequency Range (MHz)	Band
Low	Low	880–2200	B1, B2, B3, B4, B8, B25, B66
Low	High	791–894	B5, B18, B19, B20, B26, B27
High	Low	698–803	B12, B13, B17, B28

4 GNSS Receiver

4.1. General Description

BG952A-GL QuecOpen supports GPS and GLONASS satellite systems using dedicated hardware accelerators in a power and cost-efficient manner.

The module supports standard *NMEA-0183* protocol, and outputs GNSS NMEA sentences at 1 Hz data update rate via CLI UART interface by default.

By default, BG772A-GL QuecOpen GNSS engine is switched off. It has to be switched on via AT command. The module does not support concurrent operation of WWAN and GNSS. For more details about GNSS engine technology and configurations, see ***document [1].***

4.2. GNSS Performance

Table 24: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-145	dBm
	Reacquisition	Autonomous	-153	dBm
	Tracking	Autonomous	-158	dBm
TTFF (GNSS)	Cold start @ open sky	Autonomous	29.42	s
		XTRA enabled	TBD	s
	Warm start @ open sky	Autonomous	28.38	s
		XTRA enabled	TBD	s
	Hot start @ open sky	Autonomous	1.07	s

		XTRA enabled	TBD	s
Accuracy (GNSS)	CEP-50	Autonomous @ open sky	1.41	m

NOTES

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Cold start sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in application designs.

- Maximize the distance between the GNSS antenna and the main antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module, display connector and SD card should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50 Ω characteristic impedance for ANT_GNSS trace.

See ***Chapter 5*** for GNSS antenna reference design and antenna installation information.

5 Antenna Interfaces

The module includes a main antenna interface and a GNSS antenna interface. The impedance of antenna ports is 50 Ω.

5.1. Main Antenna Interface

5.1.1. Pin Definition

The pin definition of the main antenna interface is shown below.

Table 25: Pin Definition of the Main Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance

5.1.2. Operating Frequency

Table 26: BG952A-GL QuecOpen Operating Frequency

3GPP Band	Transmit	Receive	Unit
LTE HD-FDD B1	1920–1980	2110–2170	MHz
LTE HD-FDD B2	1850–1910	1930–1990	MHz
LTE HD-FDD B3	1710–1785	1805–1880	MHz
LTE HD-FDD B4	1710–1755	2110–2155	MHz
LTE HD-FDD B5	824–849	869–894	MHz
LTE HD-FDD B8	880–915	925–960	MHz
LTE HD-FDD B12	699–716	729–746	MHz

LTE HD-FDD B13	777–787	746–756	MHz
LTE HD-FDD B17 [4]	704–716	734–746	MHz
LTE HD-FDD B18	815–830	860–875	MHz
LTE HD-FDD B19	830–845	875–890	MHz
LTE HD-FDD B20	832–862	791–821	MHz
LTE HD-FDD B25	1850–1915	1930–1995	MHz
LTE HD-FDD B26 [5]	814–849	859–894	MHz
LTE HD-FDD B27 [5]	807–824	852–869	MHz
LTE HD-FDD B28	703–748	758–803	MHz
LTE HD-FDD B66	1710–1780	2110–2180	MHz

5.1.3. Reference Design

A reference design of main antenna interface is shown as below. It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (R1/C1/C2) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

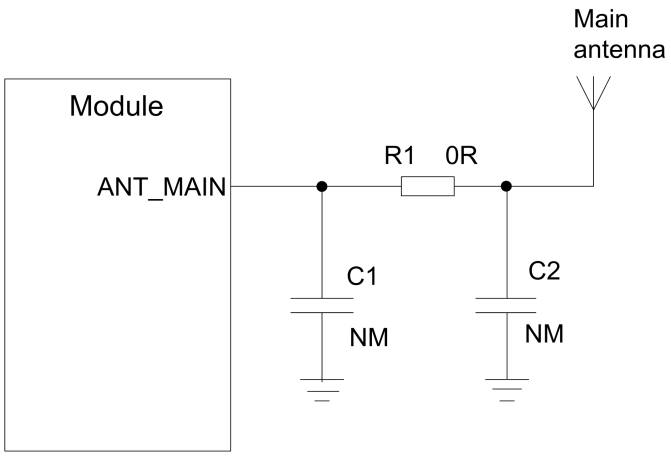


Figure 22: Reference Design of Main Antenna Interface

[4] LTE HD-FDD B17 is supported in Cat NB1/Cat NB2* only.
[5] LTE HD-FDD B26 and B27 are supported in Cat M1 only.

5.2. GNSS Antenna Interface

5.2.1. Pin Definition

Table 27: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	49	AI	GNSS antenna interface	50 Ω impedance

5.2.2. GNSS Operating Frequency

Table 28: GNSS Operating Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz

5.2.3. Reference Design

A reference design of GNSS antenna interface is shown as below.

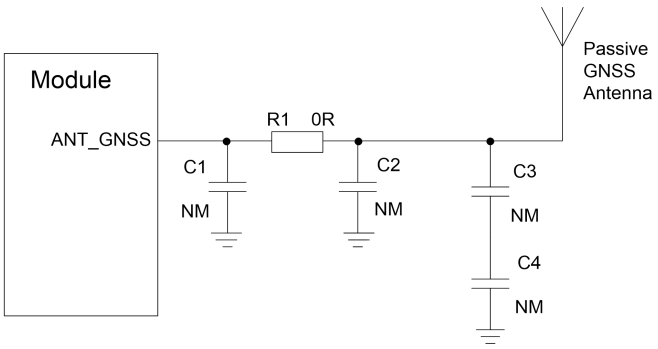


Figure 23: Reference Design of GNSS Antenna Interface

NOTES

The module is designed with a built-in LNA, and supports passive GNSS antenna only. Active antenna and external LNA are not supported.

5.3. Reference Design of RF Layout

For users' PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

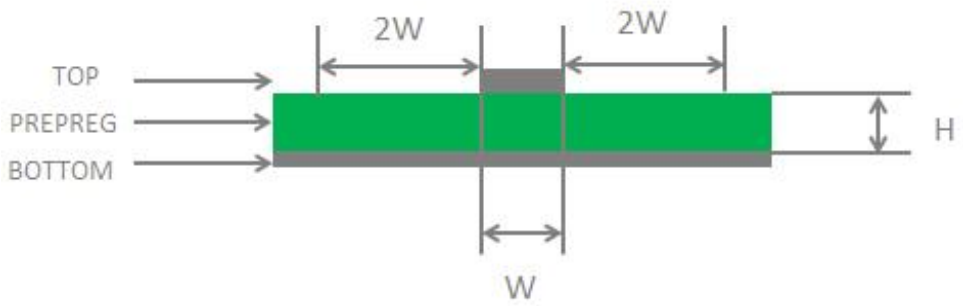


Figure 24: Microstrip Design on a 2-layer PCB

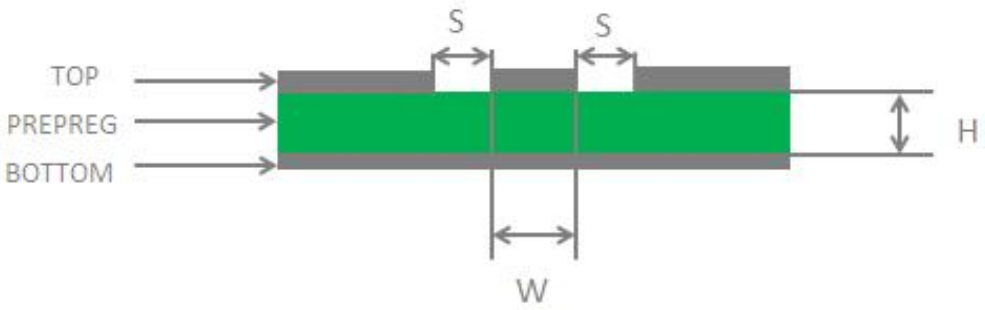


Figure 25: Coplanar Waveguide Design on a 2-layer PCB

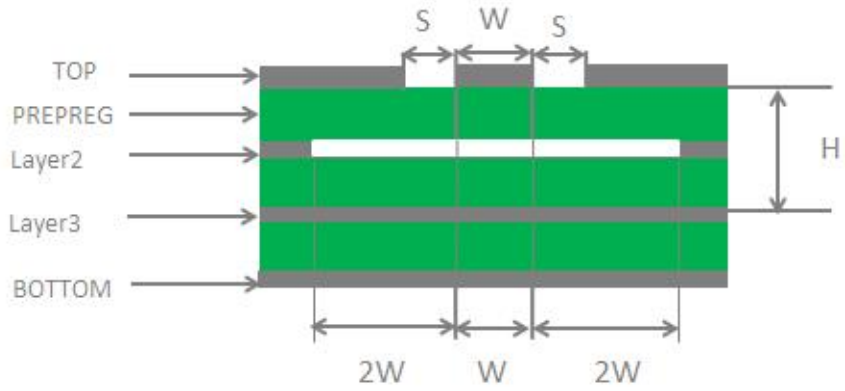


Figure 26: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

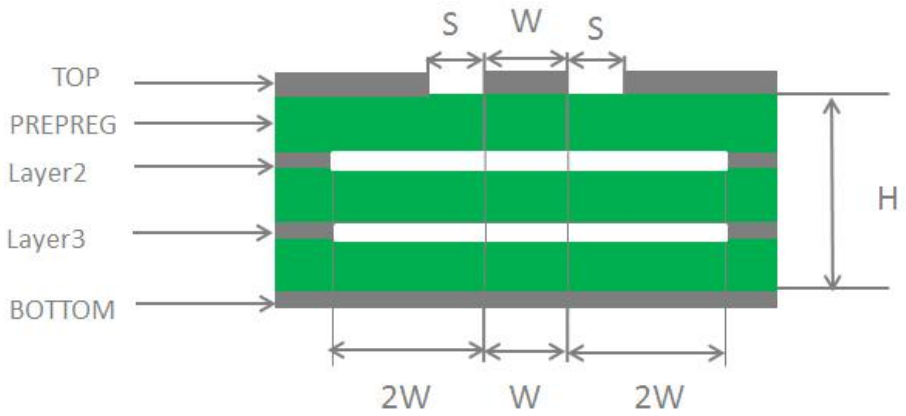


Figure 27: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [6]***.

5.4. Antenna Installation

5.4.1. Antenna Requirements

Table 29: Antenna Requirements

Antenna Type	Requirements
GNSS	Frequency range: 1559–1609 MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0 dBi
LTE	VSWR: ≤ 2 Efficiency: > 30 % Max. Input Power: 50 W Input Impedance: 50 Ω Cable Insertion Loss: **< 1 dB:** LB (< 1 GHz) **< 1.5 dB:** MB (1–2.3 GHz)

5.4.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connectors provided by *HIROSE*.

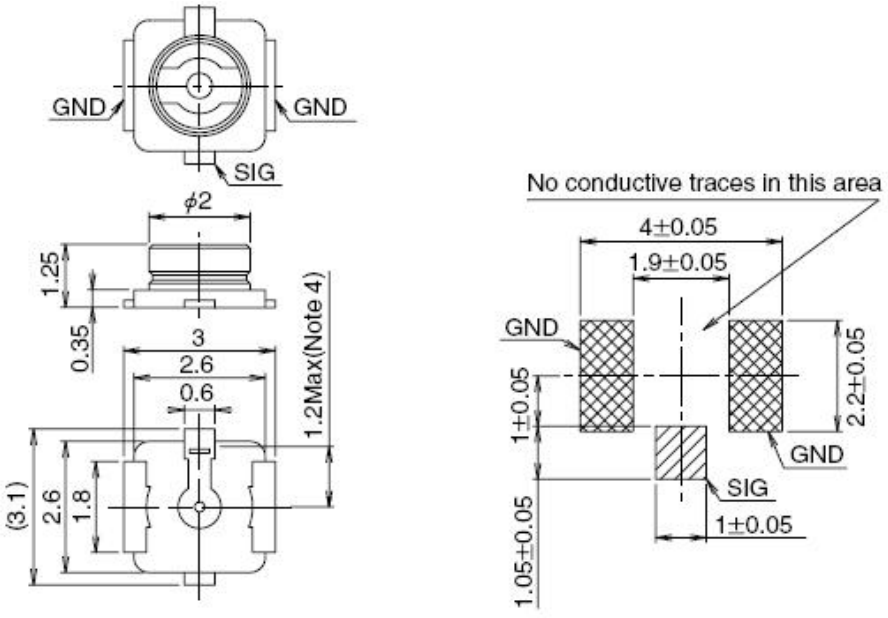


Figure 28: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

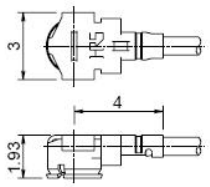
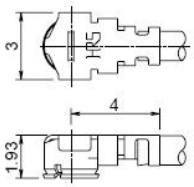
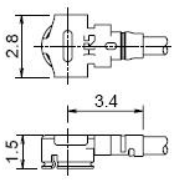
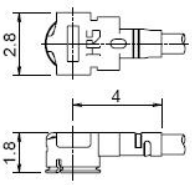
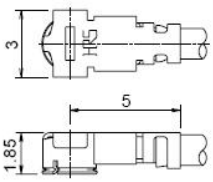
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 29: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connectors.

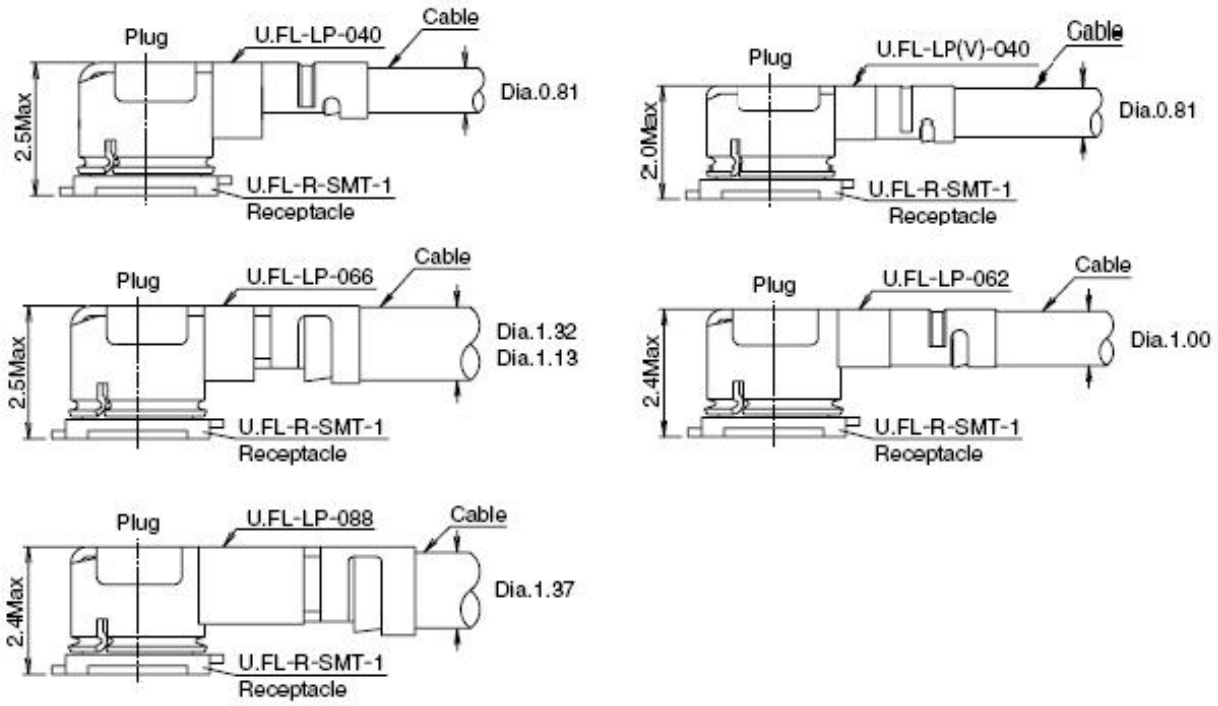


Figure 30: Space Factor of Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Reliability, Radio and Electrical Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 30: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_BB	-0.2	4.5	V
VBAT_RF	-0.2	4.5	V
USB_VBUS	1.19	2.0	V
Voltage at Digital Pins	-0.3	2.0	V

6.2. Power Supply Ratings

Table 31: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT_BB	Power supply for the module's baseband part	The actual input voltages must be kept between the minimum and the maximum values. BG95-MF	2.2	3.3	4.35	V
VBAT_RF	Power supply for the module's RF part					
USB_VBUS	USB connection detection	-	-	5.0	-	V

6.3. Operating and Storage Temperatures

Table 32: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [1)]	-35	+ 25	+ 75	ºC
Extended Temperature Range [2)]	-40		+ 85	ºC
Storage Temperature Range	-40		+ 90	°C

NOTES

1. [1)] Within the operating temperature range, the module meets 3GPP specifications.
2. [2)] Within the extended temperature range, the module remains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

6.4. Power Consumption

Table 33: Power Consumption (Power Supply: 3.3 V, Room Temperature)

Description	Conditions	Avg.	Max.	Unit
Leakage	Power-off @ USB/UART disconnected	TBD	-	μA
PSM	PSM @ USB/UART disconnected	TBD	-	μA
Rock Bottom	**AT+CFUN=0** @ Sleep mode	TBD	-	μA
Sleep Mode (USB/UART disconnected)	LTE Cat M1 DRX = 1.28 s	TBD	-	mA
	LTE Cat NB1 DRX = 1.28 s	TBD	-	mA

	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	TBD	-	mA
	LTE Cat NB1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	TBD	-	mA
Idle State (USB/UART disconnected)	LTE Cat M1 DRX = 1.28 s	TBD	-	mA
	LTE Cat NB1 DRX = 1.28 s	TBD	-	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	TBD	-	mA
	LTE Cat NB1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	TBD	-	mA
LTE Cat M1 data transfer (GNSS OFF)	LTE HD-FDD B1 @ 22.8 dBm	TBD	-	mA
	LTE HD-FDD B2 @ 23.37 dBm	TBD	-	mA
	LTE HD-FDD B3 @ 23.22 dBm	TBD	-	mA
	LTE HD-FDD B4 @ 23.25 dBm	TBD	-	mA
	LTE HD-FDD B5 @ 23.32 dBm	TBD	-	mA
	LTE HD-FDD B8 @ 23.56 dBm	TBD	-	mA
	LTE HD-FDD B12 @ 23.49 dBm	TBD	-	mA
	LTE HD-FDD B13 @ 23.16 dBm	TBD	-	mA
	LTE HD-FDD B18 @ 23.24 dBm	TBD	-	mA
	LTE HD-FDD B19 @ 23.34 dBm	TBD	-	mA
	LTE HD-FDD B20 @ 23.37 dBm	TBD	-	mA
	LTE HD-FDD B25 @ 23.37 dBm	TBD	-	mA
	LTE HD-FDD B26 @ 23.29 dBm	TBD	-	mA
	LTE HD-FDD B27 @ 23.16 dBm	TBD	-	mA
	LTE HD-FDD B28A @ 23.41 dBm	TBD	-	mA
	LTE HD-FDD B28B @ 23.33 dBm	TBD	-	mA

	LTE HD-FDD B66 @ 23.19 dBm	TBD	-	mA
LTE Cat NB1 data transfer (GNSS OFF)	LTE HD-FDD B1 @ 22.7 dBm	TBD	-	mA
	LTE HD-FDD B2 @ 22.72 dBm	TBD	-	mA
	LTE HD-FDD B3 @ 23.24 dBm	TBD	-	mA
	LTE HD-FDD B4 @ 23.19 dBm	TBD	-	mA
	LTE HD-FDD B5 @ 23.32 dBm	TBD	-	mA
	LTE HD-FDD B8 @ 22.71 dBm	TBD	-	mA
	LTE HD-FDD B12 @ 22.8 dBm	TBD	-	mA
	LTE HD-FDD B13 @ 23.23 dBm	TBD	-	mA
	LTE HD-FDD B17 @ 22.73 dBm	TBD	-	mA
	LTE HD-FDD B18 @ 23.28 dBm	TBD	-	mA
	LTE HD-FDD B19 @ 23.36 dBm	TBD	-	mA
	LTE HD-FDD B20 @ 23.39 dBm	TBD	-	mA
	LTE HD-FDD B25 @ 23.4 dBm	TBD	-	mA
	LTE HD-FDD B28 @ 22.75 dBm	TBD	-	mA
	LTE HD-FDD B66 @ 23.26 dBm	TBD	-	mA

Table 34: GNSS Current Consumption of (3.3 V Power Supply, Room Temperature)

Description	Conditions	Typ.	Unit
Searching (**AT+CFUN=0**)	Cold start @ Instrument	TBD	mA
	Hot start @ Instrument	TBD	mA
	Lost state @ Instrument	TBD	mA
Tracking (**AT+CFUN=0**)	Instrument environment @ Passive antenna	TBD	mA
	Half sky @ Real network, Passive antenna	TBD	mA

6.5. Tx Power

Table 35: Tx Power

Frequency Bands	Max. Tx Power	Min. Tx Power
LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B17 [6]/B18/ B19/B20/B25/B26 [7]/B27 [7]/B28/B66	23 dBm ±2.7 dB	< -39 dBm

6.6. RF Receiving Sensitivity

Table 36: Conducted RF Receiving Sensitivity of BG952A-GL QuecOpen

Frequency Band	Primary	Diversity	Receiving Sensitivity (dBm)	
			Cat M1/3GPP	Cat NB1[8]/3GPP
LTE HD-FDD B1	Supported	-	-106.6/-102.3	-115.3/-107.5
LTE HD-FDD B2			-106.2/-100.3	-114.3/-107.5
LTE HD-FDD B3			-106.2/-99.3	-114/-107.5
LTE HD-FDD B4			-106.6/-102.3	-114/-107.5
LTE HD-FDD B5			-106.8/-100.8	-115/-107.5
LTE HD-FDD B8			-107/-99.8	-115/-107.5
LTE HD-FDD B12			-106.4/-99.3	-114.3/-107.5
LTE HD-FDD B13			-106.4/-99.3	-114.6/-107.5
LTE HD-FDD B17 [6]			-	-114.6/-107.5
LTE HD-FDD B18			-107.2/-102.3	-115.3/-107.5

[6] LTE HD-FDD B17 is supported in Cat NB1/Cat NB2* only.
[7] LTE HD-FDD B26 and B27 are supported in Cat M1 only.
[8] LTE Cat NB1 receiving sensitivity without repetitions.

LTE HD-FDD B19	-107/-102.3	-115.3/-107.5
LTE HD-FDD B20	-106.6/-99.8	-114.6/-107.5
LTE HD-FDD B25	-106.4/-100.3	-114.3/-107.5
LTE HD-FDD B26 [9]	-107/-100.3	-
LTE HD-FDD B27 [9]	-107.2/-100.8	-
LTE HD-FDD B28	-106.6/-100.8	-114.6/-107.5
LTE HD-FDD B66	-106.8/-101.8	-114.9/-107.5

6.7. ESD

If the static electricity generated by various ways discharges to the module, the module maybe damaged to a certain extent. Thus, please take proper ESD countermeasures and handling methods. For example, wearing anti-static gloves during the development, production, assembly and testing of the module; adding ESD protective components to the ESD sensitive interfaces and points in the product design.

Table 37: Electrostatic Discharge Characteristics (25 ºC, 45 % Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	TBD	TBD	kV
Main/GNSS Antenna Interfaces	TBD	TBD	kV

[9] LTE HD-FDD B26 and B27 are supported in Cat M1 only.

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.05 mm unless otherwise specified.

7.1. Mechanical Dimensions

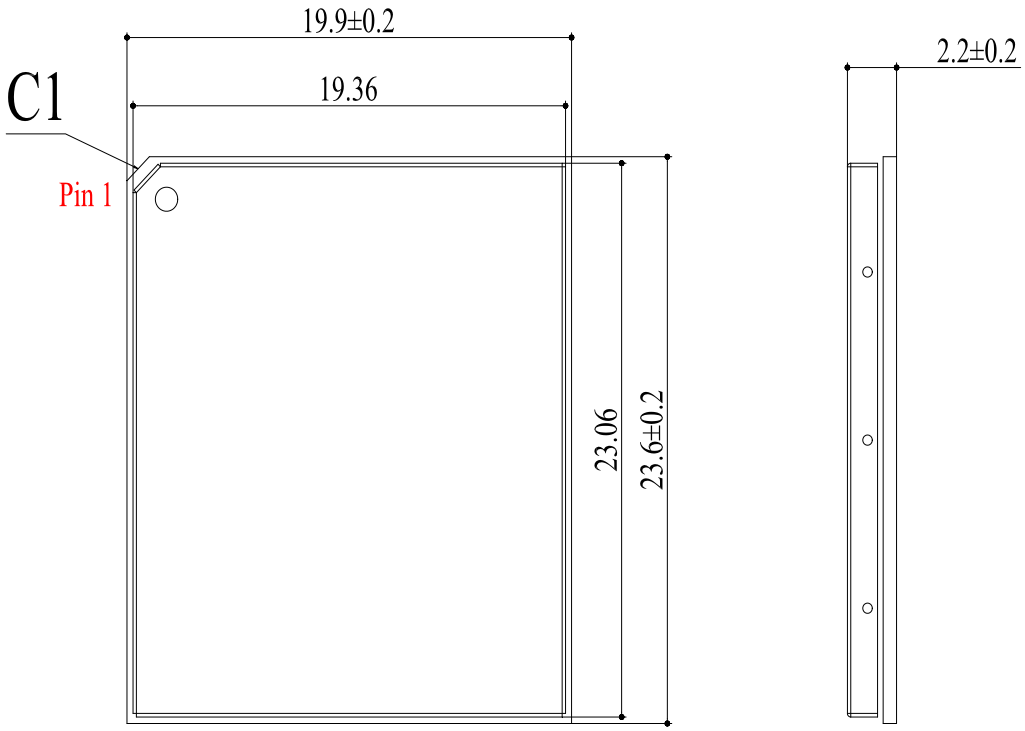


Figure 31: Module Top and Side Dimensions

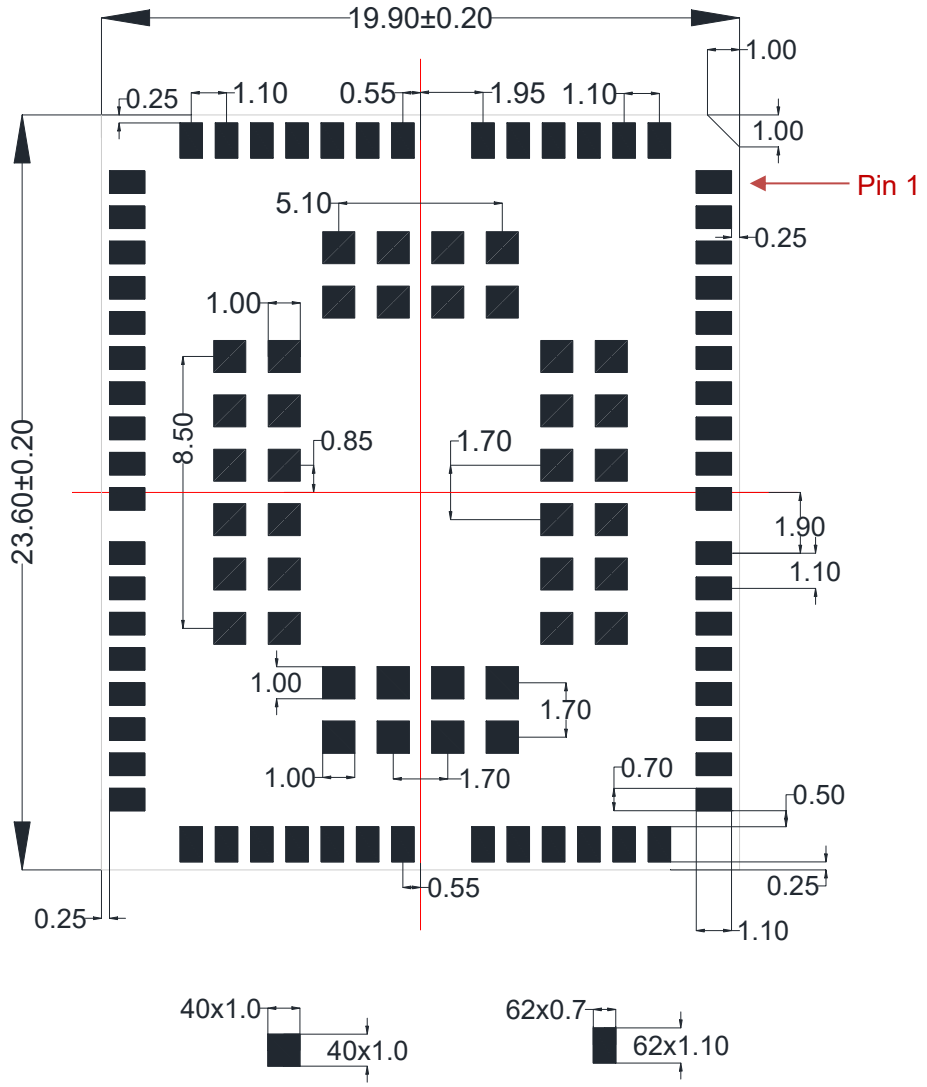


Figure 32: Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

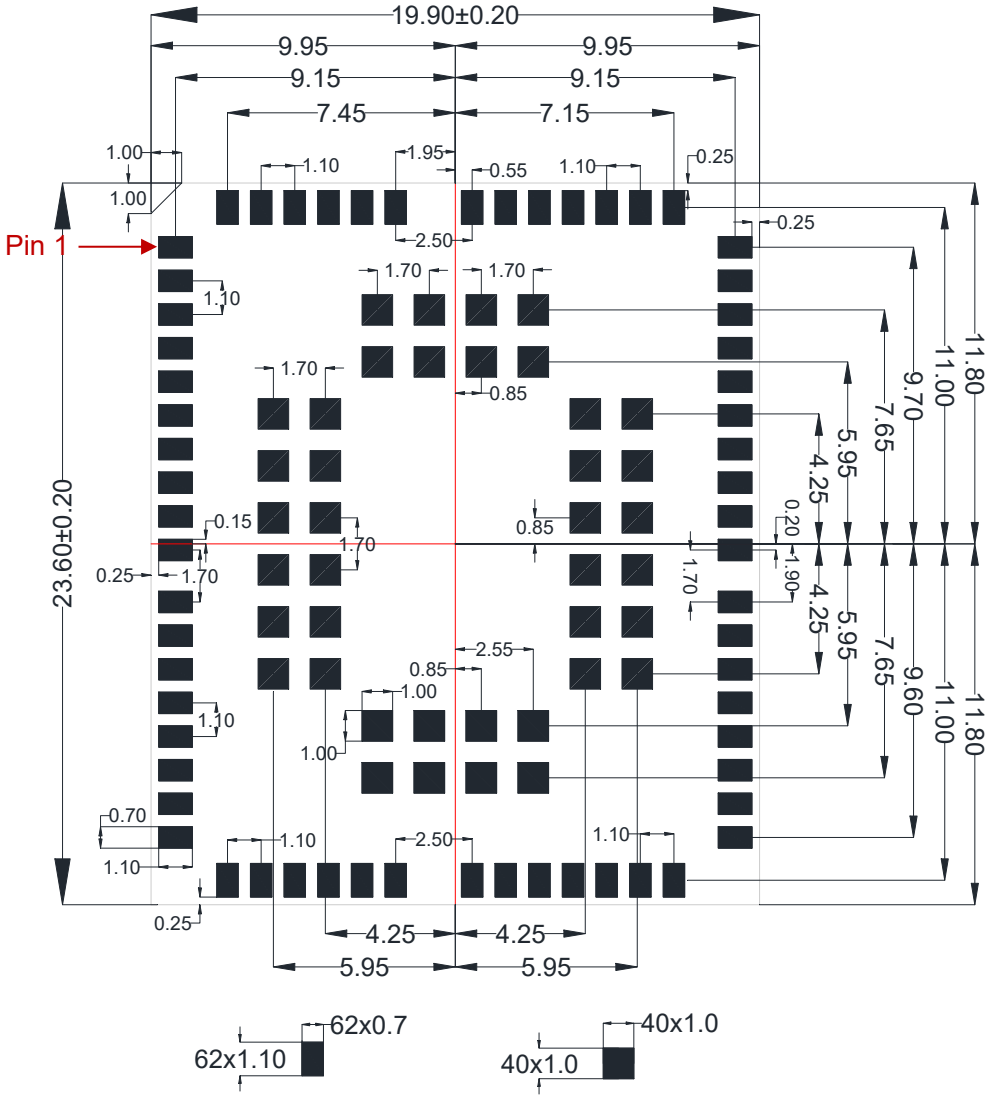


Figure 33: Recommended Footprint (Top View)

NOTES

1. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.
2. All reserved pins must be kept open.
3. For stencil design requirements of the module, see ***document [6]***.

7.3. Top and Bottom Views

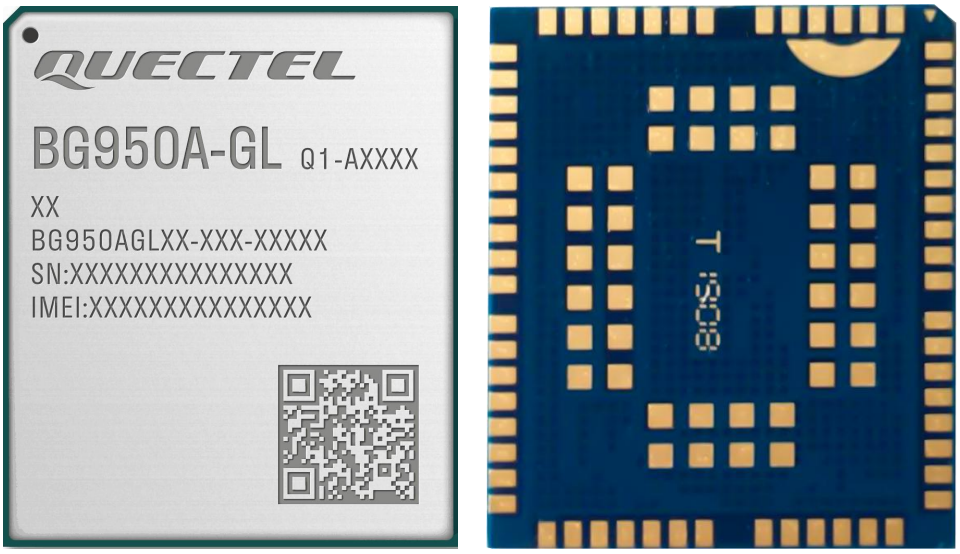


Figure 34: Top and Bottom Views

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [1)] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

NOTES

1. [1)] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*.
2. To avoid blistering, layer separation and other soldering issues, it is forbidden to expose the modules to the air for a long time. If the temperature and moisture do not conform to *IPC/JEDEC J-STD-033* or the relative moisture is over 60 %, it is recommended to start the solder reflow process within 24 hours after the package is removed. And do not remove the packages of tremendous modules if they are not ready for soldering.
3. Take the module out of the packaging and put it on high-temperature resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [7]***.

It is suggested that the peak reflow temperature is 238 °C to 246 ºC, and the absolute maximum reflow temperature is 246 ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

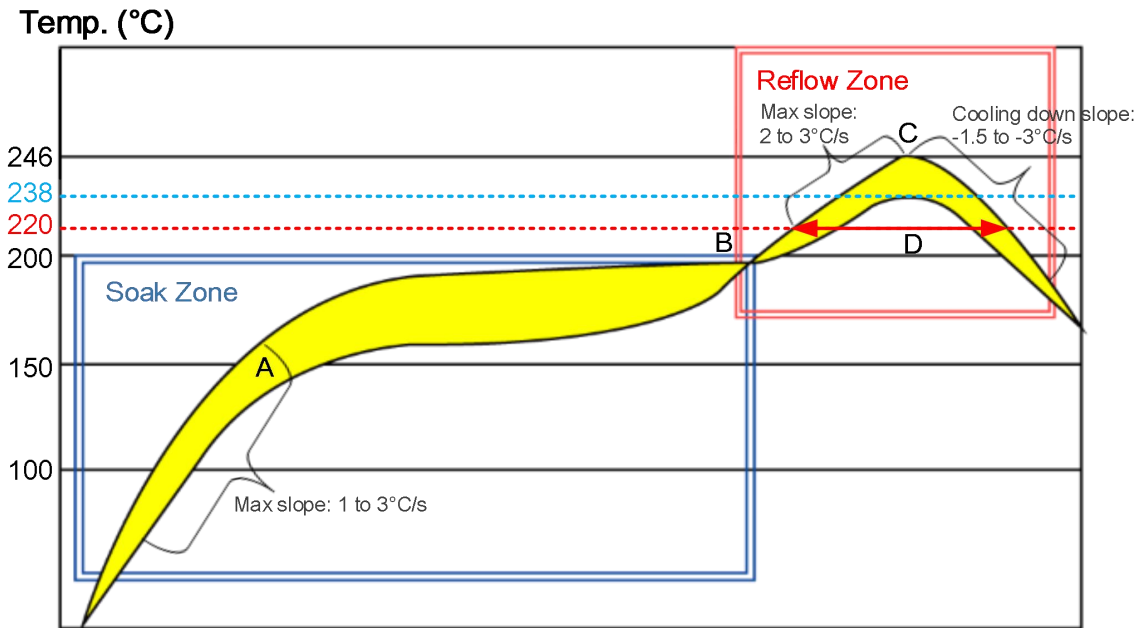


Figure 35: Recommended Reflow Soldering Thermal Profile

Table 38: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	1–3 °C/s
Reflow time (D: over 220 °C)	45–70 s
Max temperature	235–246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. If the module requires conformal coating, DO NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
2. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
3. Due to the SMT process complexity, please contact Quectel Technical Support in advance regarding any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document [6]***.

8.3. Packaging

The module is delivered in a tape carrier packaging and details are as follows:

8.3.1. Carrier Tape

Dimension details:

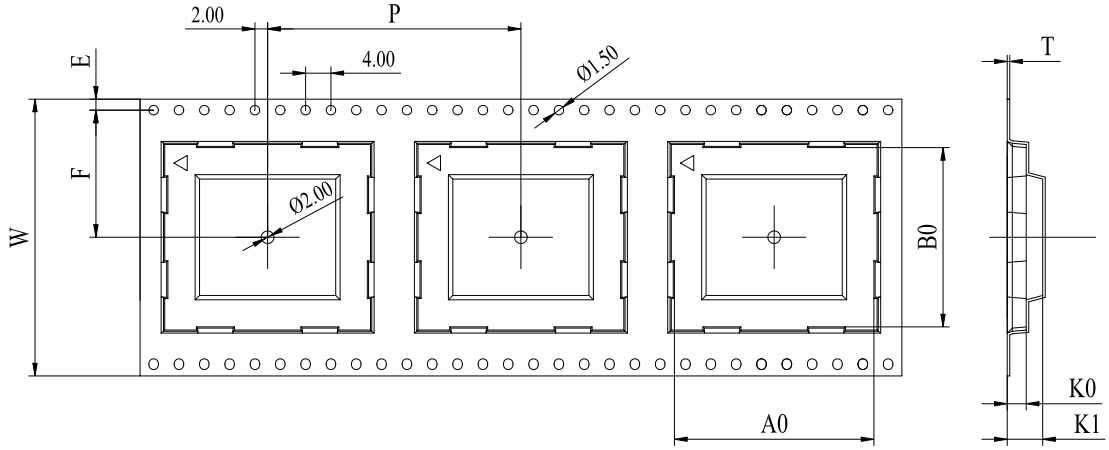


Figure 36: Carrier Tape Dimension Drawing

Table 39: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	20.2	24	3.15	6.65	20.2	1.75

8.3.2. Plastic Reel

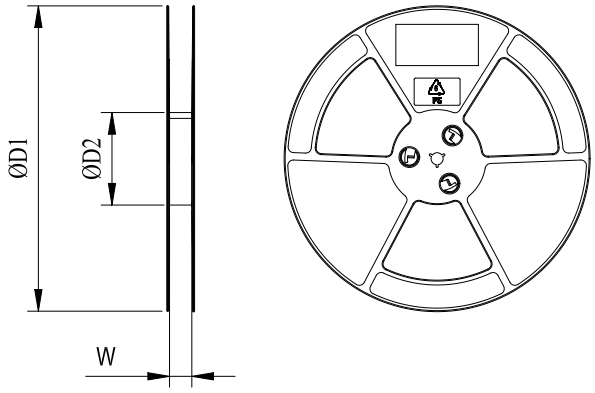


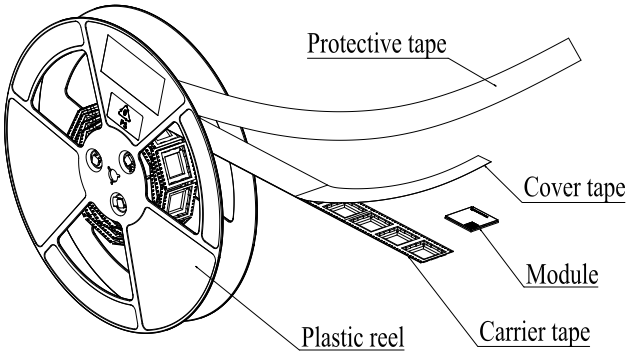
Figure 37: Plastic Reel Dimension Drawing

Table 40: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W

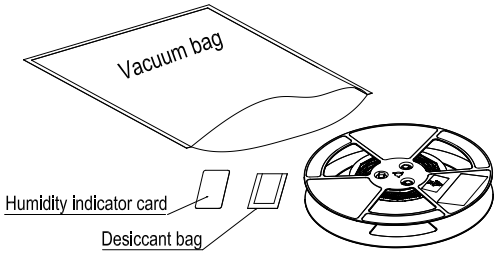
330	100	44.5

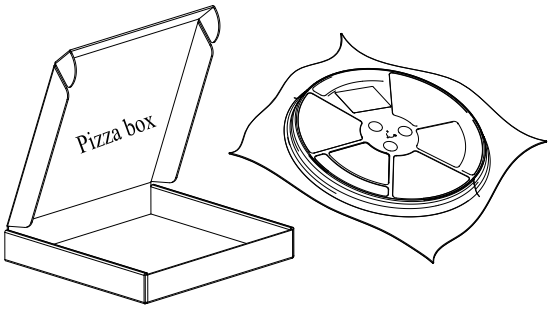
8.3.3. Packing Process



Place the module onto the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape on the plastic reel and use the protective tape for protection. One plastic reel can load 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag inside a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel inside a pizza box.

Place 4 pizza boxes inside 1 carton and seal it. One carton can pack 1000 modules.

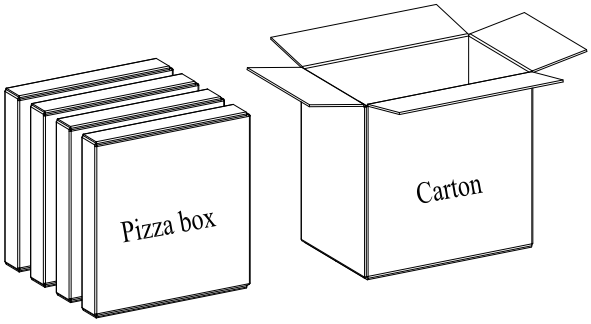


Figure 38: Packaging Process

9 Appendix A References

Table 41: Related Documents

SN	Document Name
[1]	Quectel_BG770A-GL&BG95xA-GL_GNSS_Application_Note
[2]	Quectel_LTE_OPEN_EVB_User_Guide
[3]	Quectel_BG77xA-GL&BG95xA-GL_AT_Commands_Manual
[4]	Quectel_BG77xA-GL&BG95xA-GL_QCFG_AT_Commands_Manual
[5]	Quectel_RF_Layout_Application_Note
[6]	Quectel_Module_Secondary_SMT_Application_Note
[7]	Quectel_BG952A-GL_QuecOpen_GPIO_Configuration
[8]	Quectel_BG950A-GL&BG951A-GL_TE-A_User_Guide

Table 42: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
e-I-DRX	Extended Idle Mode Discontinuous Reception
EDGE	Enhanced Data Rates for GSM Evolution

EGPRS	Enhanced General Packet Radio Service
EGSM	Extended GSM (Global System for Mobile Communications)
EPC	Evolved Packet Core
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
HSS	Home Subscriber Server
I2C	Inter-Integrated Circuit
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MO	Mobile Originated
MS	Mobile Station
MSL	Moisture Sensitivity Level
MT	Mobile Terminated
PA	Power Amplifier
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
PSM	Power Saving Mode
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SAW	Surface Acoustic Wave
SMS	Short Message Service

SPI	Serial Peripheral Interface
TDM	Time-Division Multiplexing
TVS	Transient Voltage Suppressor
UL	Uplink
UE	User Equipment
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnom	Nominal Voltage Value
Vmin	Minimum Voltage Value
$V_{IH}max$	Maximum Input High Level Voltage Value
$V_{IH}min$	Minimum Input High Level Voltage Value
$V_{IL}max$	Maximum Input Low Level Voltage Value
$V_{IL}min$	Minimum Input Low Level Voltage Value
$V_{OH}min$	Minimum Output High Level Voltage Value
$V_{OL}max$	Maximum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WWAN	Wireless Wide Area Network
Wi-Fi	Wireless Fidelity

CE Statement

The minimum distance between the user and/or any bystander and the radiating structure of the transmitter is 20cm.

Hereby, We, Quectel Wireless Solutions Co., Ltd. declares that the radio equipment type BG951A-GL is in compliance with the Directive 2014/53/EU.

The full text of the EU declaration of conformity is available at the following internet address:

Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai

200233, China

https://www.quectel.com/support/downloadb/TechnicalDocuments.htm

The device operates with the following frequency bands and transmitting power:

FCC Certification Requirements.

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.

And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based time-averaging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.

2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

3.A label with the following statements must be attached to the host end product: This device contains FCC ID: XMR2022BG952AGL.

4.To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

- Catm LTE Band2/25:≤11.000dBi
- Catm LTE Band4/66:≤8.000dBi
- Catm LTE Band5/26:≤12.541dBi
- Catm LTE Band12:≤11.798dBi
- Catm LTE Band13:≤12.214dBi

- ❒ NB LTE Band2/25:≤11.000dBi
- ❒ NB LTE Band4/66:≤8.000dBi
- ❒ NB LTE Band5:≤12.541 dBi
- ❒ NB LTE Band12:≤11.798dBi
- ❒ NB LTE Band13:≤12.214dBi

5. This module must not transmit simultaneously with any other antenna or transmitter

6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

For this device, OEM integrators must be provided with labeling instructions of finished products. Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module:"Contains Transmitter Module FCC ID: XMR2022BG952AGL" or "Contains FCC ID: XMR2022BG952AGL" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

IC Statement

IRSS-GEN

"This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device." or "Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

1) l'appareil ne doit pas produire de brouillage; 2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Déclaration sur l'exposition aux rayonnements RF

The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body

and must not transmit simultaneously with any other antenna or transmitter.

L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.

To comply with IC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

- Catm LTE Band2/25:≤11.000dBi
- Catm LTE Band4/66:≤8.000dBi
- Catm LTE Band5/26:≤12.541dBi
- Catm LTE Band12:≤11.798dBi
- Catm LTE Band13:≤12.214dBi
- Catm LTE Band85:≤11.798dBi
- NB LTE Band2/25:≤11.000dBi
- NB LTE Band4/66:≤8.000dBi
- NB LTE Band5:≤12.541 dBi
- NB LTE Band12:≤11.798dBi
- NB LTE Band13:≤12.214dBi

The host product shall be properly labelled to identify the modules within the host product.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word “Contains” or similar wording expressing the same meaning, as follows:

“Contains IC: 10224A-022BG952AGL” or “where: 10224A-022BG952AGL is the module’s certification number”.

Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte.

L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installédans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, précédé du mot «Contient» ou d'un libellé semblable exprimant la même signification, comme suit:"Contient IC: 10224A-022BG952AGL " ou "où: 10224A-022BG952AGL est le numéro de certification du module.