AG568N Series QuecOpen Hardware Design

Automotive Module Series

Version: 1.0.6

Date: 2023-01-19

Status: Preliminary

At Quectel, our aim is to provide timely and comprehensive services to our customers. If you require any assistance, please contact our headquarters:

Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local offices. For more information, please visit:
http://www.quectel.com/support/sales.htm.

For technical support, or to report documentation errors, please visit:
http://www.quectel.com/support/technical.htm.
Or email us at: support@quectel.com.

Legal Notices

We offer information as a service to you. The provided information is based on your requirements and we make every effort to ensure its quality. You agree that you are responsible for using independent analysis and evaluation in designing intended products, and we provide reference designs for illustrative purposes only. Before using any hardware, software or service guided by this document, please read this notice carefully. Even though we employ commercially reasonable efforts to provide the best possible experience, you hereby acknowledge and agree that this document and related services hereunder are provided to you on an “as available” basis. We may revise or restate this document from time to time at our sole discretion without any prior notice to you.

Use and Disclosure Restrictions

License Agreements

Documents and information provided by us shall be kept confidential, unless specific permission is granted. They shall not be accessed or used for any purpose except as expressly provided herein.

Copyright

Our and third-party products hereunder may contain copyrighted material. Such copyrighted material shall not be copied, reproduced, distributed, merged, published, translated, or modified without prior written consent. We and the third party have exclusive rights over copyrighted material. No license shall be granted or conveyed under any patents, copyrights, trademarks, or service mark rights. To avoid ambiguities, purchasing in any form cannot be deemed as granting a license other than the normal non-exclusive, royalty-free license to use the material. We reserve the right to take legal action for noncompliance with abovementioned requirements, unauthorized use, or other illegal or malicious use of the material.

Trademarks

Except as otherwise set forth herein, nothing in this document shall be construed as conferring any rights to use any trademark, trade name or name, abbreviation, or counterfeit product thereof owned by Quectel or any third party in advertising, publicity, or other aspects.

Third-Party Rights

This document may refer to hardware, software and/or documentation owned by one or more third parties ("third-party materials"). Use of such third-party materials shall be governed by all restrictions and obligations applicable thereto.

We make no warranty or representation, either express or implied, regarding the third-party materials, including but not limited to any implied or statutory, warranties of merchantability or fitness for a particular purpose, quiet enjoyment, system integration, information accuracy, and non-infringement of any third-party intellectual property rights with regard to the licensed technology or use thereof. Nothing herein constitutes a representation or warranty by us to either develop, enhance, modify, distribute, market, sell, offer for sale, or otherwise maintain production of any our products or any other hardware, software, device, tool, information, or product. We moreover disclaim any and all warranties arising from the course of dealing or usage of trade.

Privacy Policy

To implement module functionality, certain device data are uploaded to Quectel's or third-party's servers, including carriers, chipset suppliers or customer-designated servers. Quectel, strictly abiding by the relevant laws and regulations, shall retain, use, disclose or otherwise process relevant data for the purpose of performing the service only or as permitted by applicable laws. Before data interaction with third parties, please be informed of their privacy and data security policy.

Disclaimer

a) We acknowledge no liability for any injury or damage arising from the reliance upon the information.
b) We shall bear no liability resulting from any inaccuracies or omissions, or from the use of the information contained herein.
c) While we have made every effort to ensure that the functions and features under development are free from errors, it is possible that they could contain errors, inaccuracies, and omissions. Unless otherwise provided by valid agreement, we make no warranties of any kind, either implied or express, and exclude all liability for any loss or damage suffered in connection with the use of features and functions under development, to the maximum extent permitted by law, regardless of whether such loss or damage may have been foreseeable.
d) We are not responsible for the accessibility, safety, accuracy, availability, legality, or completeness of information, advertising, commercial offers, products, services, and materials on third-party websites and third-party resources.

Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2021-08-31	Cathy CHEN/ Jason FAN	Creation of the document
1.0.0	2021-08-31	Cathy CHEN/ Jason FAN	Preliminary
1.0.1	2021-10-19	Cathy CHEN/ Jason FAN	1. Updated the pin 60, pin 163 and pin 166 from RESERVED to ADC3, ADC4, ADC5. 2. Updated the pin 132, pin 136 and pin 428 from RESERVED to GPIO 22, GPIO23, GPIO24. 3. Updated the pin 411 and pin 412 from RESERVED to UART3_RXD, UART3_TXD. 4. Updated the pin 275, pin 276, pin 277 and pin 278 from RESERVED to SPI_MISO, SPI3_CLK, SPI3_MOSI, SPI_CS. 5. Updated the package information of the module (Chapter 8.3).
1.0.2	2021-12-03	Spencer YANG/ Jason FAN	Added the related information of AG568N-EU.
1.0.3	2021-02-18	Cathy CHEN/ Jason FAN	1. Modified the pin name of pin 96 and pin 99 (Figure 2). 2. Updated the power domain and DC characteristic of USB_BOOT (Table 6). 3. Updated the description of thermal dissipation (Chapter 6.6). 4. Updated the max slope of manufacturing and soldering (Figure 45&Table 52).
1.0.4	2022-05-23	Cathy CHEN/ Jason FAN/ Pepe HU	1. Added the sub-models of AG568N-NA and AG568N-ROW. 2. Added the information of module weight (Table 2). 3. Updated the maximum clock frequency rate from

			up to 52 MHz to 50 MHz of SPI interface at master mode (Table 4). 4. Updated the information of USB serial driver (Table 4). 5. Modified the information of transmitting power (Table 4). 6. Updated the DL/UL transmitting rate of LTE-FDD and LTE-TDD on AG568N-CN and AG568N-EU (Table 4). 7. Updated the way of firmware grade from DFOTA to FOTA (Table 4). 8. Added the max. output current of VDD_EXT (Table 6). 9. Updated the description and comment of USB_VBUS. (Table 6) 10. Updated the chapter “USB Application with USB Remote Wakeup Function” to “USB Application without USB Suspend Function” (Chapter 3.2.1.1). 11. Updated the turn-off time by driving PWRKEY low (Chapter 3.6.1) 12. Updated the reset time by driving RESET_N low (Chapter 3.7). 13. Updated the R3 in the reference circuit of USB application from “NM_0R” to “0R” (Tabel 15). 14. Deleted the simple block diagram for Ethernet application (Chapter 4.12&4.13) 15. Updated the information of Tx power (Chapter 5.1.2). 16. Updated the information of Rx sensitivity (Chapter 5.1.3). 17. Added the conditions and typical value of power consumption on AG568N-CN and added the conditions of power consumption on AG568N-EU (Table 51&52).
1.0.5	2022-08-30	Cathy CHEN/ Kiasher WANG/ Pepe HU	1. Updated the information of USB serial driver (Table 4). 2. Updated the information of receiving sensitivity (Chapter 5.1.3). 3. Deleted the information of GNSS power consumption.
1.0.6	2023-01-19	Cathy CHEN/ Jason FAN	1. Updated the frequency bands of AG568N-NA and AG568N-ROW. 2. Updated the baud rates of Debug UART (Table 4 & Table 12).

	3. Updated the data rates (Table 4). 4. Updated the LTE features (Table 4). 5. Updated the description of tests points for VDD_EXT, RESET_N, USB_VBUS, USB_DP/DM, DBG_RXD/TXD, USB_BOOT (Table 6 & Table 10 & Table 11 & Table 13 & Table 28). 6. Updated the information of turning on with PWRKEY (Chapter 3.5.1). 7. Updated the data of powering-down timing (Figure 11). 8. Updated the timing and parameters of SPI interfaces in master mode (Figure 26 & Table 27). 9. Updated the pin definition of cellular network interface (Chapter 5.1.1.1). 10. Updated the operating frequency (Chapter 5.1.1.2). 11. Updated Rx sensitivity (Chapter 5.1.3). 12. Updated GNSS performance (Chapter 5.2.2). 13. Updated the antenna design requirements (Table 48). 14. Updated the power supply ratings (Table 50). 15. Updated the data of power consumption (Chapter 6.3). 16. Updated the information of manufacturing and soldering (Chapter 8.2). 17. Added the mounting direction (Chapter 8.3.3).

Contents

Table Index

Figure Index

1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio

This document defines the AG568N series in QuecOpen® solution and describes its air interface and hardware interfaces which are connected with your applications.

It can help you quickly understand interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, you can use this module to design and to set up automotive industry mobile applications easily.

FCC Certification Requirements.
According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.
And the following conditions must be met:
1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based timeaveraging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.
2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.
3. A label with the following statements must be attached to the host end product: This device contains FCC ID: XMR2022AG568NNA
4. To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

radiation, maximum antenna gain (including cable loss) must not exceed: Operating Band	FCC Max Antenna Gain (dBi)	IC Max Antenna Gain (dBi)
LTE BAND 2	8.00	8.00
LTE BAND 4	5.00	5.00

LTE BAND 5	9.41	6.12
LTE BAND 12	8.70	5.64
LTE BAND 66	5.00	5.00
NR BAND 2	8.00	8.00
NR BAND 5	9.42	6.13
NR BAND 12	8.71	5.64
NR BAND 66	5.00	5.00
NR BAND 77	3.00	/
NR BAND 78	3.00	/

5. This module must not transmit simultaneously with any other antenna or transmitter
6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

For this device, OEM integrators must be provided with labeling instructions of finished products.

Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: XMR2022AG568NNA" or "Contains FCC ID: XMR2022AG568NNA" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier's Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Product Marketing Name： Quectel AG568N-NA

IC Statement

IRSS-GEN

"This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device." or "Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

1) l'appareil ne doit pas produire de brouillage; 2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Déclaration sur l'exposition aux rayonnements RF

L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.

The host product shall be properly labeled to identify the modules within the host product.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word "Contains" or similar wording expressing the same meaning, as follows: "Contains IC: 10224A-022AG568NNA" or "where: 10224A-022AG568NNAis the module's certification number".

Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte.

L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installédans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, précédé du mot «Contient» ou d'un libellé semblable exprimant la même signification, comme suit:

"Contient IC: 10224A-022AG568NNA" ou "où: 10224A-022AG568NNA est le numéro de certification du module".

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

AG568N series module is an SMD type module which is engineered to meet the demanding requirements in automotive applications and other harsh operating conditions. More specifically, the module will be commonly found in telematics boxes (T-Box), telematics control units (TCU), advanced driver-assistance systems (ADAS), on-board units (OBU), roadside units (RSU), and other automotive/traffic systems.

Related information and details are listed in the table below:

Table 2: Brief Introduction of the Module

Basic Information	
Pin number and package	426 LGA pins
Dimensions	(45.0 ±0.2) mm × (46.9 ±0.2) mm × (3.25 ±0.2) mm.
Weight	Approx. 16 g
Wireless technologies	● 5G NR, LTE, WCDMA, GSM ● Single-frequency GNSS/dual-frequency GNSS
Variants	● AG568N-CN ● AG568N-EU ● AG568N-NA ● AG568N-ROW

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions of AG568N Series

Mode		AG568N-CN	AG568N-EU	AG568N-NA	AG568N-ROW
5G NR	SA	n1/n3/n28A [1]/n41/n78	n1/n3/n7/n8/n20/n28/n77/n78	n2/n5/n12/n66/n77/n78	n28/n77/n78/n79
	NSA	n41/n78	n77/n78	n2/n5/n66/n77	n77/n78/n79
LTE	FDD	B1/B3/B5/B7/B8	B1/B3/B5/B7/B8/B20/B28/B32 [2]	B2/B4/B5/B12/B29 [2]/B66	B1/B3/B19/B21 [3]/B28
	TDD	B34/B38/B39/B40/B41	B38/B40	-	-
WCDMA		B1/B8	B1/B3/B5/B8	-	B1/B3
GSM		EGSM900/DCS1800	EGSM900/DCS1800	-	-
GNSS [4]		● Single-frequency GNSS (GPS, GLONASS, BDS, Galileo): L1 ● Dual-frequency GNSS (GPS, GLONASS, BDS, Galileo): L1 + L5			

[1] 5G FDD n28A supports Tx at 703–733 MHz (UL) and Rx at 758–788 MHz (DL).
[2] LTE B29 and B32 support Rx only.
[3] LTE B21 only supports 2 × 2 MIMO.
[4] AG568N series only supports dual-frequency GNSS (L1 + L5) by default, but the module is designed to be compatible with single-frequency GNSS (L1). For more details, please contact Quectel Technical Support.

2.2. Key Features

Table 4: Key Features

Features	Details
Power Supply	**VBAT_BB/VBAT_RF:** ● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interfaces	● Supports (U)SIM card: 1.8/3.0 V ● Supports Dual SIM Dual Standby (DSDS) [5]
Audio Features	● Support two digital audio interfaces: I2S interface and PCM interface ● GSM: HR/FR/EFR/AMR/AMR-WB ● WCDMA: AMR/AMR-WB ● LTE: AMR/AMR-WB ● Support echo cancellation and noise suppression
Digital Audio Interfaces	**PCM:** ● Used for Bluetooth audio transmission by default ● Supports 16-bit and 24-bit precision in PCM data path ● Supports long frame synchronization and short frame synchronization ● Supports master and slave modes **I2S:** ● Supports 8–192 kHz sampling rate ● Used for audio function with external codec IC by default
SPI Interfaces	● Three SPI interfaces: SPI1 and SPI2 only support master mode, SPI3 supports both master and slave modes. ● Maximum clock frequency rate: – Master mode: 50 MHz – Slave mode: 26 MHz
I2C Interfaces	● Two I2C interfaces ● Compliant with *UM10204 I2C-bus specification and user manual* ● Multi-master mode is not supported
SGMII Interface	● Supports 10/100/1000/2500 Mbps in full duplex mode ● Supports 10/100 Mbps in half duplex mode

[5] DSDS function is optional.

RGMII Interface	Supports 10/100/1000 Mbps in half/full duplex mode
WLAN and Bluetooth Application Interfaces	● Supports PCIe interface for WLAN function ● Supports Bluetooth UART and PCM interfaces for Bluetooth function
USB Interface	● Compliant with USB 3.1 and 2.0 specifications, with transmission rates up to 480 Mbps on USB 2.0 and 5 Gbps on USB 3.1 ● Used for AT command communication, data transmission, software debugging, firmware upgrade and GNSS NMEA sentences output ● USB 3.1 and USB 2.0 support data communication with external AP, and cannot be used simultaneously since they share the same controller ● USB serial driver: supports USB serial driver for Windows 7/8/8.1/10/11, Linux 2.6–5.18 and Android 4.x–12.x systems
SDIO Interface	Supports eMMC version 5.1 and HS400 mode
UART Interfaces	**UART1 (Main UART):** ● Used for AT command communication and data transmission ● Baud rate: 115200 bps by default ● Supports RTS and CTS hardware flow control **UART2 (Bluetooth UART):** ● Used for Bluetooth function ● Baud rate: 9600 bps by default ● Supports RTS and CTS hardware flow control **UART3 (V2X):** ● Used for external V2X function ● Baud rate: 9600 bps by default **Debug UART:** ● Used for Linux console and log output ● Baud rate: 115200 bps by default
PCIe Interface	● Compliant with PCIe Gen 3, supports 2-lane, 8 Gbps/lane ● Compliant with *PCI Express Base Specification Revision 3.0* ● Supports RC and EP mode in hardware design, but only supports RC mode in the software design ● Can be used to connect with an external WLAN IC and used for Wi-Fi communication by default
AT Commands	● Compliant with *3GPP TS 27.007* and *3GPP TS 27.005* ● Quectel enhanced AT commands
Rx-diversity	5G NR/LTE/WCDMA
Antenna Interface	● One main antenna interface (ANT_MAIN) ● One diversity antenna interface (ANT_DRX) ● Two MIMO antenna interfaces (ANT_MIMO3, ANT_MIMO4) ● One GNSS antenna interface (ANT_GNSS) ● 50 Ω impedance
Tx Power	● 5G NR TDD bands: Class 2 (26 dBm +1/-2 dB)

	• 5G NR FDD bands: Class 3 (23 dBm ±2 dB) • LTE bands: Class 3 (23 dBm ±2 dB) • WCDMA bands: Class 3 (23 dBm ±2 dB) • EGSM900: Class 4 (33 dBm ±2 dB) • DCS1800: Class 1 (30 dBm ±2 dB) • EGSM900 8-PSK: Class E2 (27 dBm ±3 dB) • DCS1800 8-PSK: Class E2 (26 dBm ±3 dB)
5G NR Features	• Support 3GPP Rel-15 • Support uplink 256QAM and downlink 256QAM • Support 4 × 4 MIMO for MHB bands in DL direction • Support SCS 15 kHz @ FDD and 30 kHz @ TDD • Support SA and NSA operation modes – NSA: supports option 3x, 3a, and option 3 – SA: supports option 3 • Max. data rates: **AG568N-CN/-EU** – NSA: Max. 2.4 Gbps (DL)/550 Mbps (UL) – SA: Max. 3.8 Gbps (DL 2CA)/480 Mbps (UL) **AG568N-NA** – NSA: Max. 3.5 Gbps (DL)/550 Mbps (UL) – SA: Max. 3.8 Gbps (DL 2CA)/480 Mbps (UL) **AG568N-ROW** – NSA: Max. 2.7 Gbps (DL)/550 Mbps (UL) – SA: Max. 3.8 Gbps (DL 2CA)/480 Mbps (UL)
LTE Features	**AG568N-CN:** • Support up to DL CA Cat 15 LTE-FDD and TDD • Support 1.4/3/5/10/15/20 MHz RF bandwidth • Support 4 × 4 MIMO for MHB bands in DL direction • Supports QPSK, 16QAM and 64QAM and 256QAM modulation in UL/DL direction • FDD: Max. 750 Mbps (DL)/80 Mbps (UL) • TDD: Max. 650 Mbps (DL)/50 Mbps (UL) **AG568N-EU:** • Support up to DL CA Cat 19 LTE-FDD and TDD • Support 1.4/3/5/10/15/20 MHz RF bandwidth • Support 4 × 4 MIMO for MHB bands in DL direction • Supports QPSK, 16QAM and 64QAM and 256QAM modulation in UL/DL direction • FDD: Max 1.6 Gbps (DL)/150 Mbps (UL) • TDD: Max 1.0 Gbps (DL)/100 Mbps (UL) **AG568N-NA:** • Support up to DL CA Cat 18 LTE-FDD • Support 1.4/3/5/10/15/20 MHz RF bandwidth • Support 4 ×4 MIMO for MHB bands in DL direction

	● Supports QPSK, 16QAM and 64QAM and 256QAM modulation in UL/DL direction ● FDD: Max 1.5 Gbps (DL)/150 Mbps (UL) **AG568N-ROW:** ● Support up to DL CA Cat 16 LTE-FDD ● Support 1.4/3/5/10/15/20 MHz RF bandwidth ● Support 4 ×4 MIMO for MHB [6] bands in DL direction ● Supports QPSK, 16QAM and 64QAM and 256QAM modulation in UL/DL direction ● FDD: Max 1.1 Gbps (DL)/150 Mbps (UL)
UMTS Features [7]	● Support 3GPP Rel-8 DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA ● Support QPSK, 16QAM and 64QAM modulation ● DC-HSDPA: Max. 42 Mbps (DL) ● DC-HSUPA: Max. 11 Mbps (UL) ● WCDMA: Max. 384 kbps (DL)/384 kbps (UL)
GSM Features [8]	**GPRS:** ● Support GPRS multi-slot class 33 (by default) ● Coding scheme: CS 1–4 ● Max. 107 kbps (DL)/85.6 kbps (UL) **EDGE:** ● Support EDGE multi-slot class 33 (by default) ● Supports GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) ● Downlink coding schemes: MCS 1–9 ● Uplink coding schemes: MCS 1–9 ● Max. 296 kbps (DL)/236.8 kbps (UL)
GNSS Features	● Supports GPS, GLONASS, BDS, Galileo ● Support single-frequency GNSS: L1 ● Support dual-frequency GNSS L1 + L5 ● Protocol: NMEA 0183 ● Update rate: 1 Hz by default, up to 10 Hz
Temperature Range	● Operating temperature range [9]: -35 °C to +75 °C ● Extended operating temperature range [10]: -40 °C to +85 °C ● eCall temperature range [11]: -40 °C to +95 °C ● Storage temperature range: -40 °C to +95 °C

[6] LTE B21 only support to 2 × 2 MIMO.
[7] AG568N-NA does not support UMTS function.
[8] AG568N-NA and AG568N-ROW do not support GSM function.
[9] Within the operating temperature range, the module meets 3GPP specifications.
[10] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, eCall*, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.
[11] Within eCall temperature range, the eCall function must be functional until the module is broken. When the ambient temperature is between 75 °C and 95 °C and the module temperature has reached the threshold value, the module will trigger protective measures (such as reduce power, decrease throughput, unregister the device, etc.) to ensure the full function of eCall.

Firmware Upgrade	• USB 2.0 interface • FOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- LPDDR4X+ NAND flash
- Radio frequency
- Peripheral interfaces

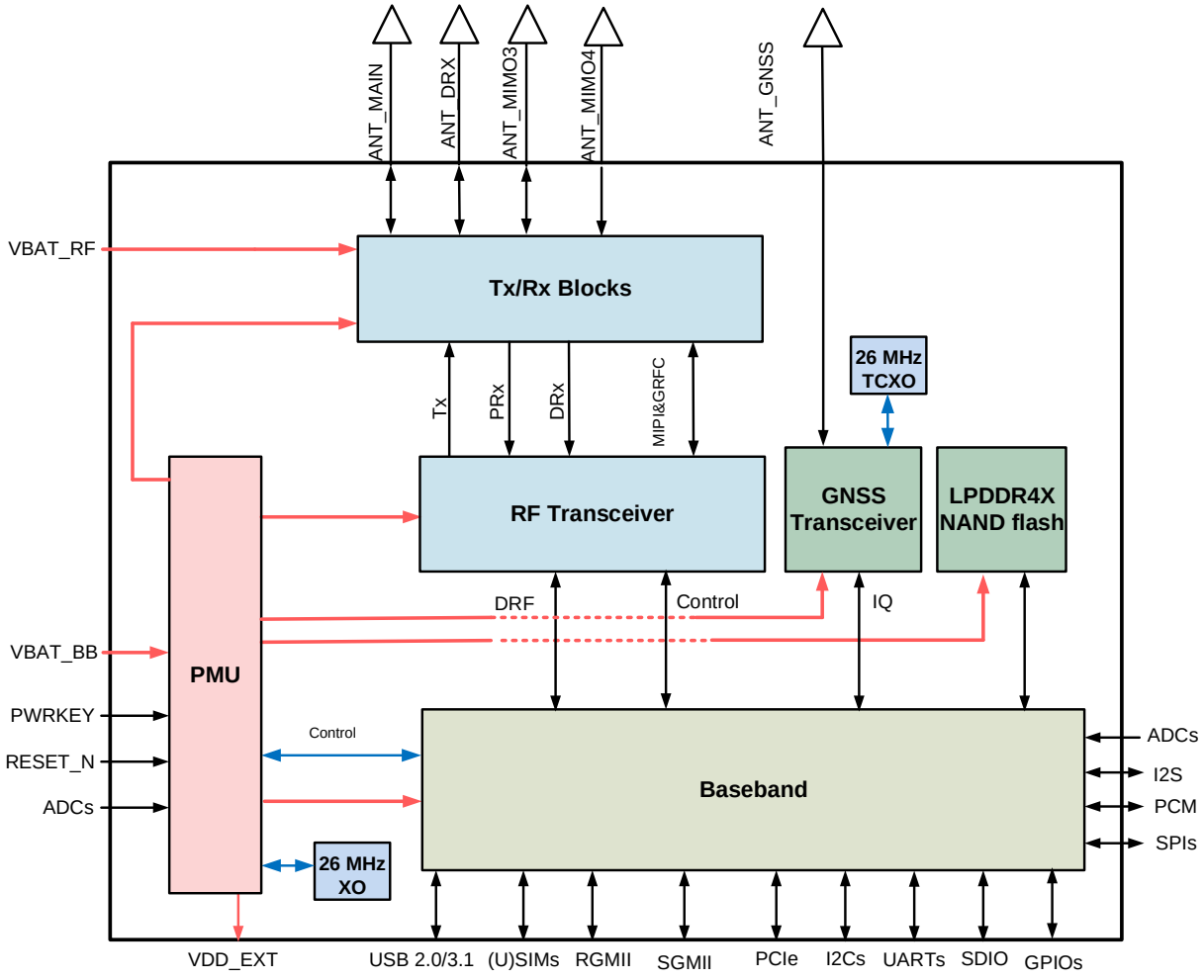


Figure 1: Functional Diagram

2.4. Pin Assignment

The following figure illustrates the pin assignment of the module.

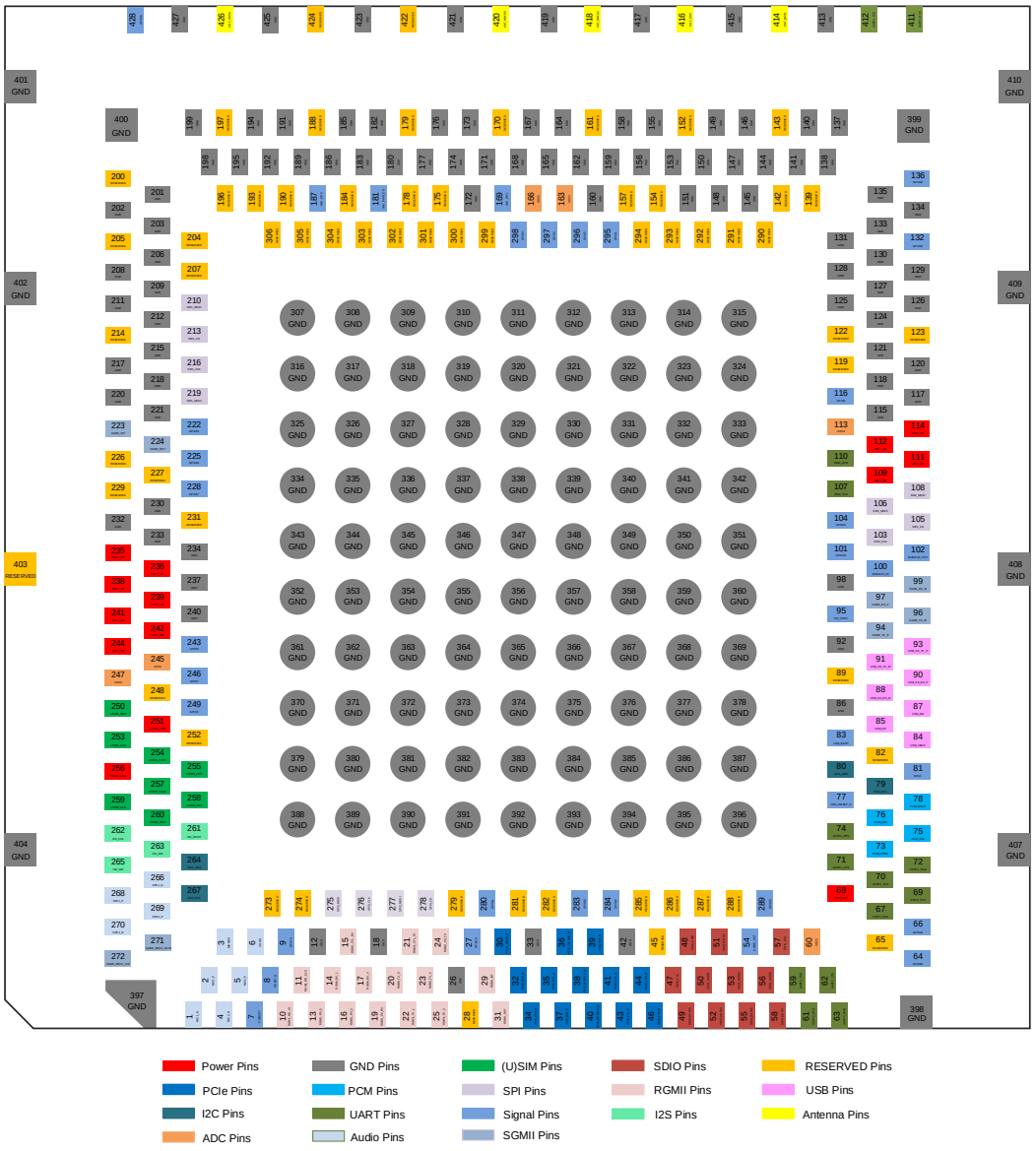


Figure 2: Pin Assignment (Top View)

NOTE

1. Keep all RESERVED pins and unused pins unconnected.
2. GND pins should be connected to ground.

2.5. Pin Description

The following table shows the DC characteristics and pin descriptions. DC characteristics include power domain, rate current, etc.

Table 5: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	241, 242, 244	PI	Power supply for the module's BB part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 1.5 A.
VBAT_RF	109, 111, 112, 114, 235, 236, 238, 239	PI	Power supply for the module's RF part		It must be provided with sufficient current up to 2.0 A.

VDD_EXT	68	PO	Provide 1.8 V for external circuits	Vnom = 1.8 V Iomax = 50 mA	Power supply only for external pull up circuits. It is recommended to reserve test points.
GND	12, 18, 26, 33, 42, 86, 92, 98, 115, 117, 118, 120, 121, 124–131, 133–135, 137, 138, 140, 141, 144–151, 153, 155, 156, 158, 159, 160, 162, 164, 165, 167, 168, 171–174, 176, 177, 180, 182, 183, 185, 186, 189, 191, 192, 194, 195, 198, 199, 201, 202, 203, 206, 208, 209, 211, 212, 215, 217, 218, 220, 221, 230, 232, 233, 234, 237, 240, 307–402, 404, 407–410, 413, 415, 417, 419, 421, 423, 425, 427				

Turn On/Off

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	7	DI	Turn on/off the module	V_{IH}max = 1.98 V V_{IH}min = 1.45 V V_{IL}max = 0.3 V	Internally pulled up to 1.8 V. Active low.
RESET_N	8	DI	Reset the module		Internally pulled up to 1.8 V. Active low. It is recommended to reserve test points.

USB Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	84	DI	Turn-on/ USB connection detect	Vmax = 21 V Vmin = 4.2 V Vnom = 5.0 V	It is recommended to keep it open before the module is powered on. Test points must be reserved.
USB_DP	85	AIO	USB 2.0 differential data (+)		Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	87	AIO	USB 2.0 differential data (-)		
USB_SS_TX_P	93	AO	USB 3.1 SuperSpeed transmit (+)		Require differential impedance of 90 Ω. If these pins are unused, connect Rx pairs with GND directly and keep other pins open.
USB_SS_TX_M	91	AO	USB 3.1 SuperSpeed transmit (-)		
USB_SS_RX_P	90	AI	USB 3.1 SuperSpeed receive (+)		
USB_SS_	88	AI	USB 3.1 SuperSpeed		

RX_M			receive (-)		
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	251	PO	(U)SIM1 card power supply		Either 1.8/3.0 V is supported by the module automatically.
USIM1_ DATA	254	DIO	(U)SIM1 card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.27 V V_{IH}min = 1.4 V V_{OL}max = 0.27 V V_{OH}min = 1.4 V **For 3.0 V (U)SIM:** V_{IL}max = 0.4 V V_{IH}min = 2.6 V V_{OL}max = 0.4 V V_{OH}min = 2.6 V	If unused, keep it open.
USIM1_CLK	253	DO	(U)SIM1 card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.22 V V_{OH}min = 1.62 V **For 3.0 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 2.7 V	
USIM1_RST	250	DO	(U)SIM1 card reset	**For 1.8 V (U)SIM:** V_{OL}max = 0.36 V V_{OH}min = 1.62 V **For 3.0 V (U)SIM:** V_{OL}max = 0.36 V V_{OH}min = 2.7 V	
USIM1_DET	255	DI	(U)SIM1 card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep it open.
USIM2_VDD	256	PO	(U)SIM2 card power supply		Either 1.8/3.0 V is supported by the module automatically.
USIM2_ DATA	257	DIO	(U)SIM2 card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.27 V V_{IH}min = 1.4 V	If unused, keep these pins open.

				V_{OL}max = 0.27 V V_{OH}min = 1.4 V **For 3.0 V (U)SIM:** V_{IL}max = 0.4 V V_{IH}min = 2.6 V V_{OL}max = 0.4 V V_{OH}min = 2.6 V	
USIM2_CLK	259	DO	(U)SIM2 card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.22 V V_{OH}min = 1.62 V **For 3.0 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 2.7 V	
USIM2_RST	260	DO	(U)SIM2 card reset	**For 1.8 V (U)SIM:** V_{OL}max = 0.36 V V_{OH}min = 1.62 V **For 3.0 V (U)SIM:** V_{OL}max = 0.36 V V_{OH}min = 2.7 V	
USIM2_DET	258	DI	(U)SIM2 card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep it open.
UART1 (Main UART)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART1_CTS	71	DO	DTE clear to send signal from DCE	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	Connect to DTE's CTS. 1.8 V power domain. If unused, keep these pins open.
UART1_RTS	74	DI	DTE request to send signal to DCE	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	Connect to DTE's RTS. 1.8 V power domain. If unused, keep these pins open.
UART1_RXD	72	DI	UART1 receive		1.8 V power domain. If unused, keep these pins open.
UART1_TXD	70	DO	UART1 transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	

UART2 (Bluetooth UART)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART2_TXD	59	DO	UART2 transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep these pins open.
UART2_RXD	63	DI	UART2 receive	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
UART2_RTS	61	DI	DTE request to send signal from DCE		Connect to DTE's CTS. 1.8 V power domain. If unused, keep these pins open.
UART2_CTS	62	DO	DTE clear to send signal to DCE	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	Connect to DTE's CTS. 1.8 V power domain. If unused, keep these pins open.
UART3 (V2X)					
UART3_RXD	411	DI	UART3 receive	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	Used for external V2X function by default. 1.8 V power domain. If unused, keep them open.
UART3_TXD	412	DO	UART3 transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	110	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. Test points must be reserved.
DBG_TXD	107	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C1_SCL	79	DO	I2C serial clock	V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{OL}max = 0.36 V	1.8 V power domain. If unused, keep them open. Used for external

					audio codec IC. Reserve pull-up resistors and not mount by default.
I2C1_SDA	80	DIO	I2C serial data		
I2C2_SCL	267	DO	I2C serial clock		1.8 V power domain. If unused, keep them open. Used for external IMU sensor. Reserve pull-up resistors and not mount by default.
I2C2_SDA	264	DIO	I2C serial data		
I2S Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2S_WS	265	DIO	I2S word select	V_{OL}max = 0.45 V V_{OH}min = 1.35V V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep these pins open.
I2S_CLK	262	DIO	I2S clock		
I2S_DIN	263	DI	I2S data input	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
I2S_DOUT	261	DO	I2S data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
MCLK	81	DO	Master clock output for codec		
CDC_ RESET_N	77	DO	External codec reset		
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	73	DIO	PCM data frame sync	V_{OL}max = 0.45 V V_{OH}min = 1.35V V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep them open.
PCM_CLK	75	DIO	PCM clock		
PCM_DIN	76	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	

				V_{IH}max = 2.1 V	
PCM_DOUT	78	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PCIe Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE_ REFCLK_P	40	AIO	PCIe reference clock (+)		Compliant with PCIe revision 3.0 specification. Requires differential impedance of 85 Ω. If unused, connect Rx pairs with GND directly and keep others open.
PCIE_ REFCLK_M	38	AIO	PCIe reference clock (-)		
PCIE_TX0_P	46	AO	PCIe transmit 0 (+)		
PCIE_TX0_M	44	AO	PCIe transmit 0 (-)		
PCIE_RX0_P	34	AI	PCIe receive 0 (+)		
PCIE_RX0_M	32	AI	PCIe receive 0 (-)		
PCIE_TX1_P	43	AO	PCIe transmit 1 (+)		
PCIE_TX1_M	41	AO	PCIe transmit 1 (-)		
PCIE_RX1_P	37	AI	PCIe receive 1 (+)		
PCIE_RX1_M	35	AI	PCIe receive 1 (-)		
PCIE_ CLKREQ_N	36	DIO	PCIe clock request	V_{OL}max = 0.45 V V_{OH}min = 1.35V V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep these pins open.
PCIE_RST_N	39	DO	PCIe reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PCIE_ WAKE_N	30	DI	PCIe wake up	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
SGMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SGMII_RX_P	97	AI	SGMII receive (+)		Requires differential

SGMII_RX_M	99	AI	SGMII receive (-)		impedance of 100 Ω. If unused, connect Rx pairs with GND directly and keep others open.
SGMII_TX_P	94	AO	SGMII transmit (+)		
SGMII_TX_M	96	AO	SGMII transmit (-)		
SGMII_INT	223	DI	PHY interrupt output	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep them open.
SGMII_RST	224	DO	SGMII reset external PHY	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SGMII_ MDIO_DATA	271	DIO	SGMII management data	V_{OL}max = 0.45 V V_{OH}min = 1.35V V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
SGMII_ MDIO_CLK	272	DO	SGMII management data clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
RGMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RGMII_MD_ IO	10	DIO	RGMII management data		Single-ended impedance of 50 Ω. 1.8 V power domain. If unused, keep these pins open.
RGMII_MD_ CLK	11	DO	RGMII management data clock		
RGMII_RX_0	13	DI	RGMII receive data bit 0		
RGMII_RX_1	14	DI	RGMII receive data bit 1		
RGMII_RX_2	16	DI	RGMII receive data bit 2		
RGMII_RX_3	17	DI	RGMII receive data bit 3		
RGMII_CTL_ RX	15	DI	RGMII receive control		
RGMII_CK_ RX	19	DI	RGMII receive clock		
RGMII_TX_0	20	DO	RGMII transmit data bit 0		
RGMII_TX_1	22	DO	RGMII transmit data bit 1		
RGMII_TX_2	23	DO	RGMII transmit data bit 2		

RGMII_TX_3	25	DO	RGMII transmit data bit 3		
RGMII_CTL_TX	21	DO	RGMII transmit control		
RGMII_CK_TX	24	DO	RGMII transmit clock		
RGMII_INT	29	DI	PHY interrupt output	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep them open.
RGMII_RST	31	DO	RGMII reset external PHY	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SDIO Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
EMMC_RST	54	DO	eMMC reset	V_{OL}max = 0.45 V V_{OH}min = 1.4 V	1.8 V power domain. If unused, keep these pins open.
SDIO_DATA0	49	DIO	SDIO data bit 0	V_{OL}max = 0.45 V V_{OH}min = 1.4V V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
SDIO_DATA1	50	DIO	SDIO data bit 1		
SDIO_DATA2	51	DIO	SDIO data bit 2		
SDIO_DATA3	52	DIO	SDIO data bit 3		
SDIO_DATA4	53	DIO	SDIO data bit 4		
SDIO_DATA5	55	DIO	SDIO data bit 5		
SDIO_DATA6	56	DIO	SDIO data bit 6		
SDIO_DATA7	58	DIO	SDIO data bit 7		
SDIO_CMD	48	DIO	SDIO command		
SDIO_CLK	47	DO	SDIO clock	V_{OL}max = 0.45 V V_{OH}min = 1.4 V	
SDIO_DSL	57	DI	SDIO data strobe	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
RF Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

ANT_GNSS	426	AI	GNSS antenna interface		Single-ended impedance of 50 Ω. Supports active antenna only.
ANT_MAIN	414	AIO	Main antenna interface		Single-ended impedance of 50 Ω.
ANT_DRX	416	AIO	Diversity antenna interface		
ANT_MIMO3	418	AIO [12]	4 × 4 MIMO antenna interface		
ANT_MIMO4	420	AI	4 × 4 MIMO antenna interface		
SPI Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI1_CS	213	DO	SPI1 chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	Master mode only. 1.8 V power domain. If unused, keep them open.
SPI1_CLK	216	DO	SPI1 clock		
SPI1_MOSI	210	DO	SPI1 master-out slave-in		
SPI1_MISO	219	DI	SPI1 master-in slave-out	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
SPI2_CS	105	DO	SPI2 chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SPI2_CLK	103	DO	SPI2 clock		
SPI2_MOSI	108	DO	SPI2 master-out slave-in		
SPI2_MISO	106	DI	SPI2 master-in slave-out	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
SPI3_CS	278	DO	SPI3 chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	Master and slave mode. 1.8 V power domain. Used for external V2X function by default. If unused, keep them open.
SPI3_CLK	276	DO	SPI3 clock		
SPI3_MOSI	277	DO	SPI3 master-out slave-in		
SPI3_MISO	275	DI	SPI3 master-in slave-out	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	

[12] The I/O is AI on AG568N-EU/-ROW/-NA.

				V_{IH}max = 2.1 V	
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	247	AI	General-purpose ADC interface	Voltage range: 0.04–1.78 V	If unused, connect them with ground.
ADC1	245	AI	General-purpose ADC interface		
ADC2	113	AI	General-purpose ADC interface	Voltage range: 0.05–1.45 V	
ADC3	60	AI	General-purpose ADC interface		
ADC4	163	AI	General-purpose ADC interface		
ADC5	166	AI	General-purpose ADC interface		
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	295	DIO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.4 V V_{IL}min = -0.3 V V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep these pins open.
GPIO2	296	DIO	General-purpose input/output		
GPIO3	297	DIO	General-purpose input/output		
GPIO4	298	DIO	General-purpose input/output		
GPIO5	116	DIO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
GPIO6	243	DIO	General-purpose input/output		
GPIO7	246	DIO	General-purpose input/output		
GPIO8	249	DIO	General-purpose input/output		
GPIO9	9	DIO	General-purpose input/output		
GPIO10	283	DIO	General-purpose input/output		

GPIO11	280	DIO	General-purpose input/output		
GPIO12	284	DIO	General-purpose input/output		
GPIO13	289	DIO	General-purpose input/output		
GPIO14	66	DIO	General-purpose input/output		
GPIO15	222	DIO	General-purpose input/output		Do not pull down this pin before powering on if the module does not need to enter Fast Meta mode. 1.8 V power domain. If unused, keep it open.
GPIO16	225	DIO	General-purpose input/output		
GPIO17	228	DIO	General-purpose input/output		
GPIO18	101	DIO	General-purpose input/output		1.8 V power domain. If unused, keep these pins open.
GPIO19	27	DIO	General-purpose input/output		
GPIO20	64	DIO	General-purpose input/output		
GPIO21	104	DIO	General-purpose input/output		
GPIO22	132	DIO	General-purpose input/output		Used for external V2X function by default. 1.8 V power domain. If unused, keep these pins open.
GPIO23	136	DIO	General-purpose input/output		
GPIO24	428	DIO	General-purpose input/output		
Coexistence Control Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
COEX_RXD	67	DI	LTE & WLAN/ Bluetooth coexistence receive	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep them open.

COEX_TXD	69	DO	LTE & WLAN/ Bluetooth coexistence transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
Analog Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC1_P	2	AI	Microphone analog input 1 (+)		The analog audio function is optional. It is not configured by default.
MIC1_N	1	AI	Microphone analog input 1 (-)		
MIC2_P	5	AI	Microphone analog input 2 (+)		
MIC2_N	4	AI	Microphone analog input 2 (-)		
MICBIAS	3	PO	Bias voltage output for microphone		
SPK1_P	268	AO	Analog audio differential output 1 (+)		
SPK1_N	266	AO	Analog audio differential output 1 (-)		
SPK2_P	269	AO	Analog audio differential output 2 (+)		
SPK2_N	270	AO	Analog audio differential output 2 (-)		
AGND	6	-	Analog ground		
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	83	DI	Force the module into emergency download mode	V_{IL}min = -0.3 V V_{IL}max = 0.3 V V_{IH}min = 1.2 V V_{IH}max = 3.5 V	1.8/3.3 V power domain. It is recommended to reserve test points.
DR_SYNC	95	DO	Dead reckoning sync	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep these pins open.
WAKEUP_OUT	102	DO	Wakeup signal from the module		
WAKEUP_IN	100	DI	External wakeup signal to the module	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
IMU_INT1	169	DI	IMU interrupt 1		

IMU_INT2	187	DI	IMU interrupt 2	V_{IH}max = 2.1 V
IMU_PWR_EN	181	DO	IMU power enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V
RESERVED Pins				
Pin Name	**Pin No.**			**Comment**
RESERVED	28, 45, 65, 82, 89, 119, 122, 123, 139, 142, 143, 152, 154, 157, 161, 170, 175, 178, 179, 184, 188, 190, 193, 196, 197, 200, 204, 205, 207, 214, 226, 227, 229, 231, 248, 252, 273, 274, 279, 281, 282, 285–288, 290–294, 299–306, 403, 422, 424			

2.6. EVB Kit

To help you develop applications with the module, Quectel supplies an evaluation board (V2X&5G EVB) with accessories to control or test the module. For more details, see ***document [1].***

3 Operating Characteristics

3.1. Operating Modes

The table below outlines operating modes of the module.

Table 7: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	The module remains registered on the network, and is ready to send and receive data. In this mode, the software is active.
	Voice/Data	The module is connected to network. Its power consumption varies with the network setting and data transfer rate.
Airplane Mode	**AT+CFUN=4** or device management related API function can set the module to airplane mode where the RF function is invalid.	
Minimum Functionality Mode	**AT+CFUN=0** or device management related API function can set the module to a minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.	
Sleep Mode	The module retains the ability to receive paging message, SMS, voice call and TCP/UDP data from the network normally. In this mode, the power consumption of the module is reduced to a very low level.	
Power Down Mode	The module's power supply is cut off by its power management unit. In this mode, the software is inactive, the serial interfaces are inaccessible, while the operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

NOTE

See ***document [2]*** for details of device management API functions, and ***document [3]*** for details of **AT+CFUN**.

3.2. Sleep Mode

The module is able to reduce the power consumption to a minimum value during the sleep mode. This chapter mainly introduces the way to enter or exit from sleep mode. The diagram below illustrates the power consumption of the module during the sleep mode. See ***document [4]*** for more details about the low power mode of the module.

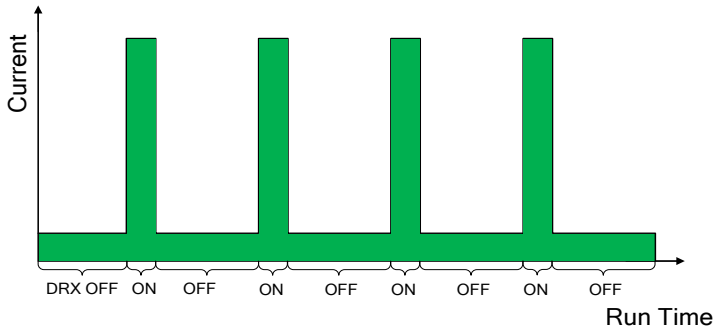


Figure 3: Sleep Mode Power Consumption Diagram

NOTE

The DRX cycle values are broadcasted by the wireless network.

3.2.1.1. USB Application Scenario (without USB Suspend Function)

If the host does not support USB suspend function, USB_VBUS should be connected with an external control circuit to set the module to sleep mode. In this case, the following three preconditions can make the module enter the sleep mode:

- Use sleep and wakeup related API functions to enable the sleep mode.
- Ensure that all pins configured to interrupt the wake-up function are in the non-wakeup state.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

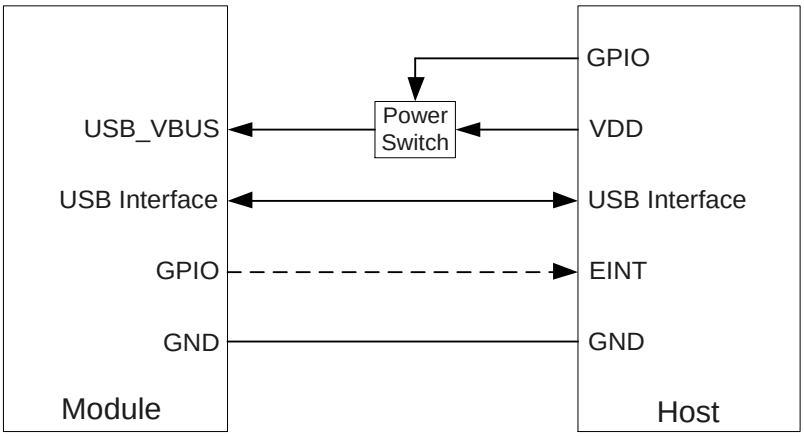


Figure 4: Sleep-Mode Application without Suspend Function

NOTE

1. Pay attention to the level match of the connection signals between the module and the external MCU.
2. USB_VBUS pin can turn on the module when it is turned off.

3.3. Airplane Mode

When the module enters airplane mode, the RF function does not work, and all AT commands and API functions correlative with RF function will be inaccessible.

AT command:

The mode can be set via **AT+CFUN=<fun>**. For more details about this command, see ***document [3]***. The parameter **<fun>** of **AT+CFUN** indicates the module's functionality levels, as shown below.

- **AT+CFUN=0:** Minimum functionality mode. (Both (U)SIM and RF functions are disabled.)
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. (RF function is disabled.)

API functions:

The mode can be set via device management related API functions. For more details about device management API functions, see ***document [2].***

NOTE

The execution of **AT+CFUN** or related API functions will not affect GNSS function.

3.4. Power Supply

3.4.1. Power Supply Pins

The module provides eleven VBAT pins dedicated to the connection with the external power supply. There are two separate voltage domains for VBAT.

- Eight VBAT_RF pins for RF part.
- Three VBAT_BB pins for BB part.

Table 8: Pin Definition of Power Supply

Pin Name	Pin No.	I/O	Description	Comment
VBAT_BB	241, 242, 244	PI	Power supply for the module's BB part	It must be provided with sufficient current up to 1.5 A.
VBAT_RF	109, 111, 112, 114, 235, 236, 238, 239	PI	Power supply for the module's RF part	It must be provided with sufficient current up to 2.0 A.
GND	12, 18, 26, 33, 42, 86, 92, 98, 115, 117, 118, 120, 121, 124–131, 133–135, 137, 138, 140, 141, 144–151, 153, 155, 156, 158, 159, 160, 162, 164, 165, 167, 168, 171–174, 176, 177, 180, 182, 183, 185, 186, 189, 191, 192, 194, 195, 198, 199, 201, 202, 203, 206, 208, 209, 211, 212, 215, 217, 218, 220, 221, 230, 232, 233, 234, 237, 240, 307–402, 404, 407–410, 413, 415, 417, 419, 421, 423, 425, 427			

3.4.2. Reference Design for Power Supply

The performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of 3.5 A at least. VBAT_BB needs at least 1.5 A and VBAT_RF needs at least 2 A.

If the voltage drop between the input and output is not too high, it is applicable to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply. If the input power supply is not within the power supply range of the module, it is necessary to add a power conversion circuit.

The following figure shows a reference design for DC +12 V/+24 V input power source. The designed output for the power supply is 3.8 V, and the maximum rated current is 5 A.

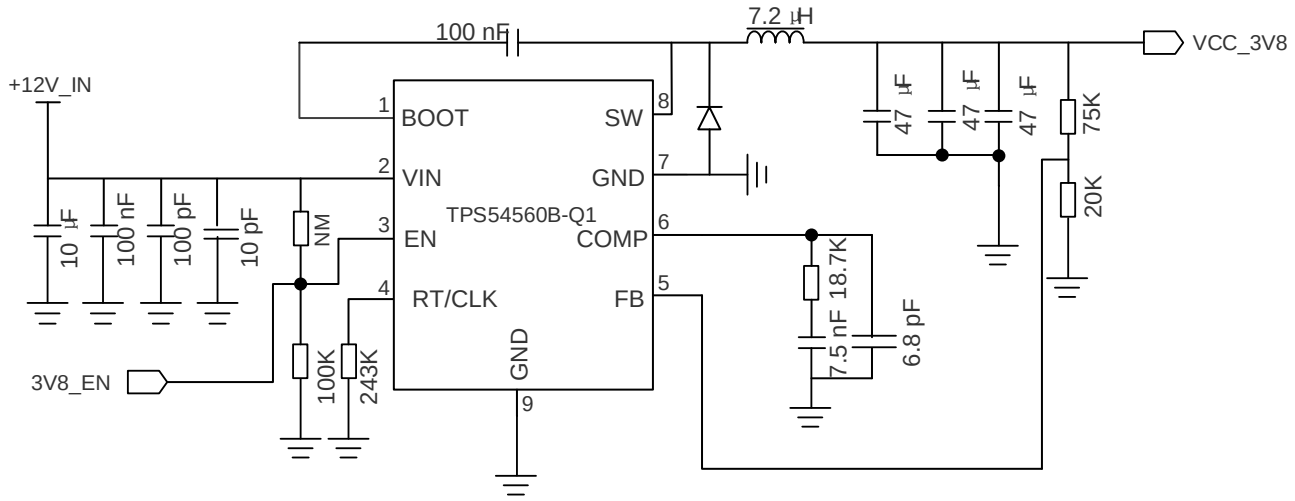


Figure 5: Reference Design of Power Supply

NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut off the power supply.

3.4.3. Voltage Stability Requirements

The power supply range of the module is from 3.3 V to 4.3 V. Please make sure the input voltage will never drop below 3.3 V.

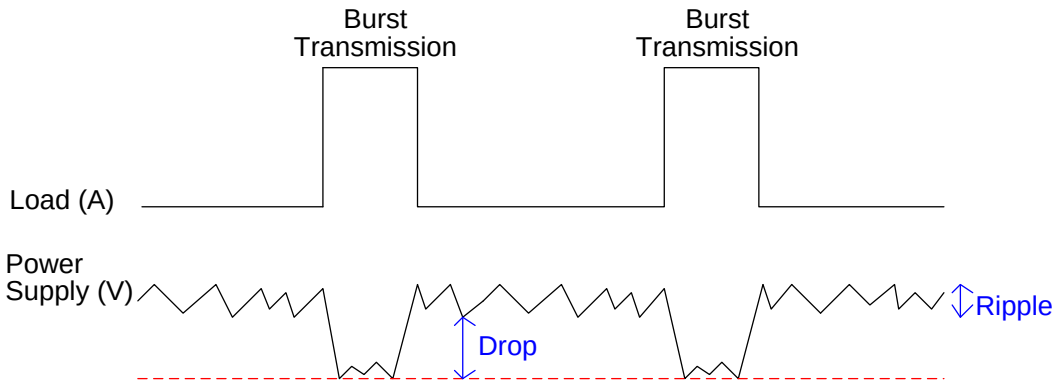


Figure 6: Power Supply Limits During Burst Transmission

To decrease the voltage drop, bypass capacitors of about 100 μF with low ESR should be used for VBAT_BB and VBAT_RF respectively, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to their ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application must be a single voltage source and can be expanded to two sub paths with the star structure. The width of VBAT_BB trace should be not less than 1.5 mm. The width of VBAT_RF trace should be not less than 2 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to get a stable power source, it is necessary to add two high-power TVS components at the front end of the power supply. Also, the TVS should be placed as close to the VBAT pins as possible.

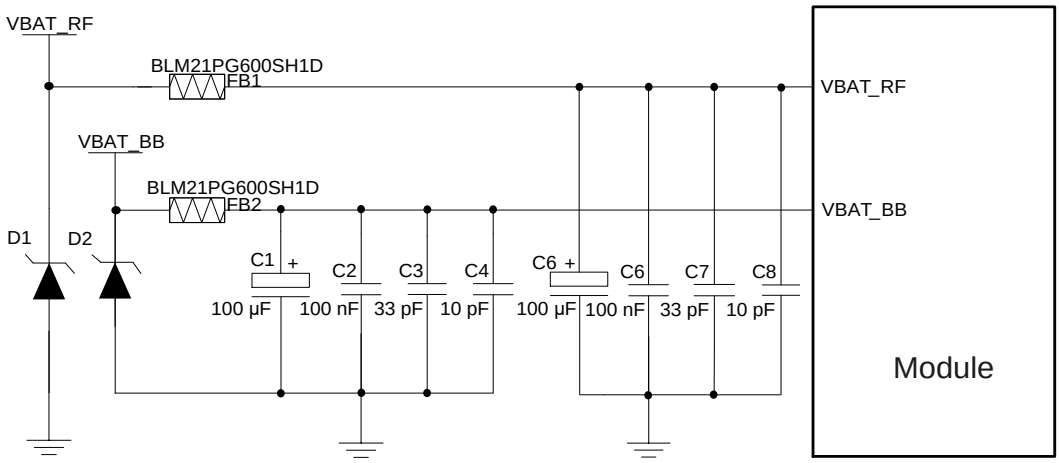


Figure 7: Star Structure of the Power Supply

3.5. Turn On

3.5.1. Turn On with PWRKEY

Table 9: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	7	DI	Turn on/off the module	Internally pulled up to 1.8 V. Active low.

When the module is in turn-off mode, it can be turned on by driving the PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY.

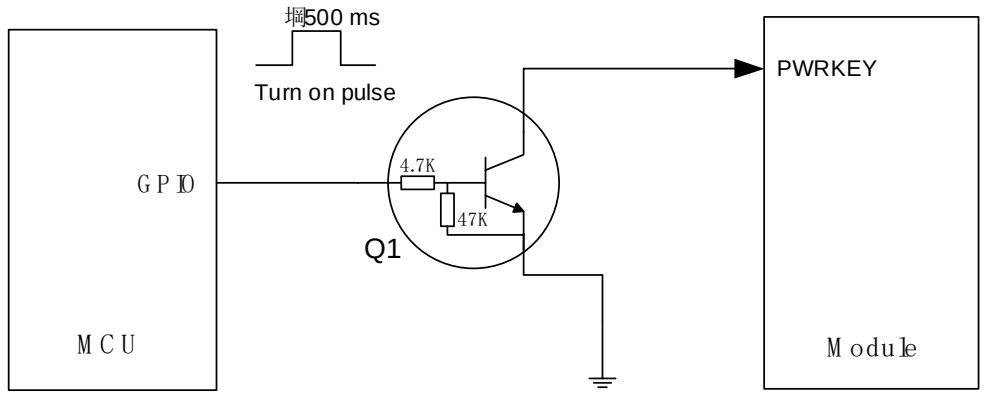


Figure 8: Turn On the Module Using Driving Circuit

Another way to control the PWRKEY is by using a button directly. When pressing the button, an electrostatic strike may generate from finger. Therefore, a TVS component shall be placed near the button for ESD protection.

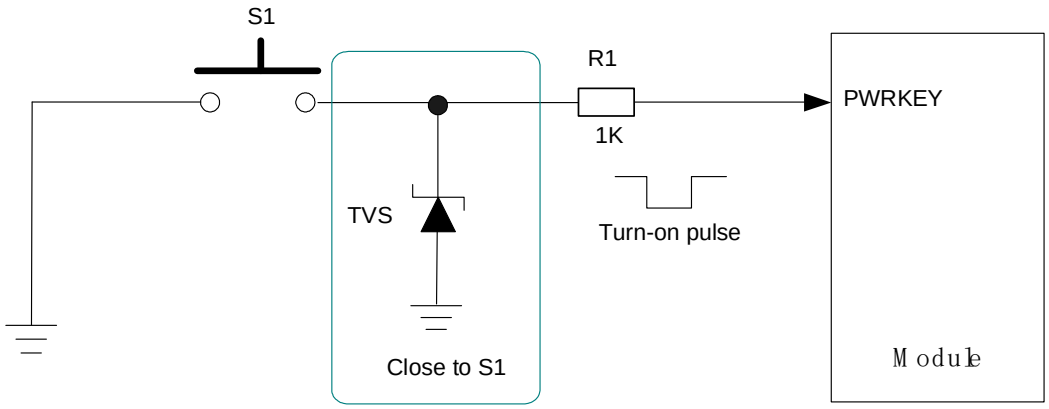


Figure 9: Turn On the Module Using a Button

The power-up timing is illustrated in the following figure.

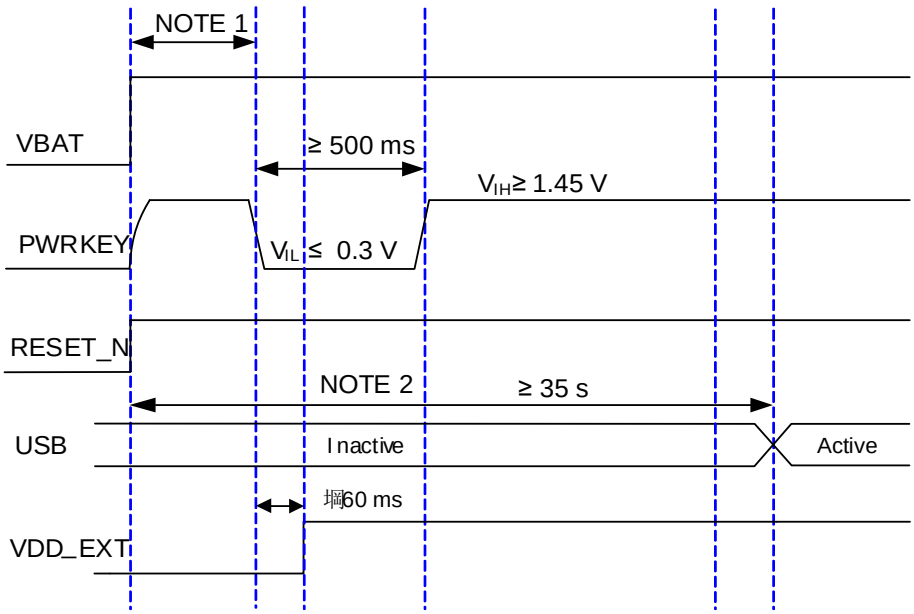


Figure 10: Power-up Timing

NOTE

1. Ensure that VBAT is stable for at least 30 ms before pulling down the PWRKEY.
2. If USB_VBUS is connected, the module will start automatically after power-on.
3. Do not connect PWRKEY to GND all the time. Pull up PWRKEY to a high level after the module is turned on.
4. It is recommended to use an external OD/OC circuit to control the PWRKEY.

3.6. Turn Off

The following procedures can be used to turn off the module normally.

3.6.1. Turn Off with PWRKEY

Driving PWRKEY low for at least 2 s, the module will execute power-down procedure after the PWRKEY is released.

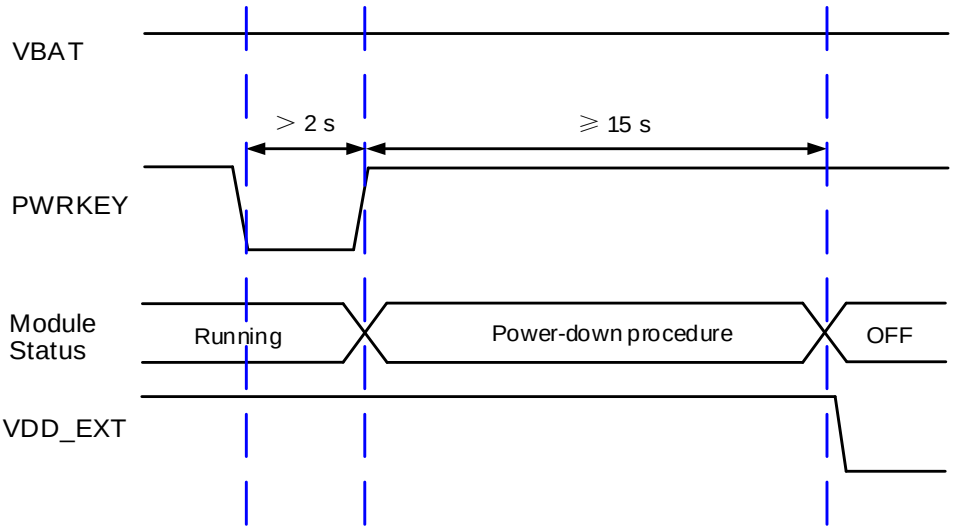


Figure 11: Power-down Timing

3.6.2. Turn Off with Linux Commands

The module can be turned off safely with Linux commands, such as **shutdown** and **poweroff**, which are similar to turning off the module via the PWRKEY pin.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after the module is turned off by PWRKEY or Linux commands, the power supply can be cut off.
2. When turning off the module with Linux commands, keep PWRKEY at a high level after the execution of the commands. Otherwise, the module will be turned on again after successfully turn-off.
3. Ensure that there is no large capacitance on PWRKEY pin.
4. Do not pull down PWRKEY to GND all the time (≥ 8 s). Driving PWRKEY high after the module executes power-down procedure.

3.7. Reset

The module can be reset by driving the RESET_N low for 250–550 ms and then releasing it. As the RESET_N pin is sensitive to interference, the routing trace is recommended to be as short as possible and totally ground surrounded.

Table 10: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	8	DI	Reset the module	Internally pulled up to 1.8 V. Active low. It is recommended to reserve test points.

The recommended circuit is equal to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

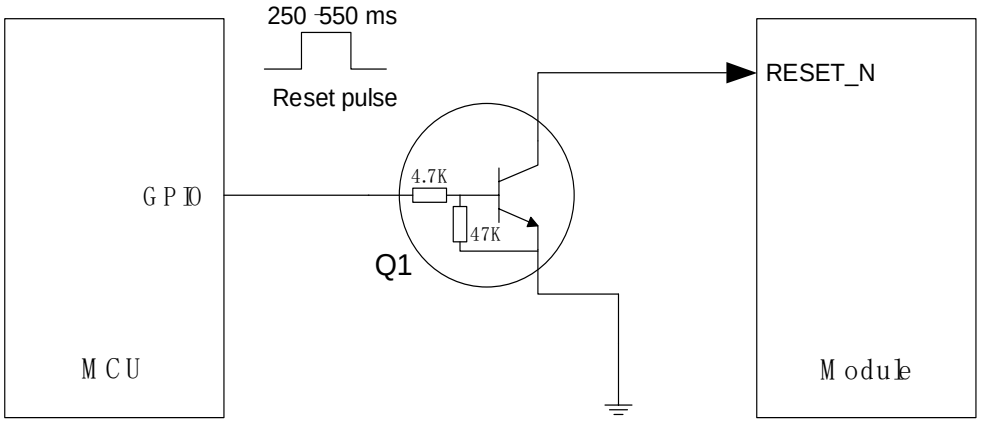


Figure 12: Reference Circuit of RESET_N with Driving Circuit

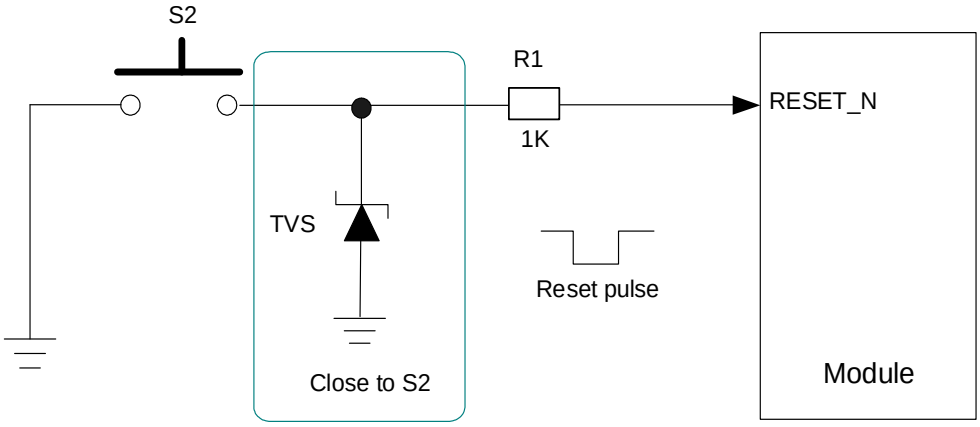


Figure 13: Reference Circuit of RESET_N with Button

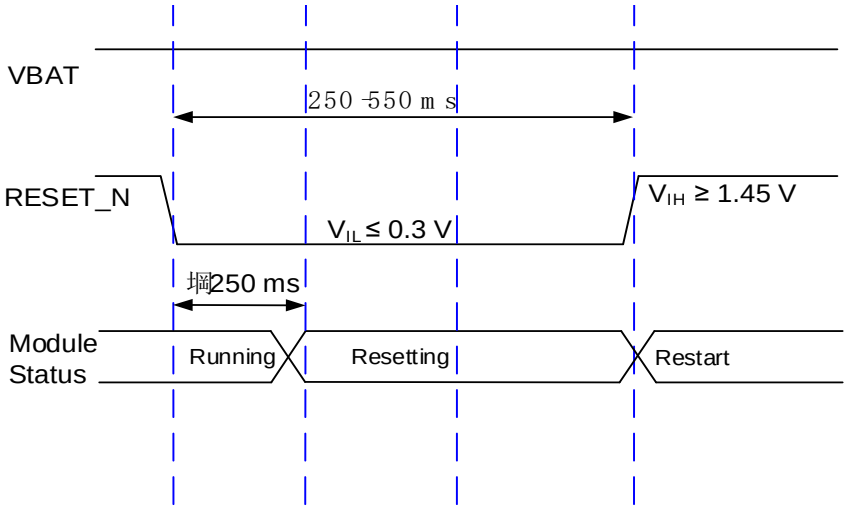


Figure 14: Reset Timing

NOTE

1. RESET_N should only be used when turning off the module by Linux commands and PWRKEY pin all failed.
2. Ensure that there is no large capacitance on RESET_N pin.

4 Application Interfaces

4.1. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface. The USB interface complies with the USB 3.1 and USB 2.0 specifications. USB 3.1 and USB 2.0 support data communication with external AP, and cannot be used simultaneously since they share the same controller. The USB interface supports SuperSpeed (5 Gbps) for USB 3.1, high-speed (480 Mbps), full-speed (12 Mbps) and low-speed (1.5 Mbps) for USB 2.0. It can be used for AT command communication, data transmission, software debugging, firmware upgrade, GNSS NMEA sentences output.

Pin definition of the USB interface is here as follows.

Table 11: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	84	DI	Turn-on/USB connection detect	It is recommended to keep it open before the module is powered on. Test points must be reserved.
USB_DP	85	AIO	USB 2.0 differential data (+)	Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	87	AIO	USB 2.0 differential data (-)	
USB_SS_TX_P	93	AO	USB 3.1 SuperSpeed transmit (+)	Require differential impedance of 90 Ω. If these pins are unused, connect Rx pairs with GND directly and keep other pins open.
USB_SS_TX_M	91	AO	USB 3.1 SuperSpeed transmit (-)	
USB_SS_RX_P	90	AI	USB 3.1 SuperSpeed receive (+)	
USB_SS_RX_M	88	AI	USB 3.1 SuperSpeed receive (-)	

Test points of USB 2.0 interface must be reserved, which can be used for debugging and firmware upgrading in your designs. The following figure shows a reference circuit of USB interface.

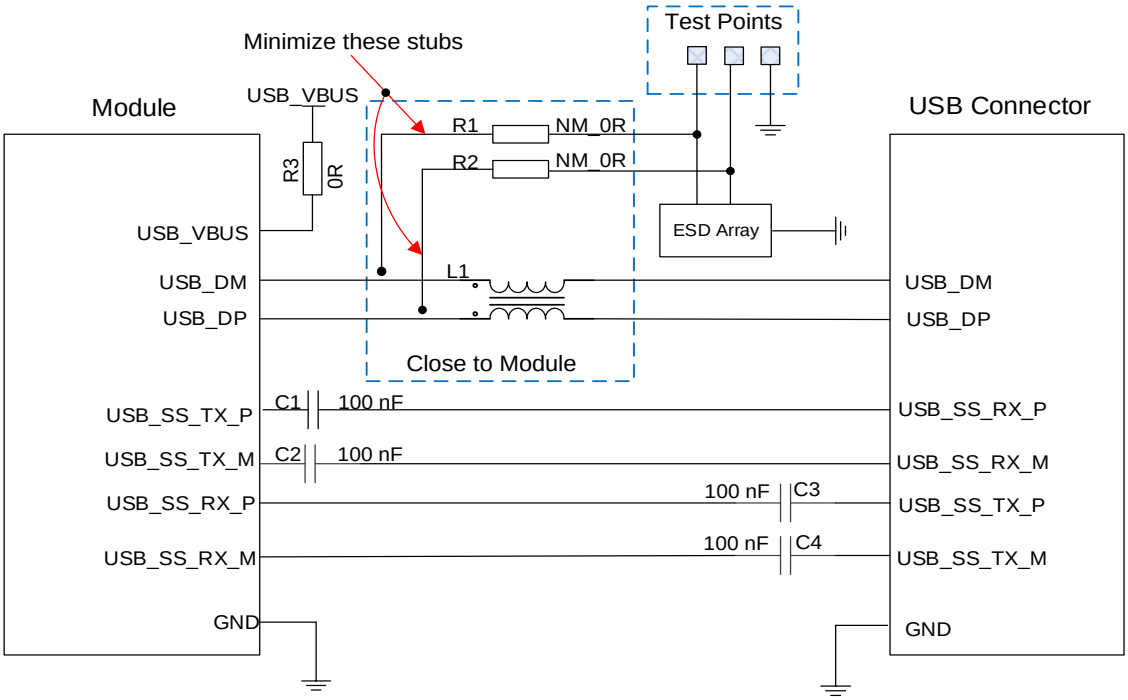


Figure 15: Reference Circuit of USB Application

For USB 2.0 application, a common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points to facilitate debugging, and the resistors are not mounted by default. To ensure the integrity of USB data trace signal, L1, R1 and R2 components must be placed close to the module, and also resistors R1 and R2 should be placed close to each other. The extra trace stubs must be as short as possible.

For USB 3.1 application, place C1 and C2 near the module, and place C3 and C4 near the other device. The extra stubs of trace must be as short as possible. As USB_VBUS is an input signal for turn-on condition, it is suggested to keep it open before the module is turned on.

To meet USB 2.0 and USB 3.1 specifications, the following principles of USB interface should be complied with.

- It is important to route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.
- For USB 2.0 signal traces, length matching of each differential data pair (Tx/Rx) should be less than 60 mil. For USB 3.1 signal traces, length matching of each differential data pair (Tx/Rx) should be less than 5 mil.

- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. It is important to route the USB differential traces in PCB inner-layer, and surround the traces with ground on that layer and ground planes above and below.
- Junction capacitance of the ESD protection device might cause influences on USB data traces, so pay attention to the selection of the device. Typically, the stray capacitance should be less than 3.0 pF for USB 2.0, and less than 0.5 pF for USB 3.1.
- If possible, reserve a 0 Ω resistor on USB_DP and USB_DM traces respectively.

For more details about the USB specifications, visit http://www.usb.org/home.

NOTE

1. The module supports USB host mode and slave mode, but works in slave mode only by default.
2. The high-speed PHY and SuperSpeed PHY share the same controller inside baseband chipset, so USB 2.0 and USB 3.1 cannot be used simultaneously.

4.2. UART Interfaces

The module provides four UART interfaces: UART1, UART2, UART3 and Debug UART. The module serves as DCE (Data Communication Equipment), which is connected in the traditional DCE-DTE (Data Terminal Equipment) mode. The features of UART interfaces are shown in the following table.

Table 12: Features of UART Interfaces

UART Types	Supported Baud Rates (bps)	Default Baud Rates (bps)	Functions
UART1 (Main UART interface)	4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600	115200	● Data transmission ● AT command communication ● RTS and CTS hardware flow control
UART2 (Bluetooth UART Interface)		9600	● Data transmission for Bluetooth function ● RTS and CTS hardware flow control
UART3 (V2X Interface)		9600	● External V2X function
Debug UART Interface	115200	115200	● Linux console ● Log output

Pin definition of the UART interface is here as follows:

Table 13: Pin Definition of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
UART1_CTS	71	DO	DTE clear to send signal from DCE	Connect to DTE's CTS. 1.8 V power domain. If unused, keep these pins open.
UART1_RTS	74	DI	DTE request to send signal to DCE	Connect to DTE's RTS. 1.8 V power domain. If unused, keep these pins open.
UART1_RXD	72	DI	UART1 receive	1.8 V power domain. If unused, keep these pins open.
UART1_TXD	70	DO	UART1 transmit	
UART2_TXD	59	DO	UART2 transmit	
UART2_RXD	63	DI	UART2 receive	
UART2_RTS	61	DI	DTE request to send signal from DCE	Connect to DTE's RTS. 1.8 V power domain. If unused, keep these pins open.
UART2_CTS	62	DO	DTE clear to send signal to DCE	Connect to DTE's CTS. 1.8 V power domain. If unused, keep these pins open.
UART3_RXD	411	DI	UART3 receive	Used for external V2X function by default. 1.8 V power domain. If unused, keep them open.
UART3_TXD	412	DO	UART3 transmit	
DBG_RXD	110	DI	Debug UART receive	1.8 V power domain. Test points must be reserved.
DBG_TXD	107	DO	Debug UART transmit	

The module provides 1.8 V UART interfaces. A voltage-level translator should be used if the application is equipped with a 3.3 V UART interface. The following figure shows a reference design.

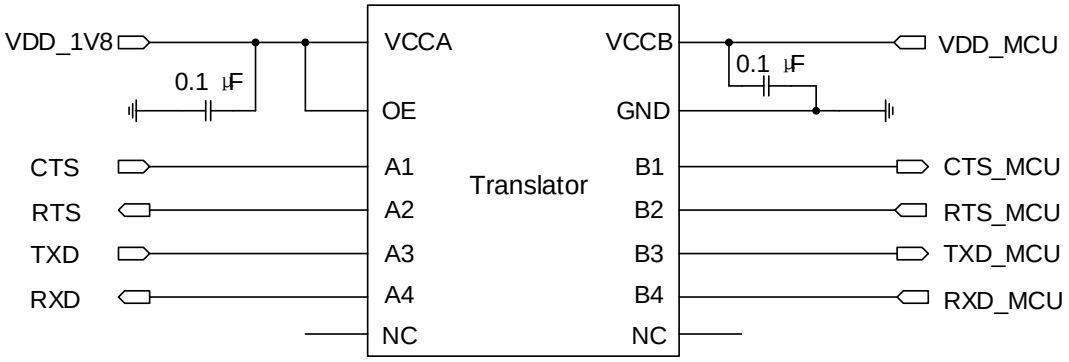


Figure 16: Reference Circuit with Translator Chip

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

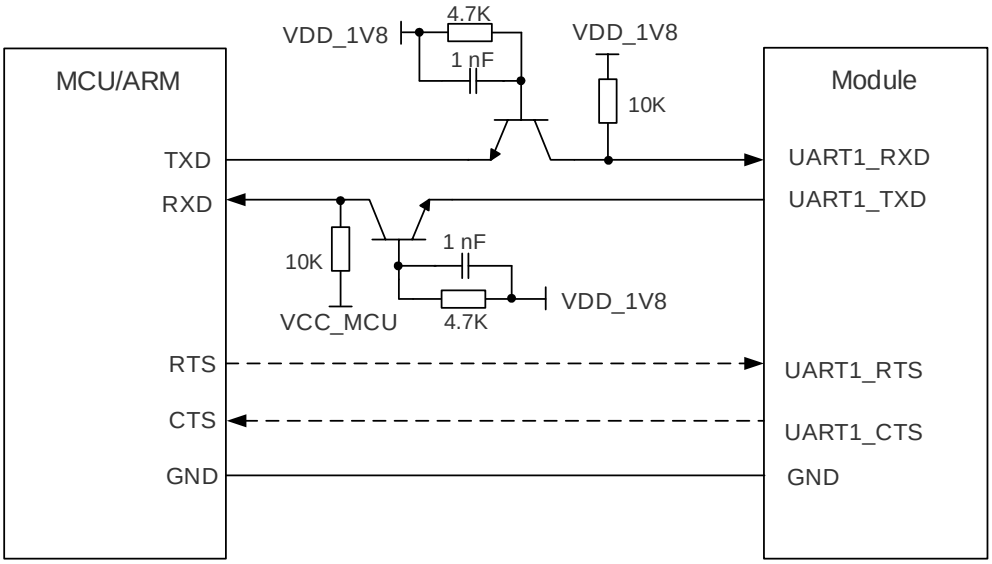


Figure 17: Reference Circuit with Transistor Circuit (UART1)

The following figure illustrates the reference design for UART2 interface connection between different modules.

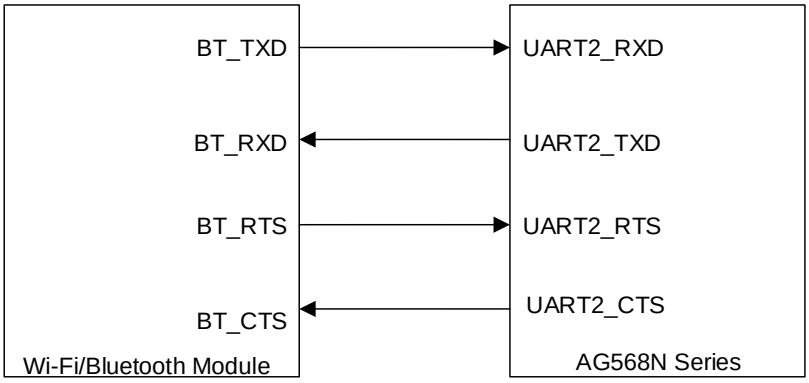


Figure 18: UART Interface Connection (UART2)

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. If hardware flow control function is intended to be used, then CTS and RTS should also be designed with the level-shifting circuit.
3. Please note that the module's CTS is connected to the host's CTS, and the module's RTS is connected to the host's RTS.

4.3. (U)SIM Interfaces

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V (U)SIM card is supported, and Dual SIM Dual Standby (DSDS) [13] function is supported.

Table 14: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	251	PO	(U)SIM1 card power supply	Either 1.8/3.0 V is supported by the module automatically.
USIM1_DATA	254	DIO	(U)SIM1 card data	If unused, keep these pins open.
USIM1_CLK	253	DO	(U)SIM1 card clock	
USIM1_RST	250	DO	(U)SIM1 card reset	
USIM1_DET	255	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep it open.

[13] DSDS function is optional.

USIM2_VDD	256	PO	(U)SIM2 card power supply	Either 1.8/3.0 V is supported by the module automatically.
USIM2_DATA	257	DIO	(U)SIM2 card data	If unused, keep these pins open.
USIM2_CLK	259	DO	(U)SIM2 card clock	
USIM2_RST	260	DO	(U)SIM2 card reset	
USIM2_DET	258	DI	(U)SIM2 card hot-plug detect	1.8 V power domain. If unused, keep it open.

The module supports (U)SIM card hot-plug via the USIM_DET pin, and both high and low level detection are supported. The function is enabled by default.

The following figure illustrates a reference design for (U)SIM card interface with an 8-pin (U)SIM card connector.

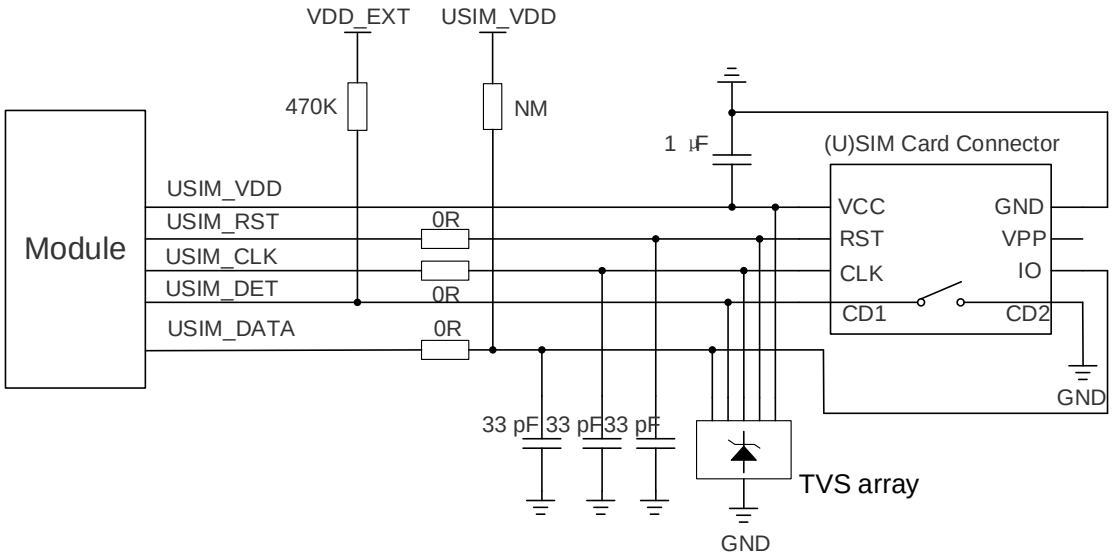


Figure 19: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_DET pin unconnected. A reference circuit for (U)SIM card interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

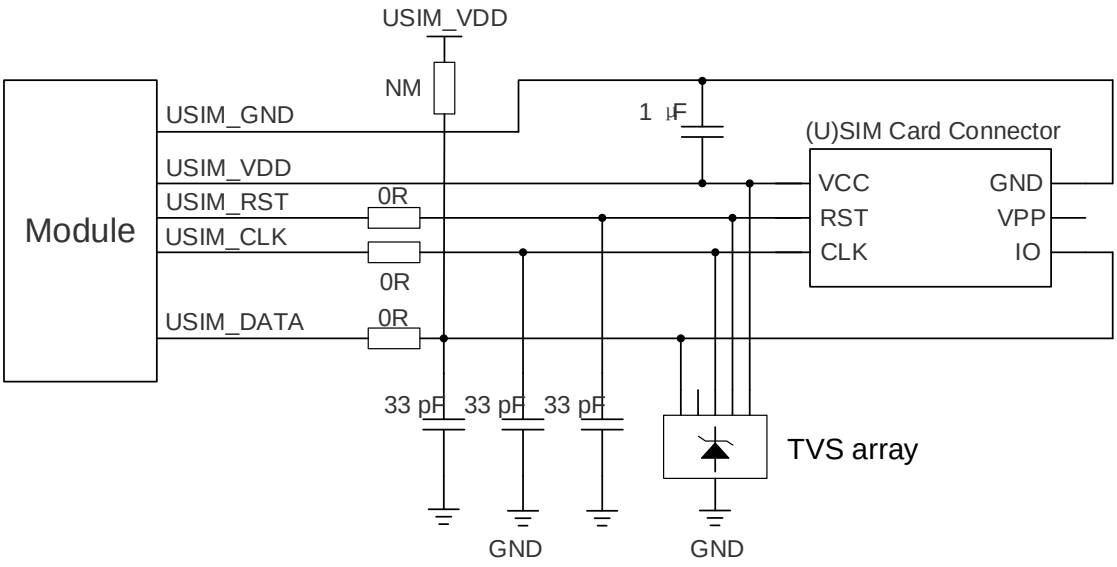


Figure 20: Reference Circuit of a 6-Pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in (U)SIM circuit design.

- Place the (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signal traces away from RF and power supply traces.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with ground surrounded.
- For better ESD protection, it is recommended to add a TVS array with a parasitic capacitance not exceeding 10 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card connector to suppress EMI spurious transmission and enhance ESD protection. The 33 pF capacitors are used for filtering out RF interference. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA trace improves anti-jamming capability when long layout trace and sensitive occasions are applied, and should be placed close to the (U)SIM card connector. It should be not mounted by default.
- Reserve 1 μF capacitor on the power rails of (U)SIM interface with shunt connection and the capacitor should be placed close to (U)SIM connector.

NOTE

The load capacitance of (U)SIM interfaces will affect the rising and falling time of the data exchange.

4.4. I2C Interfaces

The module provides two I2C interfaces. The I2C interfaces have been pulled to 1.8 V inside. It is recommended to reserve pull-up resistors and not mount by default.

Table 15: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C1_SCL	79	DO	I2C serial clock	1.8 V power domain. If unused, keep them open. Used for external audio codec IC. Reserve pull-up resistors and not mount by default.
I2C1_SDA	80	DIO	I2C serial data	
I2C2_SCL	267	DO	I2C serial clock	1.8 V power domain. If unused, keep them open. Used for external IMU sensor. Reserve pull-up resistors and not mount by default.
I2C2_SDA	264	DIO	I2C serial data	

4.5. I2S Interface

The module provides one I2S interface, supports 8–192 kHz sampling rates.

Table 16: Pin Definition of I2S Interface

Pin Name	Pin No.	I/O	Description	Comment
I2S_WS	265	DIO	I2S word select	1.8 V power domain. If unused, keep these pins open.
I2S_DIN	263	DI	I2S data input	
I2S_DOUT	261	DO	I2S data output	
I2S_CLK	262	DIO	I2S clock	
MCLK	81	DO	Master clock output for codec	
CDC_RESET_N	77	DO	External codec reset	

The following figure shows a reference design of I2S interface with an external codec IC.

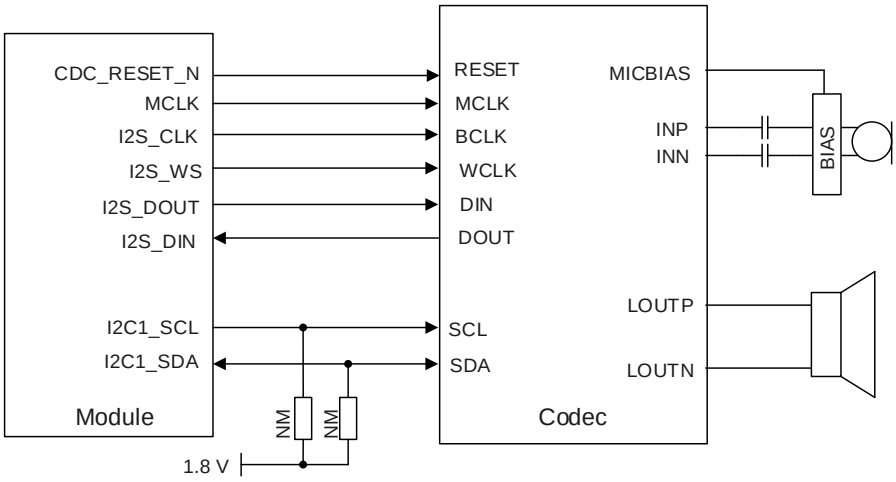


Figure 21: I2S and I2C1 Application with External Audio Codec

NOTE

The module works as a master device pertaining to I2C interface.

4.6. PCM Interface

The module provides one Pulse Code Modulation (PCM) digital interface for Bluetooth audio transmission by default. The interface supports master and slave modes.

Table 17: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	73	DIO	PCM data frame sync	1.8 V power domain. If unused, keep these pins open.
PCM_CLK	75	DIO	PCM clock	
PCM_DIN	76	DI	PCM data input	
PCM_DOUT	78	DO	PCM data output	

4.7. WLAN and Bluetooth Application Interfaces

The module provides one PCIe interface for WLAN function (see ***Chapter 4.17*** for more details), and one Bluetooth UART and one PCM interface for Bluetooth function (see ***Chapter 4.2*** and ***Chapter 4.6*** for more details).

The following table shows the pin definition of coexistence control interface.

Table 18: Pin Definition of Coexistence Control Interface

Pin Name	Pin No.	I/O	Description	Comment
COEX_RXD	67	DI	LTE & WLAN/Bluetooth coexistence receive	1.8 V power domain. If unused, keep them open.
COEX_TXD	69	DO	LTE & WLAN/Bluetooth coexistence transmit	

The following figure shows a reference design of interfaces for WLAN and Bluetooth applications.

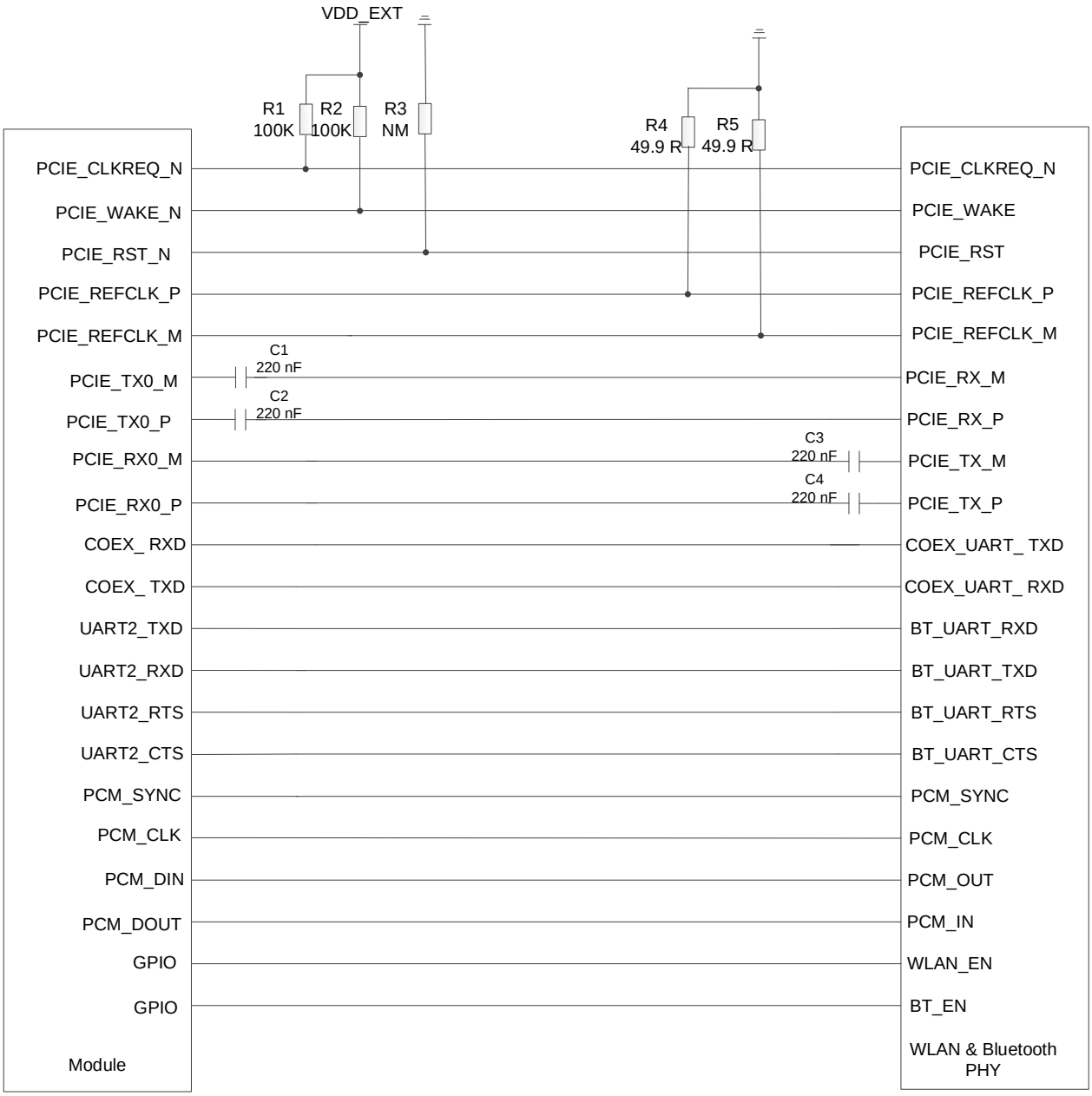


Figure 22: WLAN & Bluetooth Application Interfaces Connection Block Diagram

4.8. Analog Audio Interfaces (Optional)

The module is designed with a built-in audio codec to enable analog audio function. The analog audio interfaces are optional. If you need this function, please contact Quectel Technical Support.

Table 19: Pin Definition of Analog Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MIC1_P	2	AI	Microphone analog input 1 (+)	The analog audio function is optional. It is not configured by default.
MIC1_N	1	AI	Microphone analog input 1 (-)	
MIC2_P	5	AI	Microphone analog input 2 (+)	
MIC2_N	4	AI	Microphone analog input 2 (-)	
MICBIAS	3	PO	Bias voltage output for microphone	
SPK1_P	268	AO	Analog audio differential output 1 (+)	
SPK1_N	266	AO	Analog audio differential output 1 (-)	
SPK2_P	269	AO	Analog audio differential output 2 (+)	
SPK2_N	270	AO	Analog audio differential output 2 (-)	
AGND	6	-	Analog ground	

4.9. GPIOs

The module provides 24 GPIOs for your design, which all support wake-up interrupt.

Table 20: Pin Description of GPIO Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GPIO1	295	DIO	General-purpose input/output	1.8 V power domain. If unused, keep these pins open.
GPIO2	296	DIO	General-purpose input/output	
GPIO3	297	DIO	General-purpose input/output	
GPIO4	298	DIO	General-purpose input/output	
GPIO5	116	DIO	General-purpose input/output	
GPIO6	243	DIO	General-purpose input/output	

GPIO7	246	DIO	General-purpose input/output	
GPIO8	249	DIO	General-purpose input/output	
GPIO9	9	DIO	General-purpose input/output	
GPIO10	283	DIO	General-purpose input/output	
GPIO11	280	DIO	General-purpose input/output	
GPIO12	284	DIO	General-purpose input/output	
GPIO13	289	DIO	General-purpose input/output	
GPIO14	66	DIO	General-purpose input/output	
GPIO15	222	DIO	General-purpose input/output	Do not pull down this pin before powering on if the module does not need to enter Fast Meta mode. 1.8 V power domain. If unused, keep it open.
GPIO16	225	DIO	General-purpose input/output	1.8 V power domain. If unused, keep these pins open.
GPIO17	228	DIO	General-purpose input/output	
GPIO18	101	DIO	General-purpose input/output	
GPIO19	27	DIO	General-purpose input/output	
GPIO20	64	DIO	General-purpose input/output	
GPIO21	104	DIO	General-purpose input/output	
GPIO22	132	DIO	General-purpose input/output	Used for external V2X function by default. 1.8 V power domain. If unused, keep these pins open.
GPIO23	136	DIO	General-purpose input/output	
GPIO24	428	DIO	General-purpose input/output	

4.10. SDIO Interface

The module provides one SDIO interface only for eMMC application, which supports eMMC 5.1 protocol and HS400 mode.

Table 21: Pin Definition of SDIO Interface

Pin Name	Pin No.	I/O	Description	Comment
EMMC_RST	54	DO	eMMc reset	1.8 V power domain. If unused, keep these pins open.
SDIO_DATA0	49	DIO	SDIO data bit 0	
SDIO_DATA1	50	DIO	SDIO data bit 1	
SDIO_DATA2	51	DIO	SDIO data bit 2	
SDIO_DATA3	52	DIO	SDIO data bit 3	
SDIO_DATA4	53	DIO	SDIO data bit 4	
SDIO_DATA5	55	DIO	SDIO data bit 5	
SDIO_DATA6	56	DIO	SDIO data bit 6	
SDIO_DATA7	58	DIO	SDIO data bit 7	
SDIO_CMD	48	DIO	SDIO command	
SDIO_CLK	47	DO	SDIO clock	
SDIO_DSL	57	DI	SDIO data strobe	

4.10.1. Reference Design for eMMC Application

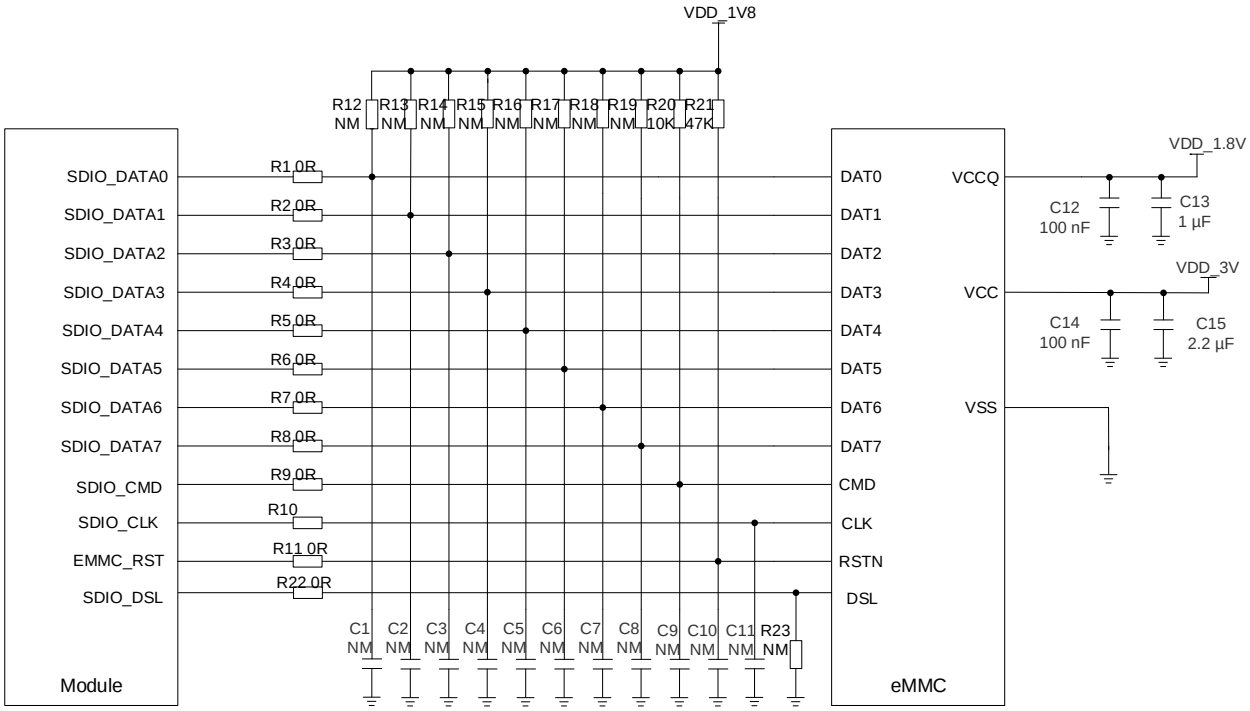


Figure 23: Reference Design for eMMC Application

Follow the principles below in eMMC circuit design:

- To avoid jitter of bus, it is recommended to reserve resistors R12–R19 (10–100 kΩ) to pull up SDIO traces to VDD_1V8. R12–R19 are not mounted by default.
- To improve signal quality, it is recommended to add 0 Ω R1–R9, R11 and R22 in series between the module and eMMC. The resistance of R10 depends on your specific device. R23 and bypass capacitors C1–C11 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- SDIO signal traces should comply with the following principles:
  1) It is important to route the SDIO signal traces with ground surrounded. The impedance of SDIO data trace should be 50 Ω ±10 %.
  2) Keep the spacing between adjacent SDIO_DATA traces and spacing between SDIO_DATA and SDIO_CLK traces two times the trace width.
  3) Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
  4) It is recommended to keep the trace length difference between SDIO_CLK and SDIO_DATA[0:7]/SDIO_CMD less than 1 mm and the total routing length less than 50 mm. The total trace length inside the module is 10 mm, so the exterior total trace length should be less than 40 mm.
  5) Keep the spacing between SDIO and other signal traces at least two times the trace width and the load capacitance of SDIO bus less than 3 pF.

4.11. ADC Interfaces

The module provides six Analog-to-Digital Converter (ADC) interfaces. In order to improve the accuracy of ADC, the trace of ADC interfaces should be surrounded by ground.

Table 22: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	247	AI	General-purpose ADC interface	If unused, connect them with ground.
ADC1	245	AI	General-purpose ADC interface	
ADC2	113	AI	General-purpose ADC interface	
ADC3	60	AI	General-purpose ADC interface	
ADC4	163	AI	General-purpose ADC interface	
ADC5	166	AI	General-purpose ADC interface	

The resolution of ADC0 and ADC1 is 15-bit, ADC2–ADC5 is 12-bit. The following table describes the characteristics of the ADC interfaces.

Table 23: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.
ADC0 Voltage Range	0.04 V	-	1.78 V
ADC1 Voltage Range		-	
ADC2 Voltage Range	0.05 V	-	1.45 V
ADC3 Voltage Range		-	
ADC4 Voltage Range		-	
ADC5 Voltage Range		-	
ADC Resolution	-	ADC0 & ADC1: 15 bit ADC2–ADC5: 12 bit	-
ADC Sample Rate	-	ADC0 & ADC1: 100 kHz ADC2–ADC5: 3.25 MHz	-

NOTE

1. The input voltage of ADC should not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC pin when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.

4.12. SGMII Interface

The module includes an integrated Ethernet MAC with an SGMII interface and one MDIO management interface. Key features of the SGMII interface are shown below:

- IEEE 802.3 compliance
- Supports 10/100/1000/2500 Mbps in full duplex mode and 10/100 Mbps in half duplex mode
- Can be connected to an external Ethernet PHY or an external switch
- The power domain of management interface: 1.8 V

Table 24: Pin Definition of SGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
SGMII_RX_P	97	AI	SGMII receive (+)	Requires differential impedance of 100 Ω. If unused, connect Rx pairs with GND directly and keep other pins open.
SGMII_RX_M	99	AI	SGMII receive (-)	
SGMII_TX_P	94	AO	SGMII transmit (+)	
SGMII_TX_M	96	AO	SGMII transmit (-)	
SGMII_INT	223	DI	PHY interrupt output	1.8 V power domain. If unused, keep these pins open.
SGMII_RST	224	DO	SGMII reset external PHY	
SGMII_MDIO_DATA	271	DIO	SGMII management data	
SGMII_MDIO_CLK	272	DO	SGMII management data clock	

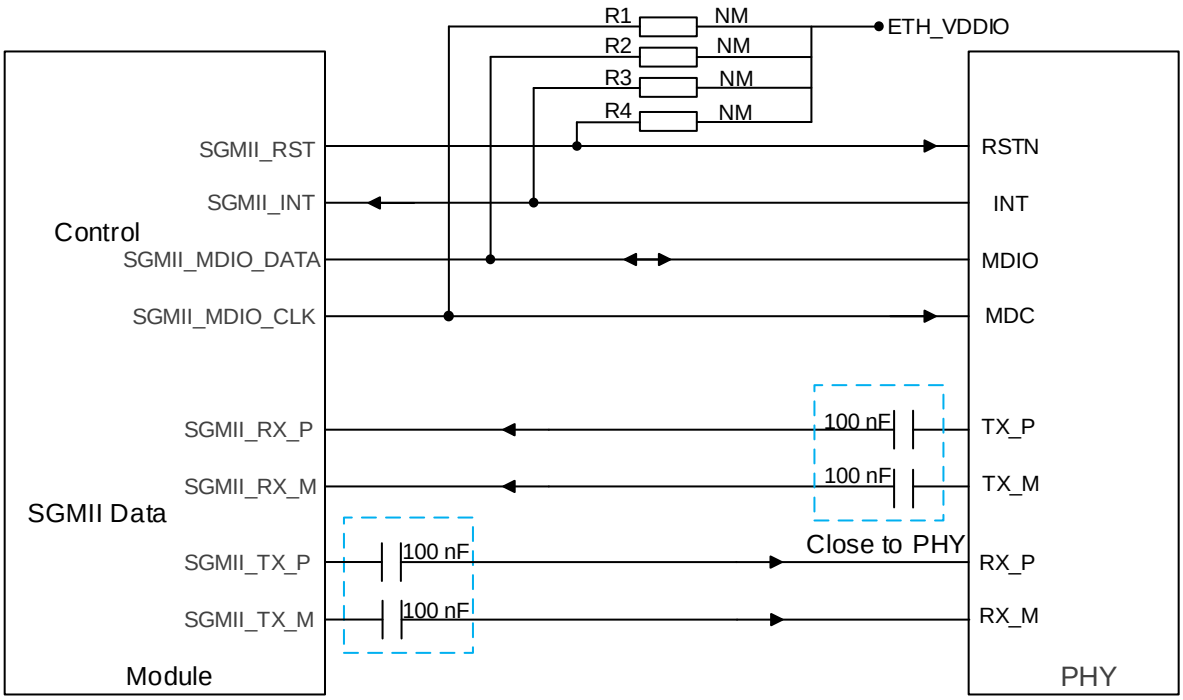


Figure 24: Reference Circuit of SGMII Interface with PHY Application

To enhance the reliability and availability of your application, follow the criteria below in the SGMII circuit design:

- Keep SGMII data and control signals away from RF and power supply traces.
- Keep the maximum trace length less than 12.7 cm and keep skew on the differential pairs less than 5 mils.
- The differential impedance of SGMII data trace should be 100 Ω ±10 %.
- To minimize crosstalk, the distance between separate adjacent pairs that are on the same layer must be equal to or larger than 40 mils.
- It is recommended to be less than 2 total vias in the differential pair.
- It is recommended to insert GND between SGMII_MDIO_CLK and SGMII_MDIO_DATA to prevent crosstalk.
- Both SGMII_TX_P and SGMII_TX_N should be connected to 100 nF AC coupling capacitance.

4.13. RGMII Interface

The module provides one RGMII interface, which can be connected with a PHY IC.

- Supports IEEE 1588–2008, IEEE 802.1AS-2011 and IEEE 802.1-Qav-2009
- Supports half/full duplex for 10/100/1000 Mbps
- Supports connection to an external Ethernet PHY or an external switch

Table 25: Pin Definition of RGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
RGMII_MD_IO	10	DIO	RGMII management data	Single-ended impedance of 50 Ω. 1.8 V power domain. If unused, keep them open.
RGMII_MD_CLK	11	DO	RGMII management data clock	
RGMII_RX_0	13	DI	RGMII receive data bit 0	
RGMII_RX_1	14	DI	RGMII receive data bit 1	
RGMII_RX_2	16	DI	RGMII receive data bit 2	
RGMII_RX_3	17	DI	RGMII receive data bit 3	
RGMII_CK_RX	19	DI	RGMII receive clock	
RGMII_CTL_RX	15	DI	RGMII receive control	
RGMII_TX_0	20	DO	RGMII transmit data bit 0	
RGMII_TX_1	22	DO	RGMII transmit data bit 1	
RGMII_TX_2	23	DO	RGMII transmit data bit 2	
RGMII_TX_3	25	DO	RGMII transmit data bit 3	
RGMII_CK_TX	24	DO	RGMII transmit clock	
RGMII_CTL_TX	21	DO	RGMII transmit control	1.8 V power domain. If unused, keep them open.
RGMII_INT	29	DI	PHY interrupt output	
RGMII_RST	31	DO	RGMII reset external PHY	

The following figure shows a reference design of RGMII interface with PHY application. For more details, see ***document [5].***

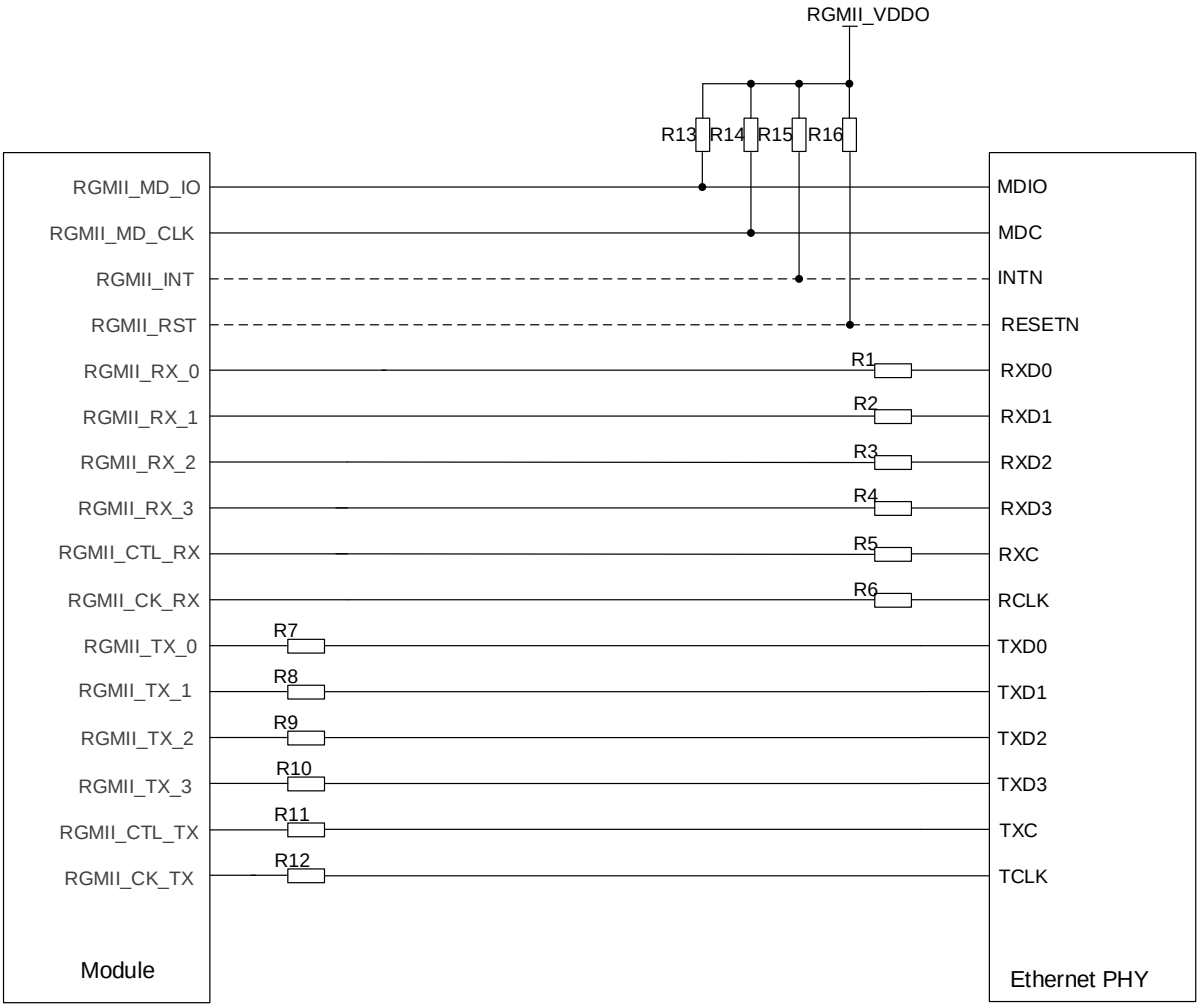


Figure 25: Reference Circuit of RGMII Interface with PHY Application

To enhance the reliability and availability of your application design, follow the criteria below in the Ethernet PHY circuit design:

- Keep RGMII data and control signals away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- The single-ended impedance of RGMII data traces should be 50 Ω ±20 %.
- The length match within Tx signal traces (RGMII_CK_TX, RGMII_CTL_TX and RGMII_TX_[0:3]) and Rx signal traces (RGMII_CK_RX, RGMII_CTL_RX and RGMII_RX_[0:3]) should be less than 2 mm.
- Keep the spacing between Tx bus and Rx bus traces at least 2.5 times trace width.
- Keep the spacing between Tx bus traces (RGMII_CK_TX, RGMII_CTL_TX, RGMII_TX_[0:3]) or that between Rx bus traces (RGMII_CK_RX, RGMII_CTL_RX, RGMII_RX_[0:3]) at least twice the trace width.
- Keep the spacing between of RGMII and other signal traces at least 3 times trace width.
- The resistors R7–R12 should be placed near the module. The resistors R1–R6 should be placed near the Ethernet PHY. The value of R1–R12 may be varied with the selection of PHY.

4.14. RTC

The module has a real time clock within the PMIC, but has no dedicated RTC power supply pin. The RTC is powered by VBAT_BB. If VBAT_BB is removed, the RTC will not be maintained. Therefore, VBAT_BB must be powered continuously in actual applications if you need to maintain the RTC function.

4.15. SPI Interfaces

The module provides three SPI interfaces. SPI1 and SPI2 only support master mode. SPI3 supports both master and slave modes. The maximum clock frequency is up to 50 MHz at master mode and 26 MHz at slave mode.

Table 26: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI1_CS	213	DO	SPI1 chip select	Master mode only. 1.8 V power domain. If unused, keep them open.
SPI1_CLK	216	DO	SPI1 clock	
SPI1_MOSI	210	DO	SPI1 master-out slave-in	
SPI1_MISO	219	DI	SPI1 master-in slave-out	
SPI2_CS	105	DO	SPI2 chip select	
SPI2_CLK	103	DO	SPI2 clock	
SPI2_MOSI	108	DO	SPI2 master-out slave-in	
SPI2_MISO	106	DI	SPI2 master-in slave-out	
SPI3_CS	278	DO	SPI3 chip select	Master and slave mode. 1.8 V power domain. Used for external V2X function by default. If unused, keep them open.
SPI3_CLK	276	DO	SPI3 clock	
SPI3_MOSI	277	DO	SPI3 master-out slave-in	
SPI3_MISO	275	DI	SPI3 master-in slave-out	

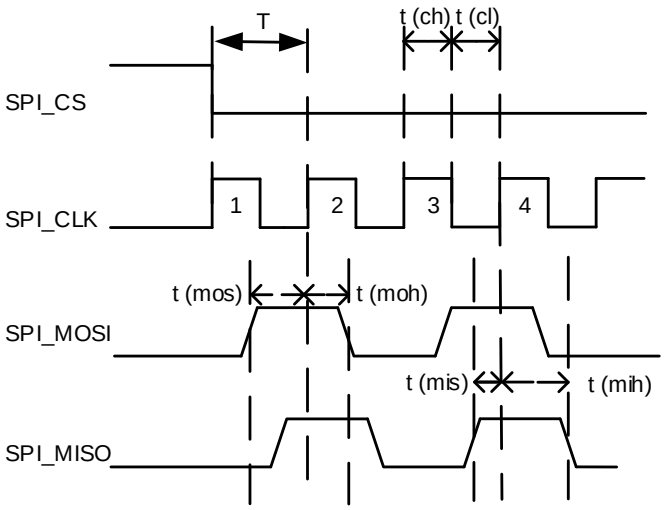


Figure 26: SPI Interfaces Timing in Master Mode

The related parameters of SPI timing in master mode are listed in the following table.

Table 27: Parameters of SPI Interfaces Timing in Master Mode

Parameter	Description	Min.	Typ.	Max.	Unit
T	SPI clock cycle	-	-	50	MHz
t (ch)	SPI clock high-level period	7.2	-	-	ns
t (cl)	SPI clock low-level period	7.2	-	-	ns
t (mos)	SPI master data output setup time	7.1	-	-	ns
t (moh)	SPI master data output hold time	7.1	-	-	ns
t (mis)	SPI master data input setup time	0	-	-	ns
t (mih)	SPI master data input hold time	0	-	-	ns

The module provides three 1.8 V SPI interfaces. A voltage-level translator between the module and the host should be used if the application is equipped with a 3.3 V processor or device interface.

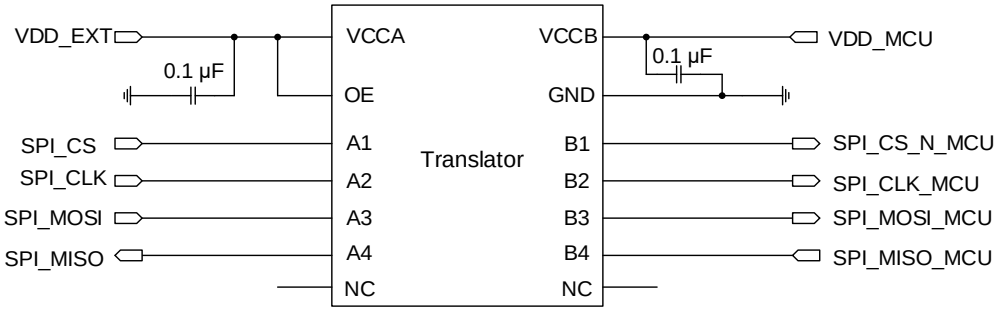


Figure 27: Reference Circuit of SPI Interfaces with a Voltage-level Translator

4.16. USB_BOOT

The module provides a USB_BOOT pin. Pull up USB_BOOT to VDD_EXT or external MCU controlling pin before powering on the module, thus the module will enter emergency download mode when powered on. In this mode, the module supports firmware upgrade over USB 2.0 interface.

Table 28: Pin Definition of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	83	DI	Force the module into emergency download mode	1.8/3.3 V power domain. It is recommended to reserve test points.

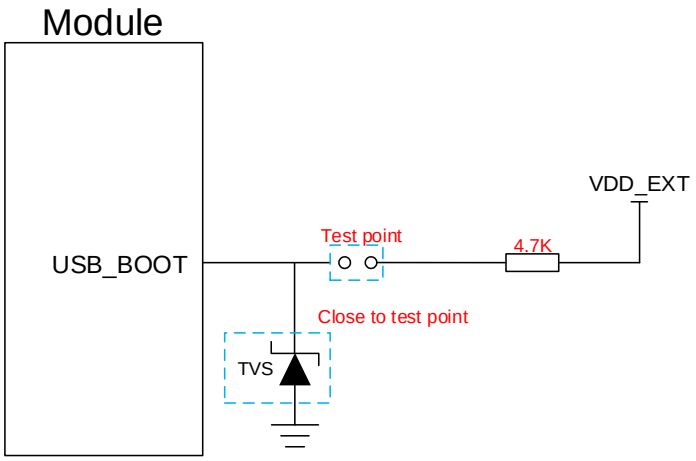


Figure 28: Reference Circuit of USB_BOOT

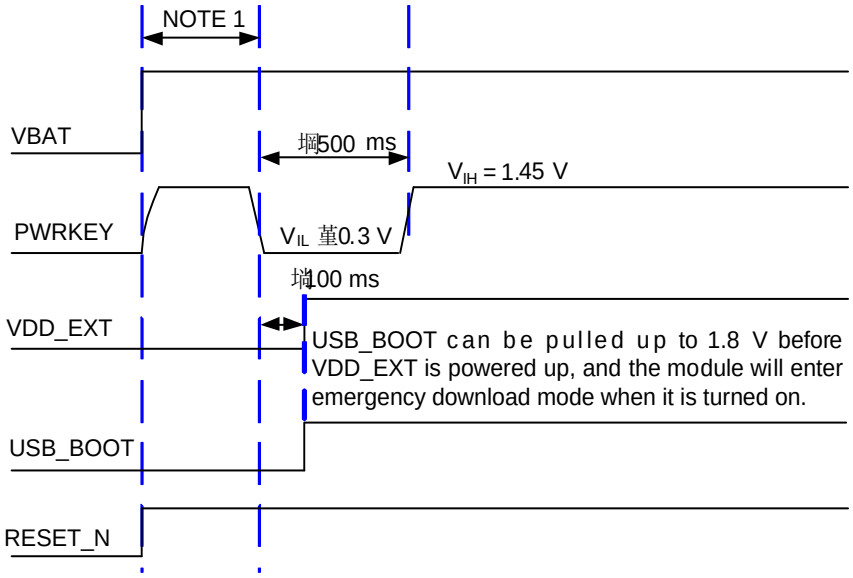


Figure 29: Timing Sequence for Entering Emergency Download Mode

NOTE

1. Ensure VBAT is stable before driving PWRKEY low. The time period between powering VBAT up and driving PWRKEY low shall be not less than 30 ms.
2. Follow the above timing sequence when using MCU to control the module to enter the emergency download mode. Do not pull up USB_BOOT to VDD_EXT or external MCU controlling pin before powering up VBAT. Directly connect the test points as shown in ***Figure 28*** can manually force the module to enter emergency download mode.

4.17. PCIe Interface

The module provides an integrated PCIe (Peripheral Component Interconnect Express) interface which follows *PCI Express Base Specification Revision 3.0*. The key features of the PCIe interface are mentioned below:

- *PCI Express Base Specification Revision 3.0* compliant
- Supports 2-lane and maximum data rate at 8 Gbps/lane.
- Dedicated to connect to an external WLAN IC and used for Wi-Fi communication by default.
- The module supports RC and EP mode in hardware design, but only supports RC mode in the software design.

Table 29: Pin Definition of PCIe Interface

Pin Name	Pin No.	I/O	Description	Comment
PCIE_REFCLK_P	40	AIO	PCIe reference clock (+)	Compliant with PCIe revision 3.0 specification. Requires differential impedance of 85 Ω. If unused, connect Rx pairs with GND directly and keep others open.
PCIE_REFCLK_M	38	AIO	PCIe reference clock (-)	
PCIE_TX0_P	46	AO	PCIe transmit 0 (+)	
PCIE_TX0_M	44	AO	PCIe transmit 0 (-)	
PCIE_RX0_P	34	AI	PCIe receive 0 (+)	
PCIE_RX0_M	32	AI	PCIe receive 0 (-)	
PCIE_TX1_P	43	AO	PCIe transmit 1 (+)	
PCIE_TX1_M	41	AO	PCIe transmit 1 (-)	
PCIE_RX1_P	37	AI	PCIe receive 1 (+)	
PCIE_RX1_M	35	AI	PCIe receive 1 (-)	
PCIE_CLKREQ_N	36	DIO	PCIe clock request	1.8 V power domain. If unused, keep these pins open.
PCIE_RST_N	39	DO	PCIe reset	
PCIE_WAKE_N	30	DI	PCIe wake up	

The following figure illustrates the PCIe interface connection.

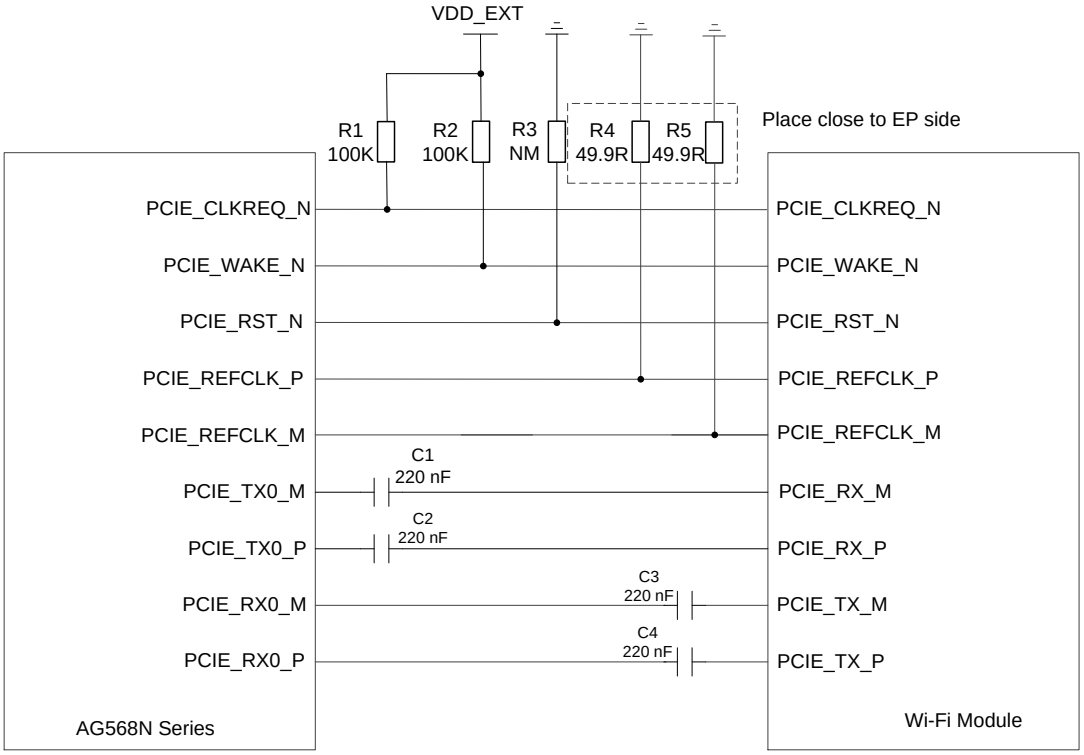


Figure 30: PCIe Interface Connection

The following principles of PCIe interface design should be complied with to meet PCIe specifications.

- It is important to route the PCIe signal and PCIE_REFCLK traces as differential pairs with ground surrounded. The differential impedance of 85 Ω ± 10% is recommended.
- PCIe signals must be protected from noisy signals (clocks, DC-DC, RF and so forth). All other sensitive/high-speed signals and circuits must be routed far away from PCIe traces.
- For each differential pair, intra-lane length match should be less than 5 mil.
- Inter-lane length match, that is, the trace length matching between the reference clock, TX, and RX pairs is not required.
- The space between TX and RX, and the spacing between PCIe lanes and all other signals, should be at least 4 times the trace width.
- It is better to place PCIe TX AC coupling capacitors close to source or connector side to keep good signal integrity of main route on PCB.
- Do not stagger the capacitors, as this can affect the differential integrity of the design and can generate EMI.
- TX AC coupling capacitors should be 220 nF for PCIe Gen 3, and 100 nF is recommended for PCIe Gen 2 application.
- Use a serpentine to keep the differential pairs equal in the break out region as much as possible, to ensure that the traces stay differential thereafter.
- To reduce the probability for layer-to-layer manufacturing variation, minimize layer transitions on the main route (In other words, apply layer transitions only at module breakouts and connectors to ensure minimum layer transitions on the main route).

- The PCIE_REFCLK pair must add resistors near the slot (EP) side. The recommended resistor value is 49.9 Ω +/-1%.

4.18. Control Signals

4.18.1. WAKEUP_IN

The module can be woken up by other devices.

Table 30: Pin Definition of WAKEUP_IN

Pin Name	Pin No.	I/O	Description	Comment
WAKEUP_IN	100	DI	External wakeup signal to the module	1.8 V power domain. If unused, keep it open.

4.18.2. WAKEUP_OUT

The module can wake up other devices.

Table 31: Pin Definition of WAKEUP_OUT

Pin Name	Pin No.	I/O	Description	Comment
WAKEUP_OUT	102	DO	Wakeup signal from the module	1.8 V power domain. If unused, keep it open.

NOTE

GPIOs can also be configured as wake-up interrupt pins. For more details, see ***Chapter 4.9.***

5 RF Specifications

The module includes one main antenna interface, one Rx-diversity antenna interface [14], two MIMO antenna interfaces, and one GNSS antenna interface. The impedance of antenna port is 50 Ω.

5.1. Cellular Network

5.1.1. Antenna Interfaces & Frequency Bands

5.1.1.1. Pin Definition of Cellular Network Interface

The pin definition is shown as below:

Table 32: Pin Definition of AG568N-CN Cellular Network Interface

Pin Name	Pin No.	I/O	Description
ANT_MAIN	414	AIO	2G/3G/4G LMHB TRx0 5G NR n1/n3/n28A/n41 TRx0 SA 5G NR n41 Rx1 NSA 5G NR n78 DRx0 SA/NSA
ANT_DRX	416	AIO	2G/3G/4G LMHB DRx0 5G NR n1/n3/n28A/n41 DRx0 SA 5G NR n41 DRx1 NSA 5G NR n78 TRx0 SA/NSA
ANT_MIMO3	418	AIO	4G MHB Rx1 5G NR n1/n3/n41 Rx1 SA 5G NR n41 TRx0 NSA 5G NR n78 DRx1 SA/NSA
ANT_MIMO4	420	AI	4G MHB DRx1 5G NR n1/n3/n41 DRx1 SA 5G NR n41 DRx0 NSA 5G NR n78 Rx1 SA/NSA

[14] Rx-diversity antenna interface is used to resist the fall of signals caused by high-speed movement and multipath effect.

Table 33: Pin Definition of AG568N-EU Cellular Network Interface

Pin Name	Pin No.	I/O	Description
ANT_MAIN	414	AIO	2G/3G/4G LMHB TRx0 5G NR n1/n3/n7/n8/n20/n28 TRx0 SA 5G NR n77/n78 DRx0 SA/NSA
ANT_DRX	416	AIO	2G/3G/4G LMHB DRx0 5G NR n1/n3/n7/n8/n20/n28 DRx0 SA 5G NR n77/n78 TRx0 SA/NSA
ANT_MIMO3	418	AI	4G MHB Rx1 5G NR n1/n3/n7 Rx1 SA 5G NR n77/n78 DRx1 SA/NSA
ANT_MIMO4	420	AI	4G MHB DRx1 5G NR n1/n3/n7 DRx1 SA 5G NR n77/n78 Rx1 SA/NSA

Table 34: Pin Definition of AG568N-NA Cellular Network Interface

Pin Name	Pin No.	I/O	Description
ANT_MAIN	414	AIO	4G MHB TRx0 4G LB DRx0 5G NR n5 DRx0 SA/NSA 5G NR n12 DRx0 SA 5G NR n2/n66 TRx0 SA/NSA 5G NR n77 DRx0 SA/NSA @ MHB LTE 5G NR n77 Tx0/DRx0 NSA @ LB LTE 5G NR n78 DRx0 SA
ANT_DRX	416	AIO	4G MHB DRx0 4G LB TRx0 5G NR n5 TRx0 SA/NSA 5G NR n12 TRx0 SA 5G NR n2/n66 DRx0 SA/NSA 5G NR n77 TRx0 SA/NSA @ MHB LTE 5G NR n77 Rx0 NSA @ LB LTE 5G NR n78 TRx0 SA
ANT_MIMO3	418	AI	4G MHB Rx1 5G NR n2/n66 Rx1 SA/NSA 5G NR n77 DRx1 SA/NSA @ LMHB LTE 5G NR n78 DRx1 SA
ANT_MIMO4	420	AI	4G MHB DRx1 5G NR n2/n66 DRx1 SA/NSA 5G NR n77 Rx1 SA/NSA @ LMHB LTE

	5G NR n78 Rx1 SA

Table 35: Pin Definition of AG568N-ROW Cellular Network Interface

Pin Name	Pin No.	I/O	Description
ANT_MAIN	414	AIO	3G/4G LMHB TRx0 5G NR n28 TRx0 SA 5G NR n77/n78/n79 DRx0
ANT_DRX	416	AIO	3G/4G LMHB DRx0 5G NR n28 DRx0 SA 5G NR n77/n78/n79 TRx0 SA/NSA
ANT_MIMO3	418	AI	4G MHB Rx1 5G NR n77/n78/n79 DRx1
ANT_MIMO4	420	AI	4G MHB DRx1 5G NR n77/n78/n79 Rx1

NOTE

1. Only passive antennas are supported.
2. LTE B21 only supports TRx0 and DRx0 on AG568N-ROW.
3. 5G n78 only supports SA on AG568N-NA.

5.1.1.2. Operating Frequency

Table 36: AG568N-CN Operating Frequency

Operating Frequency	Transmit (MHz)	Receive (MHz)
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
WCDMA B1	1920–1980	2110–2170
WCDMA B8	880–915	925–960
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894

LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-TDD B34	2010–2025	2010–2025
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B39	1880–1920	1880–1920
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2496–2690	2496–2690
5G NR FDD n1	1920–1980	2110–2170
5G NR FDD n3	1710–1785	1805–1880
5G NR FDD n28A	703–733	758–788
5G NR TDD n41	2496–2690	2496–2690
5G NR TDD n78	3300–3800	3300–3800

Table 37: AG568N-EU Operating Frequency

Operating Frequency	Transmit (MHz)	Receive (MHz)
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
WCDMA B1	1920–1980	2110–2170
WCDMA B3	1710–1785	1805–1880
WCDMA B5	824–849	869–894
WCDMA B8	880–915	925–960
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690

LTE-FDD B8	880–915	925–960
LTE-FDD B20	832–862	791–821
LTE-FDD B28	703–748	758–803
LTE-FDD B32	-	1452–1496
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B40	2300–2400	2300–2400
5G NR FDD n1	1920–1980	2110–2170
5G NR FDD n3	1710–1785	1805–1880
5G NR FDD n7	2500–2570	2620–2690
5G NR FDD n8	880–915	925–960
5G NR FDD n20	832–862	791–821
5G NR FDD n28	703–748	758–803
5G NR TDD n77	3300–4200	3300–4200
5G NR TDD n78	3300–3800	3300–3800

Table 38: AG568N-NA Operating Frequency

Operating Frequency	Transmit (MHz)	Receive (MHz)
LTE-FDD B2	1850–1910	1930–1990
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894
LTE-FDD B12	699–716	729–746
LTE-FDD B29	-	717–728
LTE-FDD B66	1710–1780	2110–2200
5G NR FDD n2	1850–1910	1930–1990
5G NR FDD n5	824–849	869–894

5G NR FDD n12	699–716	729–746
5G NR FDD n66	1710–1780	2110–2200
5G NR TDD n77	3300–4200	3300–4200
5G NR TDD n78	3300–3800	3300–3800

Table 39: AG568N-ROW Operating Frequency

Operating Frequency	Transmit (MHz)	Receive (MHz)
WCDMA B1	1920–1980	2110–2170
WCDMA B3	1710–1785	1805–1880
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B19	830–845	875–890
LTE-FDD B21	1447.9–1462.8	1495.9–1510.8
LTE-FDD B28	703–748	758–803
5G NR FDD n28	703–748	758–803
5G NR TDD n77	3300–4200	3300–4200
5G NR TDD n78	3300–3800	3300–3800
5G NR TDD n79	4400–5000	4400–5000

5.1.2. Tx Power

The following table shows the Tx power of the module.

Table 40: Tx Power (25 °C, 3.8 V Power Supply)

Frequency	Max. Tx Power	Min. Tx Power
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB

DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
EGSM900 8-PSK	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800 8-PSK	26 dBm ±3 dB	0 dBm ±5 dB
WCDMA bands	23 dBm ±2 dB	< -49 dBm
LTE bands	23 dBm ±2 dB	< -49 dBm
5G NR TDD	26 dBm+1/-2 dB	< -39 dBm
5G NR FDD	23 dBm ±2 dB	< -39 dBm

NOTE

1. In GPRS 4 slots Tx mode, the maximum output power is reduced by 4 dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.
2. For 5G NR FDD/TDD bands, refer to the specifications as described in ***Clause 6.2*** of *TS 38.101-1-g80*.
3. WCDMA specified power tolerance conforms to *3GPP TS 34.121-1* requirements.
4. The specified typical power tolerance of LTE conforms to *3GPP TS 36.521-1* requirements and the module is tested @ BW = 10 MHz,1 RB.

5.1.3. Rx Sensitivity

The following table shows conducted RF receiving sensitivity of the module.

Table 41: AG568N-CN Conducted RF Receiving Sensitivity (Unit: dBm)

Frequency Band	SIMO [15]			3GPP SIMO
	Min.	Typ.	Max.	
EGSM900	-104	-108	-110	-102
DCS1800	-104	-108	-110	-102
WCDMA B1	-108	-109	-111.7	-106
WCDMA B8	-105	-109	-111.6	-103

[15] Test conditions for the receiving sensitivity of AG568N-CN:
1) GSM/WCDMA: tested with 1 antenna (1Rx);
2) LTE B5/B8: tested with 2 antennas (2Rx). Other 4G bands: tested with 4 antennas (4Rx);
3) 5G NR SA n28A: tested with 2 antennas (2Rx). Other 5G NR SA bands: tested with 4 antennas (4Rx).

LTE-FDD B1 (10 MHz)	-101	-103	-105.3	-99
LTE-FDD B3 (10 MHz)	-98	-100	-104.8	-96
LTE-FDD B5 (10 MHz)	-96.3	-98.3	-103.6	-94.3
LTE-FDD B7 (10 MHz)	-99	-101	-103.8	-97
LTE-FDD B8 (10 MHz)	-95.3	-97.3	-103.1	-93.3
LTE-TDD B34 (10 MHz)	-101	-102	-105.9	-99
LTE-TDD B38 (10 MHz)	-101	-102	-104.9	-99
LTE-TDD B39 (10 MHz)	-101	-102	-106.1	-99
LTE-TDD B40 (10 MHz)	-101	-102	-104.9	-99
LTE-TDD B41 (10 MHz)	-99	-100	-104.5	-97
5G NR FDD n1 (20 MHz)	-95.8	-97.3	-101.7	-95.8
5G NR FDD n3 (20 MHz)	-92.8	-94.3	-100.6	-92.8
5G NR FDD n28A (20 MHz)	-90.1	-91.6	-100.6	-90.1
5G NR TDD n41 (100 MHz)	-86.7	-88.2	-93.4	-86.7
5G NR TDD n78 (100 MHz)	-86.8	-88.3	-93.2	-86.8

Table 42: AG568N-EU Conducted RF Receiving Sensitivity (Unit: dBm)

Frequency Bands	SIMO [16]			3GPP SIMO
	Min.	Typ.	Max.	
EGSM900	TBD	TBD	TBD	-102
DCS1800	TBD	TBD	TBD	-102
WCDMA B1	TBD	TBD	TBD	-106
WCDMA B3	TBD	TBD	TBD	-103
WCDMA B5	TBD	TBD	TBD	-104

[16] Test conditions for the receiving sensitivity of AG568N-EU:
1) GSM/WCDMA: tested with 1 antenna (1Rx);
2) LTE B5/B8/B20/B28: tested with 2 antennas (2Rx). Other 4G bands: tested with 4 antennas (4Rx);
3) LTE B32 supports Rx only and cannot be tested under single-band conditions;
4) 5G NR SA n8/n20/n28: tested with 2 antennas (2Rx). Other 5G NR SA bands: tested with 4 antennas (4Rx);

WCDMA B8	TBD	TBD	TBD	-103
LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	-99
LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	-96
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	-94.3
LTE-FDD B7 (10 MHz)	TBD	TBD	TBD	-97
LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B20 (10 MHz)	TBD	TBD	TBD	-93.3
LTE-FDD B28 (10 MHz)	TBD	TBD	TBD	-94.8
LTE-FDD B32 (10 MHz)	-	-	-	-
LTE-TDD B38 (10 MHz)	TBD	TBD	TBD	-99
LTE-TDD B40 (10 MHz)	TBD	TBD	TBD	-99
5G NR FDD n1 (20 MHz)	TBD	TBD	TBD	-95.8
5G NR FDD n3 (20 MHz)	TBD	TBD	TBD	-92.8
5G NR FDD n7 (20 MHz)	TBD	TBD	TBD	-93.8
5G NR FDD n8 (20 MHz)	TBD	TBD	TBD	-89.3
5G NR FDD n20 (20 MHz)	TBD	TBD	TBD	-89.1
5G NR FDD n28 (20 MHz)	TBD	TBD	TBD	-90.1
5G NR TDD n77 (100 MHz)	TBD	TBD	TBD	-86.8
5G NR TDD n78 (100 MHz)	TBD	TBD	TBD	-86.8

Table 43: AG568N-NA Conducted RF Receiving Sensitivity (Unit: dBm)

Frequency Bands	SIMO [17]			3GPP SIMO
	Min.	Typ.	Max.	
LTE-FDD B2 (10 MHz)	-99	-101	-104.6	-97

[17] Test conditions for the receiving sensitivity of AG568N-NA:
1) LTE B5/B12: tested with 2 antennas (2Rx). Other 4G bands: tested with 4 antennas (4Rx);
2) LTE B29 supports Rx only and cannot be tested under single-band conditions;
3) 5G NR SA n5/n12: tested with 2 antennas (2Rx). Other 5G NR SA bands: tested with 4 antennas (4Rx);

LTE-FDD B4 (10 MHz)	-101	-103	-105.1	-99
LTE-FDD B5 (10 MHz)	-96.3	-98.3	-102.7	-94.3
LTE-FDD B12 (10 MHz)	-95.3	-97.3	-103.6	-93.3
LTE-FDD B29 (10 MHz)	-	-	-	-
LTE-FDD B66 (10 MHz)	-100.5	-102.5	-104.2	-98.5
5G NR FDD n2 (20 MHz)	-93.8	-95.3	-102.5	-93.8
5G NR FDD n5 (20 MHz)	-90.1	-91.6	-100.7	-90.1
5G NR FDD n12 (15 MHz)	-83.3	-84.8	-99.2	-83.3
5G NR FDD n66 (20 MHz)	-95.3	-96.8	-102.5	-95.3
5G NR TDD n77 (100 MHz)	-86.8	-88.3	-93.7	-86.8
5G NR TDD n78 (100 MHz)	-86.8	-88.3	-93.9	-86.8

Table 44: AG568N-ROW Conducted RF Receiving Sensitivity (Unit: dBm)

Frequency Bands	SIMO [18]			3GPP SIMO
	Min.	Typ.	Max.	
WCDMA B1	-108	-109	-111.1	-106
WCDMA B3	-105	-109	-111.6	-103
LTE-FDD B1 (10 MHz)	-101	-103	-104.4	-99
LTE-FDD B3 (10 MHz)	-98	-100	-104.0	-96
LTE-FDD B19 (10 MHz)	-98.3	-100.3	-103.1	-96.3
LTE-FDD B21 (10 MHz)	-98.3	-99	-101.4	-96.3
LTE-FDD B28 (10 MHz)	-96.8	-98.8	-102.9	-94.8
5G NR FDD n28 (20 MHz)	-90.1	-91.6	-100.4	-90.1
5G NR TDD n77 (100 MHz)	-86.8	-88.3	-93.9	-86.8

[18] Test conditions for the receiving sensitivity of AG568N-ROW:
1) WCDMA: tested with 1 antenna (1Rx);
2) LTE B19/B21/B28: tested with 2 antennas (2Rx). Other 4G bands: tested with 4 antennas (4Rx);
3) 5G NR SA n28: tested with 2 antennas (2Rx). Other 5G NR SA bands: tested with 4 antennas (4Rx).

5G NR TDD n78 (100 MHz)	-86.8	-88.3	-94.0	-86.8
5G NR TDD n79 (100 MHz)	-86.8	-88.3	-92.4	-86.8

NOTE

1. 5G NR FDD n1, n3, n7, n8, n12, n20, n28A and n28 support SA only.
2. 5G NR FDD n2, n5 and n66 support SA and NSA ;5G NR TDD n41, n77, n78 and n79 support SA and NSA.
3. GSM specified sensitivity values conforms to *3GPP TS 51.010-1* requirements.
4. WCDMA specified sensitivity values conforms to *3GPP TS 34.121-1* requirements.
5. LTE specified sensitivity values conforms to *3GPP TS 36.521-1* requirements.
6. 5G NR specified sensitivity values conforms to *3GPP TS 38.521-1* requirements, FDD test @ SCS 15 kHz, TDD test @ SCS 30 kHz.

5.1.4. Reference Design

The module provides the main and Rx-diversity RF antenna interfaces for antenna connection.

It is recommended to reserve a Π-type matching circuit for better RF performance, and the Π-type matching components (R1/C1/C2 and R2/C3/C4) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

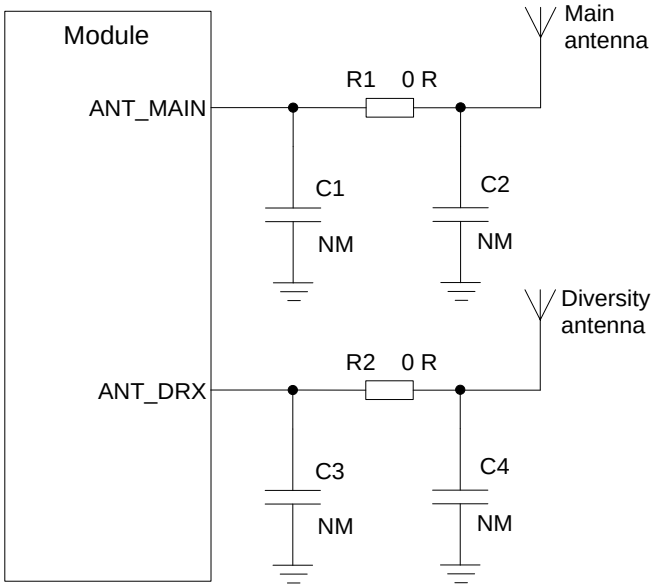


Figure 31: Reference Circuit for RF Antenna Interfaces

NOTE

1. The reference design of MIMO antenna interfaces is the same as that of main antenna interface.
2. Keep a proper distance between each antenna to improve receiving sensitivity.

5.2. GNSS

The module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, Galileo, and supports L1 + L5 dual-frequency positioning [19].

The module supports standard NMEA 0183 protocol, and outputs NMEA sentences via USB interface (data update rate: 1–10 Hz, 1 Hz by default).

5.2.1. Antenna Interfaces & Frequency Bands

The following table shows the pin definition, frequency, and performance of GNSS antenna interface.

Table 45: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	426	AI	GNSS antenna interface	Single-ended impedance of 50 Ω. Supports active antenna only.

Table 46: GNSS Frequency (Unit: MHz)

Type	Frequency
GPS	1575.42 ±1.023 (L1) 1176.45 ±10.23 (L5)
GLONASS	1597.5–1605.8
Galileo	1575.42 ±2.046 (E1) 1176.45 ±10.23 (E5a)
BDS	1561.098 ±2.046

[19] AG568N series only supports dual-frequency GNSS (L1 + L5) by default, but the module is designed to be compatible with single-frequency GNSS (L1). For more details, please contact Quectel Technical Support.

5.2.2. GNSS Performance

Table 47: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-149	dBm
	Reacquisition	Autonomous	-162	
	Tracking	Autonomous	-168	
TTFF	Cold start @ open sky	Autonomous	30	s
		EPO Enabled	15	
	Warm start @ open sky	Autonomous	25	
		EPO Enabled	5	
	Hot start @ open sky	Autonomous	1	
		EPO Enabled	1	
Accuracy	CEP-50	Autonomous @ open sky	2	M

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (the module lost lock 3 times in 5 minutes for 10 seconds each time).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 5 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.
4. The above GNSS performance test data is measured under dual-frequency L1 + L5.
5. For more details about GNSS performance, please consult Quectel Technical Support for GNSS performance test report.

5.2.3. Reference Design

The reference circuit of GNSS antenna is shown as below.

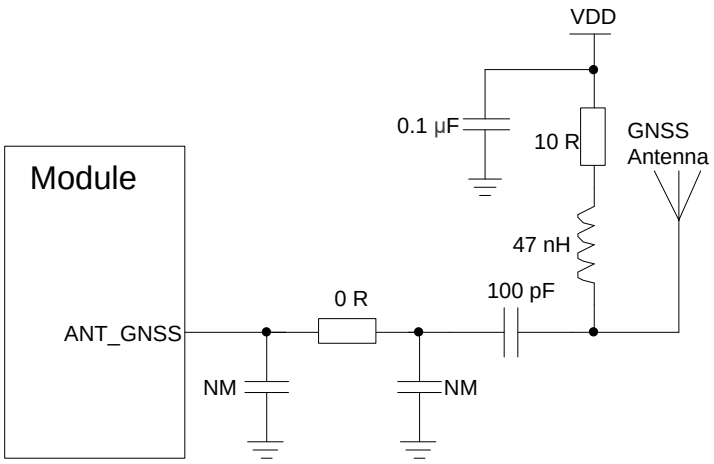


Figure 32: Reference Circuit of GNSS Antenna

NOTE

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.
3. Junction capacitance of ESD protection components on the antenna interface should not exceed 0.05 pF.

The following layout guidelines should be considered in application design:

- Maximize the distance among GNSS antenna, main antenna, Rx-diversity antenna and MIMO antennas.
- Digital circuits such as (U)SIM card, USB interface, camera module, SDIO interface and display connector should be kept away from antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep the characteristic impedance for ANT_GNSS trace as 50 Ω.
- Select an external active antenna, since there is no LNA inside the module. The optimal value of the gain of the external active antenna minus the loss of RF cable is 18–24 dB, otherwise the performance of GNSS positioning will be affected.

5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control

characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

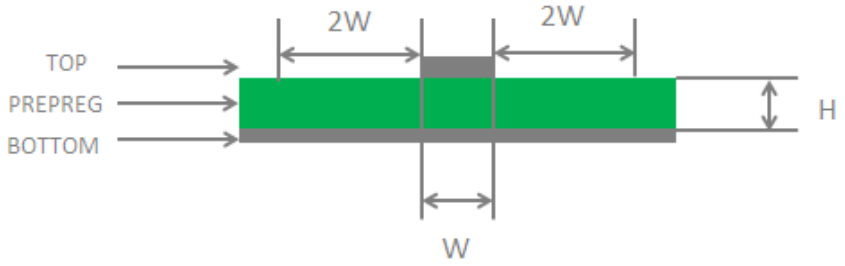


Figure 33: Microstrip Design on a 2-layer PCB

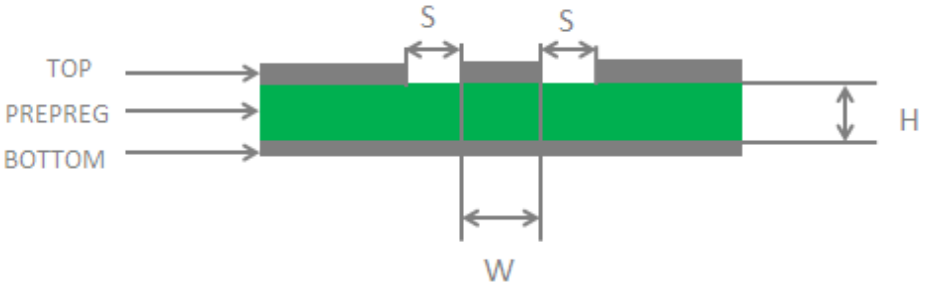


Figure 34: Coplanar Waveguide Design on a 2-layer PCB

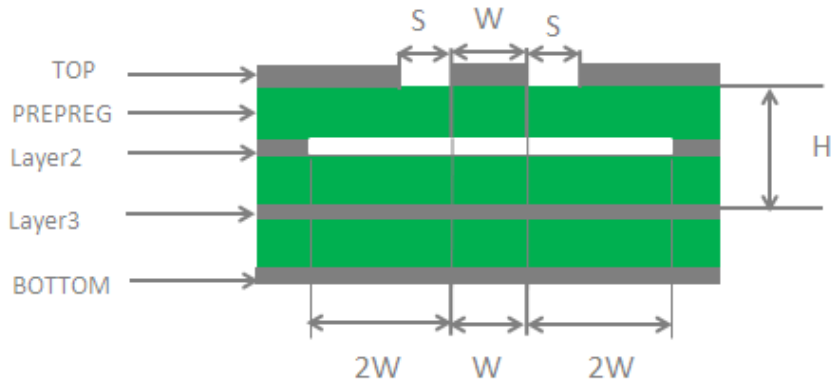


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

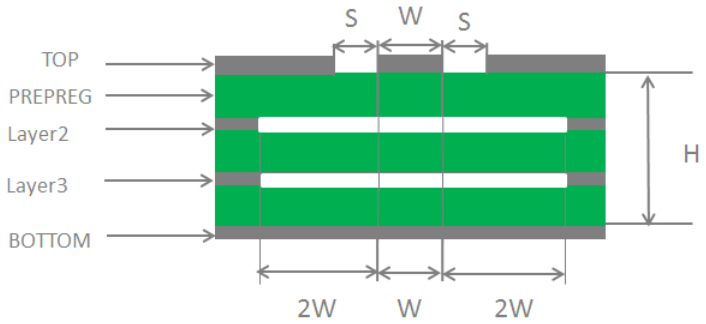


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [6].***

5.4. Antenna Design Requirements

Table 48: Antenna Design Requirements

Antenna Type	Requirements
GNSS	• Frequency range: L1: 1559–1609 MHz L5: 1166–1187 MHz • Polarization: RHCP or linear • VSWR: ≤ 2 (Typ.)

	• Passive antenna gain: > 0 dBi • Active antenna noise figure: < 1.5 dB • Active antenna gain: > 0 dBi • Active antenna embedded LNA gain: < 24 dB
5G NR/LTE/UMTS/GSM	• VSWR: ≤ 2 • Efficiency: > 30 % • Gain:1dBi • Max input power: 50 W • Input impedance: 50 Ω • Vertical polarization • Cable insertion loss: **< 1 dB:** LB (< 1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)

5.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the HFM connector provided by Rosenberger.

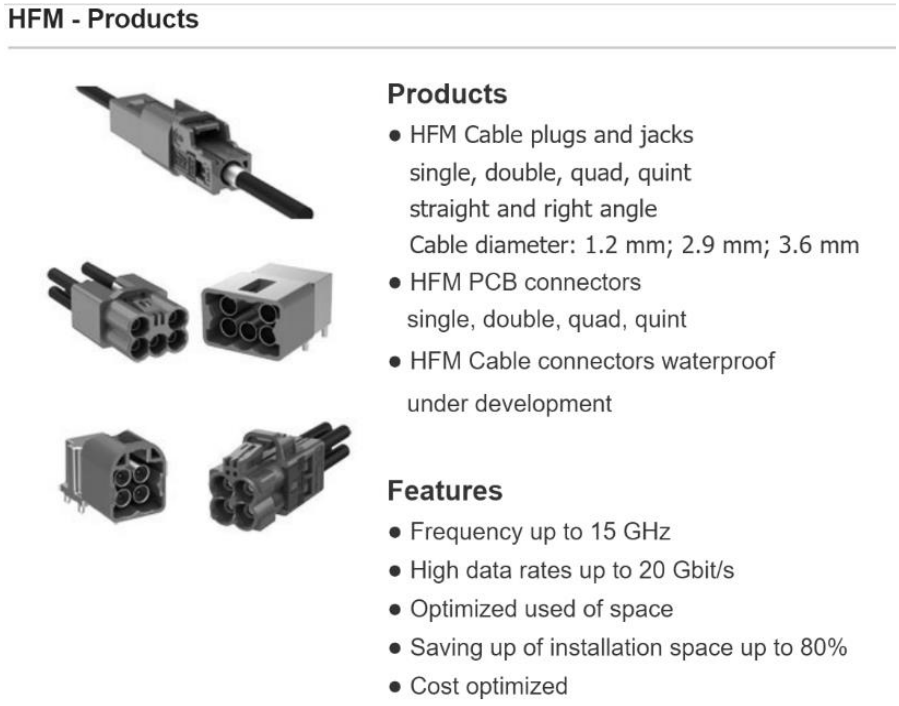


Figure 37: Description of the HFM Connector

For more details, visit https://www.rosenbergerap.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 49: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	0	5	V
USB_VBUS	0	21	V
Peak current of VBAT_BB	-	1.5	A
Peak current of VBAT_RF	-	2	A
Voltage on Digital Pins	-0.3	1.98	V
Voltage at ADC0	0	1.98	V
Voltage at ADC1	0	1.98	V
Voltage at ADC2	0	1.98	V
Voltage at ADC3	0	1.98	V
Voltage at ADC4	0	1.98	V
Voltage at ADC5	0	1.98	V

6.2. Power Supply Ratings

Table 50: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V
USB_VBUS	Turn-on/ USB connection detect	-	4.2	5.0	21	V

6.3. Power Consumption

6.3.1. AG568N-CN Power Consumption

Table 51: AG568N-CN Power Consumption (25 °C, 3.8 V Power Supply)

Description	Conditions	Typ.	Unit
OFF state	Power down	53	μA
Sleep state	**AT+CFUN=0**	2.840	mA
	AT+CFUN=4	2.936	mA
	EGSM900 DRX = 2	4.4	mA
	EGSM900 DRX = 5	3.6	mA
	EGSM900 DRX = 9	3.3	mA
	DCS1800 DRX = 2	4.5	mA
	DCS1800 DRX = 5	3.6	mA
	DCS1800 DRX = 9	3.3	mA
	WCDMA @ DRX = 0.64 s	4.2	mA
	WCDMA @ DRX = 1.28 s	3.5	mA
	WCDMA @ DRX = 2.56 s	3.2	mA

	WCDMA @ DRX = 5.12s	3.0	mA
	LTE-FDD @ DRX = 0.32 s	6.1	mA
	LTE-FDD @ DRX = 0.64 s	4.4	mA
	LTE-FDD @ DRX = 1.28 s	3.9	mA
	LTE-FDD @ DRX = 2.56 s	3.4	mA
	LTE-TDD @ DRX = 0.32 s	6.0	mA
	LTE-TDD @ DRX = 0.64 s	4.6	mA
	LTE-TDD @ DRX = 1.28 s	3.6	mA
	LTE-TDD @ DRX = 2.56 s	3.1	mA
	5G NR FDD @ DRX = 0.32 s	12.7	mA
	5G NR FDD @ DRX = 0.64 s	7.8	mA
	5G NR FDD @ DRX = 1.28 s	5.3	mA
	5G NR FDD @ DRX = 2.56 s	4.4	mA
	5G NR TDD @ DRX = 0.32 s	10.9	mA
	5G NR TDD @ DRX = 0.64 s	7.1	mA
	5G NR TDD @ DRX = 1.28 s	5.3	mA
	5G NR TDD @ DRX = 2.56 s	5.1	mA
Idle state	EGSM900 CH62 @ DRX = 5	139.0	mA
	EGSM900 CH62 @ DRX = 5 (USB active)	147.2	mA
	WCDMA @ Paging Frame= 64	138.7	mA
	WCDMA @ Paging Frame = 64 (USB active)	146.7	mA
	LTE-FDD @ DRX = 0.64 s	140.4	mA
	LTE-FDD @ DRX = 0.64 s (USB active)	149.0	mA
	LTE-TDD @ DRX = 0.64 s	139.4	mA
	LTE-TDD @ DRX = 0.64 s (USB active)	147.3	mA

	5G NR FDD @ DRX = 0.64 s	143.8	mA
	5G NR FDD @ DRX = 0.64 s (USB active)	149.6	mA
	5G NR TDD @ DRX = 0.64 s	143.2	mA
	5G NR TDD @ DRX = 0.64 s (USB active)	149.3	mA
GSM voice call	EGSM900 CH1 PCL = 5 @ 32.55 dBm	454.9	mA
	EGSM900 CH62 PCL = 5 @ 32.54 dBm	456.3	mA
	EGSM900 CH62 PCL = 12 @ 18.87 dBm	258.4	mA
	EGSM900 CH62 PCL = 19 @ 5.15 dBm	214.3	mA
	EGSM900 CH124 PCL = 5 @ 32.57 dBm	458.9	mA
	DCS1800 CH512 PCL = 0 @ 28.75 dBm	347.3	mA
	DCS1800 CH698 PCL = 0 @ 28.80 dBm	345.0	mA
	DCS1800 CH698 PCL = 7 @ 15.80 dBm	242.4	mA
	DCS1800 CH698 PCL = 15 @ 0.43 dBm	212.3	mA
	DCS1800 CH885 PCL = 0 @ 28.77 dBm	343.7	mA
GPRS data transfer (GNSS OFF)	EGSM900 CH1 1DL/4UL @ 29.05 dBm	899.1	mA
	EGSM900 CH62 4DL/1UL @ 32.58 dBm	450.8	mA
	EGSM900 CH62 3DL/2UL @ 31.84 dBm	666.0	mA
	EGSM900 CH62 2DL/3UL @ 30.39 dBm	804.2	mA
	EGSM900 CH62 1DL/4UL @ 28.91 dBm	900.6	mA
	EGSM900 CH124 1DL/4UL @ 28.92 dBm	912.8	mA
	DCS1800 CH512 1DL/4UL @ 25.76 dBm	654.3	mA
	DCS1800 CH698 4DL/1UL @ 28.74 dBm	350.3	mA
	DCS1800 CH698 3DL/2UL @ 28.18 dBm	478.2	mA
	DCS1800 CH698 2DL/3UL @ 26.67 dBm	573.2	mA
	DCS1800 CH698 1DL/4UL @ 25.77 dBm	646.9	mA

	DCS1800 CH885 1DL/4UL @ 25.76 dBm	650.2	mA
EDGE data transfer (GNSS OFF)	EGSM900 CH1 1DL/4UL @ 23.68 dBm	711.3	mA
	EGSM900 CH62 4DL/1UL @ 28.05 dBm	379.8	mA
	EGSM900 CH62 3DL/2UL @ 27.39 dBm	517.5	mA
	EGSM900 CH62 2DL/3UL @ 25.14 dBm	613.5	mA
	EGSM900 CH62 1DL/4UL @ 23.68 dBm	709.2	mA
	EGSM900 CH124 1DL/4UL @ 23.45 dBm	708.3	mA
	DCS1800 CH512 1DL/4UL @ 22.30 dBm	683.9	mA
	DCS1800 CH698 4DL/1UL @ 26.78 dBm	348.9	mA
	DCS1800 CH698 3DL/2UL @ 25.50 dBm	474.6	mA
	DCS1800 CH698 2DL/3UL @ 24.16 dBm	575.8	mA
	DCS1800 CH698 1DL/4UL @ 22.85 dBm	683.0	mA
	DCS1800 CH885 1DL/4UL @ 22.57 dBm	681.1	mA
WCDMA voice call	WCDMA B1 CH10562 @ 23.14 dBm	689.7	mA
	WCDMA B1 CH10700 @ 23.12 dBm	716.7	mA
	WCDMA B1 CH10838 @ 23.11 dBm	735.5	mA
	WCDMA B8 CH2937 @ 23.26 dBm	752.2	mA
	WCDMA B8 CH3012 @ 23.18 dBm	722.2	mA
	WCDMA B8 CH3088 @ 23.18 dBm	770.2	mA
WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA CH10562 @ 22.67 dBm	679.5	mA
	WCDMA B1 HSDPA CH10700 @ 22.11 dBm	674.3	mA
	WCDMA B1 HSDPA CH10838 @ 22.11 dBm	687.6	mA
	WCDMA B8 HSDPA CH2937 @ 22.26 dBm	695.1	mA
	WCDMA B8 HSDPA CH3012 @ 22.22 dBm	670.5	mA
	WCDMA B8 HSDPA CH3088 @ 22.16 dBm	712.2	mA

	WCDMA B1 HSUPA CH10562 @ 23.19 dBm	710.4	mA
	WCDMA B1 HSUPA CH10700 @ 22.16 dBm	685.2	mA
	WCDMA B1 HSUPA CH10838 @ 22.12 dBm	699.1	mA
	WCDMA B8 HSUPA CH2937 @ 22.28 dBm	707.1	mA
	WCDMA B8 HSUPA CH3012 @ 22.24 dBm	681.1	mA
	WCDMA B8 HSUPA CH3088 @ 22.19 dBm	72764	mA
LTE data transfer (GNSS OFF)	LTE-FDD B1 CH100 @ 23.15 dBm	718.5	mA
	LTE-FDD B1 CH300 @ 23.29 dBm	748.2	mA
	LTE-FDD B1 CH500 @ 23.22 dBm	839.9	mA
	LTE-FDD B3 CH1300 @ 22.84 dBm	750.9	mA
	LTE-FDD B3 CH1575 @ 22.79 dBm	738.4	mA
	LTE-FDD B3 CH1850 @ 22.80 dBm	785.6	mA
	LTE-FDD B5 CH2450 @ 22.94 dBm	696.3	mA
	LTE-FDD B5 CH2525 @ 22.97 dBm	674.9	mA
	LTE-FDD B5 CH2600 @ 23.01 dBm	690.7	mA
	LTE-FDD B7 CH2850 @ 22.99 dBm	927.6.	mA
	LTE-FDD B7 CH3100 @ 22.97 dBm	910.6	mA
	LTE-FDD B7 CH3350 @ 23.43 dBm	1024.1	mA
	LTE-FDD B8 CH3500 @ 23.08 dBm	741.8	mA
	LTE-FDD B8 CH3625 @ 23.07 dBm	720.1	mA
	LTE-FDD B8 CH3750 @ 23.08 dBm	754.9	mA
	LTE-TDD B34 CH36275 @ 23.05 dBm	460.1	mA
	LTE-TDD B38 CH37850 @ 23.01 dBm	521.76	mA
	LTE-TDD B38 CH38000 @ 22.98 dBm	520.2	mA
	LTE-TDD B38 CH38150 @ 22.99 dBm	520.1	mA

	LTE-TDD B39 CH38350 @ 22.76 dBm	410.1	mA
	LTE-TDD B39 CH38450 @ 22.83 dBm	414.7	mA
	LTE-TDD B39 CH38550 @ 22.80 dBm	418.2	mA
	LTE-TDD B40 CH38750 @ 22.75 dBm	483.8	mA
	LTE-TDD B40 CH39150 @ 22.74 dBm	470.7	mA
	LTE-TDD B40 CH39550 @ 22.79 dBm	478.2	mA
	LTE-TDD B41 CH39750 @ 22.56 dBm	584.2	mA
	LTE-TDD B41 CH40620 @ 23.00 dBm	517.9	mA
	LTE-TDD B41 CH41490 @ 22.83 dBm	555.1	mA
5G NR SA data transfer (GNSS OFF)	n1A CH427000 @ 23.13 dBm	784.5	mA
	n1A CH428000 @ 23.02 dBm	792.7	mA
	n1A CH429000 @ 23.12 dBm	807.2	mA
	n3A CH365000 @ 21.99 dBm	691.2	mA
	n3A CH368500 @ 21.82 dBm	672.4	mA
	n3A CH372000 @ 21.81 dBm	701.8	mA
	n28A CH154600 @ 22.78 dBm	778.0	mA
	n41A CH509202 @ 26.36 dBm	585.3	mA
	n41A CH518598 @ 26.37 dBm	573.0	mA
	n41A CH528000 @ 25.82 dBm	584.1	mA
	n78A CH623334 @ 26.79 dBm	570.6	mA
	n78A CH636666 @ 26.97 dBm	614.0	mA
	n78A CH650000 @ 26.89 dBm	626.2	mA
5G NR NSA data transfer (GNSS OFF)	3A_n41A CH509202 @ 23.79 dBm	979.0	mA
	3A_n41A CH518598 @ 25.79 dBm	1031.0	mA
	3A_n41A CH5280008 @ 25.73 dBm	1043.0	mA

	5A_n41A CH509202 @ 22.64 dBm	750.0	mA
	5A_n41A CH518598 @ 22.88 dBm	749.0	mA
	5A_n41A CH5280008 @ 22.43 dBm	769.0	mA
	8A_n41A CH509202 @ 22.70 dBm	787.0	mA
	8A_n41A CH518598 @ 23.13 dBm	785.0	mA
	8A_n41A CH5280008 @ 22.89 dBm	805.0	mA
	39A_n41A CH509202 @ 22.85 dBm	652.0	mA
	39A_n41A CH518598 @ 22.85 dBm	736.0	mA
	39A_n41A CH5280008 @ 22.85 dBm	858.0	mA
	40A_n41A CH509202 @ 22.85 dBm	590.0	mA
	40A_n41A CH518598 @ 22.85 dBm	591.0	mA
	40A_n41A CH5280008 @ 22.85 dBm	581.0	mA
	1A_n78A CH623334 @ 22.51 dBm	781.0	mA
	1A_n78A CH636666 @ 22.72 dBm	805.0	mA
	1A_n78A CH650000 @ 22.88 dBm	854.0	mA
	3A_n78A CH623334 @ 25.42 dBm	1069.0	mA
	3A_n78A CH636666 @ 25.45 dBm	1069.0	mA
	3A_n78A CH650000 @ 25.45 dBm	1093.0	mA
	5A_n78A CH623334 @ 22.95 dBm	761.0	mA
	5A_n78A CH636666 @ 23.09 dBm	745.0	mA
	5A_n78A CH650000 @ 23.16 dBm	732.0	mA
	7A_n78A CH623334 @ 22.88 dBm	893.0	mA
	7A_n78A CH636666 @ 23.04 dBm	872.0	mA
	7A_n78A CH650000 @ 23.18 dBm	921.0	mA
	8A_n78A CH623334 @ 22.99 dBm	786.0	mA

	8A_n78A CH636666 @ 23.13 dBm	782.0	mA
	8A_n78A CH650000 @ 23.21 dBm	829.0	mA
	38A_n78A CH623334 @ 23.04 dBm	629.0	mA
	38A_n78A CH636666 @ 23.16 dBm	604.0	mA
	38A_n78A CH650000 @ 23.25 dBm	651.0	mA
	40A_n78A CH623334 @ 22.80 dBm	612.0	mA
	40A_n78A CH636666 @ 22.97 dBm	595.0	mA
	40A_n78A CH650000 @ 23.09 dBm	652.0	mA
	41A_n78A CH623334 @ 23.00 dBm	623.0	mA
	41A_n78A CH636666 @ 23.16 dBm	605.0	mA
	41A_n78A CH650000 @ 23.28 dBm	652.0	mA

6.3.2. AG568N-EU Power Consumption

Table 52: AG568N-EU Power Consumption (25 °C, 3.8 V Power Supply)

Description	Conditions	Typ.	Unit
OFF state	Power down	53	μA
Sleep state	**AT+CFUN=0**	TBD	mA
	AT+CFUN=4	TBD	mA
	EGSM900 DRX = 2	TBD	mA
	EGSM900 DRX = 5	TBD	mA
	EGSM900 DRX = 9	TBD	mA
	DCS1800 DRX = 2	TBD	mA
	DCS1800 DRX = 5	TBD	mA
	DCS1800 DRX = 9	TBD	mA
	WCDMA @ DRX = 0.64 s	TBD	mA

	WCDMA @ DRX = 1.28 s	TBD	mA
	WCDMA @ DRX = 2.56 s	TBD	mA
	WCDMA @ DRX = 5.12 s	TBD	mA
	LTE-FDD @ DRX = 0.32 s	TBD	mA
	LTE-FDD @ DRX = 0.64 s	TBD	mA
	LTE-FDD @ DRX = 1.28 s	TBD	mA
	LTE-FDD @ DRX = 2.56 s	TBD	mA
	LTE-TDD @ DRX = 0.32 s	TBD	mA
	LTE-TDD @ DRX = 0.64 s	TBD	mA
	LTE-TDD @ DRX = 1.28 s	TBD	mA
	LTE-TDD @ DRX = 2.56 s	TBD	mA
	5G NR FDD @ DRX = 0.32 s	TBD	mA
	5G NR FDD @ DRX = 0.64 s	TBD	mA
	5G NR FDD @ DRX = 1.28 s	TBD	mA
	5G NR FDD @ DRX = 2.56 s	TBD	mA
	5G NR TDD @ DRX = 0.32 s	TBD	mA
	5G NR TDD @ DRX = 0.64 s	TBD	mA
	5G NR TDD @ DRX = 1.28 s	TBD	mA
	5G NR TDD @ DRX = 2.56 s	TBD	mA
Idle state	EGSM900 CH62 @ DRX = 5	TBD	mA
	EGSM900 CH62 @ DRX = 5 (USB active)	TBD	mA
	WCDMA @ Paging Frame = 64	TBD	mA
	WCDMA @ Paging Frame = 64 (USB active)	TBD	mA
	LTE-FDD @ DRX = 0. 64 s	TBD	mA
	LTE-FDD @ DRX = 0. 64 s (USB active)	TBD	mA

	LTE-TDD @ DRX = 0. 64 s	TBD	mA
	LTE-TDD @ DRX = 0. 64s (USB active)	TBD	mA
	5G NR FDD @ DRX = 0.64 s	TBD	mA
	5G NR FDD @ DRX = 0.64 s (USB active)	TBD	mA
	5G NR TDD @ DRX = 0.64 s	TBD	mA
	5G NR TDD @ DRX = 0.64 s (USB active)	TBD	mA
GSM voice call	EGSM900 CH1 PCL = 5 @ TBD dBm	TBD	mA
	EGSM900 CH62 PCL = 5 @ TBD dBm	TBD	mA
	EGSM900 CH62 PCL = 12 @ TBD dBm	TBD	mA
	EGSM900 CH62 PCL = 19 @ TBD dBm	TBD	mA
	EGSM900 CH124 PCL = 5 @ TBD dBm	TBD	mA
	DCS1800 CH512 PCL = 0 @ TBD dBm	TBD	mA
	DCS1800 CH698 PCL = 0 @ TBD dBm	TBD	mA
	DCS1800 CH698 PCL = 7 @ TBD dBm	TBD	mA
	DCS1800 CH698 PCL = 15 @ TBD dBm	TBD	mA
	DCS1800 CH885 PCL = 0 @ TBD dBm	TBD	mA
GPRS data transfer (GNSS OFF)	EGSM900 CH1 1DL/4UL @ TBD dBm	TBD	mA
	EGSM900 CH62 4DL/1UL @ TBD dBm	TBD	mA
	EGSM900 CH62 3DL/2UL @ TBD dBm	TBD	mA
	EGSM900 CH62 2DL/3UL @ TBD dBm	TBD	mA
	EGSM900 CH62 1DL/4UL @ TBD dBm	TBD	mA
	EGSM900 CH124 1DL/4UL @ TBD dBm	TBD	mA
	DCS1800 CH512 1DL/4UL @ TBD dBm	TBD	mA
	DCS1800 CH698 4DL/1UL @ TBD dBm	TBD	mA
	DCS1800 CH698 3DL/2UL @ TBD dBm	TBD	mA

	DCS1800 CH698 2DL/3UL @ TBD dBm	TBD	mA
	DCS1800 CH698 1DL/4UL @ TBD dBm	TBD	mA
	DCS1800 CH885 1DL/4UL @ TBD dBm	TBD	mA
EDGE data transfer (GNSS OFF)	EGSM900 CH1 1DL/4UL @ TBD dBm	TBD	mA
	EGSM900 CH62 4DL/1UL @ TBD dBm	TBD	mA
	EGSM900 CH62 3DL/2UL @ TBD dBm	TBD	mA
	EGSM900 CH62 2DL/3UL @ TBD dBm	TBD	mA
	EGSM900 CH62 1DL/4UL @ TBD dBm	TBD	mA
	EGSM900 CH124 1DL/4UL @ TBD dBm	TBD	mA
	DCS1800 CH512 1DL/4UL @ TBD dBm	TBD	mA
	DCS1800 CH698 4DL/1UL @ TBD dBm	TBD	mA
	DCS1800 CH698 3DL/2UL @ TBD dBm	TBD	mA
	DCS1800 CH698 2DL/3UL @ TBD dBm	TBD	mA
	DCS1800 CH698 1DL/4UL @ TBD dBm	TBD	mA
	DCS1800 CH885 1DL/4UL @ TBD dBm	TBD	mA
WCDMA voice call	WCDMA B1 CH10562 @ TBD dBm	TBD	mA
	WCDMA B1 CH10700 @ TBD dBm	TBD	mA
	WCDMA B1 CH10838 @ TBD dBm	TBD	mA
	WCDMA B3 CH1162 @ TBD dBm	TBD	mA
	WCDMA B3 CH1338 @ TBD dBm	TBD	mA
	WCDMA B3 CH1513 @ TBD dBm	TBD	mA
	WCDMA B5 CH4357 @ TBD dBm	TBD	mA
	WCDMA B5 CH4408 @ TBD dBm	TBD	mA
	WCDMA B5 CH4458 @ TBD dBm	TBD	mA
	WCDMA B8 CH2937 @ TBD dBm	TBD	mA

	WCDMA B8 CH3012 @ TBD dBm	TBD	mA
	WCDMA B8 CH3088 @ TBD dBm	TBD	mA
WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA CH10562 @ TBD dBm	TBD	mA
	WCDMA B1 HSDPA CH10700 @ TBD dBm	TBD	mA
	WCDMA B1 HSDPA CH10838 @ TBD dBm	TBD	mA
	WCDMA B3 HSDPA CH1162 @ TBD dBm	TBD	mA
	WCDMA B3 HSDPA CH1338 @ TBD dBm	TBD	mA
	WCDMA B3 HSDPA CH1513 @ TBD dBm	TBD	mA
	WCDMA B5 HSDPA CH4357 @ TBD dBm	TBD	mA
	WCDMA B5 HSDPA CH4408 @ TBD dBm	TBD	mA
	WCDMA B5 HSDPA CH4458 @ TBD dBm	TBD	mA
	WCDMA B8 HSDPA CH2937 @ TBD dBm	TBD	mA
	WCDMA B8 HSDPA CH3012 @ TBD dBm	TBD	mA
	WCDMA B8 HSDPA CH3088 @ TBD dBm	TBD	mA
	WCDMA B1 HSUPA CH10562 @ TBD dBm	TBD	mA
	WCDMA B1 HSUPA CH10700 @ TBD dBm	TBD	mA
	WCDMA B1 HSUPA CH10838 @ TBD dBm	TBD	mA
	WCDMA B3 HSUPA CH1162 @ TBD dBm	TBD	mA
	WCDMA B3 HSUPA CH1338 @ TBD dBm	TBD	mA
	WCDMA B3 HSUPA CH1513 @ TBD dBm	TBD	mA
	WCDMA B5 HSUPA CH4357 @ TBD dBm	TBD	mA
	WCDMA B5 HSUPA CH4408 @ TBD dBm	TBD	mA
	WCDMA B5 HSUPA CH4458 @ TBD dBm	TBD	mA
	WCDMA B8 HSUPA CH2937 @ TBD dBm	TBD	mA
	WCDMA B8 HSUPA CH3012 @ TBD dBm	TBD	mA

	WCDMA B8 HSUPA CH3088 @ TBD dBm	TBD	mA
LTE data transfer (GNSS OFF)	LTE-FDD B1 CH100 @ TBD dBm	TBD	mA
	LTE-FDD B1 CH300 @ TBD dBm	TBD	mA
	LTE-FDD B1 CH500 @ TBD dBm	TBD	mA
	LTE-FDD B3 CH1300 @ TBD dBm	TBD	mA
	LTE-FDD B3 CH1575 @ TBD dBm	TBD	mA
	LTE-FDD B3 CH1850 @ TBD dBm	TBD	mA
	LTE-FDD B5 CH2450 @ TBD dBm	TBD	mA
	LTE-FDD B5 CH2525 @ TBD dBm	TBD	mA
	LTE-FDD B5 CH2600 @ TBD dBm	TBD	mA
	LTE-FDD B7 CH2850 @ TBD dBm	TBD	mA
	LTE-FDD B7 CH3100 @ TBD dBm	TBD	mA
	LTE-FDD B7 CH3350 @ TBD dBm	TBD	mA
	LTE-FDD B8 CH3500 @ TBD dBm	TBD	mA
	LTE-FDD B8 CH3625 @ TBD dBm	TBD	mA
	LTE-FDD B8 CH3750 @ TBD dBm	TBD	mA
	LTE-TDD B20 CH6250 @ TBD dBm	TBD	mA
	LTE-TDD B20 CH6300 @ TBD dBm	TBD	mA
	LTE-TDD B20 CH6350 @ TBD dBm	TBD	mA
	LTE-TDD B28 CH9310 @ TBD dBm	TBD	mA
	LTE-TDD B28 CH9435 @ TBD dBm	TBD	mA
	LTE-TDD B28 CH9560 @ TBD dBm	TBD	mA
	LTE-TDD B38 CH37850 @ TBD dBm	TBD	mA
	LTE-TDD B38 CH38000 @ TBD dBm	TBD	mA
	LTE-TDD B38 CH38150 @ TBD dBm	TBD	mA

	LTE-TDD B40 CH38750 @ TBD dBm	TBD	mA
	LTE-TDD B40 CH39150 @ TBD dBm	TBD	mA
	LTE-TDD B40 CH39550 @ TBD dBm	TBD	mA
5G NR SA data transfer (GNSS OFF)	n1A CH426000 @ TBD dBm	TBD	mA
	n1A CH428000 @ TBD dBm	TBD	mA
	n1A CH430000 @ TBD dBm	TBD	mA
	n3A CH364000 @ TBD dBm	TBD	mA
	n3A CH368500 @ TBD dBm	TBD	mA
	n3A CH373000 @ TBD dBm	TBD	mA
	n7A CH526000 @ TBD dBm	TBD	mA
	n7A CH531000 @ TBD dBm	TBD	mA
	n7A CH536000 @ TBD dBm	TBD	mA
	n8A CH187000 @ TBD dBm	TBD	mA
	n8A CH188500 @ TBD dBm	TBD	mA
	n8A CH190000 @ TBD dBm	TBD	mA
	n20A CH160200 @ TBD dBm	TBD	mA
	n20A CH161200 @ TBD dBm	TBD	mA
	n20A CH162200 @ TBD dBm	TBD	mA
	n28A CH154600 @ TBD dBm	TBD	mA
	n28A CH156100 @ TBD dBm	TBD	mA
	n28A CH157600 @ TBD dBm	TBD	mA
	n77A CH623334 @ TBD dBm	TBD	mA
	n77A CH650000 @ TBD dBm	TBD	mA
	n77A CH676666 @ TBD dBm	TBD	mA
	n78A CH623334 @ TBD dBm	TBD	mA

	n78A CH636666 @ TBD dBm	TBD	mA
	n78A CH650000 @ TBD dBm	TBD	mA
5G NR NSA data transfer (GNSS OFF)	1A_n77A CH623334 @ TBD dBm	TBD	mA
	1A_n77A CH650000 @ TBD dBm	TBD	mA
	1A_n77A CH676666 @ TBD dBm	TBD	mA
	3A_n77A CH623334 @ TBD dBm	TBD	mA
	3A_n77A CH650000 @ TBD dBm	TBD	mA
	3A_n77A CH676666 @ TBD dBm	TBD	mA
	5A_n77A CH623334 @ TBD dBm	TBD	mA
	5A_n77A CH650000 @ TBD dBm	TBD	mA
	5A_n77A CH676666 @ TBD dBm	TBD	mA
	8A_n77A CH623334 @ TBD dBm	TBD	mA
	8A_n77A CH650000 @ TBD dBm	TBD	mA
	8A_n77A CH676666 @ TBD dBm	TBD	mA
	20A_n77A CH623334 @ TBD dBm	TBD	mA
	20A_n77A CH650000 @ TBD dBm	TBD	mA
	20A_n77A CH676666 @ TBD dBm	TBD	mA
	28A_n77A CH623334 @ TBD dBm	TBD	mA
	28A_n77A CH650000 @ TBD dBm	TBD	mA
	28A_n77A CH676666 @ TBD dBm	TBD	mA
	40A_n77A CH623334 @ TBD dBm	TBD	mA
	40A_n77A CH650000 @ TBD dBm	TBD	mA
	40A_n77A CH676666 @ TBD dBm	TBD	mA
	1A_n78A CH623334 @ TBD dBm	TBD	mA
	1A_n78A CH636666 @ TBD dBm	TBD	mA

	1A_n78A CH650000 @ TBD dBm	TBD	mA
	3A_n78A CH623334 @ TBD dBm	TBD	mA
	3A_n78A CH636666 @ TBD dBm	TBD	mA
	3A_n78A CH650000 @ TBD dBm	TBD	mA
	5A_n78A CH623334 @ TBD dBm	TBD	mA
	5A_n78A CH636666 @ TBD dBm	TBD	mA
	5A_n78A CH650000 @ TBD dBm	TBD	mA
	7A_n78A CH623334 @ TBD dBm	TBD	mA
	7A_n78A CH636666 @ TBD dBm	TBD	mA
	7A_n78A CH650000 @ TBD dBm	TBD	mA
	8A_n78A CH623334 @ TBD dBm	TBD	mA
	8A_n78A CH636666 @ TBD dBm	TBD	mA
	8A_n78A CH650000 @ TBD dBm	TBD	mA
	20A_n78A CH623334 @ TBD dBm	TBD	mA
	20A_n78A CH636666 @ TBD dBm	TBD	mA
	20A_n78A CH650000 @ TBD dBm	TBD	mA
	28A_n78A CH623334 @ TBD dBm	TBD	mA
	28A_n78A CH636666 @ TBD dBm	TBD	mA
	28A_n78A CH650000 @ TBD dBm	TBD	mA
	38A_n78A CH623334 @ TBD dBm	TBD	mA
	38A_n78A CH636666 @ TBD dBm	TBD	mA
	38A_n78A CH650000 @ TBD dBm	TBD	mA
	40A_n78A CH623334 @ TBD dBm	TBD	mA
	40A_n78A CH636666 @ TBD dBm	TBD	mA
	40A_n78A CH650000 @ TBD dBm	TBD	mA

6.3.3. AG568N-NA Power Consumption

Table 53: AG568N-NA Power Consumption (25 °C, 3.8 V Power Supply)

Description	Conditions	Typ.	Unit
OFF state	Power down	52	μA
Sleep state	**AT+CFUN=0**	2.865	mA
	AT+CFUN=4	2.955	mA
	LTE-FDD @ DRX = 0.32 s	5.843	mA
	LTE-FDD @ DRX = 0.64 s	4.378	mA
	LTE-FDD @ DRX = 1.28 s	3.695	mA
	LTE-FDD @ DRX = 2.56 s	3.360	mA
	5G NR FDD @ DRX = 0.32 s	10.079	mA
	5G NR FDD @ DRX = 0.64 s	6.515	mA
	5G NR FDD @ DRX = 1.28 s	4.850	mA
	5G NR FDD @ DRX = 2.56 s	4.546	mA
	5G NR TDD @ DRX = 0.32 s	11.080	mA
	5G NR TDD @ DRX = 0.64 s	7.083	mA
	5G NR TDD @ DRX = 1.28 s	5.156	mA
	5G NR TDD @ DRX = 2.56 s	4.797	mA
Idle state	LTE-FDD @ DRX = 0. 64 s	143.49	mA
	LTE-FDD @ DRX = 0. 64 s (USB active)	152.00	mA
	5G NR FDD @ DRX = 0.64 s	144.95	mA
	5G NR FDD @ DRX = 0.64 s (USB active)	153.47	mA
	5G NR TDD @ DRX = 0.64 s	142.74	mA
	5G NR TDD @ DRX = 0.64 s (USB active)	151.00	mA
LTE data transfer	LTE-FDD B2 CH700 @ 22.35 dBm	935	mA

(GNSS OFF)	LTE-FDD B2 CH900 @ 22.42 dBm	804	mA
	LTE-FDD B2 CH1100 @ 22.44 dBm	920	mA
	LTE-FDD B4 CH2000 @ 22.36 dBm	901	mA
	LTE-FDD B4 CH2175 @ 22.43 dBm	836	mA
	LTE-FDD B4 CH2350 @ 22.40 dBm	830	mA
	LTE-FDD B5 CH2450 @ 22.47 dBm	724	mA
	LTE-FDD B5 CH2525 @ 22.50 dBm	832	mA
	LTE-FDD B5 CH2600 @ 22.52 dBm	837	mA
	LTE-FDD B12 CH5060 @ TBD dBm	747	mA
	LTE-FDD B12 CH5095 @ TBD dBm	758	mA
	LTE-FDD B12 CH5130 @ TBD dBm	742	mA
	LTE-FDD B66 CH66536 @ 22.37 dBm	894	mA
	LTE-FDD B66 CH66886 @ 22.43 dBm	855	mA
	LTE-FDD B66 CH67036 @ 22.44 dBm	828	mA
5G NR SA data transfer (GNSS OFF)	n2A CH388000 @ 23.15 dBm	980	mA
	n2A CH392000 @ 23.14 dBm	925	mA
	n2A CH396000 @ 23.18 dBm	969	mA
	n5A CH175800 @ 22.85 dBm	1013	mA
	n5A CH176300 @ 22.87 dBm	1058	mA
	n5A CH176800 @ 22.85 dBm	1065	mA
	n12A CH147300 @ 22.86 dBm	905	mA
	n12A CH147500 @ 22.84 dBm	897	mA
	n12A CH147700 @ 22.84 dBm	895	mA
	n66A CH426000 @ 23.32 dBm	912	mA
	n66A CH429000 @ 23.31 dBm	900	mA

	n66A CH432000 @ 23.30 dBm	922	mA
	n77A CH623334@ 25.63 dBm	552	mA
	n77A CH650000@ 25.86 dBm	601	mA
	n77A CH676666@ 25.88 dBm	625	mA
	n78A CH623334 @ 26.03 dBm	568	mA
	n78A CH636666 @ 26.18 dBm	597	mA
	n78A CH650000 @ 26.03 dBm	618	mA
5G NR NSA data transfer (GNSS OFF)	5A_n2A CH388000 @ 22.66 dBm	1095	mA
	5A_n2A CH392000 @ 23.03 dBm	1074	mA
	5A_n2A CH396000 @ 22.95 dBm	1090	mA
	2A_n77A CH623334 @ 22.56 dBm	815	mA
	2A_n77A CH650000 @ 22.76 dBm	810	mA
	2A_n77A CH6766666 @ 22.86 dBm	815	mA
	5A_n77A CH623334 @ 22.62 dBm	865	mA
	5A_n77A CH650000 @ 22.88 dBm	851	mA
	5A_n77A CH6766666 @ 22.98 dBm	845	mA
	12A_n77A CH623334 @ 22.87 dBm	816	mA
	12A_n77A CH650000 @ 22.96 dBm	795	mA
	12A_n77A CH6766666 @ 23.08 dBm	788	mA
	66A_n77A CH623334 @ 22.63 dBm	820	mA
	66A_n77A CH650000 @ 22.72 dBm	808	mA
	66A_n77A CH6766666 @ 22.90 dBm	812	mA
	12A_n2A CH388000 @ 23.08 dBm	1056	mA
	12A_n2A CH392000 @ 22.70 dBm	1027	mA
	12A_n2A CH396000 @ 22.99 dBm	1037	mA

	2A_n5A CH175800 @ 22.52 dBm	1023	mA
	2A_n5A CH176300 @ 22.70 dBm	1048	mA
	2A_n5A CH176800 @ 22.62 dBm	1053	mA
	66A_n5A CH175800 @22.65 dBm	1046	mA
	66A_n5A CH176300 @ 22.64 dBm	1062	mA
	66A_n5A CH176800 @ 22.60 dBm	1067	mA
	5A_n66A CH426000 @ 22.67 dBm	1074	mA
	5A_n66A CH429000 @ 22.85 dBm	1080	mA
	5A_n66A CH432000 @ 22.94 dBm	1076	mA
	12A_n66A CH426000 @ 23.08dBm	1020	mA
	12A_n66A CH429000 @ 22.61 dBm	1029	mA
	12A_n66A CH432000 @ 22.64 dBm	1024	mA

6.3.4. AG568N-ROW Power Consumption

Table 54: AG568N-ROW Power Consumption (25 °C, 3.8 V Power Supply)

Description	Conditions	Typ.	Unit
OFF state	Power down	46	μA
Sleep state	**AT+CFUN=0**	3.877	mA
	AT+CFUN=4	3.890	mA
	WCDMA @ DRX = 0.64 s	5.391	mA
	WCDMA @ DRX = 1.28 s	4.638	mA
	WCDMA @ DRX = 2.56 s	4.238	mA
	WCDMA @ DRX = 5.12s	4.099	mA
	LTE-FDD @ DRX = 0.32 s	6.941	mA
	LTE-FDD @ DRX = 0.64 s	5.504	mA

	LTE-FDD @ DRX = 1.28 s	4.828	mA
	LTE-FDD @ DRX = 2.56 s	4.530	mA
	5G NR FDD @ DRX = 0.32 s	TBD	mA
	5G NR FDD @ DRX = 0.64 s	TBD	mA
	5G NR FDD @ DRX = 1.28 s	TBD	mA
	5G NR FDD @ DRX = 2.56 s	TBD	mA
	5G NR TDD @ DRX = 0.32 s	11.735	mA
	5G NR TDD @ DRX = 0.64 s	8.143	mA
	5G NR TDD @ DRX = 1.28 s	5.706	mA
	5G NR TDD @ DRX = 2.56 s	5.448	mA
Idle state	WCDMA @ Paging Frame = 64	148.65	mA
	WCDMA @ Paging Frame = 64 (USB active)	157.66	mA
	LTE-FDD @ DRX = 0.64 s	148.15	mA
	LTE-FDD @ DRX = 0.64 s (USB active)	159.57	mA
	5G NR FDD @ DRX = 0.64 s	TBD	mA
	5G NR FDD @ DRX = 0.64 s (USB active)	TBD	mA
	5G NR TDD @ DRX = 0.64 s	153.07	mA
	5G NR TDD @ DRX = 0.64 s (USB active)	156.68	mA
WCDMA voice call	WCDMA B1 CH10562 @ 23.17dBm	756	mA
	WCDMA B1 CH10700 @ 23.09 dBm	774	mA
	WCDMA B1 CH10838 @ 23.05 dBm	802	mA
	WCDMA B3 CH1162 @ 22.69 dBm	752	mA
	WCDMA B3 CH1338 @ 22.61 dBm	677	mA
	WCDMA B3 CH1513 @ 22.71 dBm	790	mA
WCDMA data	WCDMA B1 HSDPA CH10562 @ 22.04 dBm	696	mA

transfer (GNSS OFF)	WCDMA B1 HSDPA CH10700 @ 21.96 dBm	715	mA
	WCDMA B1 HSDPA CH10838 @ 21.92 dBm	725	mA
	WCDMA B3 HSDPA CH1162 @ 21.82 dBm	696	mA
	WCDMA B3 HSDPA CH1338 @ 21.83 dBm	681	mA
	WCDMA B3 HSDPA CH1513 @ 21.94 dBm	677	mA
	WCDMA B1 HSUPA CH10562 @ 21.62 dBm	640	mA
	WCDMA B1 HSUPA CH10700 @ 21.56 dBm	659	mA
	WCDMA B1 HSUPA CH10838 @ 21.47 dBm	673	mA
	WCDMA B3 HSUPA CH1162 @ 21.16 dBm	653	mA
	WCDMA B3 HSUPA CH1338 @ 21.05 dBm	620	mA
	WCDMA B3 HSUPA CH1513 @ 21.19 dBm	684	mA
LTE data transfer (GNSS OFF)	LTE-FDD B1 CH100 @ 22.79 dBm	760	mA
	LTE-FDD B1 CH300 @ 22.75 dBm	786	mA
	LTE-FDD B1 CH500 @ 22.74 dBm	791	mA
	LTE-FDD B3 CH1300 @ 22.49 dBm	804	mA
	LTE-FDD B3 CH1575 @ 22.40 dBm	812	mA
	LTE-FDD B3 CH1850 @ 22.46 dBm	866	mA
	LTE-FDD B19 CH6075@ 22.60 dBm	751	mA
	LTE-FDD B21 CH6525 @ 22.17 dBm	740	mA
	LTE-FDD B28 CH9310 @ 22.52 dBm	754	mA
	LTE-FDD B28 CH9435 @ 22.47 dBm	801	mA
	LTE-FDD B28 CH9560 @ 22.52 dBm	730	mA
5G NR SA data transfer (GNSS OFF)	n28A CH154600 @ 22.59 dBm	730	mA
	n28A CH157600 @ 22.42 dBm	804	mA
	n77A CH623334 @ 25.87 dBm	576	mA

	n77A CH650000 @ 25.93 dBm	596	mA
	n77A CH676666 @ 25.65 dBm	563	mA
	n78A CH623334 @ 26.35 dBm	596	mA
	n78A CH636666 @ 26.42 dBm	578	mA
	n78A CH650000 @ 26.43 dBm	618	mA
	n79A CH697094 @ 22.56 dBm	587	mA
	n79A CH713990 @ 22.58 dBm	587	mA
	n79A CH729468 @ 26.74 dBm	632	mA
5G NR NSA data transfer (GNSS OFF)	19A_n77A CH623334 @ 22.82 dBm	798	mA
	19A_n77A CH650000 @ 22.92 dBm	788	mA
	19A_n77A CH676666 @ 22.70 dBm	778	mA
	21A_n77A CH623334 @ 22.64 dBm	739	mA
	21A_n77A CH650000 @ 22.68 dBm	724	mA
	21A_n77A CH676666 @ 22.66 dBm	711	mA
	1A_n78A CH623334 @ 23.04 dBm	867	mA
	1A_n78A CH636666 @ 23.03 dBm	844	mA
	1A_n78A CH650000 @ 23.06 dBm	854	mA
	3A_n78A CH623334 @ 25.88 dBm	1137	mA
	3A_n78A CH636666 @ 25.95 dBm	1119	mA
	3A_n78A CH650000 @ 25.95 dBm	1140	mA
	19A_n78A CH623334 @ 23.04 dBm	814	mA
	19A_n78A CH636666 @ 23.10 dBm	783	mA
	19A_n78A CH650000 @ 23.12 dBm	793	mA
	21A_n78A CH623334 @ 22.87 dBm	743	mA
	21A_n78A CH636666 @ 22.94 dBm	717	mA

	21A_n78A CH650000 @ 22.93 dBm	727	mA
	28A_n78A CH623334 @ 22.93 dBm	808	mA
	28A_n78A CH636666 @ 22.91dBm	782	mA
	28A_n78A CH650000 @ 23.00 dBm	794	mA
	1A_n79A CH697094 @ 23.40 dBm	883	mA
	1A_n79A CH713990 @ 23.38 dBm	880	mA
	1A_n79A CH729468 @ 23.48 dBm	888	mA
	3A_n79A CH697094 @ 23.28 dBm	835	mA
	3A_n79A CH713990 @ 23.27 dBm	836	mA
	3A_n79A CH729468 @ 23.27 dBm	843	mA
	19A_n79A CH697094 @ 23.50 dBm	819	mA
	19A_n79A CH713990 @ 23.51 dBm	819	mA
	19A_n79A CH729468 @ 23.56 dBm	826	mA
	21A_n79A CH697094 @ 23.28 dBm	756	mA
	21A_n79A CH713990 @ 23.24 dBm	753	mA
	21A_n79A CH729468 @ 23.32 dBm	760	mA
	28A_n79A CH697094 @ 23.43 dBm	818	mA
	28A_n79A CH713990 @ 23.39 dBm	818	mA
	28A_n79A CH729468 @ 23.42 dBm	825	mA

6.4. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 55: ESD Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±6	±10	kV
Antenna Interfaces	±5	±10	kV
Other Interfaces	±0.5	±1	kV

6.5. Operating and Storage Temperatures

Table 56: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating temperature range [20]	-35	+25	+75	°C
Extended operating temperature range [21]	-40	-	+85	°C
eCall temperature range [22]	-40	-	+95	°C
Storage temperature range	-40	-	+95	°C

6.6. Thermal Dissipation

The module offers the best performance when all internal IC chips are working within their operating temperatures. When the IC chip reaches or exceeds the maximum junction temperature, the module may still work but the performance and function (such as RF output power, data rate, etc.) will be affected to a certain extent. Therefore, the thermal design should be maximally optimized to ensure all internal IC chips always work within the recommended operating temperature range.

The following principles for thermal consideration are provided for reference:

[20] Within the operating temperature range, the module meets 3GPP specifications.
[21] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, eCall*, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.
[22] Within eCall temperature range, the eCall function must be functional until the module is broken. When the ambient temperature is between 75 °C and 95 °C and the module temperature has reached the threshold value, the module will trigger protective measures (such as reduce power, decrease throughput, unregister the device, etc.) to ensure the full function of eCall.

- Keep the module away from heat sources on your PCB, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Follow the principles below when the heatsink is necessary:
  - Do not place large size components in the area where the module is mounted on your PCB to reserve enough place for heatsink installation.
  - Attach the heatsink to the shielding cover of the module; In general, the base plate area of the heatsink should be larger than the module area to cover the module completely;
  - Choose the heatsink with adequate fins to dissipate heat;
  - Choose a TIM (Thermal Interface Material) with high thermal conductivity, good softness and good wettability and place it between the heatsink and the module;
  - Fasten the heatsink with four screws to ensure that it is in close contact with the module to prevent the heatsink from falling off during the drop, vibration test, or transportation.

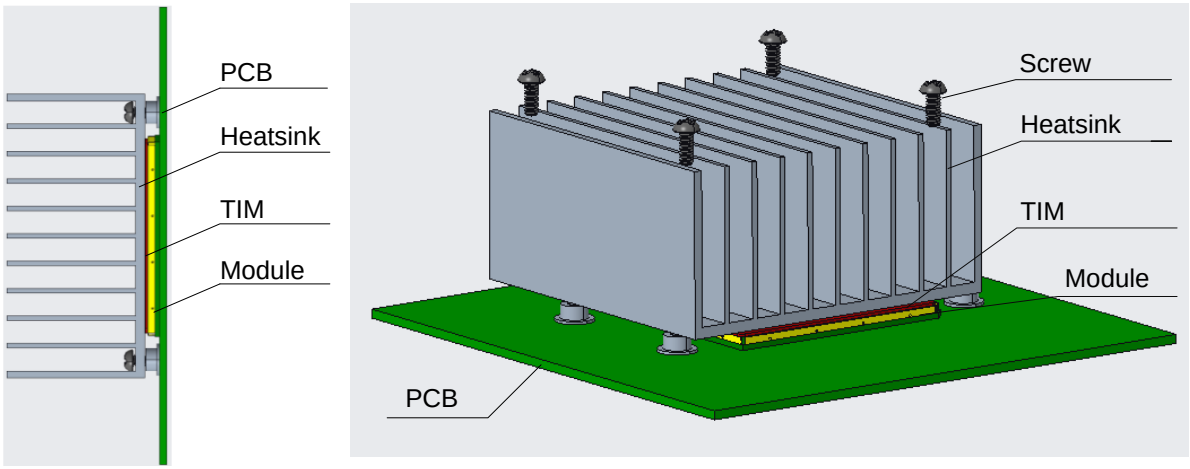


Figure 38: Placement and Fixing of the Heatsink

NOTE

1. The module offers the best performance when the internal BB chip stays below 105°C. When the maximum temperature of the BB chip reaches or exceeds 105°C, the module works normal but provides reduced performance (such as RF output power, data rate, etc.). When the maximum BB chip temperature reaches or exceeds 115°C, the module will disconnect from the network, and it will recover to network connected state after the maximum temperature falls below 115°C. Therefore, the thermal design should be maximally optimized to make sure the maximum BB chip temperature always maintains below 105°C. Customers can execute related software command to get the maximum BB chip temperature.
2. For more detailed guidelines on thermal design, see ***document [7].***

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

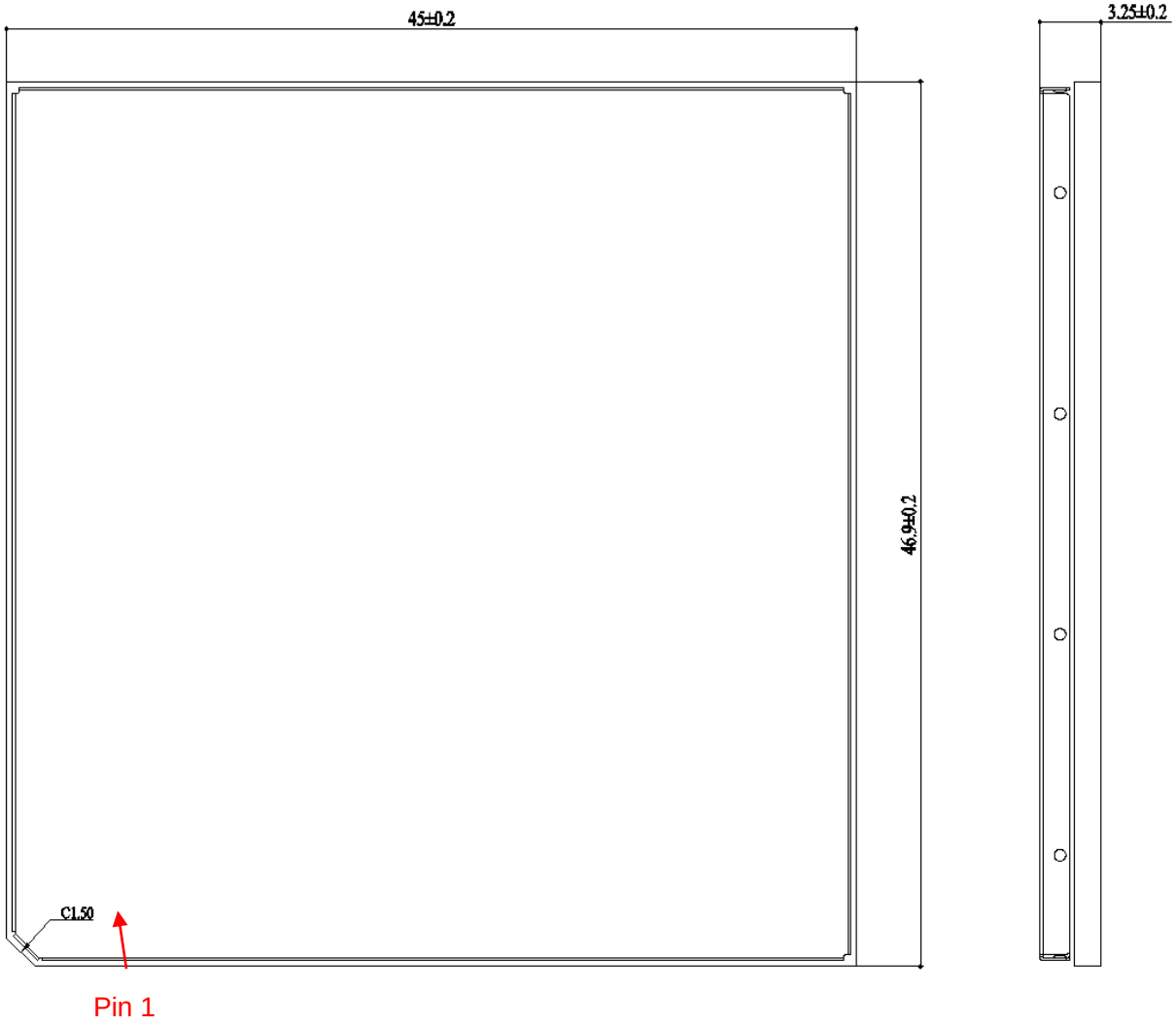


Figure 39: Module Top and Side Dimensions (Unit: mm)

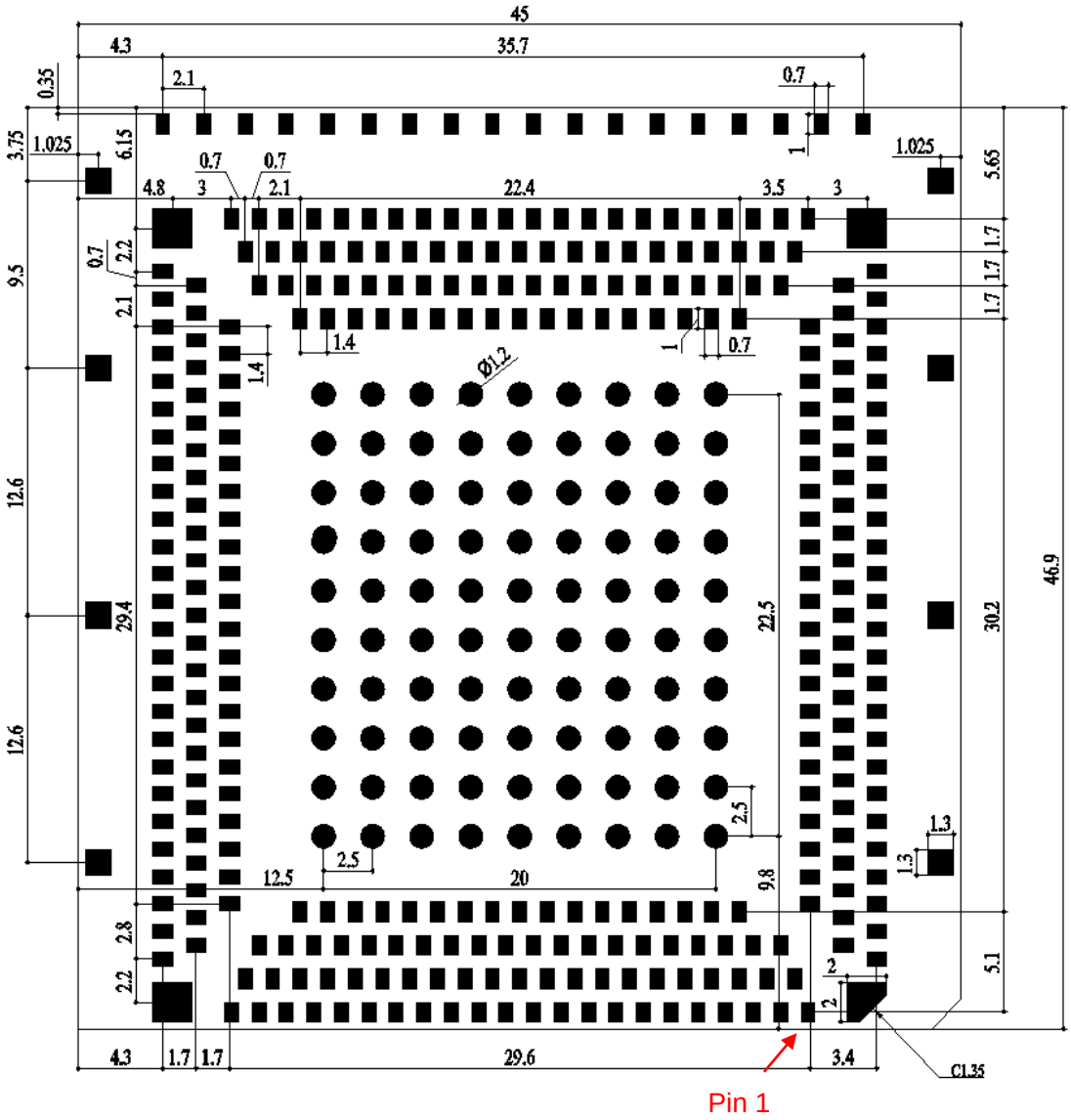


Figure 40: Module Bottom Dimensions (Bottom View, Unit: mm)

NOTE

The package warpage level of the module conforms to *JEITA ED-7306 standard*.

7.2. Recommended Footprint

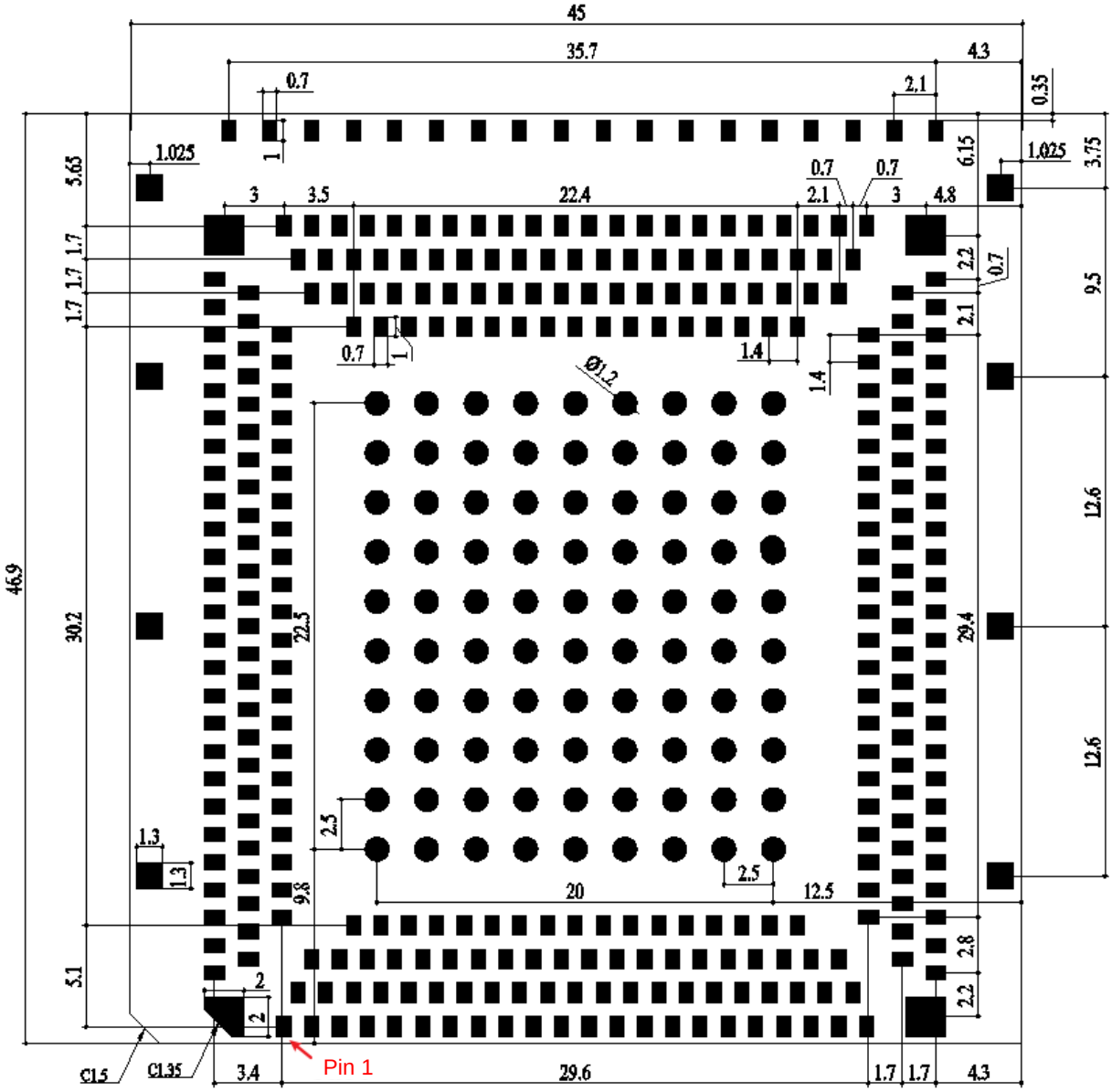


Figure 41: Recommended Footprint (Top View, Unit: mm)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

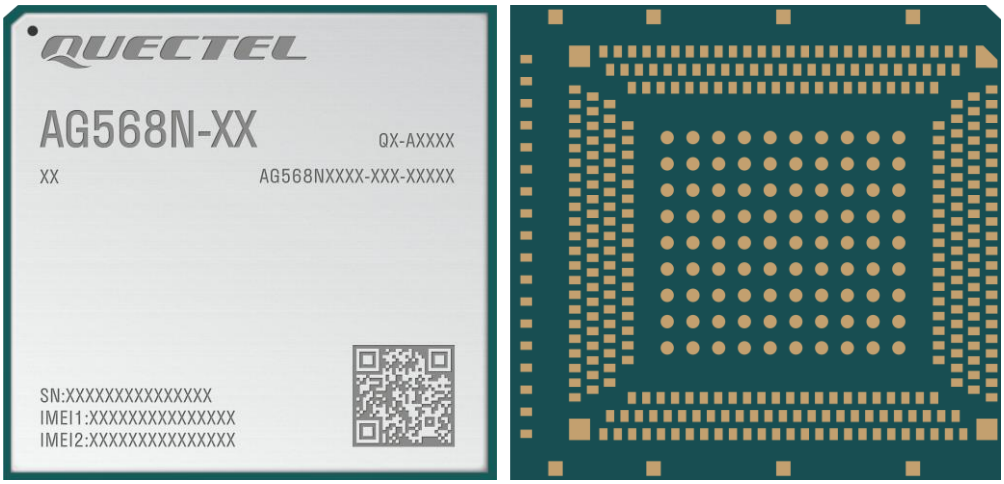


Figure 42: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [23] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[23] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [8].***

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below:

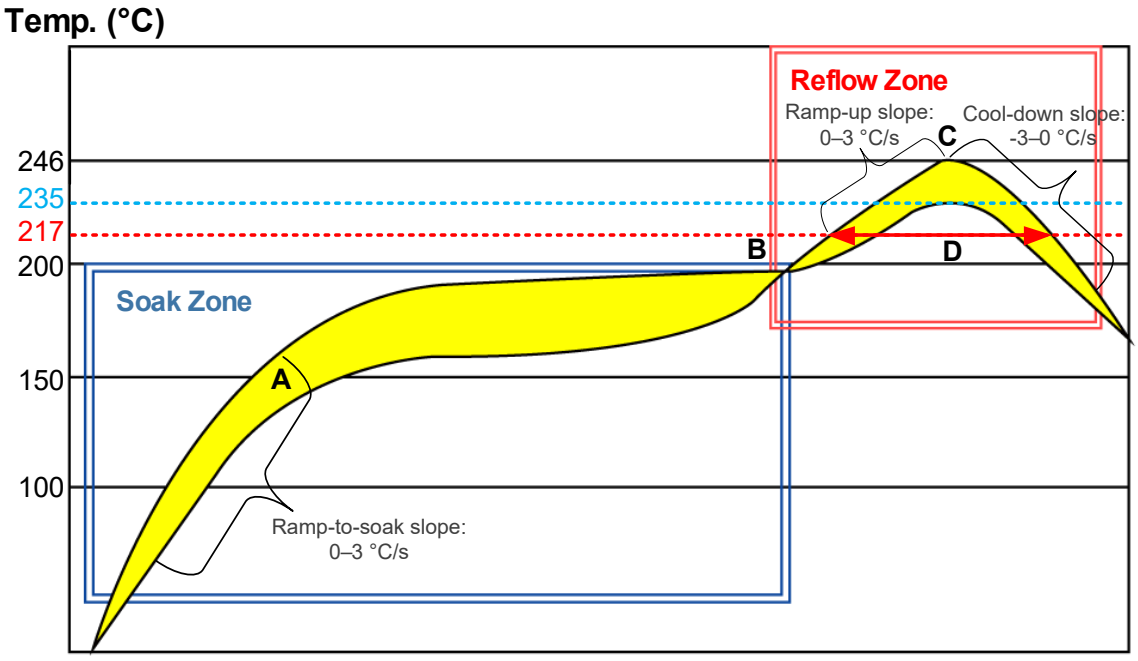


Figure 43: Recommended Reflow Soldering Thermal Profile

Table 57: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. If a conformal coating is necessary for the module, do not use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
3. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
4. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [8]***.

8.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

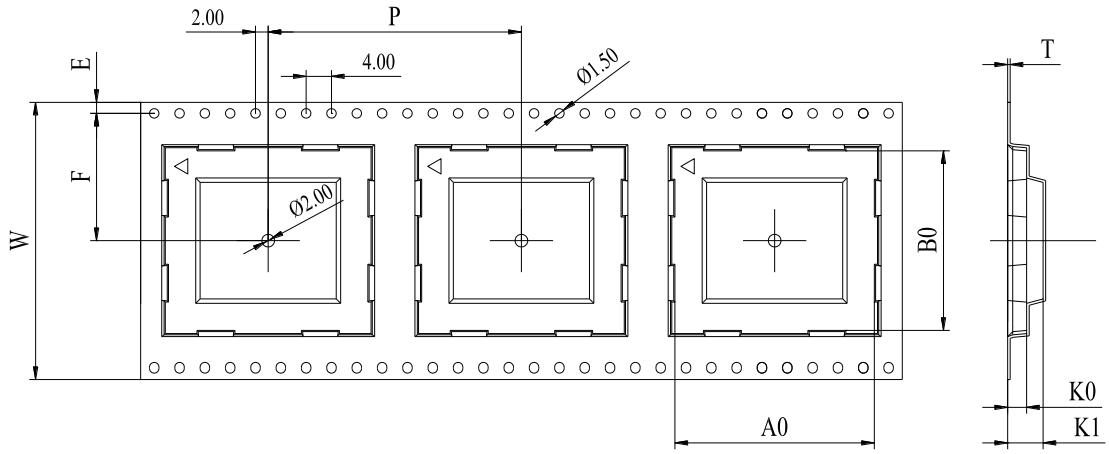


Figure 44: Carrier Tape Dimension Drawing

Table 58: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
72	64	0.4	47.5	45.6	4.55	6	34.2	1.75

8.3.2. Plastic Reel

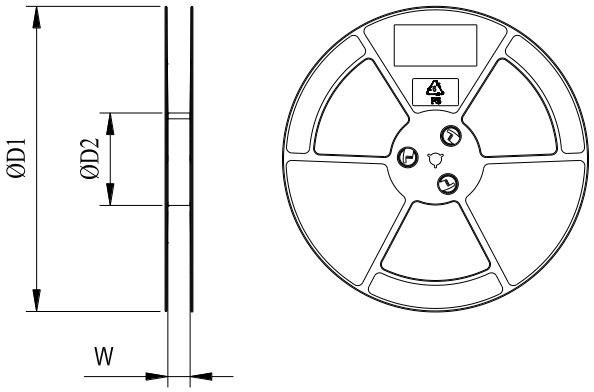


Figure 45: Plastic Reel Dimension Drawing

Table 59: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
380	180	72.5

8.3.3. Mounting Direction

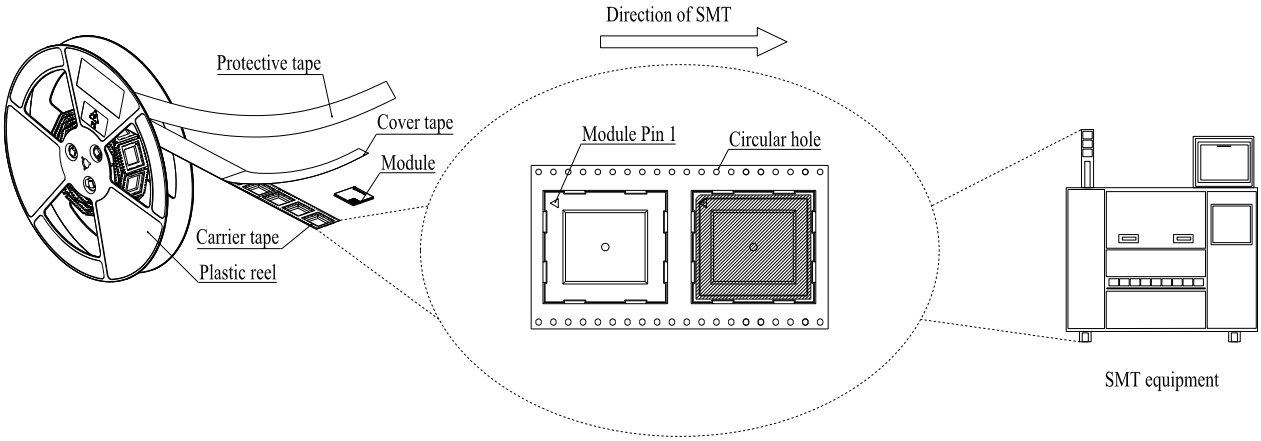
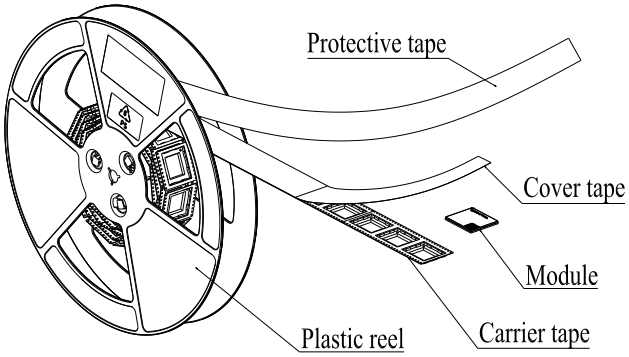


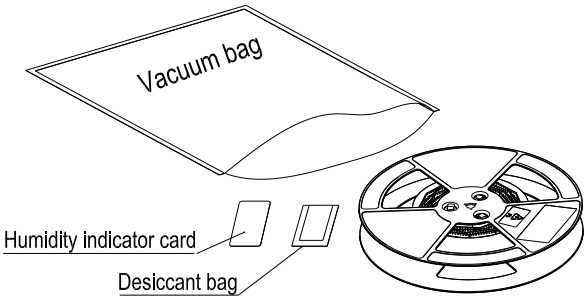
Figure 46: Mounting Direction

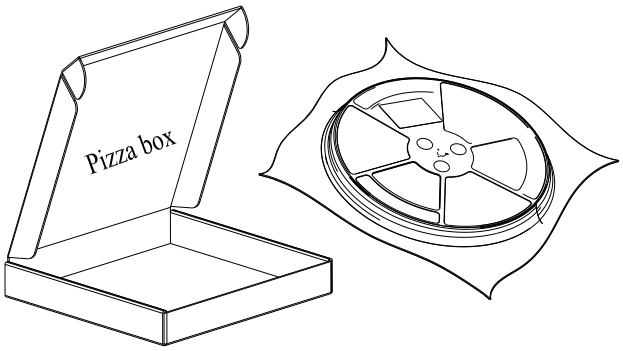
8.3.4. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 150 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 carton box and seal it. 1 carton box can pack 600 modules.

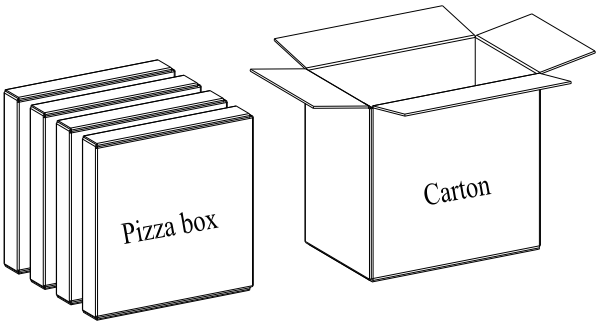


Figure 47: Packaging Process

9 Appendix References

Table 60: Related Documents

Document Name
[1] Quectel_V2X&5G_EVB_User_Guide
[2] Quectel_AG56xN_Series_QuecOpen_Device_Management_API_Reference_Manual
[3] Quectel_AG56xN_Series_QuecOpen_AT_Commands_Manual
[4] Quectel_AG56xN_Series_QuecOpen_Low_Power_Mode_Application_Note
[5] Quectel_AG568N_Series_QuecOpen_Reference_Design
[6] Quectel_RF_Layout_Application_Note
[7] Quectel_Module_Thermal_Design_Guide
[8] Quectel_Module_SMT_Application_Note

Table 61: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
5G NR	5G New Radio
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-rate
AMR-WB	Adaptive Multi-Rate Wideband
AP	Application Processor
API	Application Program Interface

ASRC	Asynchronous Sampling Rate Converter
bps	Bits Per Second
CA	Carrier Aggregation
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear To Send
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DL	Downlink
DRX	Discontinuous Reception
DSDS	Dual SIM Dual Standby
DTE	Data Terminal Equipment
EDGE	Enhanced Data Rates for GSM Evolution
EFR	Enhanced Full Rate
EGSM	Extended GSM900 Band (including standard GSM900 band)
EMI	Electromagnetic Interference
eMMC	Embedded Multimedia Card
ESD	Electrostatic Discharge
EVB	Evaluation Board
FDD	Frequency Division Duplex
FR	Full Rate
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPIOs	General-purpose Input/Output
GPRS	General Packet Radio Service

GPS	Global Positioning System
GSM	Global System for Mobile Communications
HB	High Band
HPUE	High Power User Equipment
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
IC	Integrated Circuit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
I/O	Input/Output
Inom	Nominal Current
LB	Low Band
LDO	Low-dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LMHB	Low/Middle/High Band
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MAC	Media Access Control
MB	Middle Band
MCU	Microcontroller Unit
MDIO	Management Data Input/Output
ME	Mobile Equipment

MHB	Middle/High Band
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MT	Mobile Terminated
MLCC	Multi-layer Ceramic Chip Capacitor
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
NSA	Non-Stand Alone
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PHY	Physical Layer
PMIC	Power Management Integrated Circuit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RHCP	Right Hand Circularly Polarized
Rx	Receive
SA	Stand Alone
SCS	Sub-Carrier Space
SDIO	Secure Digital Input/Output
SIMO	Single Input Multiple Output
SMD	Surface Mount Device

SMS	Short Message Service
SPI	Serial Peripheral Interface
TDD	Time Division Duplexing
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TRX	Transmit & Receive
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
V2I	Vehicle-to-Infrastructure
V2P	Vehicle to Pedestrian
V2V	Vehicle-to-Vehicle
V2X	Vehicle-to-Everything
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage Value
Vnom	Nominal Voltage Value
Vmin	Minimum Voltage Value
$V_{IH}max$	Maximum High-level Input Voltage
$V_{IH}min$	Minimum High-level Input Voltage
$V_{IL}max$	Maximum Low-level Input Voltage
$V_{IL}min$	Minimum Low-level Input Voltage
$V_{I}max$	Absolute Maximum Input Voltage
$V_{I}min$	Absolute Minimum Input Voltage

V_{OH}max	Maximum High-level Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
Wi-Fi	Wireless Fidelity
WLAN	Wireless Local Area Network