AG55xQ Series QuecOpen Hardware Design

Automotive Module Series

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Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2019-12-10	Liam CAO/ Benjamin CHAI/ Javen SHEN	Creation of the document
1.0	2021-08-27	Liam CAO/ Benjamin CHAI/ Javen SHEN	First official release
1.1	2022-03-08	Liam CAO/ Benjamin CHAI/ Javen SHEN	1. Added n48 and n77 on AG55xQ-NA. 2. Updated the DC characteristic of pins 53, 55, 56, 58 and 139; deleted the DC characteristic of pin 142 (Table 7). 3. Updated the pin description of coexistence control interface (Table 7 and Table 21). 4. Updated the reference design of power supply (Figure 6 and Figure 7). 5. Updated the power-up timing and added a note about it (Chapter 3.4.1). 6. Updated the power-down timing and added a note about it (Chapter 3.5.1). 7. Updated the recommended resistance range of the resistor between SDC1_CLK and the SD card connector from 20–35 Ω to 20–30 Ω (Chapter 4.10). 8. Updated the reference design of RGMII interface with PHY application (Figure 34). 9. Updated the recommended C-V2X antenna frequency range (Table 48). 10. Added max. current requirements for some of the power supply pins (Table 50). 11. Updated the recommended maximum slope parameter for reflow zone (Chapter 8.2).

1.2.0	2022-11-30	Liam CAO/ Benjamin CHAI/ Javen SHEN	Preliminary: 1. Deleted the WCDMA bands of AG55xQ-NA. 2. Added the dual frequency GNSS of L1 + L2 * (Table 4). 3. Updated the information of USB serial drivers (Table 5). 4. Updated the information of LPM and wakeup timing (Chapter 3.2.1.2). 5. Updated the information of PCM interface (Chapter 4.5). 6. Updated the reference design of PCIe interface (Chapter 4.6). 7. Updated the reference design of WLAN & Bluetooth application interfaces (Figure 28). 8. Updated the SPI timing (Figure 31). 9. Updated the reference design of USB_BOOT interface (Figure 34). 10. Updated the note description in GNSS performance (Chapter 5.2.3). 11. Updated the information of manufacturing and soldering (Chapter 8.2).

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1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio

AG55xQ family QuecOpen® module is a baseband processor platform based on ARM Cortex A7 kernel. The maximum dominant frequency is up to 1.5 GHz. You can use AG55xQ family QuecOpen® module as the basis for development of QuecOpen® applications.

This document defines the AG55xQ family in QuecOpen® solution and describes its air interface and hardware interfaces which are connected with your applications.

This document helps you quickly understand the interface specifications, electrical and mechanical details, as well as other related information of the module. To facilitate application designs, it also includes some reference designs for your reference. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

Table 1: Applicable Module Models

Module Family	Module Series	Module Model
AG55xQ	AG550Q	AG550Q-CN/-EU/-NA
	AG551Q	AG551Q-CN/-EU/-NA
	AG553Q	AG553Q-EU

1.1. Special Marks

Table 2: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, RGMII_TX_[0:3] refers to all four RGMII_TX pins, RGMII_TX_0, RGMII_TX_1, RGMII_TX_2, and RGMII_TX_3.

2 Product Overview

2.1. Frequency Bands and Functions

AG55xQ family is a series of automotive-grade 5G NR Sub-6 GHz wireless communication modules, and provides data connectivity on 5G NR, LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, EDGE and GPRS networks. It also provides C-V2X [1], DSSS/DSDA [2], single-frequency/dual-frequency GNSS [3] and voice functionalities to meet specific application demands.

Engineered to meet the demanding requirements in automotive applications and other harsh operating conditions, the module offers a premium solution for secure and reliable connected car solutions and self-driving solutions. It is widely used in telematics boxes (T-Box), telematics control units (TCU), advanced driver-assistance systems (ADAS), C-V2X (V2V, V2I, V2P) systems, on-board units (OBU), roadside units (RSU), and other automotive/traffic systems.

With a compact profile of 54.5 mm × 53.0 mm × 3.45 mm, the module can meet almost all requirements for automobile applications. It is an SMD type module which can be embedded into applications through its 524 LGA pins.

Table 3: Brief Introduction

Basic Information	
Pin number and package	524 LGA pins
Dimensions	(54.5 ± 0.2) mm × (53.0 ± 0.2) mm × (3.45 ± 0.2) mm
Weight	● AG550Q series: approx. 21 g ● AG551Q series: approx. 18 g ● AG553Q-EU: approx. 24 g
Wireless technologies	● 5G NR, LTE-FDD, LTE-TDD, WCDMA, GSM ● GNSS [3] ● C-V2X [1]

[1] Only AG550Q series and AG553Q-EU support C-V2X.
[2] Only AG553Q-EU supports DSDA; AG550Q and AG551Q series support DSSS.
[3] Both single-frequency and dual-frequency GNSS are optional.

Table 4: Frequency Bands and GNSS Function

Network Type/Feature		AG55xQ-CN		AG55xQ-EU			AG55xQ-NA	
		AG550Q-CN	AG551Q-CN	AG550Q-EU	AG551Q-EU	AG553Q-EU	AG550Q-NA	AG551Q-NA
5G NR	5G FDD [4]	n1/n3/n28		n1/n3/n8/n20/n28			n2/n5/n25/n66/n71	
	5G TDD	n41/n78/n79		n41/n78			n41/n48/n77/n78	
LTE	LTE-FDD [5]	B1/B3/B5/B7/B8		B1/B2/B3/B4/B5/B7/B8/B20/B28/B32			B2/B4/B5/B7/B12/B13/B14/B17/B25/ B26/B28/B29/B30/B66/B71	
	LTE-TDD	B34/B38/B39/B40/B41		B38/B40/B41/B42			B41/B48	
WCDMA		B1/B8		B1/B3/B5/B6/B8			-	
GSM		EGSM900/DCS1800		EGSM900/DCS1800/GSM850/PCS1900			PCS1900	
C-V2X		B47	-	B47	-	B47	B47	-
Dual SIM Feature		DSSS	DSSS	DSSS	DSSS	DSDA [6]	DSSS	DSSS
GNSS (optional)		● Single-frequency GNSS: L1 ● Dual-frequency GNSS: L1 + L5; L1 + L2* (optional) ● GNSS constellation: GPS, GLONASS, BDS, Galileo, QZSS						

[4] 5G NR FDD n1, n3 and n28 of AG55xQ-CN support SA only.
[5] LTE-FDD B29, B30 and B32 support reception (Rx) only.
[6] The (U)SIM2 for DSDA supports 2G/4G only.

2.2. Key Features

The following table describes the detailed features of the module.

Table 5: Key Features

Feature	Details
Power Supply	**VBAT_BB/VBAT_RF:** ● Supply voltage range: 3.3–4.3 V ● Typical supply voltage: 3.8 V **VBAT_CV2X:** ● Supply voltage range: 4.75–5.25 V ● Typical supply voltage: 5.0 V
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast
(U)SIM Interfaces	● Supports dual (U)SIM cards ● (U)SIM1 and (U)SIM2: 1.8/3.0 V
Analog Audio Interface (Optional)	● Built-in audio codec with two microphone inputs and two SPK outputs
I2S Interface	● Used for external codec configuration by default ● Supports master and slave modes
I2C Interface	● Used for external codec configuration and IMU by default ● Compliant with *I2C-bus Specification Version 3.0* ● Multi-master is not supported
PCM Interface	● Used for Bluetooth audio data transmission by default ● Supports 16-bit linear data format ● Supports long frame synchronization and short frame synchronization ● Supports master and slave modes
USB Interfaces	● Compliant with USB 3.1 Gen 2 and USB 2.0 specifications, with maximum theoretical transmission rates up to 10 Gbps on USB 3.1 and 480 Mbps on USB 2.0 ● USB 2.0 and USB 3.1 are used for AT command communication, data transmission, software debugging and GNSS NMEA sentences output. ● Only USB 2.0 can be used for firmware upgrade. ● USB 3.1 is used for data communication with AP by default. ● When USB 2.0 and USB 3.1 are connected to the same host, USB 3.1 takes effect by default. ● Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–5.18 and Android 4.x–12.x

UART Interfaces	**UART1:** ● Used for data transmission ● Baud rate reach up to 921600 bps, 115200 bps by default ● Supports RTS and CTS hardware flow control **Bluetooth UART:** ● Used for data transmission; used for Bluetooth function by default ● Baud rate reach up to 921600 bps, 115200 bps by default ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for Linux console and log output ● 115200 bps baud rate by default
SDIO Interface	● Compliant with SD 3.0 protocol ● Supports eMMC and SD card
SPI Interfaces	● Supports 2 SPI interfaces by default ● Supports master mode only ● Maximum clock frequency rate: 50 MHz
RGMII Interface	Supports 10/100/1000 Mbps Ethernet connection [7]
WLAN and Bluetooth Application Interfaces	● Supports PCIe (Gen 3) interface for WLAN ● Supports UART and PCM interfaces for Bluetooth
PCIe Interface	● Compliant with *PCI Express Base Specification Revision 3.0* ● Supports 2 PCIe lanes, with maximum rate of 8 GT/s × 1 theoretically ● Used for WLAN function by default
Antenna Interfaces	● One Main antenna interface (ANT_MAIN) ● One Rx-diversity antenna interface (ANT_DRX) ● Two MIMO antenna interfaces (ANT_MIMO3, ANT_MIMO4) ● Two DSDA antenna interfaces (ANT_DSDA_MAIN, ANT_DSDA_DIV) [8] ● Two C-V2X antenna interfaces (ANT_CV2X_TRX0, ANT_CV2X_TRX1) [9] ● One GNSS antenna interface (ANT_GNSS)
Temperature Range	● Operating temperature range: -35 to +75 °C [10] ● Extended temperature range: -40 to +85 °C [11] ● eCall temperature range: -40 to +95 °C [12] ● Storage temperature range: -40 to +95 °C
AT Commands	● *3GPP TS 27.007* and *3GPP TS 27.005* AT commands

[7] Gigabit Ethernet is an optional function; RGMII interface is supported by default.
[8] Only AG553Q-EU supports DSDA; AG550Q and AG551Q series support DSSS.
[9] Only AG550Q series and AG553Q-EU support C-V2X.
[10] Within the operating temperature range, the module meets 3GPP specifications.
[11] Within the extended temperature range, the module remains fully functional and the ability to establish and maintain functions such as voice, SMS, data transmission, emergency call, etc, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.
[12] Within eCall temperature range, the emergency call function must be functional until the module is broken. When the ambient temperature is between 75 °C and 95 °C and the module temperature has reached the threshold value, the module will trigger protective measures (such as reduce power, decrease throughput and unregister the device) to ensure the full function of emergency call.

	● Quectel enhanced AT commands
Audio Features	● GSM: HR/FR/EFR/AMR/AMR-WB ● WCDMA: AMR/AMR-WB ● LTE: AMR/AMR-WB ● Support echo cancellation and noise suppression
Transmitting Power	● Class 2 (26 dBm +1/-2 dB) for 5G NR TDD HPUE n41/n77/n78/n79 bands ● Class 3 (23 dBm ±2 dB) for 5G NR FDD bands and 5G NR TDD n48 ● Class 3 (23 dBm ±2 dB) for LTE bands ● Class 3 (23 dBm ±2 dB) for WCDMA bands ● Class 4 (33 dBm ±2 dB) for GSM850 ● Class 4 (33 dBm ±2 dB) for EGSM900 ● Class 1 (30 dBm ±2 dB) for DCS1800 ● Class 1 (30 dBm ±2 dB) for PCS1900 ● Class E2 (27 dBm ±3 dB) for GSM850 8-PSK ● Class E2 (27 dBm ±3 dB) for EGSM900 8-PSK ● Class E2 (26 dBm ±3 dB) for DCS1800 8-PSK ● Class E2 (26 dBm ±3 dB) for PCS1900 8-PSK
C-V2X Features (Optional) [13]	● Supports C-V2X TDD up to 30 Mbps (UL)/30 Mbps (DL) ● Supports globally unified ITS @ 5.9 GHz
5G NR Features	● Supports 3GPP Rel-15 ● Supported modulations: Uplink: π/2-BPSK, QPSK, 16QAM, 64QAM and 256QAM Downlink: QPSK, 16QAM, 64QAM and 256QAM ● Supports 4 × 4 MIMO for MHB bands in DL direction ● Supports SCS 15 kHz (FDD) and 30 kHz (TDD) ● Supports Option 3x, 3a and Option 2 ● Supports SA and NSA ● Max. transmission data rates: NSA: 2.4 Gbps (DL)/550 Mbps (UL) SA: 2.0 Gbps (DL)/450 Mbps (UL)
LTE Features	● Supports up to 4CA Cat 19 LTE-FDD and TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports 4 × 4 MIMO for MHB bands in DL direction ● Supports modulations: Uplink: QPSK, 16QAM, 64QAM, 256QAM* Downlink: QPSK, 16QAM, 64QAM, 256QAM ● LTE-FDD: Max. 1.6 Gbps (DL)/200 Mbps (UL) ● LTE-TDD: Max. 1.4 Gbps (DL)/120 Mbps (UL)
UMTS Features	● Supports 3GPP Rel-8 DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA ● Supports QPSK, 16QAM and 64QAM modulation

[13] Only AG550Q series and AG553Q-EU support C-V2X.

	● DC-HSDPA: Max. 42 Mbps (DL) ● HSUPA: Max. 5.76 Mbps (UL) ● WCDMA: Max 384 kbps (DL)/384 kbps (UL)
GSM Features	**GPRS:** ● Supports GPRS multi-slot class 33 (33 by default) ● Coding scheme: CS 1–4 ● Max. 107 kbps (DL)/85.6 kbps (UL) **EDGE:** ● Supports EDGE multi-slot class 33 (33 by default) ● Supports GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) ● Downlink coding schemes: MCS 1–9 ● Uplink coding schemes: MCS 1–9 ● Max. 296 kbps (DL)/236.8 kbps (UL)
Rx-diversity	Supports 5G, LTE and WCDMA Rx-diversity
GNSS (Optional)	● Supports GPS, GLONASS, BDS, Galileo, QZSS ● Supports L1 + L5/L1 + L2 * dual-frequency GNSS ● Protocol: NMEA 0183 ● Update rate: 1 Hz by default, max. up to 10 Hz
Firmware Upgrade	● USB 2.0 interface ● DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- LPDDR4X + NAND flash
- Radio frequency
- Peripheral interfaces

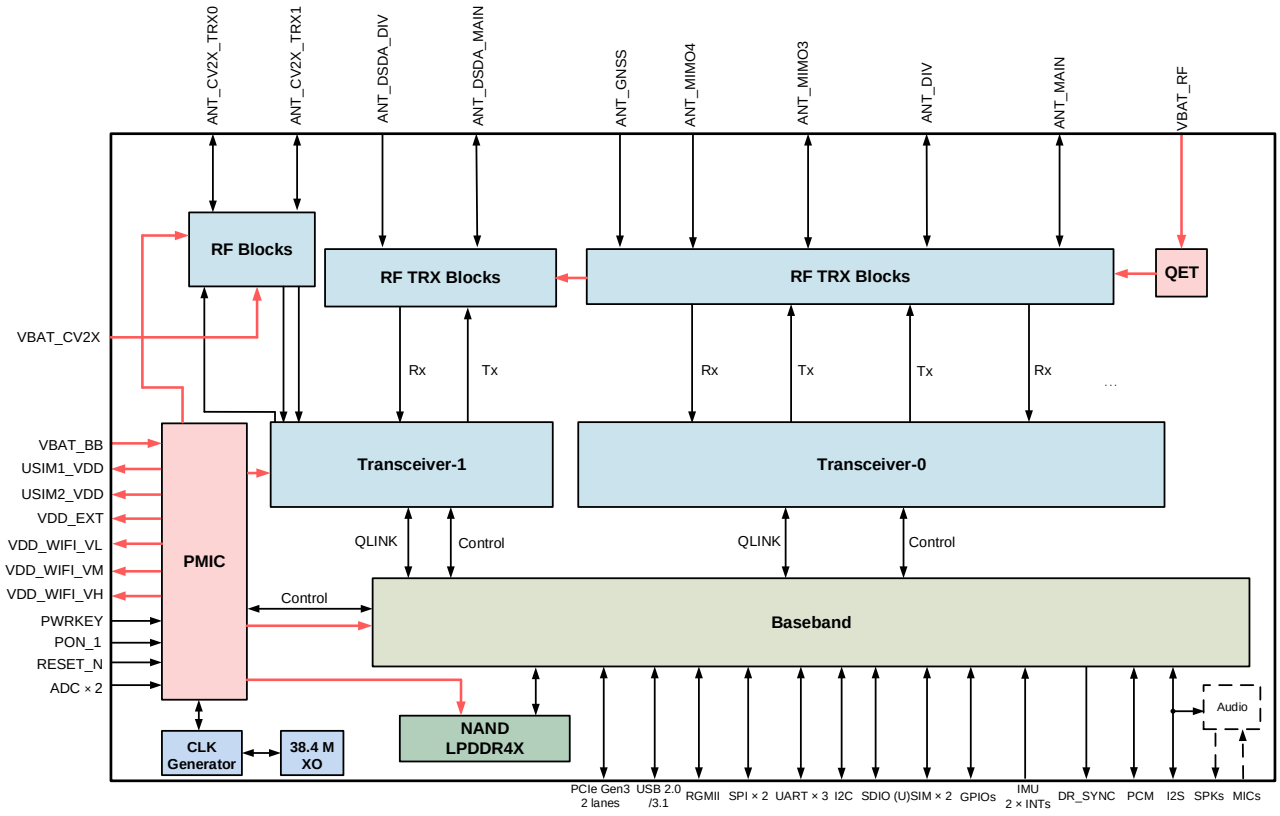


Figure 1: Functional Diagram

2.4. Pin Assignment

The following figure shows the pin assignment of the module.

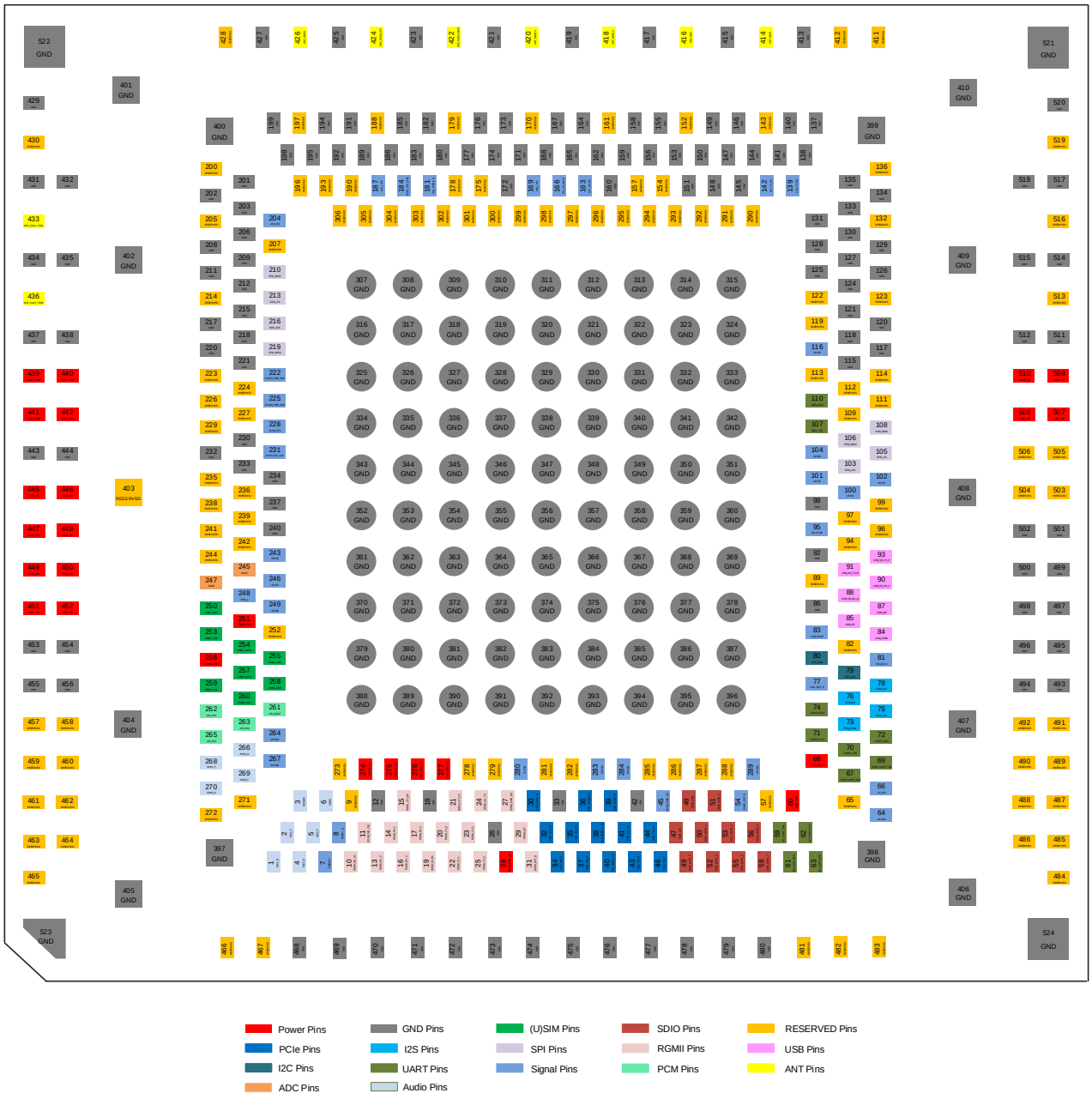


Figure 2: Pin Assignment (Top View)

NOTE

1. Unless otherwise specified, keep all RESERVED and unused pins unconnected.
2. GND pins should be connected to ground in the design.

2.5. Pin Description

2.5.1. Pin Definition

The following tables show the pin definition of the module.

Table 6: I/O Parameters Definition

Symbol	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

Table 7: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	449, 450, 451, 452	PI	Power supply for the module's baseband part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 1.5 A.
VBAT_RF	445, 446, 447, 448, 507, 508, 509,	PI	Power supply for the module's RF part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 3.0 A in a burst transmission.

	510				
VBAT_CV2X [14]	439, 440, 441, 442	PI	Power supply for the module's C-V2X part	Vmax = 5.25 V Vmin = 4.75 V Vnom = 5.0 V	It must be provided with sufficient current up to 1.6 A.
VDD_EXT	68	PO	Provide 1.8 V for external circuits	Vnom = 1.8 V $I_O$max = 50 mA	This pin can be used to connect with VDD_IO of Quectel AF50T, it also can be used as power supply for external pull up circuits. It is recommended to reserve a test point for this pin.
VDD_WIFI_VL	274, 275	PO	0.95 V low-voltage power supply for Wi-Fi & Bluetooth modules	Vmin = 0.824 V Vmax = 1.05 V $I_O$max = 1.7 A	Power supply for Quectel AF50T.
VDD_WIFI_VM	276	PO	1.35 V medium-voltage power supply for Wi-Fi & Bluetooth modules	Vmin = 1.224 V Vmax = 1.35 V $I_O$max = 400 mA	
VDD_WIFI_VH	277	PO	1.95 V high-voltage power supply for Wi-Fi & Bluetooth modules	Vmin = 1.8 V Vmax = 2.0 V $I_O$max = 400 mA	
GND	12, 18, 26, 33, 42, 86, 92, 98, 115, 117, 118, 120, 121, 124, 125, 126, 127, 128, 129, 130, 131, 133, 134, 135, 137, 138, 140, 141, 144, 145, 146, 147, 148, 149, 150, 151, 153, 155, 156, 158, 159, 160, 162, 164, 165, 167, 168, 171, 172, 173, 174, 176, 177, 180, 182, 183, 185, 186, 189, 191, 192, 194, 195, 198, 199, 201, 202, 203, 206, 208, 209, 211, 212, 215, 217, 218, 220, 221, 230, 232, 233, 234, 237, 240, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 404, 405, 406, 407, 408, 409, 410, 413, 415, 417, 419, 421, 423, 425, 427, 429, 431, 432, 434, 435, 437, 438, 443, 444, 453, 454, 455, 456, 468, 469, 470, 471, 472, 473, 474, 475, 476, 477, 478, 479, 480, 493, 494, 495, 496, 497,				

[14] AG551Q series does not support C-V2X feature, so keep all C-V2X related pins (VBAT_CV2X, ANT_CV2X_TRX0, ANT_CV2X_TRX1) unconnected.

	498, 499, 500, 501, 502, 511, 512, 514, 515, 517, 518, 520, 521, 522, 523, 524				
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	7	DI	Turn on/off the module	V_{IH}max = 1.89 V V_{IH}min = 1.17 V V_{IL}max = 0.5 V	Pulled up internally. Due to the diode voltage drop inside the chipset, this pin has a 1.1 V level after the module is powered on.
PON_1	248	DI	Drive HIGH to initiate power on	V_{IH}max = 4.3 V V_{IH}min = 0.78 V V_{IL}max = 0.42 V	PON_1 is a high-voltage tolerant pin up to 4.3 V; therefore, it can be pulled up to VBAT_BB or external 1.8 V.
RESET_N	8	DI	Reset the module	V_{IH}max = 1.89 V V_{IH}min = 0.78 V V_{IL}max = 0.42 V	Pulled up internally to 1.8 V. It is recommended to reserve test points.
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Configurable Function**	**DC Characteristics**	**Comment**
GPIO1	100	DI	WAKEUP_IN	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	This pin is used as WAKEUP_IN by default to control the module entering/exiting the low power mode. If the default function is not used, it can be configured to GPIO.
		DIO	GPIO		General-purpose input/output. Support wake-up interrupt.
GPIO2	101	DIO	GPIO		General-purpose input/output. Support wake-up

					interrupt
GPIO3	102	DIO	GPIO		General-purpose input/output.
GPIO4	104	DO	SLEEP_SYS_IND		Used as SLEEP_SYS_IND by default to indicate the low power mode of the module. If the default function is not used, it can be configured to GPIO.
		DIO	GPIO		General-purpose input/output. Support wake-up interrupt
GPIO5	116	DIO	GPIO		General-purpose input/output. Support wake-up interrupt
GPIO6	243	DO	STATUS	V_{IH}min = 1.17 V V_{IH}max = 1.89 V V_{IL}max = 0.63 V V_{OH}min = 1.44 V V_{OL}max = 0.36 V	Used as STATUS by default to indicate the operating status of the module. If the default function is not used, it can be configured to GPIO.
		DIO	GPIO		General-purpose input/output. It is recommended to be used as an output signal.
GPIO7	246	DIO	GPIO	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	General-purpose input/output
GPIO8	249	DIO			
GPIO9	280	DIO			
GPIO10	283	DIO			General-purpose input/output. Support wake-up interrupt
GPIO11	284	DIO			
GPIO12	289	DIO			
GPIO13	64	DIO			General-purpose

					input/output.
GPIO14	264	DIO			General-purpose input/output. Support wake-up interrupt
GPIO15	267	DIO			
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	84	DI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	Maximum current: 0.1 mA. Typical 5.0 V. Test points must be reserved.
USB_DP	85	AIO	USB 2.0 differential data (+)		Compliant with USB 2.0 standard specifications. Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	87	AIO	USB 2.0 differential data (-)		
USB_SS_TX_P	93	AO	USB 3.1 SuperSpeed transmit (+)		Compliant with USB 3.1 standard specifications. Require differential impedance of 70–100 Ω, and 85 Ω is recommended.
USB_SS_TX_M	91	AO	USB 3.1 SuperSpeed transmit (-)		
USB_SS_RX_P	90	AI	USB 3.1 SuperSpeed receive (+)		
USB_SS_RX_M	88	AI	USB 3.1 SuperSpeed receive (-)		
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	251	PO	(U)SIM1 card power supply	**For 1.8 V (U)SIM:** $V_O$max = 1.95 V $V_O$min = 1.65 V $V_O$nom = 1.8 V **For 3.0 V (U)SIM:**	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM2_VDD	256	PO	(U)SIM2 card power supply		

				$V_O$max = 3.05 V $V_O$min = 2.7 V $V_O$nom = 2.95 V	
USIM1_DATA	254	DIO	(U)SIM1 card data	**For 1.8 V (U)SIM:** V_{IH}min = 1.26 V V_{IL}max = 0.36 V V_{OH}min = 1.44 V V_{OL}max = 0.4 V **For 3.0 V (U)SIM:** V_{IH}min = 2.1 V V_{IL}max = 0.6 V V_{OH}min = 2.4 V V_{OL}max = 0.4 V	
USIM2_DATA	257	DIO	(U)SIM2 card data		
USIM1_RST	250	DO	(U)SIM1 card reset		
USIM2_RST	260	DO	(U)SIM2 card reset		
USIM1_CLK	253	DO	(U)SIM1 card clock		
USIM2_CLK	259	DO	(U)SIM2 card clock		
USIM1_DET	255	DI	(U)SIM1 card hot-plug detect	V_{IH}max = 2.1 V V_{IH}min = 1.26 V V_{IL}max = 0.54 V	1.8 V power domain. If unused, keep them open.
USIM2_DET	258	DI	(U)SIM2 card hot-plug detect		
UART1 Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART1_CTS	71	DO	DTE clear to send signal from DCE (Connects to DTE's CTS)	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep these pins open.
UART1_RTS	74	DI	DTE request to send signal to DCE (Connects to DTE's RTS)		
UART1_TXD	70	DO	UART1 transmit		
UART1_RXD	72	DI	UART1 receive		
Bluetooth UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BT_UART_TXD	59	DO	Bluetooth UART transmit	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
BT_UART_RXD	63	DI	Bluetooth UART receive		

BT_UART_RTS	61	DI	DTE request to send signal to DCE (Connects to DTE's RTS)	V_{OL}max = 0.45 V	
BT_UART_CTS	62	DO	DTE clear to send signal from DCE (Connects to DTE's CTS)		
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	110	DI	Debug UART receive	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. Test points must be reserved for debug UART.
DBG_TXD	107	DO	Debug UART transmit		
Analog Audio Interface (Optional)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC1_P	2	AI	Microphone input channel 1 (+)		Analog audio interface is optional, and is not supported by default. If unused, keep these pins open.
MIC1_N	1	AI	Microphone input channel 1 (-)		
MIC2_P	5	AI	Microphone input channel 2 (+)		
MIC2_N	4	AI	Microphone input channel 2 (-)		
MICBIAS	3	PO	Bias voltage output for microphone	Vmax = 1.55 V Vmin = 1.5 V Vnom = 1.525 V	
SPK1_P	268	AO	Headphone analog output 1 (+)		
SPK1_N	266	AO	Headphone analog output 1 (-)		
SPK2_P	269	AO	Headphone analog output 2 (+)		
SPK2_N	270	AO	Headphone analog output 2 (-)		
AGND	6	-	Analog ground		Connect it to GND or keep it open if

					unused.
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C1_SCL	79	OD	I2C serial clock	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	External pull-up resistors are required. 1.8 V power domain. If unused, keep them open.
I2C1_SDA	80	OD	I2C serial data		
I2S Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2S_MCLK	81	DO	Clock output for codec	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	12.288 MHz clock output
I2S_WS	265	DIO	I2S word select		1.8 V power domain. Serve as output signals in master mode. Serve as input signals in slave mode.
I2S_SCK	262	DIO	I2S clock		
I2S_DIN	263	DI	I2S data in		1.8 V power domain.
I2S_DOUT	261	DO	I2S data out		
CDC_RST_N	77	DO	External codec reset		
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	73	DIO	PCM data frame sync	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. Serve as output signals in master mode. Serve as input signals in slave mode.
PCM_CLK	75	DIO	PCM clock		
PCM_IN	76	DI	PCM data input		1.8 V power domain.

PCM_OUT	78	DO	PCM data output		
PCIe Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE_REFCLK_P	40	AIO	PCIe reference clock (+)		Serve as output signals in RC mode. Serve as input signals in EP mode. The differential impedance should be the same as that for PCIe TX/RX.
PCIE_REFCLK_M	38	AIO	PCIe reference clock (-)		
PCIE_TX0_M	44	AO	PCIe transmit 0 (-)		Require differential impedance of 70–100 Ω, and 85 Ω is recommended.
PCIE_TX0_P	46	AO	PCIe transmit 0 (+)		
PCIE_TX1_M	41	AO	PCIe transmit 1 (-)		
PCIE_TX1_P	43	AO	PCIe transmit 1 (+)		
PCIE_RX0_M	32	AI	PCIe receive 0 (-)		
PCIE_RX0_P	34	AI	PCIe receive 0 (+)		
PCIE_RX1_M	35	AI	PCIe receive 1 (-)		
PCIE_RX1_P	37	AI	PCIe receive 1 (+)		
PCIE_CLKREQ_N	36	DIO	PCIe clock request	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	Serve as input signals in RC mode. Serve as output signals in EP mode.
PCIE_WAKE_N	30	DIO	PCIe wake up		
PCIE_RST_N	39	DIO	PCIe reset		Serve as an output signal in RC mode. Serve as an input signal in EP mode.
WLAN and Bluetooth Application Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_PWR_EN1	222	DO	WLAN power supply enable control 1	V_{IH}min = 1.17 V V_{IH}max = 1.89 V V_{IL}max = 0.63 V V_{OH}min = 1.44 V	Used for Quectel AF50T 3.85 V power control.
WLAN_PWR_	225	DO	WLAN power		Reserved by default.

EN2			supply enable control 2	V_{OL}max = 0.36 V	Keep it open.
BT_EN	66	DO	Bluetooth enable control		
HOST_SW_CTRL	184	DI	Switch control		Output signal from Quectel AF50T.
WLAN_SLP_CLK	231	DO	WLAN 32 kHz sleep clock		
WLAN_EN	228	DO	WLAN function enable control		
COEX_UART_RXD	67	DI	LTE & WLAN & Bluetooth coexistence UART receive		
COEX_UART_TXD	69	DO	LTE & WLAN & Bluetooth coexistence UART transmit		
WL_PA_MUTE	166	DO	Module transceiver to disable WLAN PA	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	
LAA_AS_EN	163	DO	Allow LAA to control WLAN FEM during WLAN sleep mode		
LAA_RX	204	DO	Module sets 5 GHz WLAN xLNA to high gains or high isolation when both chains (LAA/n79 and 5 GHz WLAN) are enabled simultaneously		
LAA_TX_EN*	139	DO	The module transceiver notifies WLAN that n79/LAA transmission is ongoing and the 5 GHz WLAN should be set to isolation mode	V_{IH}min = 1.17 V V_{IH}max = 2.1 V V_{IL}max = 0.63 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	

WL_TX_EN*	142	DI	5 GHz WLAN notifies the module that WLAN transmission is ongoing and requests the module to set n79/LAA LNA to isolation mode		
RGMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RGMII_MD_IO	10	DIO	RGMII management data	**1.8 V power domain:** V_{IH}min = 1.17 V V_{IL}max = 0.63 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V **2.5 V power domain:** V_{IH}min = 1.7 V V_{IL}max = 0.7 V V_{OH}min = 2.0 V V_{OL}max = 0.4 V	Add a pull-up resistor to this pin, and place the resistor close to the external PHY end.
RGMII_MD_CLK	11	DO	RGMII management clock		Do not add any pull-up resistor to this pin, otherwise it may cause higher power consumption during low power mode.
RGMII_CK_RX	19	DI	RGMII receive clock		The power domain depends on RGMII_PWR_IN. Typ.1.8/2.5 V, and 1.8 V is recommended. The single-ended impedance requires 50 Ω.
RGMII_CTL_RX	15	DI	RGMII receive control		
RGMII_RX_0	13	DI	RGMII receive data bit 0		
RGMII_RX_1	14	DI	RGMII receive data bit 1		
RGMII_RX_2	16	DI	RGMII receive data bit 2		
RGMII_RX_3	17	DI	RGMII receive data bit 3		
RGMII_CK_TX	24	DO	RGMII transmit clock		
RGMII_CTL_TX	21	DO	RGMII transmit control		
RGMII_TX_0	20	DO	RGMII transmit data bit 0		

RGMII_TX_1	22	DO	RGMII transmit data bit 1		
RGMII_TX_2	23	DO	RGMII transmit data bit 2		
RGMII_TX_3	25	DO	RGMII transmit data bit 3		
RGMII_PWR_EN	27	DO	Enable an external power supply to power RGMII_ PWR_IN	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain.
RGMII_INT	29	DI	RGMII interrupt input		
RGMII_RST_N	31	DO	Reset output for external PHY		
RGMII_PWR_IN	28	PI	RGMII interface power supply input	**1.8 V power domain:** Vmax = 1.94 V Vmin = 1.7 V Vnom = 1.8 V **2.5 V power domain:** Vmax = 2.69 V Vmin = 2.31 V Vnom = 2.5 V	An external power supply is required to power this pin. Max. 100 mA in operating current. If RGMII interface is not used, connect this pin to VDD_EXT.
SDIO Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDIO_VDD	60	PI	SDIO power supply input	**For 1.8 V signaling:** Vmax = 1.95 V Vmin = 1.65 V Vnom = 1.8 V **For 3.0 V signaling:** Vmax = 3.05 V Vmin = 2.7 V Vnom = 2.95 V	**SD card application:** Connect to external 1.8/2.95 V power supply. **eMMC application:** Connect to external 1.8 V, and require max. current 10 mA. If SDIO interface is not used, connect this pin to VDD_EXT.
SDC1_DATA_0	49	DIO	SDIO data bit 0	**For 1.8 V**	The power domain

SDC1_DATA_1	50	DIO	SDIO data bit 1	**signaling:** V_{IH}min = 1.27 V V_{IL}max = 0.58 V V_{OH}min = 1.4 V V_{OL}max = 0.45 V **For 3.0 V signaling:** V_{IH}min = 1.85 V V_{IL}max = 0.7 V V_{OH}min = 2.25 V V_{OL}max = 0.37 V	depends on SDIO_VDD.
SDC1_DATA_2	51	DIO	SDIO data bit 2		
SDC1_DATA_3	52	DIO	SDIO data bit 3		
SDC1_CMD	48	DIO	SDIO command		
SDC1_CLK	47	DO	SDIO clock		
SDC1_DATA_4	53	DIO	SDIO data bit 4	V_{IH}min = 1.27 V V_{IH}max = 2.0 V V_{IL}max = 0.58 V V_{OH}min = 1.4 V V_{OL}max = 0.45 V	1.8 V power domain.
SDC1_DATA_5	55	DIO	**eMMC application:** SDIO data bit 5 **SD card application:** SD card detection		
SDC1_DATA_6	56	DIO	SDIO data bit 6		
SDC1_DATA_7	58	DIO	SDIO data bit 7		
EMMC_RST_N*	54	DO	eMMC reset	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain.
EMMC_PWR_EN	45	DO	eMMC power supply enable control		
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	414	AIO	Main antenna interface		50 Ω impedance
ANT_DRX	416	AIO	Diversity antenna interface		
ANT_MIMO3	418	AIO	MIMO3 antenna interface		
ANT_MIMO4	420	AI	MIMO4 antenna interface		
ANT_DSDA_MAIN [15]	422	AIO	DSDA main antenna interface		

[15] Only AG553Q-EU supports DSDA; AG550Q and AG551Q series support DSSS.

ANT_DSDA_DIV [15]	424	AI	DSDA diversity antenna interface		
ANT_GNSS [16]	426	AI	GNSS antenna		
ANT_CV2X_TRX1 [14]	433	AIO	C-V2X TRX1 antenna interface		
ANT_CV2X_TRX0 [14]	436	AIO	C-V2X TRX0 antenna interface		
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI1_CLK	216	DO	SPI1 clock	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V V_{OL}max = 0.45 V	Supports SPI master mode only.
SPI1_CS	213	DO	SPI1 chip select		
SPI1_MISO	219	DI	SPI1 master-in slave-out		
SPI1_MOSI	210	DO	SPI1 master-out slave-in		
SPI2_CLK	103	DO	SPI2 clock		
SPI2_CS	105	DO	SPI2 chip select		
SPI2_MISO	106	DI	SPI2 master-in slave-out		
SPI2_MOSI	108	DO	SPI2 master-out slave-in		
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	247	AI	General-purpose ADC interface	Voltage range: 0 V to 1.875 V	
ADC1	245	AI	General-purpose ADC interface		
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	83	DI	Force the module into emergency download mode	V_{IH}min = 1.26 V V_{IH}max = 2.1 V V_{IL}max = 0.54 V V_{OH}min = 1.35 V	1.8 V power domain. Active high. It is recommended to reserve test points.

[16] GNSS is an optional feature of AG55xQ family. When it is not supported, keep ANT_GNSS unconnected.

DR_SYNC	95	DO	Dead reckoning sync	V_{OL}max = 0.45 V	
IMU_PWR_EN	181	DO	IMU power enable control		1.8 V power domain. If unused, keep them open.
IMU_INT1	169	DI	IMU interrupt 1		
IMU_INT2	187	DI	IMU interrupt 2		
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	9, 57, 65, 82, 89, 94, 96, 97, 99, 109, 111, 112, 113, 114, 119, 122, 123, 132, 136, 143, 152, 154, 157, 161, 170, 175, 178, 179, 188, 190, 193, 196, 197, 200, 205, 207, 214, 223, 224, 226, 227, 229, 235, 236, 238, 239, 241, 242, 244, 252, 271, 272, 273, 278, 279, 281, 282, 285, 286, 287, 288, 290, 291, 292, 293, 294, 295, 296, 297, 298, 299, 300, 301, 302, 303, 304, 305, 306, 403, 411, 412, 428, 430, 457, 458, 459, 460, 461, 462, 463, 464, 465, 466, 467, 481, 482, 483, 484, 485, 486, 487, 488, 489, 490, 491, 492, 503, 504, 505, 506, 513, 516, 519				Keep these pins open.

NOTE

1. Unless otherwise specified, keep all RESERVED and unused pins unconnected.
2. GND pins should be connected to ground in the design.

2.5.2. Pin Multiplexing and BLSP Assignment

See ***document [1]*** for details about pin multiplexing and BLSP assignment of the module.

2.6. EVB Kit

To facilitate application design with the module, Quectel supplies the evaluation board (V2X&5G EVB), a USB data cable, headsets, antennas and other peripherals to control or test the module. For more details, see ***document [2]***.

3 Operating Characteristics

3.1. Operating Modes

The table below briefly summarizes the various operating modes of the module.

Table 8: Overview of Operating Modes

Mode	Details	
Functionality Operation	Idle	The module remains registered on the network, and is ready to send and receive data. In this mode, the software is active.
	Voice/Data	The module is connected to network. Its power consumption varies with the network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** or device management related API function can set the module into a minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** or device management related API function can set the module into airplane mode where the RF function is invalid.	
Sleep Mode	The module remains the ability to receive paging message, SMS, voice call and TCP/UDP data from the network normally. In this mode, the current consumption of the module is reduced to a very low level.	
Power Down Mode	The module's power supply is cut off by its power management unit. In this mode, the software is inactive, the serial interfaces are inaccessible, while the operating voltage (connected to VBAT_RF, VBAT_BB and VBAT_CV2X) remains applied.	

NOTE

See ***document [3]*** and ***document [4]*** for details of device management API functions, and ***document [5]*** for details of **AT+CFUN**.

3.2. Power Saving

3.2.1. Lowe Power Mode (LPM)

The module is able to reduce its power consumption to a minimum value during the sleep mode. This chapter mainly introduces methods to enter or exit LPM. The diagram below illustrates the current consumption of the module during LPM. See ***document [6]*** for details about LPM of the module.

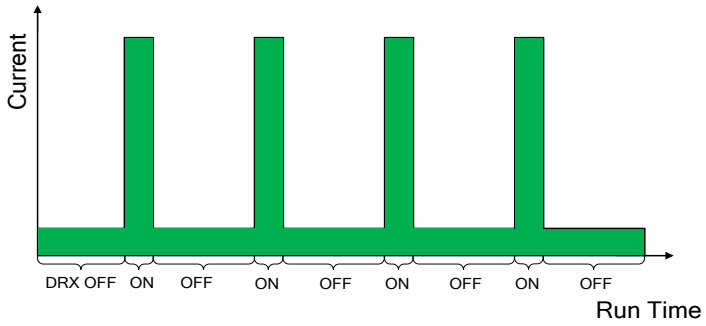


Figure 3: LPM Power Consumption Diagram

NOTE

The DRX cycle values are broadcasted by the wireless network.

3.2.1.1. USB Application Without USB Suspend Function

If the host does not support USB suspend function, USB_VBUS should be connected with an external control circuit to let the module enter sleep mode.

- Use LPM related API functions to enable the sleep mode.
- Ensure the level of pins that configured as wake-up interrupts in ***document [1]*** are under non-wakeup status.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

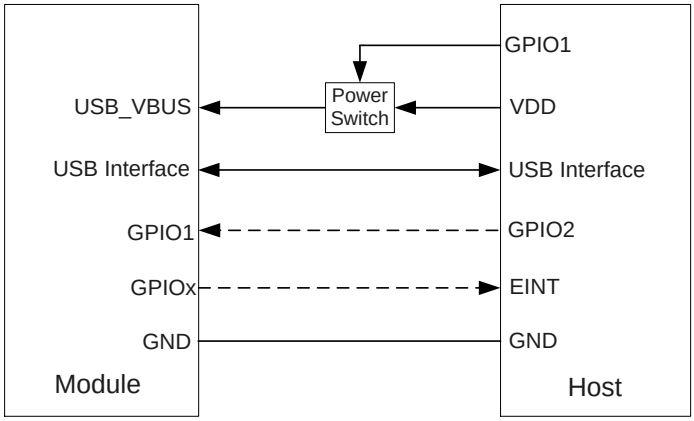


Figure 4: Sleep Mode Application Without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

1. Pay attention to the voltage-level matching of the circuit in dotted line, when the host interface is not 1.8 V power domain.
2. GPIO1 of the module is used as WAKEUP_IN (input signal) by default, through which the MCU controls the module to enter/exit LPM.
3. GPIOx can be any GPIO of the module. When defined into WAKEUP_OUT (output signal), it controls user application to enter/exit LPM.

3.2.1.2. LPM and Wakeup Timing

The following figure shows the LPM and wakeup timing of the module.

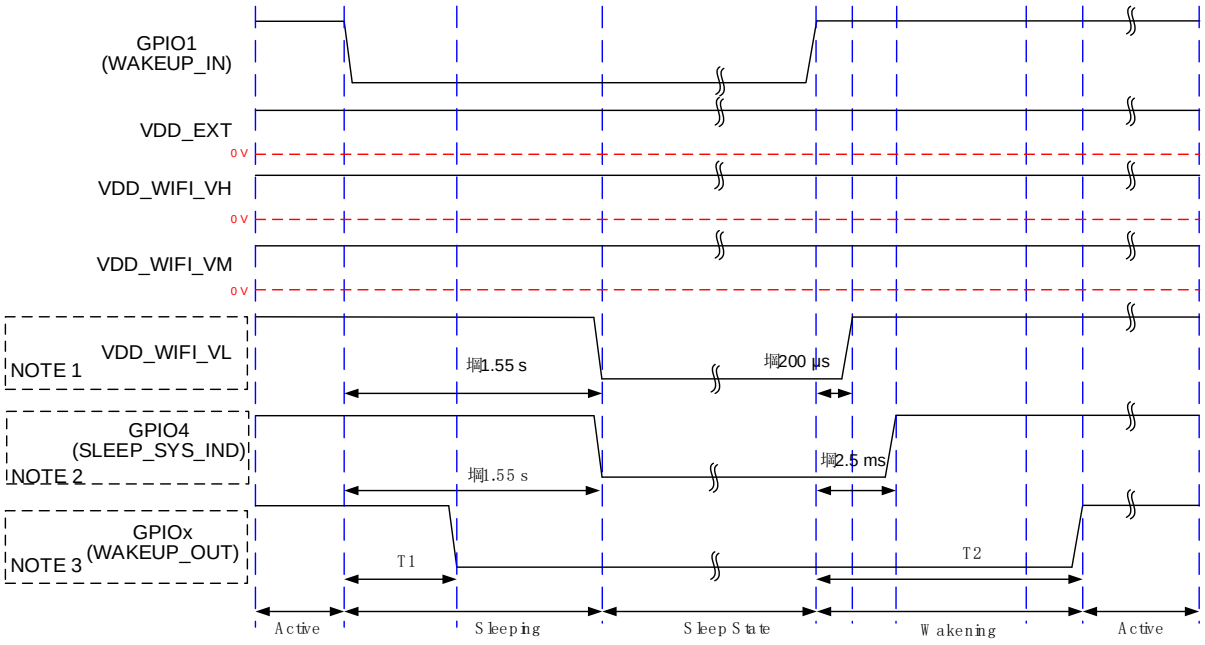


Figure 5: LPM and Wakeup Timing

NOTE

1. If the module enters LPM when **AT+CFUN=0**, VDD_WIFI_VL will be powered off, and it will be powered on for a short period of time periodically during the network registering process.
2. The time between the falling edges of WAKEUP_IN and SLEEP_SYS_IND depends on the real application scenario. If the module needs to process any task during the period, the time will be longer.
3. You can select any GPIO of the module to serve as the WAKEUP_OUT function. T1 and T2 depends on the application.

3.2.2. Airplane Mode

When the module enters airplane mode, the RF function does not work, all AT commands and API functions correlative with RF function will be inaccessible.

AT command:

The mode can be set via **AT+CFUN=<fun>**. The parameter **<fun>** of **AT+CFUN** indicates the module's functionality levels, as shown below.

- **AT+CFUN=0:** Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

API functions:

The mode can be set via device management related API functions. For more information about device management API functions, see ***document [3]*** and ***document [4]***.

NOTE

The execution of **AT+CFUN** or related API functions will not affect GNSS function.

3.3. Power Supply

3.3.1. Power Supply Pins

The module provides 16 VBAT pins for connection with external power supplies. VBAT pins are separately used to supply power for three parts of the module.

- 8 VBAT_RF pins for module's RF part, distributed on two sides of the module. Each side has 4 pins.
- 4 VBAT_BB pins for module's baseband part.
- 4 VBAT_CV2X pins for module's C-V2X part.

The following table shows the details of VBAT pins and ground pins.

Table 9: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	445, 446, 447, 448, 507, 508, 509, 510	Power supply for the module's RF part	3.3	3.8	4.3	V
VBAT_BB	449, 450, 451, 452	Power supply for the module's baseband part	3.3	3.8	4.3	V
VBAT_CV2X [17]	439, 440, 441, 442	Power supply for the module's C-V2X part	4.75	5.0	5.25	V
GND	12, 18, 26, 33, 42, 86, 92, 98, 115, 117, 118, 120, 121, 124, 125, 126, 127, 128, 129, 130, 131, 133, 134, 135, 137, 138, 140, 141, 144, 145, 146, 147, 148, 149, 150, 151, 153, 155, 156, 158, 159, 160, 162, 164, 165, 167, 168, 171, 172, 173, 174, 176, 177, 180, 182, 183, 185, 186, 189, 191, 192, 194, 195, 198, 199, 201, 202, 203, 206, 208, 209, 211, 212, 215, 217, 218, 220, 221, 230, 232, 233, 234, 237, 240, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360,				

[17] AG551Q series does not support C-V2X, so keep VBAT_CV2X pins unconnected.

	361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 404, 405, 406, 407, 408, 409, 410, 413, 415, 417, 419, 421, 423, 425, 427, 429, 431, 432, 434, 435, 437, 438, 443, 444, 453, 454, 455, 456, 468, 469, 470, 471, 472, 473, 474, 475, 476, 477, 478, 479, 480, 493, 494, 495, 496, 497, 498, 499, 500, 501, 502, 511, 512, 514, 515, 517, 518, 520, 521, 522, 523, 524

3.3.2. Reference Design for Power Supply

The performance of the module largely depends on the power source. If the voltage drop between the input and output is not too high, it is recommended to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +12/+24 V input power source when applying the module to 5G + C-V2X + DSDA solution. The designed outputs are 5.0 V and 3.8 V, and the maximum rated current is 5 A.

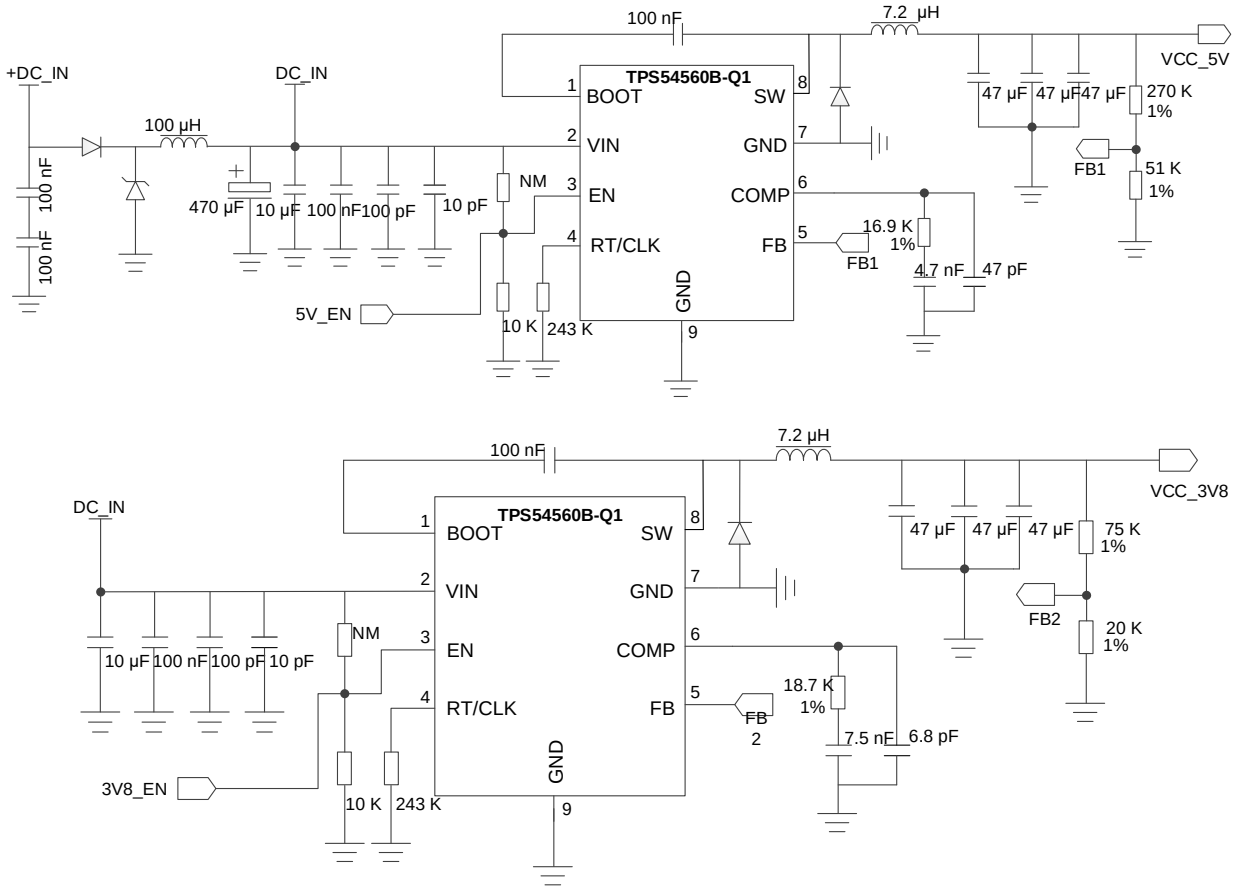


Figure 6: Reference Design of Power Supply (5G + C-V2X + DSDA Applications)

The following figure shows a reference design for +12/+24 V input power source when applying the module to 5G + C-V2X solution. The designed outputs are 5.0 V (with maximum rated current of 5 A) and 3.8 V (with maximum rated current of 3 A).

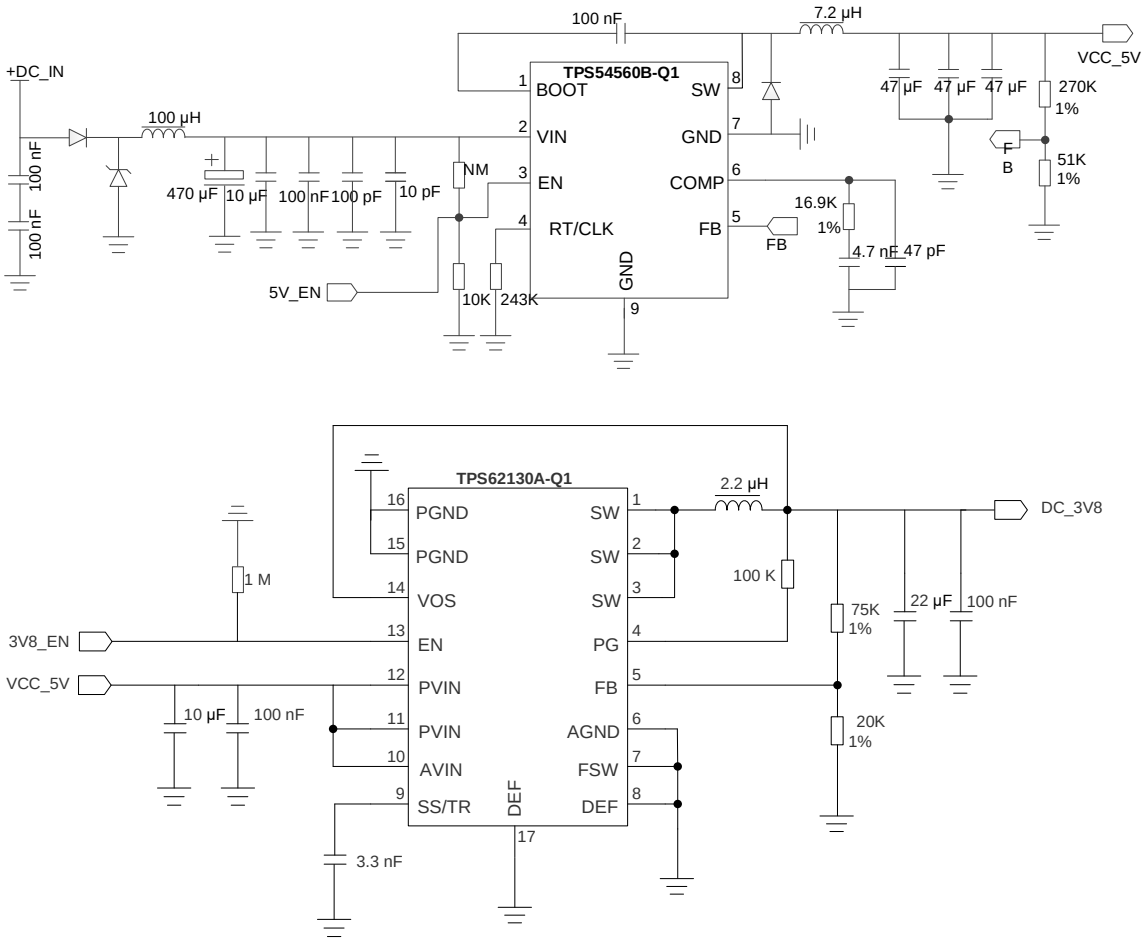


Figure 7: Reference Design of Power Supply (5G + C-V2X Applications)

NOTE

To avoid damaging the data of internal flash, do not switch off the power supply when the module works normally. The power supply can be cut off only after the module is shut down with PWRKEY or Linux power off commands.

3.3.3. Voltage Stability Requirements

The power supply range of VBAT_BB and VBAT_RF is from 3.3–4.3 V. The power supply range of VBAT_CV2X is 4.75–5.25 V. Ensure that the input voltage of VBAT_BB and VBAT_RF never drops below 3.3 V, and the input voltage of VBAT_CV2X never drops below 4.75 V. The following figure shows the voltage drop during burst transmission in GSM and 5G (NSA) networks. The voltage drop will be less in 3G, 4G and 5G (SA) networks.

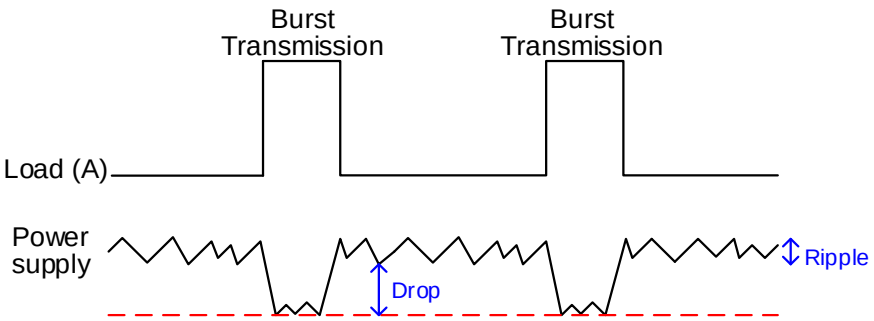


Figure 8: Power Supply Limits During Burst Transmission

To decrease voltage-drop, use bypass capacitors of at least 100 µF with low ESR for VBAT_RF and VBAT_CV2X, at least 220 µF for VBAT_BB, and reserve multi-layer ceramic chip capacitor (MLCC) arrays due to their low ESR. It is recommended to use at least three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT pins. While connecting the module to an external 3.8 V power supply, route VBAT_BB and VBAT_RF traces in star structure. The width of VBAT_BB trace should be not less than 1.5 mm. The width of VBAT_RF trace should be not less than 3 mm for the main power trace and 2 mm for the branch power trace. The width of VBAT_CV2X trace should be not less than 1.6 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to get a stable power source, it is suggested to use TVS diodes to prevent EOS, and place them as close to the VBAT pins as possible. The following figure shows the recommended power supply design.

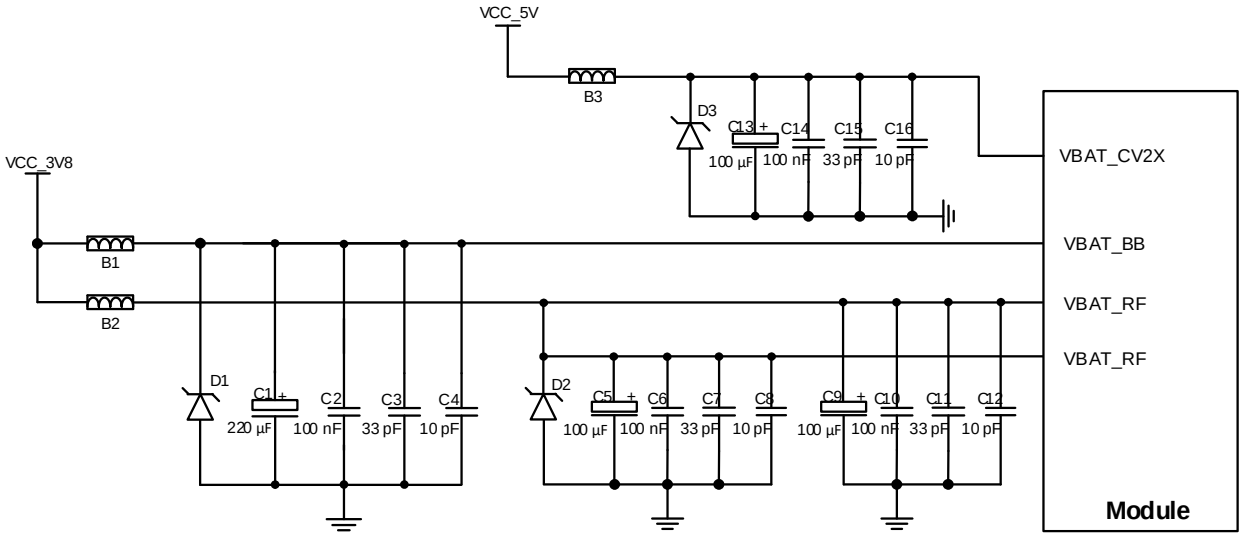


Figure 9: Power Supply Design

3.4. Turn On

3.4.1. Turn On with PWRKEY

The following table shows the pin definition of PWRKEY.

Table 10: PWRKEY Pin Description

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	7	DI	Turn on/off the module	The voltage level is about 1.1 V because of the diode drop in the baseband chipset. Pull-up internally.

When the module is in power down mode, it can be turned on by driving the PWRKEY pin low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

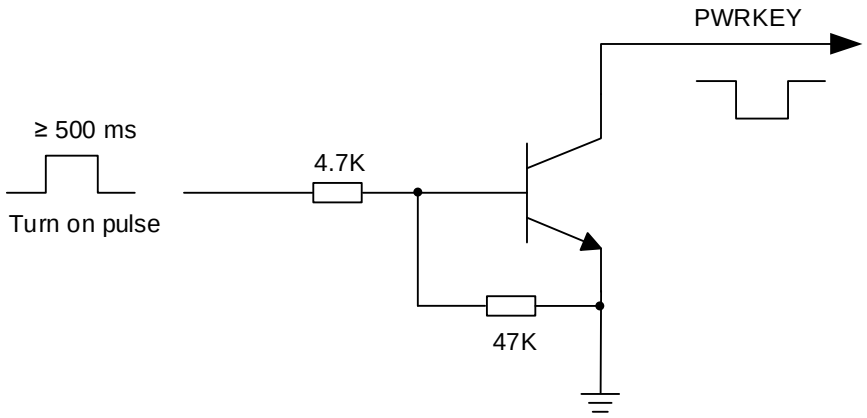


Figure 10: Turn On the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the button, electrostatic strike may generate from the finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

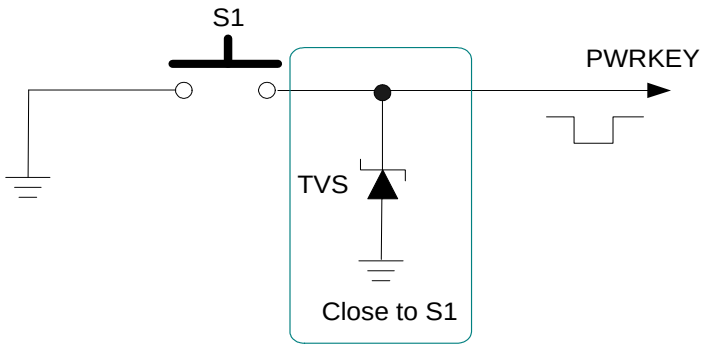


Figure 11: Turn On the Module Using a Button

The power-up timing is illustrated in the following figure.

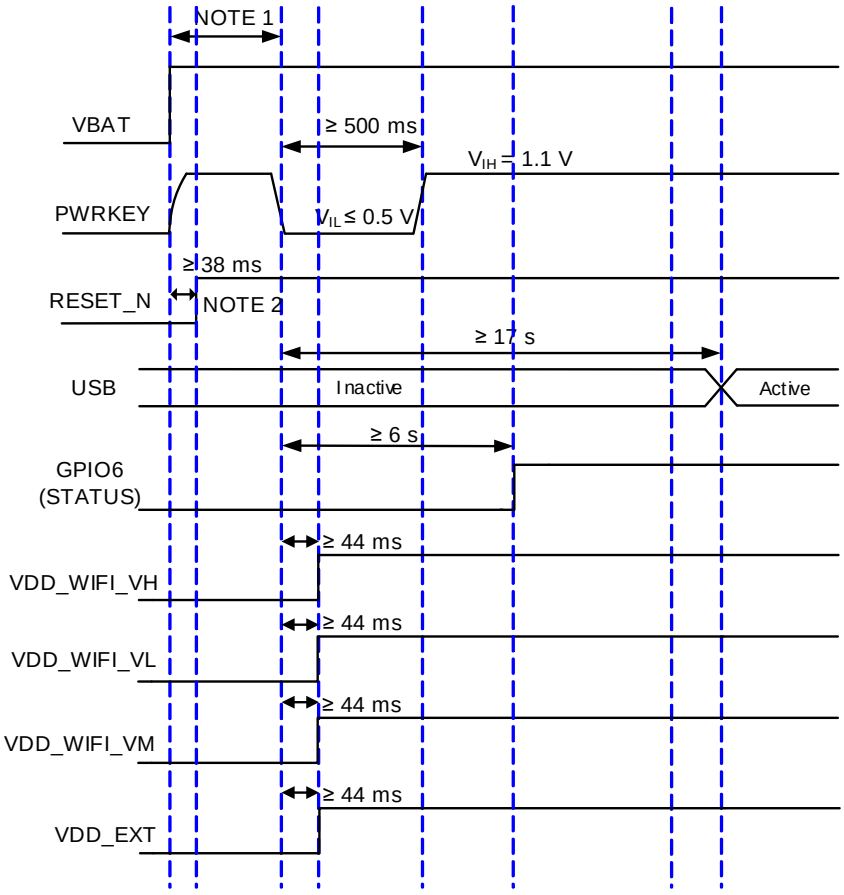


Figure 12: Power-up Timing

NOTE

1. Ensure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin is not less than 30 ms.
2. The RESET_N will be pulled high automatically when the voltage of VBAT is stable for at least 38 ms, therefore MCU does not need to control RESET_N in the power-up timing.
3. It is recommended to use an external OD/OC circuit to control the PWRKEY pin.
4. Do not connect PWRKEY or RESET_N to GND. Long press (≥ 16 s) of PWRKEY or RESET_N will trigger mandatory hardware reset.

3.4.2. Turn on with PON_1

The following table shows the pin definition of PON_1.

Table 11: PON_1 Pin Description

Pin Name	Pin No.	I/O	Description	Comment
PON_1	248	DI	Drive HIGH to initiate power on	PON_1 is a high voltage tolerant pin up to 4.3 V, therefore it can be pulled up to VBAT_BB, or an external 1.8 V power supply.

Connecting PON_1 to VBAT_BB or 1.8 V power supply through a serial resistor (10–100 kΩ) will enable the module to turn on automatically.

PON_1 is weakly pulled down internally. When it is unused, it is recommended to connect it to GND with an external pull-down resistor (10–100 kΩ).

3.5. Turn Off

Either of the following methods can be used to turn off the module normally:

- Turn off the module using the PWRKEY pin.
- Turn off the module using Linux commands.

3.5.1. Turn Off with PWRKEY

Driving PWRKEY low for at least 2 s and then releasing it will enable the module to execute power-off procedure. The power-down scenario is illustrated in the following figure.

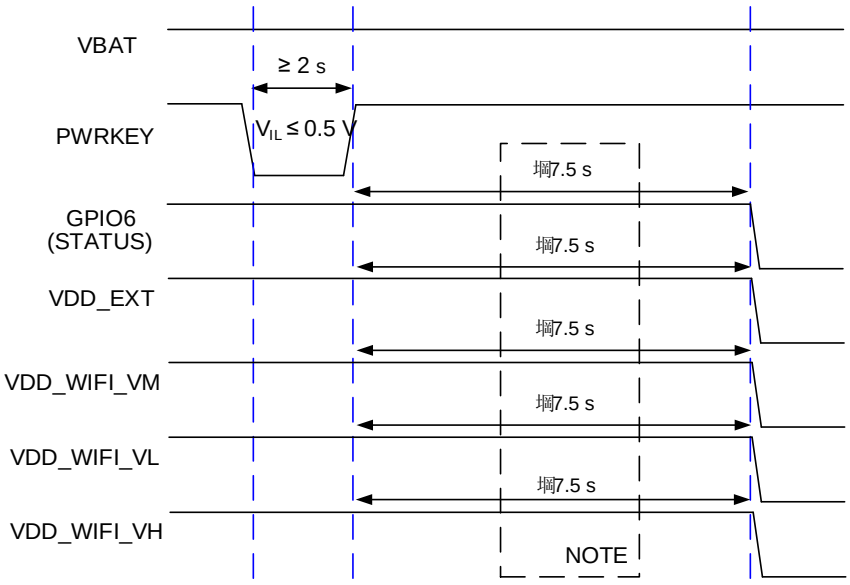


Figure 13: Power-down Timing

NOTE

The releasing time of GPIO6 and the power-down time of the power supply (e.g. VDD_EXT) depend on the actual running business, and if the module has tasks to deal with during shutdown, the time may be longer.

3.5.2. Turn off with Linux Commands

It is also a safe way to use Linux commands, such as **shutdown** and **poweroff**, to turn off the module, which is similar to turning off the module via PWRKEY pin.

NOTE

1. To avoid damaging the data of internal flash, do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or Linux commands, the power supply can be cut off.
2. When you turn off module with Linux commands, keep PWRKEY at high level after the execution of Linux command. Otherwise, the module will be turned on again after successful turn-off.

3.6. Reset

The module can be reset by driving RESET_N low for 250–550 ms. As the RESET_N pin is sensitive to interference, the routing trace is recommended to be as short as possible and totally ground surrounded.

Table 12: RESET_N Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	8	DI	Reset the module	Internally pulled up to 1.8 V. Active low.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

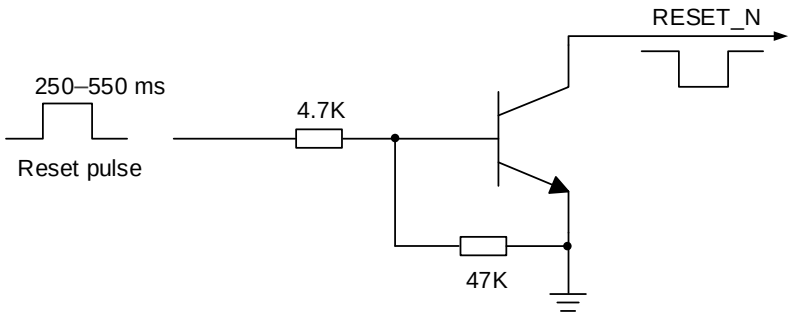


Figure 14: Reference Circuit of RESET_N by Using Driving Circuit

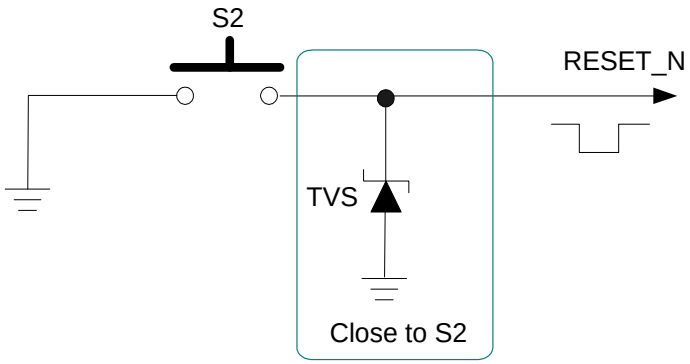


Figure 15: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the following figure.

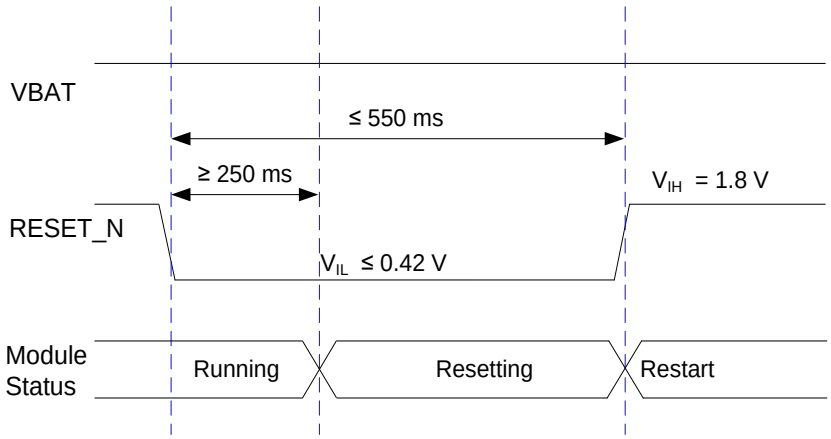


Figure 16: Reset Timing

NOTE

1. Ensure that there is no capacitance larger than 10 nF on PWRKEY and RESET_N pins.
2. RESET_N should only be used when turning off the module by Linux commands and PWRKEY pin all failed.

4 Application Interfaces

4.1. USB Interface

The module provides one USB interface. The USB interface complies with the USB 3.1 Gen 2 and USB 2.0 specifications, and supports SuperSpeed (10 Gbps theoretically) on USB 3.1, high-speed (480 Mbps theoretically) and full-speed (12 Mbps theoretically) on USB 2.0.

Both USB 2.0 interface and USB 3.1 interface can be used for AT command communication, C-V2X and cellular data transmission, GNSS NMEA sentences output and software debugging.

Only USB 2.0 can be used for firmware upgrade. The USB 3.1 interface is used for data communication with an external AP by default.

USB 2.0 and USB 3.1 share the same hardware controller, so USB 2.0 and USB 3.1 cannot be used simultaneously. When USB 2.0 and USB 3.1 are connected to the same host, USB 3.1 takes effect by default.

The following table shows the pin definition of USB interface.

Table 13: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	84	DI	USB connection detect	Maximum current: 0.1 mA Typical 5.0 V. Test points must be reserved.
USB_DP	85	AIO	USB 2.0 differential data (+)	Compliant with USB 2.0 standard specifications. Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	87	AIO	USB 2.0 differential data (-)	
USB_SS_TX_P	93	AO	USB 3.1 SuperSpeed transmit (+)	Compliant with USB 3.1

USB_SS_TX_M	91	AO	USB 3.1 SuperSpeed transmit (-)	standard specifications. Require differential impedance range of 70–100 Ω and 85 Ω is recommended.
USB_SS_RX_P	90	AI	USB 3.1 SuperSpeed receive (+)	
USB_SS_RX_M	88	AI	USB 3.1 SuperSpeed receive (-)	

It is recommended to reserve USB 2.0 for firmware upgrade in application designs, and test points must be reserved for debugging purpose. The following figure shows a reference design of USB 2.0 interface.

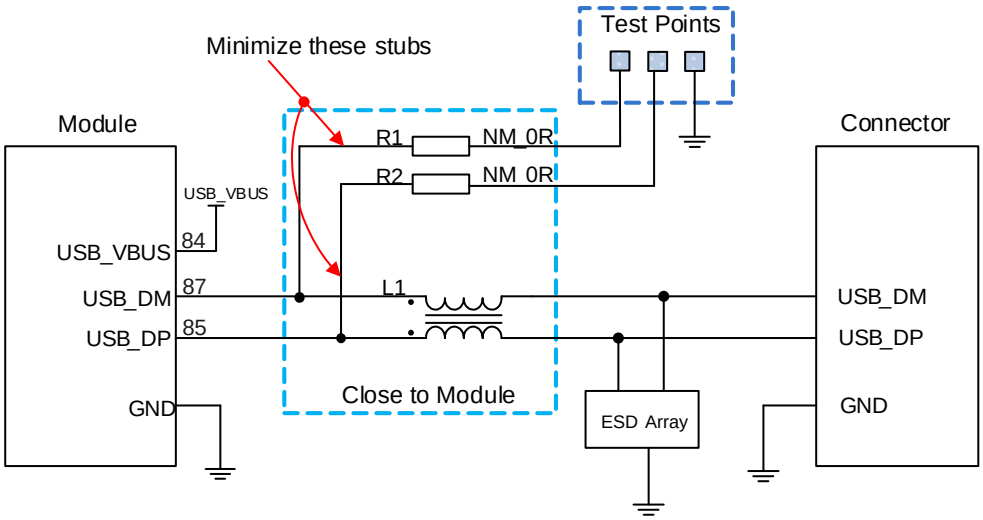


Figure 17: Reference Design of USB 2.0 Application

In USB 2.0 applications, A common mode choke L1 is recommended to be added in series between the module and the connector to suppress EMI spurious transmission. The 0 Ω resistors (R1 and R2, not mounted by default) should be added in series between the module and the test points to facilitate debugging, and the resistors are not mounted by default. To ensure signal integrity of USB data traces, place R1, R2 and L1 close to the module, and place these resistors close to each other. The extra stubs of trace must be as short as possible.

The following figure shows a reference design of USB 3.1 interface.

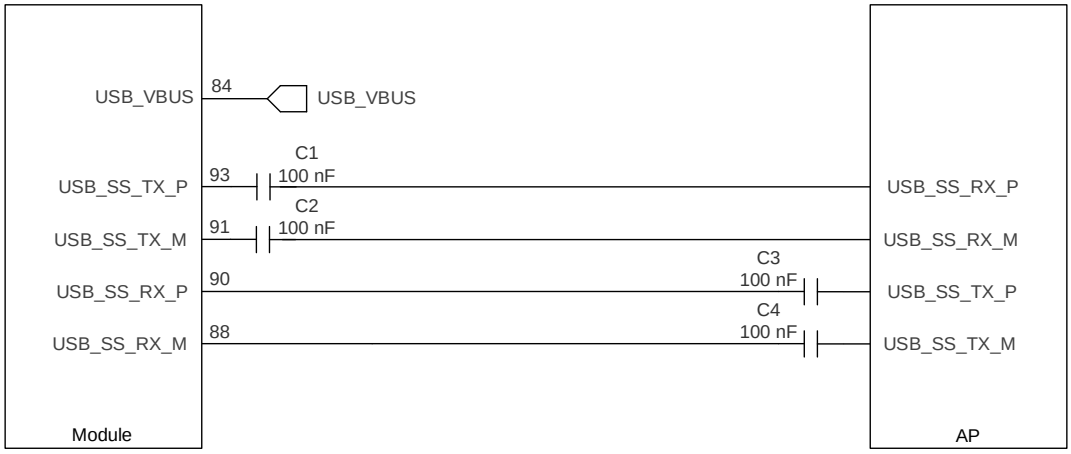


Figure 18: Reference Circuit of USB 3.1 Application

In USB 3.1 applications, place C1 and C2 near the module, and place C3 and C4 near the AP. The extra stubs of trace must be as short as possible.

To meet USB 2.0 and USB 3.1 specifications, the following principles of USB interface should be complied with.

- It is important to route the USB 2.0 and 3.1 signal traces as differential pairs with total grounding. The recommended differential impedance is 90 Ω for USB 2.0 and 85 Ω for USB 3.1.
- The intra-lane length match should be less than 2.0 mm for USB 2.0 and 0.7 mm for USB 3.1.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below. Route the RF signals operating at a 2.4 GHz frequency with the highest isolation possible from USB_SS_TX/RX traces.
- Keep isolation between the USB_SS_TX pair, USB_SS_RX pair, and USB_DP/USB_DM to avoid crosstalk.
- If a USB connector is used, keep the ESD protection components as close to the USB connector as possible. Junction capacitance of the ESD protection device might cause influences on USB data lines, so pay attention to the selection of the device. Typically, the parasitic capacitance should be less than 2.0 pF for USB 2.0 and less than 0.3 pF for USB 3.1.
- USB_SS_TX AC coupling capacitors can be anywhere along the line, but it is better to place them close to source or the ESD/connector side to keep good signal integrity of main route on PCB.

For more details about the USB 2.0 and USB 3.1 specifications, visit http://www.usb.org/home.

NOTE

1. The module supports master mode, but works in slave mode by default.
2. The high-speed PHY and super-speed PHY share the same USB 3.1 Gen 2 controller inside baseband chipset, so USB 2.0 and USB 3.1 cannot be used simultaneously.

3. As for the AC coupling capacitors C1–C4, the recommended value is 220 nF for USB 3.1 Gen 2 and 100 nF for USB 3.1 Gen 1.

4.2. (U)SIM Interfaces

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported.

The module supports dual (U)SIM cards, and (U)SIM1 is the primary interface.

Table 14: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	251	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_CLK	253	DO	(U)SIM1 card clock	
USIM1_RST	250	DO	(U)SIM1 card reset	
USIM1_DATA	254	DIO	(U)SIM1 card data	
USIM2_VDD	256	PO	(U)SIM2 card power supply	
USIM2_CLK	259	DO	(U)SIM2 card clock	
USIM2_RST	260	DO	(U)SIM2 card reset	
USIM2_DATA	257	DIO	(U)SIM2 card data	
USIM1_DET	255	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep them open.
USIM2_DET	258	DI	(U)SIM2 card hot-plug detect	

The module supports (U)SIM card hot-plug via USIM_DET pins, and either low-level or high-level detection is supported. The function is disabled by default, and can be enabled by related software command.

The following figure shows a reference design of (U)SIM interface with an 8-pin (U)SIM card connector.

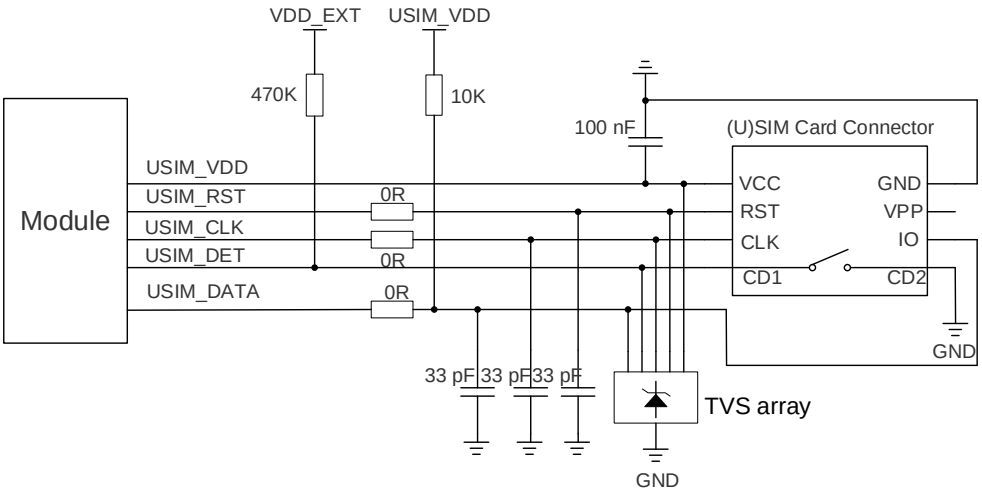


Figure 19: Reference Design of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_DET unconnected. A reference design of (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

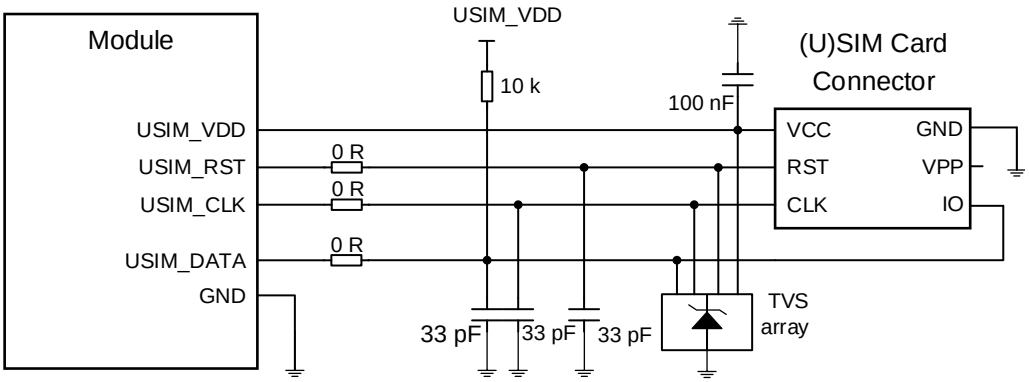


Figure 20: Reference Design of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in the (U)SIM circuit design:

- Keep the placement of (U)SIM card connector as close to the module as possible. Keep the trace length short, at most 200 mm.
- Keep (U)SIM card signals away from RF and power supply traces.
- Assure the trace between the ground of the module and that of the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD not less than 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer good ESD protection, it is recommended to add a TVS array with parasitic capacitance not

exceeding 10 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card connector to suppress EMI spurious transmission and enhance ESD protection. The 33 pF capacitors are used for filtering interference of EGSM900. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.

- The USIM_DATA must be connected to USIM_VDD with a 10 kΩ pull-up resistor. The pull-up resistor can improve anti-jamming capability when long layout trace and sensitive occasions are applied, and should be placed close to the (U)SIM card connector.

4.3. UART Interfaces

The module provides three UART interfaces: UART1, Bluetooth UART and debug UART. The following are the features of these UART interfaces. The module serves as DCE (Data Communication Equipment), which connected in the traditional DCE-DTE (Data Terminal Equipment) mode.

Table 15: Basic Information of UART Interfaces

UART Type	Supported Baud Rate (bps)	Default Baud Rate (bps)	Description
UART1	4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600	115200	● Data transmission ● Support RTS and CTS hardware flow control
Bluetooth UART [18]		115200	● Data transmission ● Support RTS and CTS hardware flow control
Debug UART [19]	115200	115200	Used for Linux console and log output

The following tables show the pin definition of the UART interfaces.

Table 16: Pin Definition of UART Interface

Pin Name	Pin No.	I/O	Description	Comment
UART1_TXD	70	DO	UART1 transmit	1.8 V power domain. If unused, keep these pins open.
UART1_RXD	72	DI	UART1 receive	
UART1_CTS	71	DO	DTE clear to send signal from DCE (Connects to DTE's CTS)	

[18] The Bluetooth UART is used for Bluetooth function by default, and also supports the connection with other peripherals. For more details about Bluetooth application, see ***Chapter 4.7***.
[19] The debug UART pins are dedicated ones and cannot be multiplexed into other functions.

UART1_RTS	74	DI	DTE request to send signal to DCE (Connects to DTE's RTS)	
BT_UART_TXD	59	DO	Bluetooth UART transmit	1.8 V power domain. If unused, keep these pins open.
BT_UART_RXD	63	DI	Bluetooth UART receive	
BT_UART_CTS	62	DO	DTE clear to send signal from DCE (Connects to DTE's CTS)	
BT_UART_RTS	61	DI	DTE request to send signal to DCE (Connects to DTE's RTS)	
DBG_TXD	107	DO	Debug UART transmit	1.8 V power domain. It is recommended to reserve test points for debug UART.
DBG_RXD	110	DI	Debug UART receive	

The module provides 1.8 V UART interfaces. Use a voltage-level translator if your application is equipped with a 3.3 V UART interface. The following figure shows a reference design.

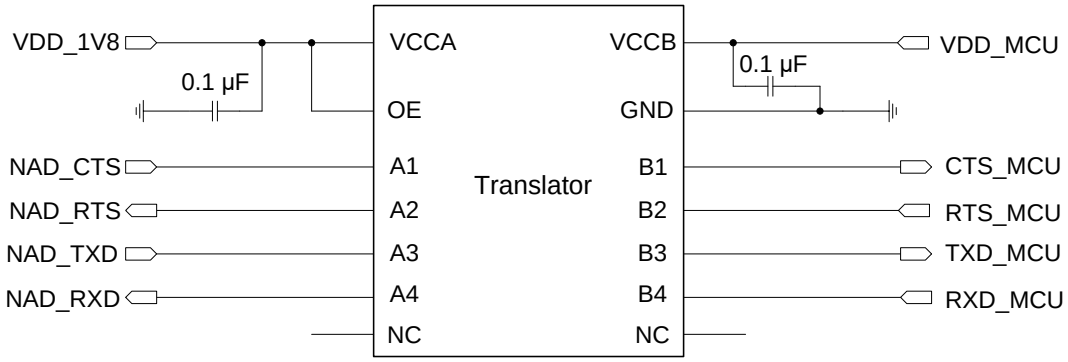


Figure 21: Reference Design of UART Interface with Translator Chip

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

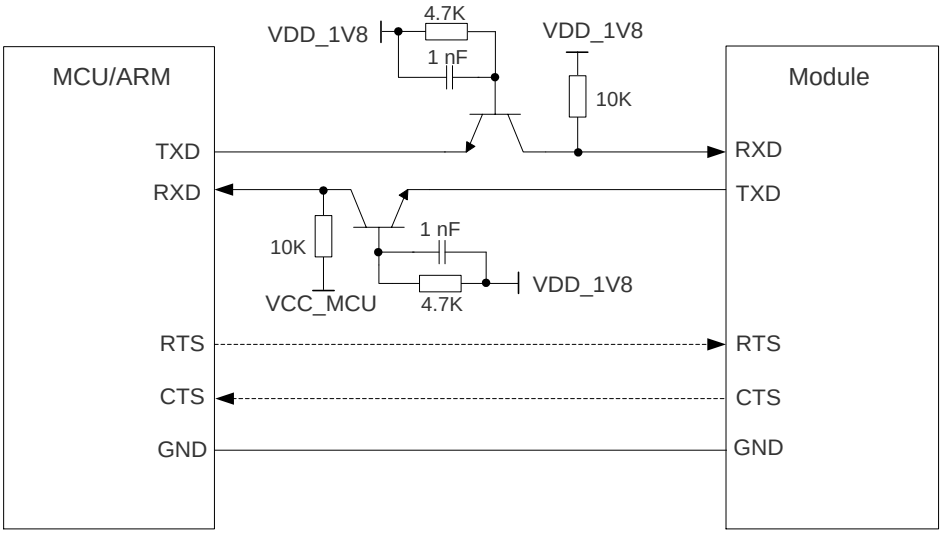


Figure 22: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. If hardware flow control is intended to be used, then CTS and RTS should also be designed with the voltage-level translation circuit.
3. When the module enters LPM, it is recommended to switch off the power supply for VDD_1V8 to reduce power consumption.
4. Please note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS.

4.4. I2S and I2C Interfaces

The module provides one I2S interface and one I2C interface for external audio codec design. The module can provide a second I2C interface through pin multiplexing. For more details, see ***document [1]***.

The following table shows the pin definition of I2S and I2C interfaces.

Table 17: Pin Definition of I2S Interface

Pin Name	Pin No.	I/O	Description	Comment
I2S_MCLK	81	DO	Clock output for codec	12.288 MHz clock output
I2S_WS	265	DIO	I2S word select	1.8 V power domain.

I2S_SCK	262	DIO	I2S clock	Serve as output signals in master mode. Serve as input signals in slave mode.
I2S_DIN	263	DI	I2S data in	1.8 V power domain.
I2S_DOUT	261	DO	I2S data out	
CDC_RST_N	77	DO	External codec reset	

Table 18: Pin Definition of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C1_SDA	80	OD	I2C serial data	Require external pull-up to 1.8 V. If unused, keep them open.
I2C1_SCL	79	OD	I2C serial clock	

The following figure shows a reference design of I2S and I2C interfaces with an external codec IC.

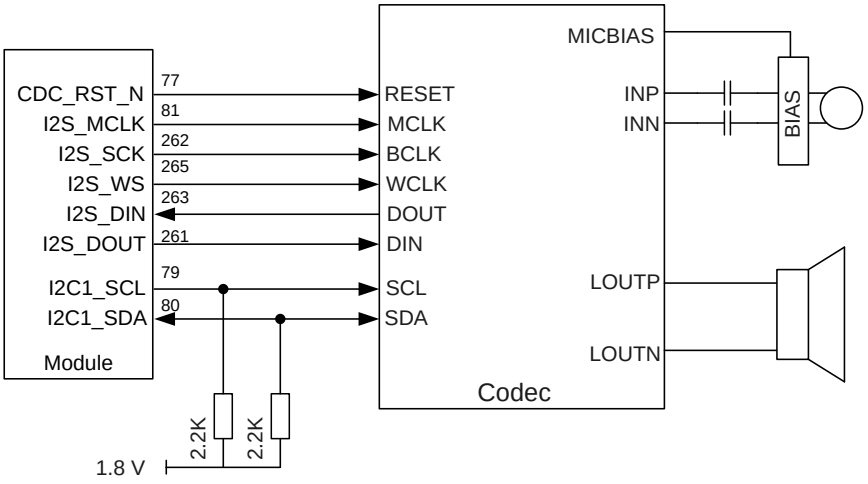


Figure 23: Reference Design of I2S and I2C Interfaces with External Audio Codec

NOTE

1. It is recommended to reserve an RC circuit on the I2S signal traces, especially for I2S_SCK and I2S_MCLK.
2. The module works as a master device in I2C applications.

4.5. PCM Interface

The module provides one PCM interface for Bluetooth audio transmission by default. See ***Chapter 4.7*** for details. The PCM interface supports primary (short frame sync) and auxiliary (long frame sync) modes.

Table 19: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	73	DIO	PCM data frame sync	1.8 V power domain. Serve as output signals in master mode. Serve as input signals in slave mode.
PCM_CLK	75	DIO	PCM clock	
PCM_IN	76	DI	PCM data input	1.8 V power domain.
PCM_OUT	78	DO	PCM data output	

The module supports 16-bit linear data format. Clock and mode can be configured, and the default configuration is primary mode using short frame sync format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. For more details, see ***document [7]***.

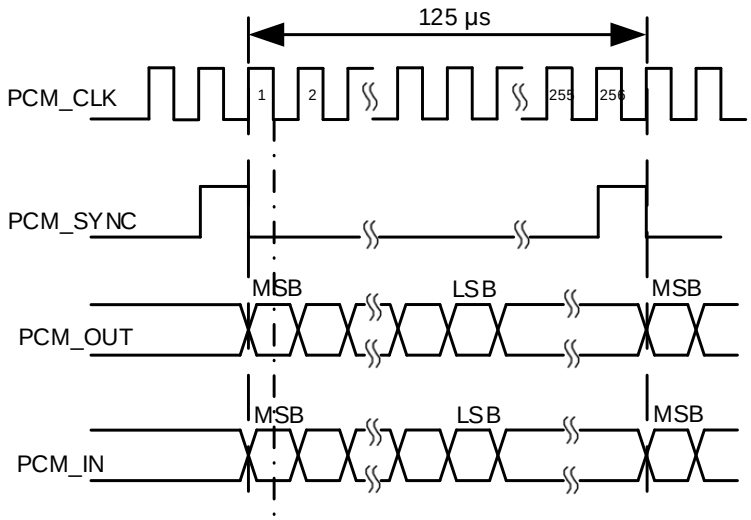


Figure 24: PCM Timing (Short Frame Sync)

NOTE

When using Bluetooth function, PCM_SYNC and PCM_CLK can only be used as output signals.

4.6. PCIe Interface

The module provides a 2-lane PCIe 3.0 interface.

- The PCIe interface supports RC and EP modes, and it works in RC mode by default
- Compliant with *PCI Express Base Specification Revision 3.0*
- Maximum rate: 8 GT/s × 1 lane theoretically
- Backward compatible
- Can be used to connect to an external WLAN chip [20]

Table 20: Pin Definition of PCIe Interface

Pin Name	Pin No.	I/O	Description	Comment
PCIE_REFCLK_P	40	AIO	PCIe reference clock (+)	Serve as output signals in RC mode. Serve as input signals in EP mode. PCIe Gen 2 is supported for WLAN function, when the interface is used for Quectel AF50T application. The differential impedance should be the same as that for PCIe TX/RX.
PCIE_REFCLK_M	38	AIO	PCIe reference clock (-)	
PCIE_TX0_M	44	AO	PCIe transmit 0 (-)	If PCIE_TX1 and PCIE_RX1 are unused, keep these pins unconnected. Require differential impedance of 70–100 Ω, and 85 Ω is recommended.
PCIE_TX0_P	46	AO	PCIe transmit 0 (+)	
PCIE_TX1_M	41	AO	PCIe transmit 1 (-)	
PCIE_TX1_P	43	AO	PCIe transmit 1 (+)	
PCIE_RX0_M	32	AI	PCIe receive 0 (-)	
PCIE_RX0_P	34	AI	PCIe receive 0 (+)	
PCIE_RX1_M	35	AI	PCIe receive 1 (-)	
PCIE_RX1_P	37	AI	PCIe receive 1 (+)	
PCIE_CLKREQ_N	36	DIO	PCIe clock request	Serve as input signals in RC mode.

[20] The PCIe interface for WLAN function is only verified with Quectel Wi-Fi & Bluetooth module AF50T presently. It is not recommended to use the interface for connection with other WLAN chips.

PCIE_WAKE_N	30	DIO	PCIe wake up	Serve as output signals in EP mode. Require a 100 kΩ pull-up to VDD_EXT. 1.8 V power domain.
PCIE_RST_N	39	DO	PCIe reset	Serves as an output signal in RC mode. Serves as an input signal in EP mode. 1.8 V power domain.

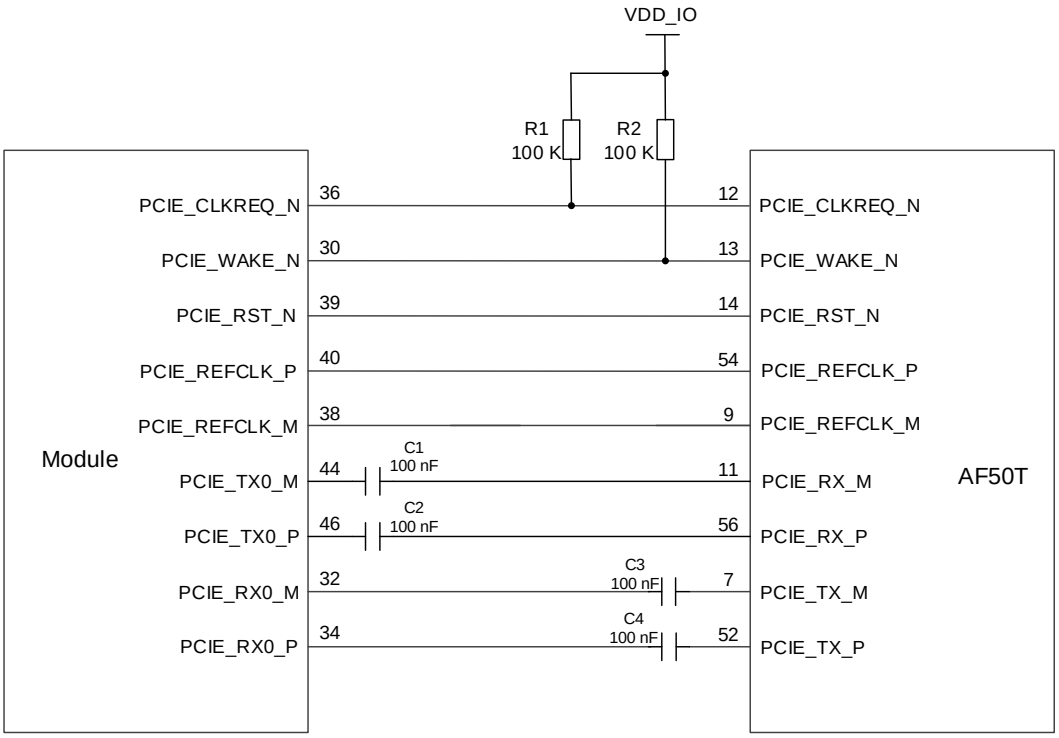


Figure 25: Reference Design of PCIe Interface

To meet PCIe specifications and enhance the reliability of applications, follow the criteria below in the PCIe interface circuit design:

- It is important to route the PCIe signal traces as differential pairs with ground surrounded. The differential impedance is 70–100 Ω and 85 Ω is recommended for PCIe Tx/Rx/REFCLK traces.
- PCIe signals must be protected from noisy signals (clocks, DC-DC, RF and so forth). All other sensitive/high-speed signals and circuits must be routed far away from PCIe traces.
- For each differential pair, the intra-lane length match should be less than 0.7 mm, while the inter-lane length match, that is, the trace length matching between the Tx, Rx and reference clock pairs is not required.
- Do not stagger the capacitors on each differential pair, as this can affect the differential integrity of the design and can create EMI.

- To reduce the probability for layer-to-layer manufacturing variation, minimize layer transitions for the main route on the PCB (that is, apply layer transitions only at break in and break out regions). When the differential signal traces changes layers, create ground vias near signal vias, and create at least 1–3 ground vias for each differential pair.
- Avoid bending of the traces to avoid common mode noise to the system. When bending is required, maintain a bend angle greater than 135° as shown in the figure below, and the shortest trace caused by bending should be at least 1.5 times the trace width (1.5W). The spacing between Tx and Rx pairs, and the spacing between PCIe lanes and all other signals, should be at least 4 times the trace width (4W).

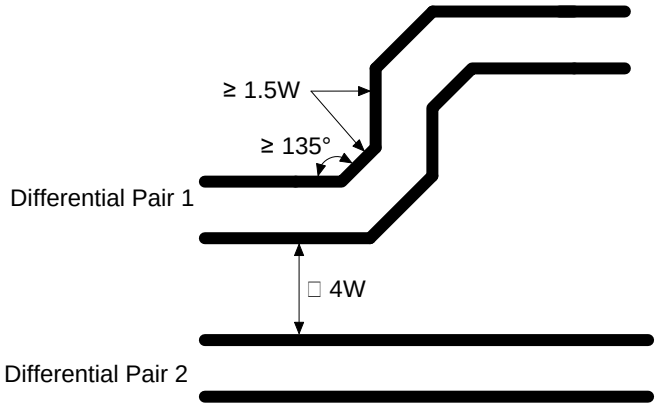


Figure 26: Curved Trace of Differential Pair

- PCIe Tx AC coupling capacitors can be anywhere along the line, but better to be placed close to the source or the receiver side to keep good signal integrity of main route on PCB. Use a serpentine to keep the difference pairs equal in the break out region as much as possible, to ensure that the traces stay differential thereafter. The length of each serpentine section should be at least 3 times the trace width (≥ 3W), and the maximum spacing between the serpentine section and the other differential trace should be less than twice of the normal differential trace spacing (S1 < 2S).

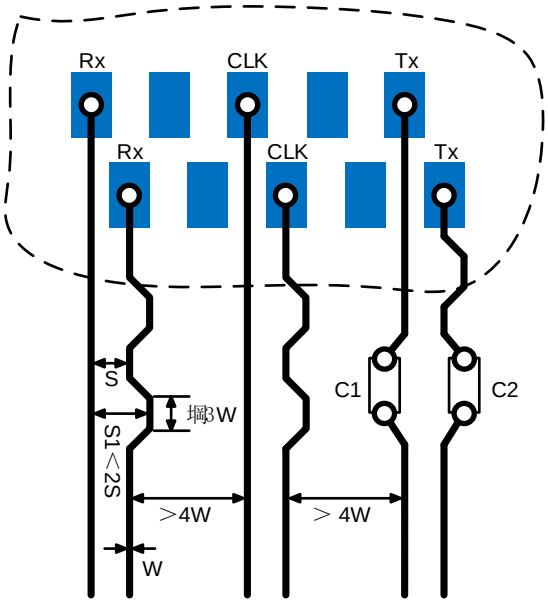


Figure 27: PCIe Trace Requirements

- PCIe Tx AC coupling capacitors should be 220 nF for PCIe Gen 3 applications, and 100 nF for PCIe Gen 2 applications.
- The maximum trace length of each differential pair for PCIe Gen 3 applications should be less than 300 mm, and that for PCIe Gen 2 applications less than 250 mm.

4.7. WLAN and Bluetooth Application Interfaces

The module provides one PCIe interface for WLAN function (see ***Chapter 4.6*** for more details), and Bluetooth UART and PCM interfaces for Bluetooth function (see ***Chapter 4.3*** and ***Chapter 4.5*** for more details).

The following table shows the pin definition of WLAN and Bluetooth application interfaces.

Table 21: Pin Definition of WLAN and Bluetooth Application Interfaces

Pin Name	Pin No.	I/O	Description	Comment
Power Supply Interface				
VDD_WIFI_VL	274, 275	PO	0.95 V low-voltage power supply for Wi-Fi & Bluetooth modules	
VDD_WIFI_VM	276	PO	1.35 V medium-voltage power	

			supply for Wi-Fi & Bluetooth modules	
VDD_WIFI_VH	277	PO	1.95 V high-voltage power supply for Wi-Fi & Bluetooth modules	
VDD_EXT	68	PO	Provide 1.8 V for external circuits	This pin can be used to connect with VDD_IO of Quectel AF50T, it also can be used as power supply for external pull up circuits. It is recommended to reserve a test point for this pin.
Coexistence Control Interface				
COEX_UART_TXD	69	DO	LTE & WLAN & Bluetooth UART coexistence UART transmit	1.8 V power domain.
COEX_UART_RXD	67	DI	LTE & WLAN & Bluetooth UART coexistence UART receive	
WL_PA_MUTE	166	DO	Module transceiver to disable WLAN PA	
LAA_AS_EN	163	DO	Allow LAA to control WLAN FEM during WLAN sleep mode	
LAA_RX	204	DO	Module sets 5 GHz WLAN xLNA to high gains or high isolation when both chains (LAA/n79 and 5 GHz WLAN) are enabled simultaneously	
LAA_TX_EN*	139	DO	The module transceiver notifies WLAN that n79/LAA transmission is ongoing and the 5 GHz WLAN should be set to isolation mode	
WL_TX_EN*	142	DI	5 GHz WLAN notifies the module that WLAN transmission is ongoing and requests the module to set n79/LAA LNA to isolation mode	
Others Interfaces				

WLAN_PWR_EN2	225	DO	WLAN power supply enable control 2	Reserved by default, if unused, keep it open.
WLAN_PWR_EN1	222	DO	WLAN power supply enable control 1	Used for Quectel AF50T VDD_RF power control.
WLAN_EN	228	DO	WLAN function enable control	
BT_EN	66	DO	Bluetooth enable control	
HOST_SW_CTRL	184	DI	Switch control	
WLAN_SLP_CLK	231	DO	WLAN 32 kHz sleep clock	If unused, keep it open.

NOTE

When WLAN or Bluetooth function is intended to be used, the coexistence UART interface must be used simultaneously. The coexistence UART interface cannot be used as general-purpose UART interface.

The following figure shows a reference design of interfaces for WLAN and Bluetooth applications. For more details, see ***document [8]***.

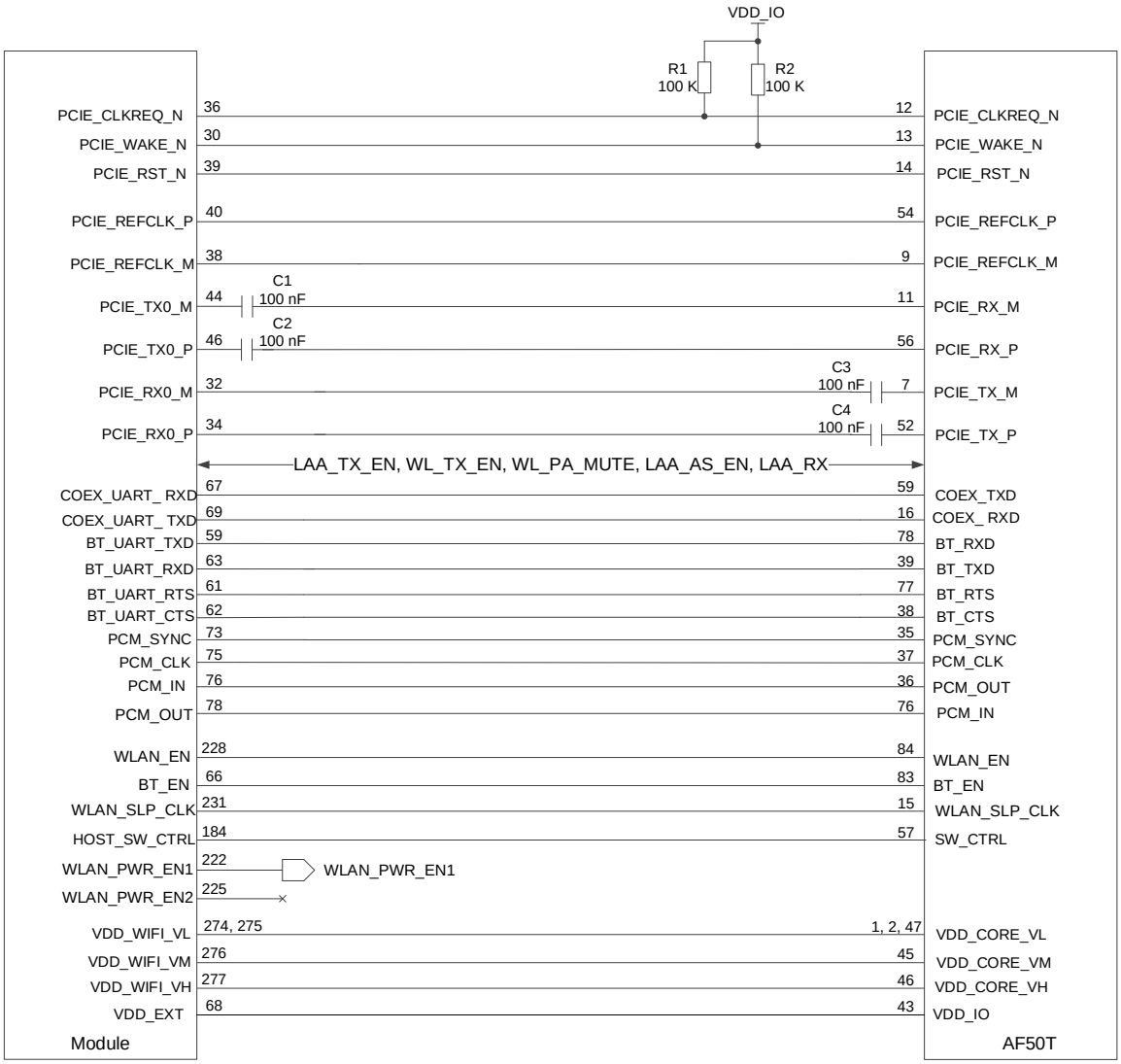


Figure 28: Reference Design of WLAN & Bluetooth Application Interfaces (AF50T)

4.8. Audio Interface (Optional)

The module is designed with an optional built-in audio codec to enable analog audio function. The following table shows the pin definition of analog audio interface.

Table 22: Pin Definition of Audio Interface

Pin Name	Pin No.	I/O	Description	Comment
MIC1_P	2	AI	Microphone input channel 1 (+)	Audio interface is not supported

MIC1_N	1	AI	Microphone input channel 1 (-)	by default, it is optional. If unused, keep these pins open.
MIC2_P	5	AI	Microphone input channel 2 (+)	
MIC2_N	4	AI	Microphone input channel 2 (-)	
MICBIAS	3	PO	Bias voltage output for microphone	
SPK1_P	268	AO	Headphone analog output 1 (+)	
SPK1_N	266	AO	Headphone analog output 1 (-)	
SPK2_P	269	AO	Headphone analog output 2 (+)	
SPK2_N	270	AO	Headphone analog output 2 (-)	
AGND	6	-	Analog ground	Connect it to GND or keep it open if unused.

Table 23: Analog Audio Interface Characteristic Parameters

Parameters	Condition	Min.	Typ.	Max.	Unit
MIC1_P/N					
Full-scale input	AV_{LINE} = 0 dB f = 1 kHz	-	-	TBD	Vp-p
Noise	AV_{LINE} = 0 dB f = 1 kHz	-	TBD	-	dB
SPK_P/N					
Max power output	Differential mode R_L = 32 Ω f = 1 kHz	-	-	TBD	mV
THD+N	Output gain = 0 dB f = 1 kHz	-	TBD	-	-

NOTE

1. The built-in codec uses the same signals as the module's I2C interface (pins 79, 80) and I2S interface (pins 261, 262, 263, 265) for external digital audio design. Therefore, when the built-in codec is utilized, the module's I2S interface cannot be used for other purposes (that is, keep pins 261, 262, 263 and 265 unconnected).
2. It is recommended to connect AGND of the analog audio interface to the main ground through a 0 Ω resistor.

3. The built-in audio codec (analog audio function) is optional.

4.9. GPIO Interfaces

The module provides 15 GPIOs for application designs. More GPIOs are available through multiplexing, and see ***document [1]*** for details.

Table 24: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	I/O	Configurable Function	Comment
GPIO1	100	DI	WAKEUP_IN	This pin is used as WAKEUP_IN by default to control the module entering/exiting the low power mode. If the default function is not used, it can be configured to GPIO.
		DIO	GPIO	General-purpose input/output. Support wake-up interrupt.
GPIO2	101	DIO	GPIO	General-purpose input/output. Support wake-up interrupt.
GPIO3	102	DIO	GPIO	General-purpose input/output
GPIO4	104	DO	SLEEP_SYS_IND	Used as SLEEP_SYS_IND by default to indicate the low power mode of the module. If the default function is not used, it can be configured to GPIO.
		DIO	GPIO	General-purpose input/output. Support wake-up interrupt.
GPIO5	116	DIO	GPIO	General-purpose input/output. Support wake-up interrupt.
GPIO6	243	DO	STATUS	Used as STATUS by default to indicate the operating status of the module. If the default function is not used, it can be configured to GPIO.
		DIO	GPIO	General-purpose input/output. It is recommended to be used as output pin.
GPIO7	246	DIO	GPIO	General-purpose input/output
GPIO8	249	DIO		

GPIO9	280	DIO		
GPIO10	283	DIO		General-purpose input/output. Support wake-up interrupt
GPIO11	284	DIO		
GPIO12	289	DIO		
GPIO13	64	DIO		General-purpose input/output
GPIO14	264	DIO		General-purpose input/output. Support wake-up interrupt
GPIO15	267	DIO		

NOTE

1. GPIO1 is used as WAKEUP_IN by default. GPIO4 is used as SLEEP_SYS_IND by default. For more details about WAKEUP_IN and SLEEP_SYS_IND, see ***document [6]***.
2. GPIO6 is used as STATUS by default. This pin is recommended to be used as an output signal.
3. If you intend to use GPIO1, GPIO4 and/or GPIO6 for other purposes, disable the corresponding default function first through software configuration.

4.10. SDIO Interface

The module provides one SDIO interface, which can be used either for eMMC (4-bit by default, max. up to 8-bit) or SD card function. The following tables show the pin definition of SDIO interface.

Table 25: Pin Definition of SDIO Interface

Pin Name	Pin No.	I/O	Description	Comment
SDIO_VDD	60	PI	Power supply input for SDIO	**SD card application**: Connect to external 1.8/2.95 V power supply. **eMMC application**: Connect to external 1.8 V power supply. If SDIO interface is not used, connect this pin to VDD_EXT.
SDC1_DATA_0	49	DIO	SDIO data bit 0	The power domain depends on SDIO_VDD.
SDC1_DATA_1	50	DIO	SDIO data bit 1	
SDC1_DATA_2	51	DIO	SDIO data bit 2	

SDC1_DATA_3	52	DIO	SDIO data bit 3	
SDC1_CMD	48	DIO	SDIO command	
SDC1_CLK	47	DO	SDIO clock	
SDC1_DATA_4	53	DIO	SDIO data bit 4	1.8 V power domain.
SDC1_DATA_5	55	DIO	**eMMC application:** SDIO data bit 5 **SD card application:** SD card detection	
SDC1_DATA_6	56	DIO	SDIO data bit 6	
SDC1_DATA_7	58	DIO	SDIO data bit 7	
EMMC_RST_N*	54	DO	eMMC reset	1.8 V power domain.
EMMC_PWR_EN	45	DO	eMMC power supply enable control	

4.10.1. Reference Design for SD Card Application

The following figure shows a reference design of SDIO interface for SD card application.

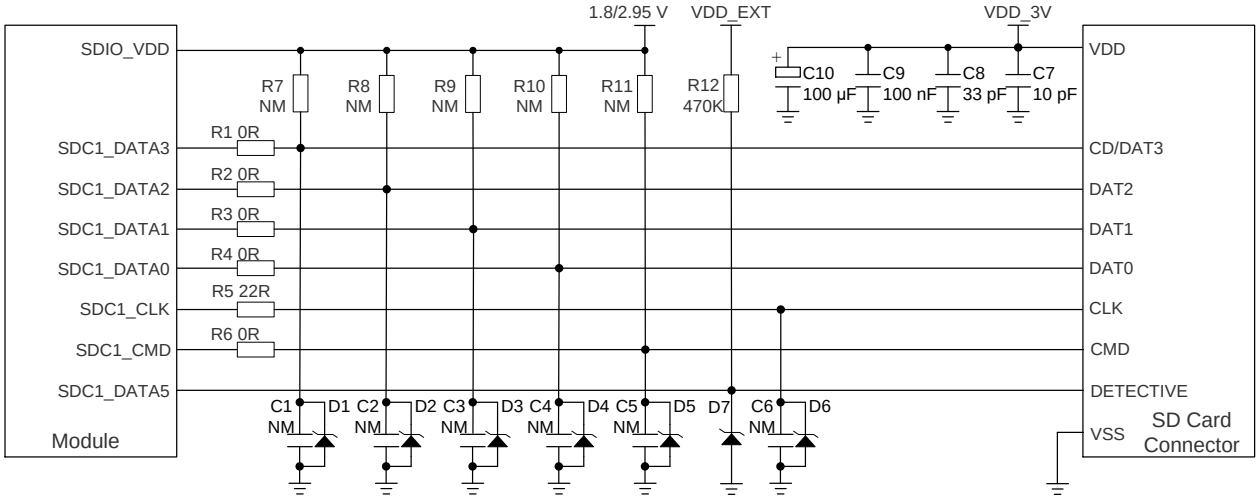


Figure 29: Reference Circuit Design for SD Card Application

To enhance the reliability and availability of applications, follow the principles below in the SD card circuit design:

- To avoid jitter of bus, it is recommended to reserve R7–R11 (10–100 kΩ) to pull up SDIOs to an

external 1.8/2.95 V power supply. The resistors are not mounted by default.

- To improve signal quality, it is recommended to add resistors R1–R6 in series between the module and the SD card connector. Resistor R5 should be 20–30 Ω and the other resistors are 0 Ω by default. The bypass capacitors C1–C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- To offer good ESD protection, it is recommended to add a 2 pF TVS on each signal pin of SD card connector, and place them close to the SD card connector.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50 Ω (±10 %).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- Spacing between DATA and DATA/CLK bus is twice larger than the trace width.
- It is recommended to keep the trace length difference between SDC1_CLK and SDC1_DATA_[0:3]/SDC1_CMD less than 1 mm and the total routing length less than 50 mm. The total trace length inside the module is 17 mm, so the exterior total trace length should be less than 33 mm.
- Keep the spacing between SDIO and other signal traces at least twice the trace width and the load capacitance of SDIO bus less than 40 pF.

4.10.2. Reference Design for eMMC Application

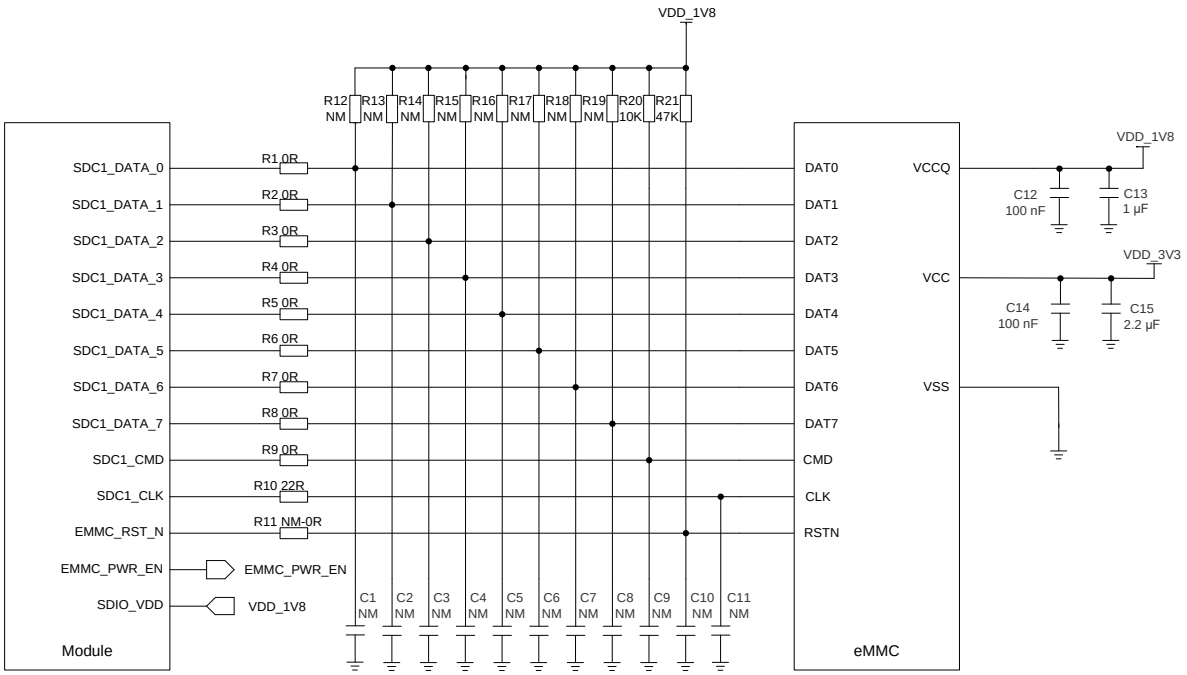


Figure 30: Reference Circuit Design for eMMC Application

Follow the principles below in eMMC circuit design:

- To avoid jitter of bus, it is recommended to reserve R12–R19 (10–100 kΩ) to pull up SDIO signals to an external 1.8 V LDO. The resistors are not mounted by default, and the recommended value is 100 kΩ.
- To improve signal quality, it is recommended to add resistors R1–R10 in series between the module and eMMC. Resistor R10 should be 20–30 Ω and the other resistors are 0 Ω by default. The bypass capacitors C1–C11 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50 Ω (±10 %).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is recommended to keep the trace length difference between SDC1_CLK and SDC1_DATA[0:7]/SDC1_CMD less than 1 mm and the total routing length less than 50 mm. The total trace length inside the module is 17 mm, so the exterior total trace length should be less than 33 mm.
- Keep the spacing between SDIO and other signal traces at least twice the trace width and the load capacitance of SDIO bus less than 40 pF.

4.11. SPI Interfaces

The module provides two SPI interfaces by default. SPI2 interface can be multiplexed into I2C2 interface, and see ***document [1]*** for more details.

Both SPI interfaces support master mode only. The maximum clock frequency is up to 50 MHz.

The following tables show the pin definition of SPI interfaces.

Table 26: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI1_MOSI	210	DO	SPI1 master-out slave-in	1.8 V power domain. Support master mode only. Keep these pins open if unused.
SPI1_MISO	219	DI	SPI1 master-in slave-out	
SPI1_CS	213	DO	SPI1 chip select	
SPI1_CLK	216	DO	SPI1 clock	
SPI2_MOSI	108	DO	SPI2 master-out slave-in	1.8 V power domain. Support master mode only. Keep these pins open if unused.
SPI2_MISO	106	DI	SPI2 master-in slave-out	

SPI2_CS	105	DO	SPI2 chip select
SPI2_CLK	103	DO	SPI2 clock

The following figure shows the timing relationship of SPI interface. The related parameters of SPI timing are shown in the table below.

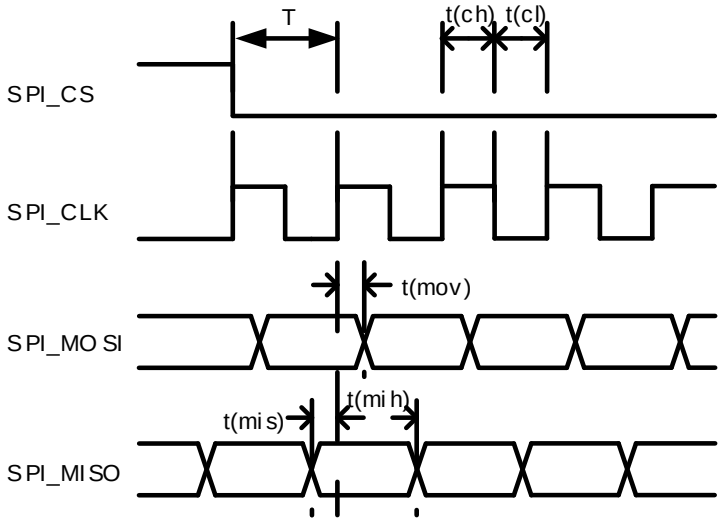


Figure 31: SPI Timing

Table 27: Parameters of SPI Interface Timing

Parameter	Description	Min.	Typ.	Max.	Unit
T	SPI clock period	20.0	-	-	ns
t(ch)	SPI clock high-level time	8.0	-	-	ns
t(cl)	SPI clock low-level time	8.0	-	-	ns
t(mov)	SPI master data output valid time	-5.0	-	5.0	ns
t(mis)	SPI master data input setup time	5.0	-	-	ns
t(mih)	SPI master data input hold time	1.0	-	-	ns

NOTE

The module provides 1.8 V SPI interfaces. A voltage-level translator should be used between the module and the host if the application is equipped with a 3.3 V processor or device interface.

4.12. RGMII Interface

The module includes an integrated Ethernet MAC with a RGMII interface which also supports EAVB. Key features of the RGMII interface are shown below:

- IEEE 802.3 compliant
- Support 10/100/1000 Mbps operation
- Support protocols such as IEEE 1722.A (AVTP), 802.1Qav (FQTSS), 802.1Qat (SRP), 802.1AS (gPTP)
- Support connection to an external Ethernet PHY like Marvell 88Q2112, or an external Ethernet switch
- Support 1.8/2.5 V I/O standards

The following table shows the pin definition of RGMII interface.

Table 28: Pin Definition of RGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
RGMII_MD_IO	10	DIO	RGMII management data	It generally requires a pull-up resistor close to the external PHY end.
RGMII_MD_CLK	11	DO	RGMII management data clock	Do not add any pull-up resistor to this pin, or it may cause higher power consumption during LPM.
RGMII_CK_RX	19	DI	RGMII receive clock	The power domain depends on RGMII_PWR_IN. Typ.1.8/2.5 V, and 1.8 V is recommended. The single-ended impedance requires 50 Ω.
RGMII_CTL_RX	15	DI	RGMII receive control	
RGMII_RX_0	13	DI	RGMII receive data bit 0	
RGMII_RX_1	14	DI	RGMII receive data bit 1	
RGMII_RX_2	16	DI	RGMII receive data bit 2	

RGMII_RX_3	17	DI	RGMII receive data bit 3	
RGMII_CK_TX	24	DO	RGMII transmit clock	
RGMII_CTL_TX	21	DO	RGMII transmit control	
RGMII_TX_0	20	DO	RGMII transmit data bit 0	
RGMII_TX_1	22	DO	RGMII transmit data bit 1	
RGMII_TX_2	23	DO	RGMII transmit data bit 2	
RGMII_TX_3	25	DO	RGMII transmit data bit 3	
RGMII_PWR_EN	27	DO	Enable an external power supply to power RGMII_ PWR_IN	1.8 V power domain
RGMII_PWR_IN	28	PI	RGMII interface power supply input	Typ.1.8/2.5 V. An external power supply is required to power this pin. Require maximum current of 100 mA. If RGMII interface is not used, connect this pin to VDD_EXT.
RGMII_INT	29	DI	RGMII interrupt input	1.8 V power domain
RGMII_RST_N	31	DO	Reset output for RGMII PHY	

The following figure shows the simplified block diagram for Ethernet application.

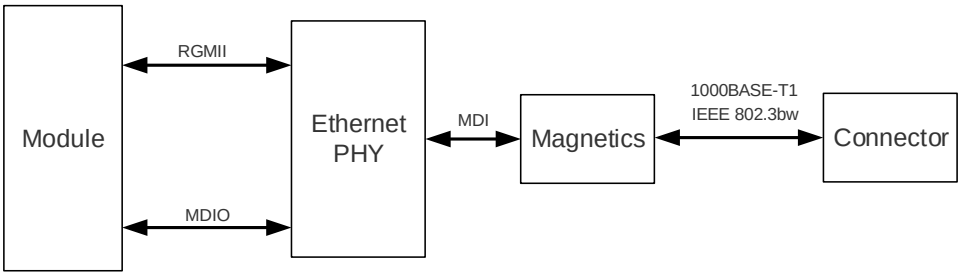


Figure 32: Simplified Block Diagram for Automotive Ethernet Application

The following figure shows a reference design of RGMII interface with PHY application. For more details, see ***document [8]***.

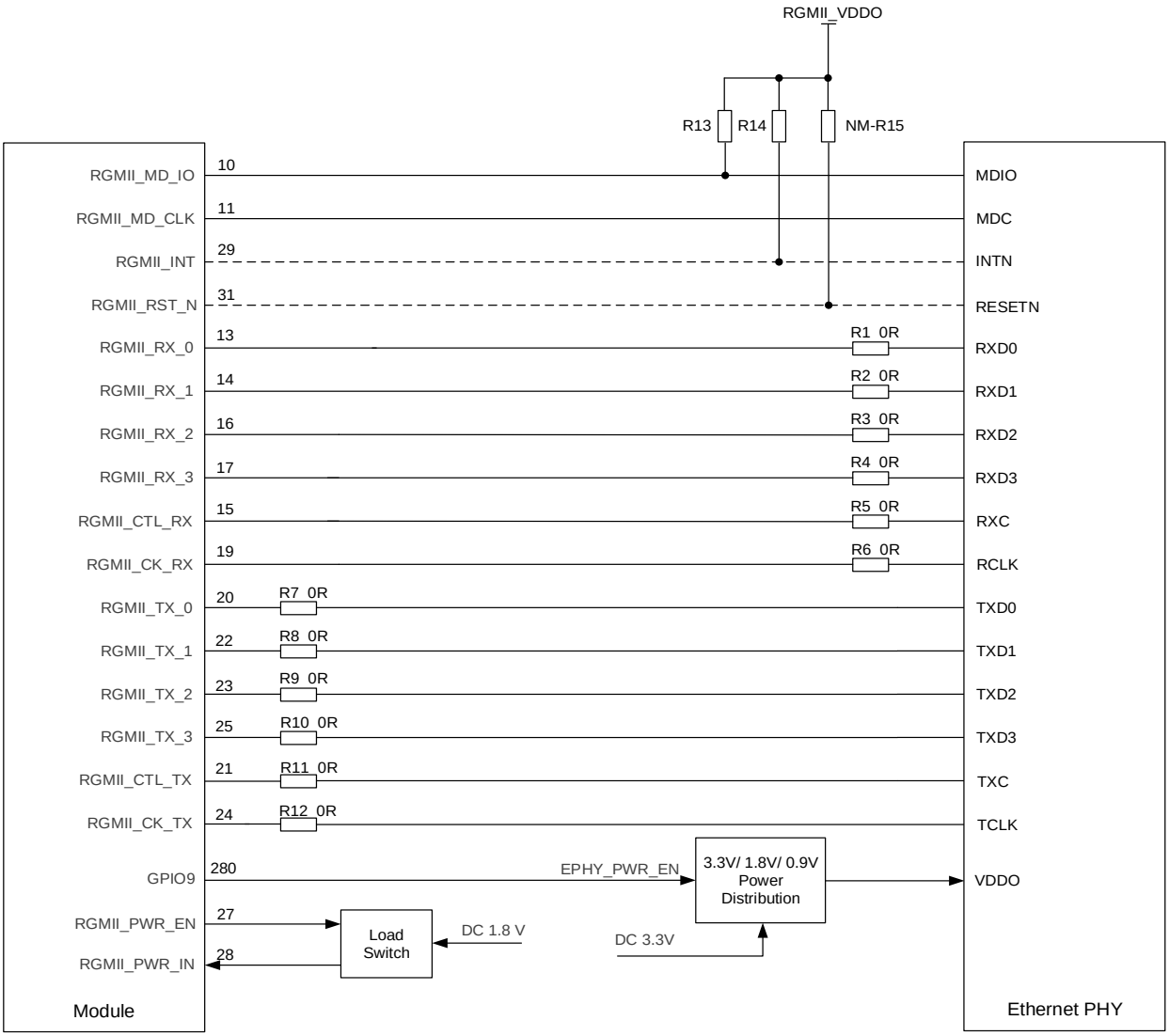


Figure 33: Reference Circuit of RGMII Interface with PHY Application

To enhance the reliability and availability of application designs, follow the criteria below in the Ethernet PHY circuit design:

- Keep RGMII data and control signals away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- The single-ended impedance of RGMII data traces is 50 Ω ±20 %.
- The length matching between Tx signals (RGMII_CK_TX, RGMII_CTL_TX and RGMII_TX_[0:3]) or Rx signals (RGMII_CK_RX, RGMII_CTL_RX and RGMII_RX_[0:3]) is less than 2 mm.
- Keep the spacing between Tx bus traces (RGMII_CK_TX to RGMII_TX_[0:3]/RGMII_CTL_TX) or that between Rx bus traces (RGMII_CK_RX to RGMII_RX_[0:3]/RGMII_CTL_RX) at least 2 times the trace width.
- Keep the spacing between Tx bus and Rx bus traces at least 2.5 times trace width.
- Keep the spacing between RGMII and other signal traces at least 3 times trace width.
- Resistors R7–R12 should be placed near the module. Resistors R1–R6 should be placed near the

Ethernet PHY. The value of R1–R15 varies with the selection of PHY.

- RGMII_INT and RGMII_RST_N are always 1.8 V power domain. A voltage-level translator should be used when module I/O level does not match with PHY.

NOTE

Gigabit Ethernet is an optional function; RGMII interface is supported by default.

4.13. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces. The voltage value on ADC pins can be read with **AT+QADC=<port>**, through setting **<port>** into 0 or 1. For more details about the AT command, see ***document [5]***.

- **AT+QADC=0**: read the voltage value on ADC0
- **AT+QADC=1**: read the voltage value on ADC1

ADC related API can also read the voltage value of ADC. For more details, see ***document [9]*** .

To improve the accuracy of ADC, the traces of ADC interfaces should be surrounded by ground.

Table 29: Pin Definition of ADC Interface

Pin Name	Pin No.	Description	Comment
ADC0	247	General-purpose ADC interface	Voltage range: 0–1.875 V
ADC1	245	General-purpose ADC interface	

The following table describes the characteristic of ADC interfaces.

Table 30: Characteristic of ADC Interface

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0	-	1.875	V
ADC1 Voltage Range	0	-	1.875	V

ADC Resolution	-	15	-	bits
ADC Sample Rate	-	4.8	-	MHz

NOTE

1. The input voltage for each ADC interface must not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.

4.14. USB_BOOT Interface

The module provides a USB_BOOT pin. Developers can pull up the USB_BOOT to VDD_EXT before powering on the module so that the module will enter emergency download mode when powered on. In this mode, the module supports firmware upgrade over USB 2.0 interface.

Table 31: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	83	DI	Force the module into emergency download mode	1.8 V power domain. Active high. It is recommended to reserve test points.

The following figure shows a reference design of USB_BOOT interface.

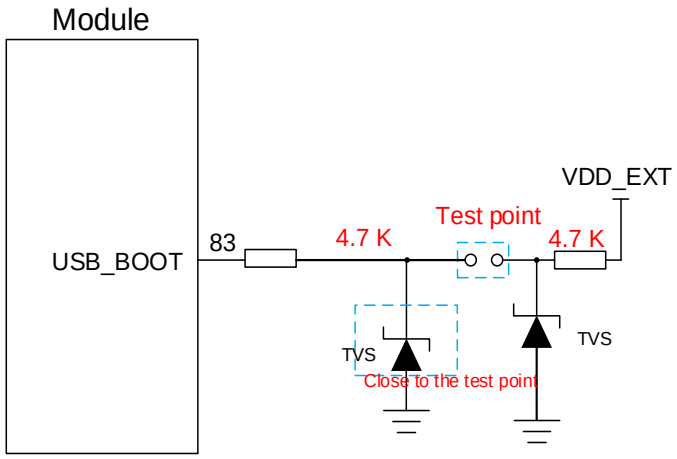


Figure 34: Reference Design of USB_BOOT Interface

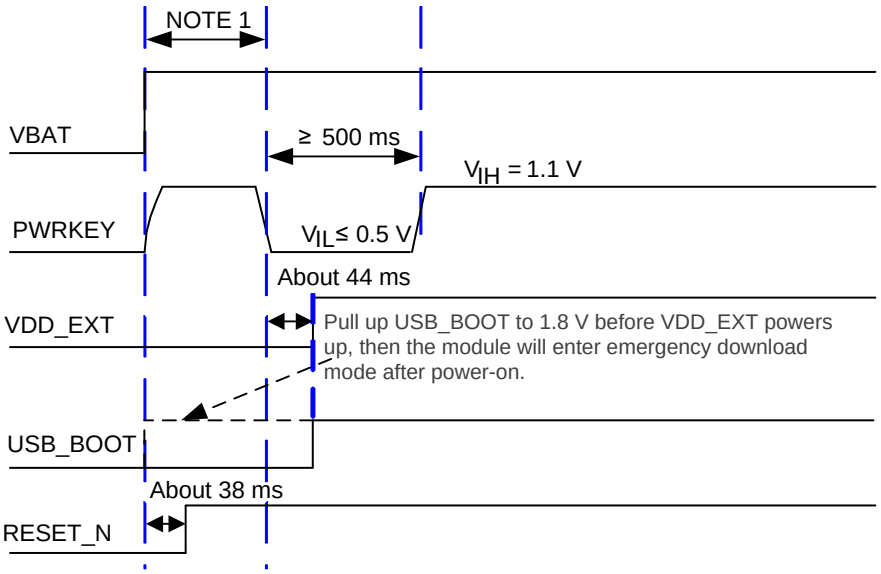


Figure 35: Emergency Download Mode Timing

NOTE

1. Ensure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin is not less than 30 ms.
2. When using MCU to control the module entering emergency download mode, follow the above timing. It is not recommended to pull up to 1.8 V before VBAT powers up. Connecting the test points as shown in ***Figure 34*** can manually force the module into emergency download mode.

4.15. RTC

The module has a real time clock within the PMIC, but has no dedicated RTC power supply pin. The RTC is powered by VBAT_BB. If VBAT_BB is removed, the RTC will not maintain. If RTC is needed, then VBAT_BB must be powered.

4.16. DR_SYNC

The module obtains time through GNSS positioning and outputs 1PPS signal for clock synchronization. The DR_SYNC pin usually connects to an external AP and an MCU to maintain the time consistency between the three.

Table 32: Pin Definition of DR_SYNC Interface

Pin Name	Pin No.	I/O	Description
DR_SYNC	95	DO	Dead reckoning sync

A reference design of DR_SYNC interface for clock synchronization applications is shown as below:

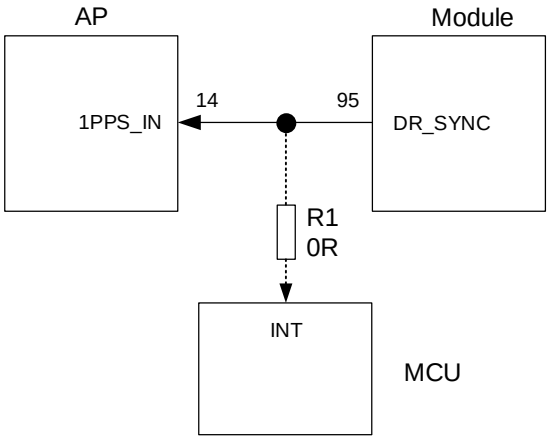


Figure 36: Reference Design of DR_SYNC for Clock Synchronization Applications

NOTE

Pay attention to the level matching of the signal shown in dotted line between the module and the MCU.

4.17. IMU Interrupt Interface

The module realizes DR (dead-reckoning) function through an external IMU (inertial measurement unit). For more details about QDR, see ***document [10].***

Table 33: Pin Definition of IMU Interrupt Interface

Pin Name	Pin No.	I/O	Description	Comment
IMU_PWR_EN	181	DO	IMU power enable control	1.8 V power domain. If unused, keep them open.
IMU_INT1	169	DI	IMU interrupt 1	

IMU_INT2	187	DI	IMU interrupt 2

A reference design of IMU interrupt interface is shown as below:

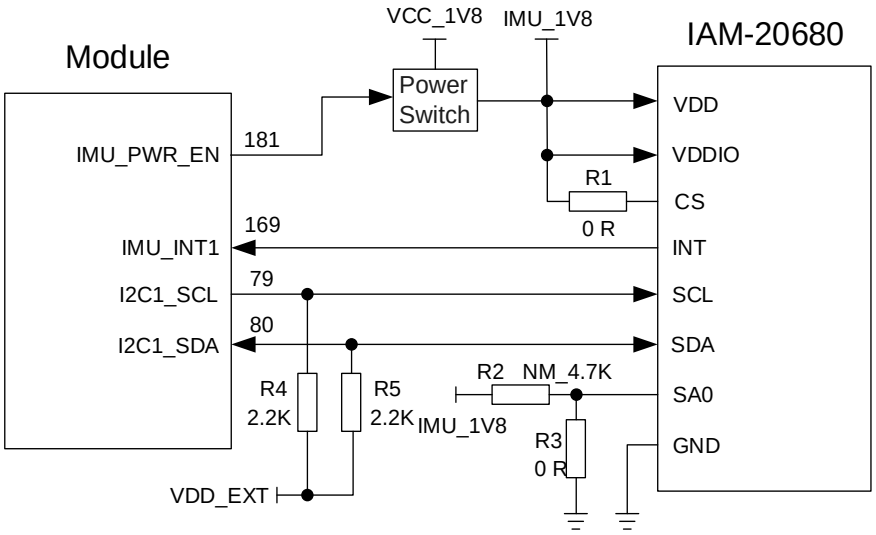


Figure 37: IMU Reference Design Circuit

NOTE

The module also supports Bosch SMI130, SMI230 and ST ASM330LHH sensors.

5 RF Specifications

The antenna interfaces of the module are shown as follows, and the impedance of antenna ports is 50 Ω.

Table 34: Antenna Interface Types

Interface Type	Interface Count	Pin Name
Main antenna interface	1	ANT_MAIN
Rx-diversity antenna interface [21]	1	ANT_DRX
C-V2X antenna interfaces [22]	2	ANT_CV2X_TRX0, ANT_CV2X_TRX1
MIMO antenna interfaces [23]	2	ANT_MIMO3, ANT_MIMO4
GNSS antenna interface [24]	1	ANT_GNSS
DSDA antenna interfaces [25]	2	ANT_DSDA_MAIN, ANT_DSDA_DIV

[21] Rx-diversity antenna interface is used to resist the fall of signals caused by high-speed movement and multipath effect.
[22] Only AG550Q series and AG553Q-EU support C-V2X.
[23] LTE-FDD B32 and LTE-TDD B34 do not support 4 × 4 MIMO. They support 2 × 2 MIMO only.
[24] GNSS function is optional.
[25] Only AG553Q-EU supports DSDA; AG550Q and AG551Q series support DSSS.

5.1. Cellular Antenna Interfaces

5.1.1. Pin Definition [26]

The pin definition of cellular antenna interfaces is shown below.

Table 35: Pin Definition of Cellular Antenna Interfaces – AG55xQ-CN

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	414	AIO	2G/3G/4G TRx0 5G NR n1/n3/n28 TRx0 SA 5G NR n41/n78/n79 Rx1	50 Ω characteristic impedance.
ANT_DRX	416	AIO	3G/4G LMHB DRx0 5G NR n1/n3/n28 DRx0 5G NR n41 DRx1 5G NR n78/n79 TRx0 SA/NSA	
ANT_MIMO3	418	AIO	4G MHB Rx1 5G NR n1/n3 Rx1 5G NR n41 TRx0 SA/NSA 5G NR n78/n79 DRx0	
ANT_MIMO4	420	AI	4G MHB DRx1 5G NR n41 DRx0 5G NR n1/n3/n78/n79 DRx1	
ANT_DSDA_MAIN	422	AIO	DSDA 2G/4G TRx	
ANT_DSDA_DIV	424	AI	DSDA 4G DRx	
ANT_CV2X_TRX1	433	AIO	C-V2X TRx1	
ANT_CV2X_TRX0	436	AIO	C-V2X TRx0	

Table 36: Pin Definition of Cellular Antenna Interfaces – AG55xQ-EU

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	414	AIO	2G/3G/4G LMHB TRx0 5G NR n1/n3/n8/n20/n28 TRx0 SA/NSA	50 Ω characteristic impedance.

[26] Frequency range of LB, MB and HB:
LB: < 1 GHz;
MB: 1–2.3 GHz;
HB: > 2.3 GHz.

			4G B42 DRx0 5G NR n41/n78 DRx0	
ANT_DRX	416	AIO	3G/4G/5G LMHB DRx0 5G NR n41 DRx1 4G B42 TRx0 5G NR n78 TRx0 SA/NSA	
ANT_MIMO3	418	AIO	4G MHB Rx1 4G B42 Rx1 5G NR n41 TRX0 SA/NSA 5G NR n1/n3/n78 Rx1	50 Ω characteristic impedance.
ANT_MIMO4	420	AI	4G MHB DRx1 4G B42 Rx1 5G NR n41 DRx1 5G NR n1/n3/n78 DRx1	
ANT_DSDA_MAIN	422	AIO	DSDA 2G/4G TRx	50 Ω characteristic impedance.
ANT_DSDA_DIV	424	AI	DSDA 4G DRx	50 Ω characteristic impedance.
ANT_CV2X_TRX1	433	AIO	C-V2X TRx1	50 Ω characteristic impedance.
ANT_CV2X_TRX0	436	AIO	C-V2X TRx0	

Table 37: Pin Definition of Cellular Antenna Interfaces – AG55xQ-NA

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	414	AIO	2G/4G TRx0 5G NR n2/n5/n25/n66/n71 TRx0 SA/NSA 4G B48 DRx0 5G NR n41/n48/n77/n78 DRx0	50 Ω characteristic impedance. If unused, keep them open.
ANT_DRX	416	AIO	4G/5G LMHB DRx0 5G NR n41 DRx1 4G B48 TRx0 5G NR n48/n77/n78 TRx0 SA/NSA	
ANT_MIMO3	418	AIO	4G MHB Rx1 5G NR n41 TRx0 SA/NSA 4G B48 Rx1 5G NR n2/n25/n66/n48/n77n78 Rx1	
ANT_MIMO4	420	AI	4G MHB DRx1 4G B48 DRx1 5G NR n41 DRx0 5G NR n2/n25/n66/n48/n77/n78 DRx1	

ANT_DSDA_MAIN	422	AIO	DSDA 2G/4G TRx
ANT_DSDA_DIV	424	AI	DSDA 4G DRx
ANT_CV2X_TRX1	433	AIO	C-V2X TRx1
ANT_CV2X_TRX0	436	AIO	C-V2X TRx0

5.1.2. Operating Frequencies

Table 38: AG55xQ-CN Operating Frequencies

3GPP Band	Transmit	Receive	Unit
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B8	880–915	925–960	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-TDD B34	2010–2025	2010–2025	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B39	1880–1920	1880–1920	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz
C-V2X B47 [27]	5855-5925	5855-5925	MHz
5G NR FDD n1 [28]	1920–1980	2110–2170	MHz

[27] Only AG550Q and AG553Q series support C-V2X.
[28] 5G NR FDD n1, n3 and n28 of AG55xQ-CN support SA only.

5G NR FDD n3 [28]	1710–1785	1805–1880	MHz
5G NR FDD n28 [28]	703–748	758–803	MHz
5G NR TDD n41	2496–2690	2496–2690	MHz
5G NR TDD n78	3300–3800	3300–3800	MHz
5G NR TDD n79	4400–5000	4400–5000	MHz

Table 39: AG55xQ-EU Operating Frequencies

3GPP Band	Transmit	Receive	Unit
GSM850	824-849	869-894	MHz
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
PCS1900	1850-1910	1930-1990	MHz
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B3	1710–1785	1805–1880	MHz
WCDMA B5	824–849	869–894	MHz
WCDMA B6	830-840	875-885	MHz
WCDMA B8	880–915	925–960	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B2	1850-1910	1930-1990	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B4	1710-1755	2110-2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B20	832–862	791–821	MHz

LTE-FDD B28	703–748	758–803	MHz
LTE-FDD B32 [29]	-	1452–1496	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz
LTE-TDD B42	3400–3600	3400–3600	MHz
C-V2X B47 [27]	5855-5925	5855-5925	MHz
5G NR FDD n1	1920–1980	2110–2170	MHz
5G NR FDD n3	1710–1785	1805–1880	MHz
5G NR FDD n8	880–915	925–960	MHz
5G NR FDD n20	832–862	791–821	MHz
5G NR FDD n28	703–748	758–803	MHz
5G NR TDD n41	2496–2690	2496–2690	MHz
5G NR TDD n78	3300–3800	3300–3800	MHz

Table 40: AG55xQ-NA Operating Frequencies

3GPP Band	Transmit	Receive	Unit
PCS1900	1850-1910	1930-1990	MHz
LTE-FDD B2	1850–1910	1930–1990	MHz
LTE-FDD B4	1710–1755	2110–2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B12	699–716	729–746	MHz
LTE-FDD B13	777–787	746–756	MHz

[29] LTE-FDD B29, B30 and B32 support reception (Rx) only.

LTE-FDD B14	788–798	758–768	MHz
LTE-FDD B17	704–716	734–746	MHz
LTE-FDD B25	1850–1915	1930–1995	MHz
LTE-FDD B26	814–849	859–894	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-FDD B29 [29]	-	717–728	MHz
LTE-FDD B30 [29]	-	2350–2360	MHz
LTE-FDD B66	1710–1780	2110–2200	MHz
LTE-FDD B71	663–698	617–652	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz
LTE-TDD B48	3550–3700	3550–3700	MHz
C-V2X B47	5855-5925	5855-5925	MHz
5G NR FDD n2	1850–1910	1930–1990	MHz
5G NR FDD n5	824–849	869–894	MHz
5G NR FDD n25	1850–1915	1930–1995	MHz
5G NR FDD n66	1710–1780	2110–2200	MHz
5G NR FDD n71	663–698	617–652	MHz
5G NR TDD n41	2496–2690	2496–2690	MHz
5G NR TDD n48	3550–3700	3550–3700	MHz
5G NR TDD n77	3300–4200	3300–4200	MHz
5G NR TDD n78	3300–3800	3300–3800	MHz

5.1.3. Tx Power

The following table shows the RF output power of the module.

Table 41: RF Output Power

Type	Frequency Band	Max. Tx Power	Min. Tx Power
GSM	GSM850	33 dBm ±2 dB	5 dBm ±5 dB
	EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
	DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
	PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
WCDMA	WCDMA bands	23 dBm ±2 dB (Class 3)	< -50 dBm
LTE	LTE bands	23 dBm ±2 dB (Class 3)	< -40 dBm
5G NR	5G NR FDD bands + 5G NR TDD n48	23 dBm ±2 dB (Class 3)	< -40 dBm
	5G NR TDD HPUE bands (n41/n77/n78/n79)	26 dBm +1/-2 dB (Class 2)	< -40 dBm

NOTE

1. In GPRS 4 slots TX mode, the maximum output power is reduced by 4.0 dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.
2. WCDMA stated typical power tolerance meets *3GPP TS 34.121-1* requirements.
3. LTE stated typical power tolerance meets *3GPP TS 36.521-1* requirements and it is tested @ BW = 10 MHz,1 RB.
4. 5G NR stated typical power tolerance meets *3GPP TS 38.521-1* requirements.

5.1.4. Rx Sensitivity

Table 42: AG55xQ-CN RF Receiving Sensitivity

Frequency Band	Receiving Sensitivity (Typical Value) (dBm)			
	Primary	Diversity	SIMO [30]	3GPP (SIMO)
EGSM900	-109	-	-	-102
DCS1800	-107.5	-	-	-102

[30] Test conditions for the receiving sensitivity of AG55xQ-CN:
- WCDMA and LTE bands: tested with 2 antennas (2Rx);
- 5G NR SA n28: tested with 2 antennas (2Rx);
- Other 5G NR SA bands: tested with 4 antennas (4Rx).

WCDMA B1	-110.5	-112	-114	-106.7
WCDMA B8	-111.5	-113	-114.5	-103.7
LTE-FDD B1 (10 MHz)	-97.9	-99.5	-101.9	-96.3
LTE-FDD B3 (10 MHz)	-97.6	-99.6	-101.8	-93.3
LTE-FDD B5 (10 MHz)	-99.5	-101.3	-103.4	-94.3
LTE-FDD B7 (10 MHz)	-98	-98.2	-101.3	-94.3
LTE-FDD B8 (10 MHz)	-98.8	-101	-103.4	-93.3
LTE-TDD B34 (10 MHz)	-97.9	-99.7	-101.3	-96.3
LTE-TDD B38 (10 MHz)	-97	-97.3	-100	-96.3
LTE-TDD B39 (10 MHz)	-97.6	-99	-99.6	-96.3
LTE-TDD B40 (10 MHz)	-96.5	-97.2	-100	-96.3
LTE-TDD B41(10 MHz)	-96.7	-96.6	-99.9	-94.3
C-V2X B47 (10 MHz) [31]	-96.8	-97.67	-	-90.4
5G NR FDD n1 (20 MHz) [32]	-96.5	-97.5	-102.5	-96.5
5G NR FDD n3 (20 MHz) [32]	-96	-97.5	-102.5	-93.5
5G NR FDD n28 (20 MHz) [32]	-97.5	-98.5	-100.5	-90.8
5G NR TDD n41 (100 MHz)	-88	-88.5	-94.5	-87.4
5G NR TDD n78 (100 MHz)	-87.5	-88.5	-94.5	-87.8
5G NR TDD n79 (100 MHz)	-87	-90	-93.5	-87.8

[31] Only AG550Q and AG553Q series support C-V2X.
[32] 5G NR FDD n1, n3 and n28 of AG55xQ-CN support SA only.

Table 43: AG55xQ-EU RF Receiving Sensitivity [33]

Frequency Band	Receiving Sensitivity (Typical Value) (dBm)			
	Primary	Diversity	SIMO [34]	3GPP (SIMO)
GSM850	-109.5	-	-	-102.0
EGSM900	-108.5	-	-	-102.0
DCS1800	-108.0	-	-	-102 .0
PCS1900	-107.4	-	-	-102.0
WCDMA B1	-111.6	-113.2	-115.4	-106.7
WCDMA B3	-112.7	-112.7	-114.4	-103.7
WCDMA B5	-112.2	-113.1	-115.8	-104.7
WCDMA B6	-112.3	-113	-115.8	-106.7
WCDMA B8	-111.8	-112.8	-115.5	-103.7
LTE-FDD B1 (10 MHz)	-98.7	-98.9	-105.2	-99.7
LTE-FDD B2 (10 MHz)	-97.7	-98.6	-101.7	-94.3
LTE-FDD B3 (10 MHz)	-98.0	-98.2	-103.7	-96.7
LTE-FDD B4 (10 MHz)	-98.6	-97.6	-101.8	-96.3
LTE-FDD B5 (10 MHz)	-99.7	-98.0	-104.1	-94.3
LTE-TDD B7 (10 MHz)	-98.2	-98.4	-104.1	-97.7
LTE-FDD B8 (10 MHz)	-99.4	-99.7	-103	-93.3
LTE-FDD B20 (10 MHz)	-100.5	-100.6	-103.7	-93.3
LTE-FDD B28 (10 MHz)	-100.1	-100.3	-103.6	-94.8
LTE-FDD B32 (10 MHz) [35]	-	-	-99.1	-96.3
LTE-TDD B38 (10 MHz)	-96.8	-97.2	-103.4	-99.7

[33] The receiving sensitivity data of AG553Q-EU will be provided in a future version of the document.
[34] Test conditions for the receiving sensitivity of AG55xQ-EU:
- WCDMA bands: tested with 2 antennas (2Rx);
- 5G NR and LTE bands: tested with the maximum antenna capacity (2Rx/4Rx); see ***document [12]*** for more details.

[35] LTE-FDD B32, B29 and B30 supports Rx only, so the sensitivity of these bands is tested with CA combination, in which B32 and B29 are tested with 2 antennas (2Rx) and B30 with 4 antennas (4Rx).

LTE-TDD B40 (10 MHz)	-97.0	-97.3	-104	-99.7
LTE-TDD B41 (10 MHz)	-97.0	-97.2	-102.8	-97.7
LTE-TDD B42 (10 MHz)	-99.0	-100.1	-103.1	-98.7
C-V2X B47 (10 MHz) [31]	-96.8	-97.7	-	-90.4
5G NR FDD n1 (20 MHz)	-99.0	-100.0	-105.0	-99.5
5G NR FDD n3 (20 MHz)	-97.0	-100.0	-104.0	-96.5
5G NR FDD n8 (20 MHz)	-99.5	-100.0	-103.0	-90.2
5G NR FDD n20 (20 MHz)	-100	-100.5	-103.5	-89.8
5G NR FDD n28 (20 MHz)	-100.5	-100.0	-103.5	-90.8
5G NR TDD n41 (100 MHz)	-89	-88.5	-93.5	-87.4
5G NR TDD n78 (100 MHz)	-88.5	-88.5	-94	-87.8

Table 44: AG55xQ-NA RF Receiving Sensitivity

Frequency Band	Receiving Sensitivity (Typical Value) (dBm)			
	Primary	Diversity	SIMO [36]	3GPP (SIMO)
PCS1900	-108.9	-	-	-102
LTE-FDD B2 (10 MHz)	-98.7	-100.2	-104.4	-97.7
LTE-FDD B4 (10 MHz)	-99.3	-99.6	-104.3	-99.7
LTE-TDD B5 (10 MHz)	-101.1	-102.2	-99.8	-94.3
LTE-FDD B7 (10 MHz)	-98.8	-100	-104.2	-97.7
LTE-FDD B12 (10 MHz)	-100.7	-102.4	-103	-93.3
LTE-FDD B13 (5 MHz)	-101.8	-102.7	-103.2	-96.3
LTE-FDD B14 (10 MHz)	-101.5	-102.3	-103.2	-93.3
LTE-FDD B17 (10 MHz)	-100.9	-102.5	-103	-93.3
LTE-FDD B25 (10 MHz)	-98.4	-100.52	-105.5	-96.3

[36] Test conditions for the receiving sensitivity of AG55xQ-EU:
5G NR and LTE bands: tested with the maximum antenna capacity (2Rx/4Rx); see ***document [12]*** for more details.

LTE-FDD B26 (10 MHz)	-100.5	-102.2	-104.5	-93.8
LTE-FDD B28 (10 MHz)	-101	-102	-104	-93.8
LTE-FDD B29 (10 MHz) [35]	-	-	-103.7	-93.3
LTE-FDD B30 (10 MHz) [35]	-	-	-104.4	-98
LTE-FDD B66 (10 MHz)	-99	-100.8	-104.6	-99.3
LTE-FDD B71 (10 MHz)	-101.4	-102.5	-104.8	-93.5
LTE-TDD B41 (10 MHz)	-98.5	-99.3	-103.1	-97.7
C-V2X B47 (10 MHz) [31]	-96.8	-97.7	-	-90.4
LTE-TDD B48 (10 MHz)	-98.5	-99.6	-104.1	-95
5G NR FDD n2 (20 MHz)	-97.5	-100.5	-104	-97.5
5G NR FDD n5 (20 MHz)	-100	-103	-103	-90.8
5G NR FDD n25 (20 MHz)	-97.5	-100	-104	-96
5G NR FDD n66 (20 MHz)	-98.5	-100.5	-104.5	-99
5G NR FDD n71 (20 MHz)	-100	-103.5	-103.5	-86
5G NR TDD n41 (100 MHz)	-89	-88.5	-93.5	-87.4
5G NR TDD n48 (20 MHz)	-95.5	-96	-101	-95.1
5G NR TDD n77 (100 MHz)	-88	-88	-93.5	-87.3
5G NR TDD n78 (100 MHz)	-88.5	-89	-94.5	-87.8

NOTE

1. GSM sensitivity values meet *3GPP TS 51.010-1* requirements.
2. WCDMA sensitivity values meet *3GPP TS 34.121-1* requirements.
3. LTE sensitivity values meet *3GPP TS 36.521-1* requirements and it is tested under BW = 10 MHz according to 3GPP 1 RB configuration.
4. 5G NR sensitivity values meet *3GPP TS 38.521-1* requirements, FDD test @ SCS 15 kHz, TDD test @ SCS 30 kHz.

5.1.5. Reference Design

A reference design of main and Rx-diversity antenna interfaces is shown as below. It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (R1/C1/C2 and R2/C3/C4) should be placed as close to the antennas as possible. The capacitors are not mounted by default.

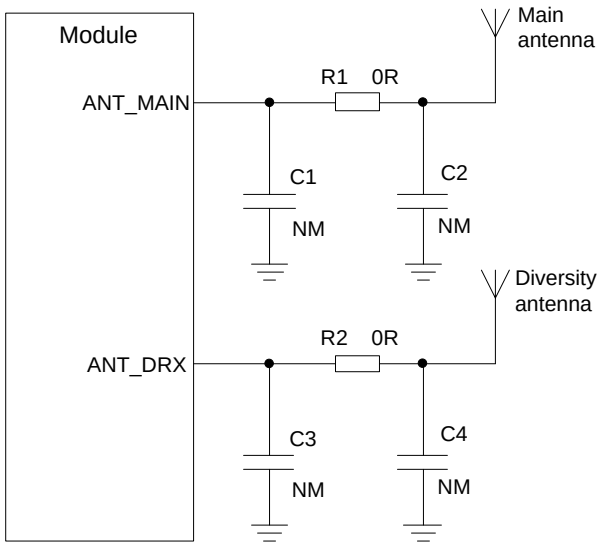


Figure 38: Reference Design of Main and Rx-diversity Antenna Interfaces

NOTE

1. The reference design of MIMO, DSDA and C-V2X antenna interfaces are the same as that of main antenna interface.
2. Keep a proper distance between each antenna to improve receiving sensitivity.

5.2. GNSS Antenna Interface (Optional)

The module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, Galileo and QZSS, and supports L1 + L5/L1 + L2* dual-frequency positioning.

The module supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1–10 Hz (1 Hz by default) data update rate via USB interface.
By default, GNSS engine of the module is switched off. It has to be switched on via an API function. For more details about GNSS engine technology and configurations, see ***document [11]***.

5.2.1. Pin Definition

The following tables show the pin definition of GNSS antenna interface.

Table 45: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	426	AI	GNSS antenna interface	50 Ω impedance. Support active antenna only.

5.2.2. Operating Frequency

Table 46: GNSS Operating Frequency

Type	Frequency Band	Unit
GPS L1	1575.42 ±1.023 (L1) 1176.45 ±10.23 (L5)	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BDS	1561.098 ±2.046	MHz
QZSS	1575.42 (L1) 1176.45 (L5)	MHz

5.2.3. GNSS Performance

The following table shows GNSS performance of the module.

Table 47: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity	Cold start	Autonomous	-150	dBm
	Reacquisition	Autonomous	-161	dBm
	Tracking	Autonomous	-158	dBm
TTFF	Cold start	Autonomous	30.13	s

	@ open sky	XTRA enabled	11.59	s
	Warm start @ open sky	Autonomous	23.69	s
		XTRA enabled	0.81	s
	Hot start @ open sky	Autonomous	0.9	s
		XTRA enabled	0.8	s
Accuracy	CEP-50	Autonomous @ open sky	1.5	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (the module lost lock 3 times in 5 minutes for 10 seconds each time).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 5 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.
4. The above GNSS performance test data is measured under single-frequency L1.

5.2.4. Reference Design

A reference design of GNSS antenna is shown as below.

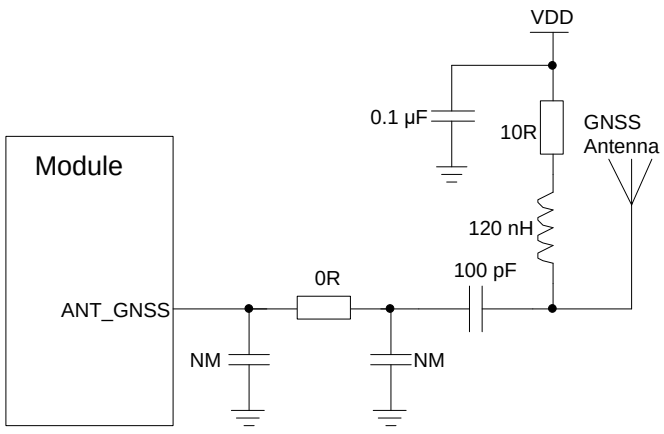


Figure 39: Reference Circuit of GNSS Antenna

NOTE

1. GNSS is an optional function. If it is not used, keep ANT_GNSS open.
2. An external LDO can be selected to supply power according to the active antenna requirement.

The following layout guidelines should be taken into account in application design.

- Maximize the distance among GNSS antenna, main antenna, Rx-diversity antenna, DSDA antenna, C-V2X antennas.
- Digital circuits such as (U)SIM card, USB interface, camera module, display connector, SD card and eMMC should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Control the characteristic impedance for ANT_GNSS trace as 50 Ω.
- Select an external active antenna, since there is no LNA inside the module. The optimal value of the gain of the external active antenna minus the loss of RF cable is 14–17 dB, otherwise the performance of GNSS positioning will be affected.

5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

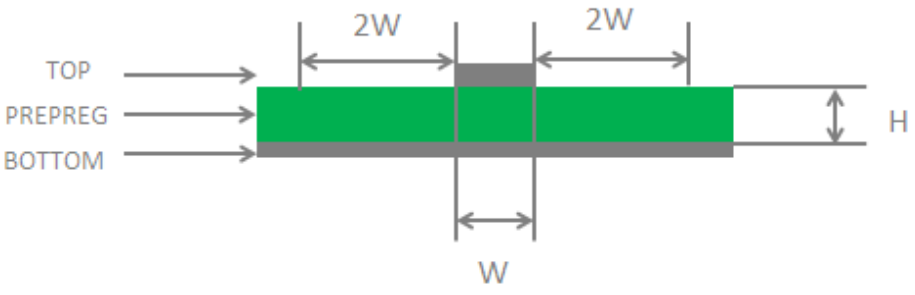


Figure 40: Microstrip Design on a 2-layer PCB

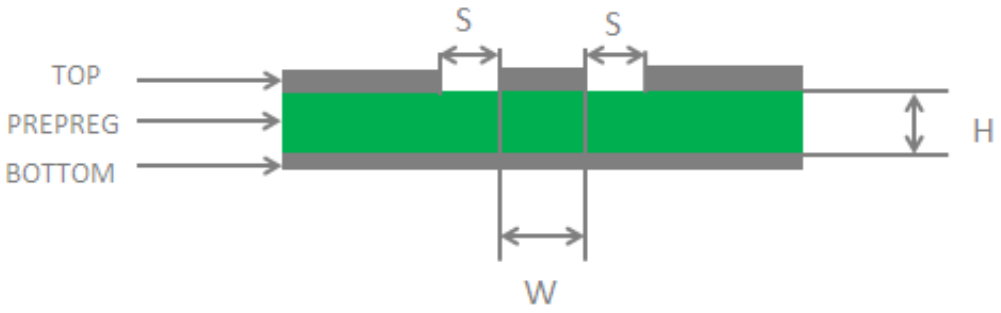


Figure 41: Coplanar Waveguide Design on a 2-layer PCB

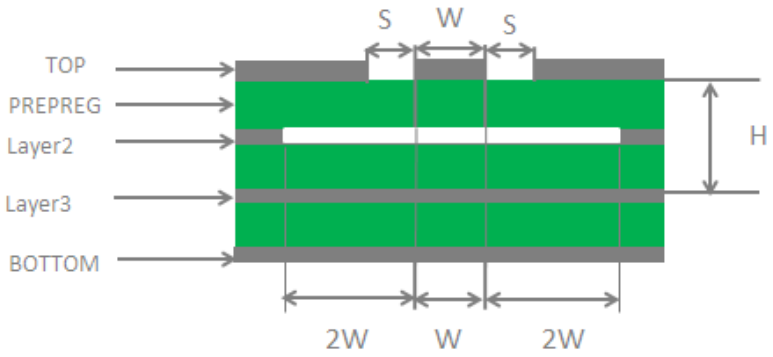


Figure 42: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

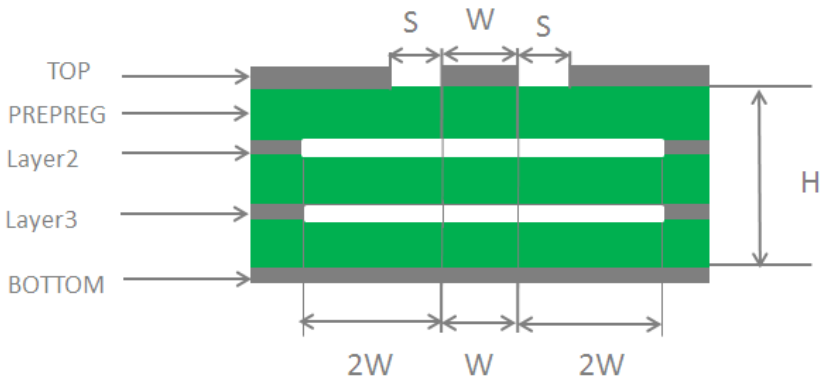


Figure 43: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice as wide as RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [13]***.

5.4. Antenna Design Requirements

The following table shows the requirements on RF antenna design.

Table 48: Antenna Design Requirements

Type	Requirements
GNSS	Frequency range: L1: 1559–1609 MHz L5: 1166–1187 MHz Polarization: RHCP or linear VSWR: ≤ 2 (Typ.) Active antenna noise figure: < 1.5 dB Active antenna gain: > 0 dBi Active antenna embedded LNA gain: < 17 dB
5G NR/LTE/WCDMA/GSM	VSWR: ≤ 2 Efficiency: > 30 % Max input power: 50 W Input impedance: 50 Ω Cable insertion loss: **< 1 dB:** LB (< 1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)
C-V2X	Frequency range: 5855–5925 MHz

	Gain: Min. 4 dBi VSWR: ≤ 2 Efficiency: > 30 % Max input power: 10 W Recommend antenna pattern: ±10–15° (Azimuth Beamwidth: 360°; Elevation Beamwidth: ±10–15°) Input impedance: 50 Ω Cable insertion loss: **< 2 dB:** C-V2X TDD B47

NOTE

It is recommended to add a 25 dB notch filter at the LNA input end of the active antenna when LTE B13 or B14 is supported.

5.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the HFM connector provided by *Rosenberger*.

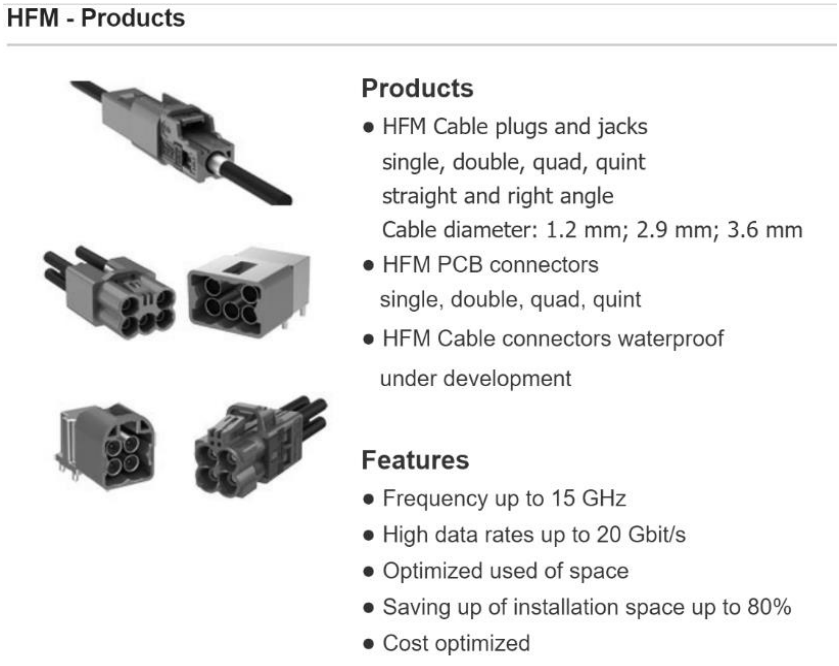


Figure 44: Feature of the HFM Connector

For more details, visit https://www.rosenbergerap.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 49: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
VBAT_CV2X	-0.5	5.5	V
USB_VBUS	-0.3	5.5	V
Voltage at Digital Pins	-0.3	2.13	V
Voltage at ADC0	0	4.8	V
Voltage at ADC1	0	4.8	V

6.2. Power Supply Ratings

Table 50: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT_BB, VBAT_RF	VBAT_BB and VBAT_RF	The actual input voltages must stay between the	3.3	3.8	4.3	V

		minimum and maximum values.				
	Voltage drop during burst transmission	Maximum transmitted power on EGSM900.	-	-	400	mV
	Voltage drop during peak data rate	Peak DL data rate on EN-DC	-	-	400	mV
VBAT_CV2X	Power supply for the module's C-V2X part	The actual input voltages must stay between the minimum and maximum values.	4.75	5.0	5.25	V
I_{VBAT_BB}, I_{VBAT_RF}	Peak supply current (5G + C-V2X)	-	-	-	3.0	A
	Peak supply current (5G + C-V2X + DSDA)	-	-	-	4.5	A
I_{VBAT_CV2X}	Peak supply current	-	-	-	1.6	A
USB_VBUS	USB connection detection	-	3.0	5.0	5.25	V
VDD_EXT	Provide 1.8 V for external circuits	-	-	1.8		V
			-	-	50	mA
VDD_WIFI_VL	0.95 V low-voltage power supply for Wi-Fi & Bluetooth modules	-	0.824	-	1.05	V
			-	-	1.7	A
VDD_WIFI_VM	1.35 V medium-voltage power supply for Wi-Fi & Bluetooth modules	-	1.224	-	1.35	V
			-	-	0.4	A
VDD_WIFI_VH	1.95 V high-voltage power supply for Wi-Fi & Bluetooth modules	-	1.8	-	2.0	V
			-	-	0.4	A
USIM_VDD	(U)SIM card power supply	1.8 V application	1.65	1.8	1.95	V
		3.0 V application	2.7	2.95	3.05	V
SDIO_VDD	Power supply input for SDIO	1.8 V application	1.65	1.8	1.95	V
		3.0 V application	2.7	2.95	3.05	V
RGMII_PWR_IN	RGMII interface power input	1.8 V application	1.7	1.8	1.94	V
		2.5 V application	2.31	2.5	2.69	V

6.3. Power Consumption

6.3.1. AG550Q-CN Power Consumption

Table 51: AG550Q-CN Power Consumption (25 °C, 3.8 V Power Supply)

Test Mode	Test Condition	Typ.	Unit
OFF state	Power down	20	μA
Sleep state	**AT+CFUN=0** (USB Disconnected)	1.01	mA
	AT+CFUN=4 (USB Disconnected)	1.06	mA
	EGSM900 @ DRX = 2	3.19	mA
	EGSM900 @ DRX = 5	2.00	mA
	EGSM900 @ DRX = 5 (USB Suspend)	4.57	mA
	EGSM900 @ DRX = 9	1.97	mA
	DCS1800 @ DRX = 2	3.11	mA
	DCS1800 @ DRX = 5	1.93	mA
	DCS1800 @ DRX = 5 (USB Suspend)	4.55	mA
	DCS1800 @ DRX = 9	1.91	mA
	WCDMA @ DRX = 0.64 s	2.39	mA
	WCDMA @ DRX = 0.64 s (USB Suspend)	5.29	mA
	WCDMA @ DRX = 1.28 s	1.78	mA
	WCDMA @ DRX = 2.56 s	1.74	mA
	WCDMA @ DRX = 5.12 s	1.49	mA
	LTE-FDD @ DRX = 0.32 s	4.34	mA
	LTE-FDD @ DRX = 0.64 s	2.75	mA
	LTE-FDD @ DRX = 0.64 s (USB Suspend)	5.66	mA
	LTE-FDD @ DRX = 1.28 s	1.96	mA
	LTE-FDD @ DRX = 2.56 s	1.85	mA

	LTE-TDD @ DRX = 0.32 s	4.49	mA
	LTE-TDD @ DRX = 0.64 s	2.88	mA
	LTE-TDD @ DRX = 0.64 s (USB Suspend)	5.68	mA
	LTE-TDD @ DRX = 1.28 s	1.99	mA
	LTE-TDD @ DRX = 2.56 s	1.86	mA
	5G NR FDD @ DRX = 0.32 s	11.15	mA
	5G NR FDD @ DRX = 0.64 s	6.03	mA
	5G NR FDD @ DRX = 0.64 s (USB Suspend)	8.73	mA
	5G NR FDD @ DRX = 1.28 s	3.49	mA
	5G NR FDD @ DRX = 2.56 s	2.54	mA
	5G NR TDD @ DRX = 0.32 s	11.55	mA
	5G NR TDD @ DRX = 0.64 s	6.22	mA
	5G NR TDD @ DRX = 0.64 s (USB Suspend)	8.90	mA
	5G NR TDD @ DRX = 1.28 s	3.57	mA
	5G NR TDD @ DRX = 2.56 s	2.69	mA
Idle state	EGSM900 CH62 @ DRX = 5	15.84	mA
	EGSM900 CH62 @ DRX = 5 (USB Active)	45.15	mA
	WCDMA @ DRX = 0.64 s	15.81	mA
	WCDMA @ DRX = 0.64 s (USB Active)	45.65	mA
	LTE-FDD @ DRX = 0.64 s	16.68	mA
	LTE-FDD @ DRX = 0.64 s (USB Active)	45.96	mA
	LTE-TDD @ DRX = 0.64 s	15.99	mA
	LTE-TDD @ DRX = 0.64 s (USB Active)	45.92	mA
	5G NR FDD @ DRX = 0.64 s	18.77	mA
	5G NR FDD @ DRX = 0.64 s (USB Active)	48.29	mA
	5G NR TDD @ DRX = 0.64 s	19.02	mA

	5G NR TDD @ DRX = 0.64 s (USB Active)	48.39	mA
WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA CH10562 @ 22.55 dBm	565.35	mA
	WCDMA B1 HSUPA CH10562 @ 22.51 dBm	567.95	mA
	WCDMA B1 HSDPA CH10700 @ 22.56 dBm	507.64	mA
	WCDMA B1 HSUPA CH10700 @ 22.54 dBm	513.96	mA
	WCDMA B1 HSDPA CH10838 @ 22.50 dBm	522.46	mA
	WCDMA B1 HSUPA CH10838 @ 22.43 dBm	522.78	mA
	WCDMA B8 HSDPA CH2937 @ 22.07 dBm	444.03	mA
	WCDMA B8 HSUPA CH2937 @ 22.09 dBm	449.16	mA
	WCDMA B8 HSDPA CH3012 @ 22.15 dBm	412.22	mA
	WCDMA B8 HSUPA CH3012 @ 22.09 dBm	449.89	mA
	WCDMA B8 HSDPA CH3088 @ 22.07 dBm	431.88	mA
	WCDMA B8 HSUPA CH3088 @ 22.08 dBm	432.53	mA
LTE data transfer (GNSS OFF, max power)	LTE-FDD B1 CH18100 @ 23.15 dBm	700.69	mA
	LTE-FDD B1 CH18300 @ 23.19 dBm	631.13	mA
	LTE-FDD B1 CH18500 @ 23.20 dBm	698.33	mA
	LTE-FDD B3 CH19300 @ 23.29 dBm	737.95	mA
	LTE-FDD B3 CH19575 @ 23.33 dBm	730.20	mA
	LTE-FDD B3 CH19850 @ 23.39 dBm	737.47	mA
	LTE-FDD B5 CH20450 @ 23.58 dBm	513.91	mA
	LTE-FDD B5 CH20525 @ 23.64 dBm	490.66	mA
	LTE-FDD B5 CH20600 @ 23.60 dBm	506.26	mA
	LTE-FDD B7 CH20850 @ 23.34 dBm	660.26	mA
	LTE-FDD B7 CH21100 @ 23.12 dBm	610.87	mA
	LTE-FDD B7 CH21350 @ 23.11 dBm	640.43	mA
	LTE-FDD B8 CH21500 @ 23.65 dBm	523.75	mA

	LTE-FDD B8 CH21625 @ 23.58 dBm	492.32	mA
	LTE-FDD B8 CH21750 @ 23.60 dBm	493.39	mA
	LTE-TDD B34 CH36275 @ 22.31 dBm	248.78	mA
	LTE-TDD B38 CH37850 @ 23.23 dBm	380.89	mA
	LTE-TDD B38 CH38000 @ 23.14 dBm	348.21	mA
	LTE-TDD B38 CH38150 @ 23.09 dBm	354.08	mA
	LTE-TDD B39 CH38350 @ 23.28 dBm	338.23	mA
	LTE-TDD B39 CH38450 @ 23.25 dBm	314.05	mA
	LTE-TDD B39 CH38550 @ 23.27 dBm	302.97	mA
	LTE-TDD B40 CH38750 @ 23.15 dBm	318.89	mA
	LTE-TDD B40 CH39150 @ 23.09 dBm	341.15	mA
	LTE-TDD B40 CH39550 @ 23.10 dBm	305.21	mA
	LTE-TDD B41 CH39750 @ 23.01 dBm	344.92	mA
	LTE-TDD B41 CH40620 @ 23.00 dBm	320.56	mA
	LTE-TDD B41 CH41490 @ 22.74 dBm	335.13	mA
WCDMA voice call	WCDMA B1 CH10562 @ 23.05 dBm	589.07	mA
	WCDMA B1 CH10700 @ 23.03 dBm	519.33	mA
	WCDMA B1 CH10838 @ 22.96 dBm	536.99	mA
	WCDMA B8 CH2937 @ 23.10 dBm	481.23	mA
	WCDMA B8 CH3012 @ 23.10 dBm	433.70	mA
	WCDMA B8 CH3088 @ 23.05 dBm	465.20	mA
LTE data transfer (GNSS OFF, max. throughput)	LTE-FDD B1 CH300 @ 20.81 dBm	535.42	mA
	LTE-FDD B3 CH1575 @ 21.08 dBm	563.04	mA
	LTE-FDD B5 CH2525 @ 22.15 dBm	452.63	mA
	LTE-FDD B7 CH3100 @ 20.75 dBm	534.93	mA
	LTE-FDD B8 CH3625 @ 21.35 dBm	404.56	mA

	LTE-FDD B34 CH36275 @ 20.07 dBm	281.48	mA
	LTE-TDD B38 CH38000 @ 20.74 dBm	381.26	mA
	LTE-TDD B39 CH38450 @ 20.97 dBm	334.91	mA
	LTE-TDD B40 CH39150 @ 20.47 dBm	344.38	mA
	LTE-TDD B41 CH40620 @ 20.41 dBm	359.10	mA
GSM voice call	EGSM900 CH1 PCL = 5 @ 32.39 dBm	348.20	mA
	EGSM900 CH62 PCL = 5 @ 32.62 dBm	324.40	mA
	EGSM900 CH62 PCL = 12 @ 18.64 dBm	97.20	mA
	EGSM900 CH62 PCL = 19 @ 4.64 dBm	82.90	mA
	EGSM900 CH124 PCL = 5 @ 32.54 dBm	321.40	mA
	DCS1800 CH512 PCL = 0 @ 29.91 dBm	215.20	mA
	DCS1800 CH698 PCL = 0 @ 30.13 dBm	215.30	mA
	DCS1800 CH698 PCL = 7 @ 16.15 dBm	89.80	mA
	DCS1800 CH698 PCL = 15 @ 0.58 dBm	82.90	mA
	DCS1800 CH885 PCL = 0 @ 30.06 dBm	213.70	mA
GPRS data transfer (GNSS OFF)	EGSM900 CH1 1DL/4UL @ 29.07 dBm	637.20	mA
	EGSM900 CH62 4DL/1UL @ 32.37 dBm	331.70	mA
	EGSM900 CH62 3DL/2UL @ 31.65 dBm	509.90	mA
	EGSM900 CH62 2DL/3UL @ 29.58 dBm	549.70	mA
	EGSM900 CH62 1DL/4UL @ 28.43 dBm	625.10	mA
	EGSM900 CH124 1DL/4UL @ 28.26 dBm	619.90	mA
	DCS1800 CH512 1DL/4UL @ 26.92 dBm	453.90	mA
	DCS1800 CH698 4DL/1UL @ 30.31 dBm	214.60	mA
	DCS1800 CH698 3DL/2UL @ 30.26 dBm	360.50	mA
	DCS1800 CH698 2DL/3UL @ 28.12 dBm	400.90	mA
	DCS1800 CH698 1DL/4UL @ 27.16 dBm	465.50	mA

	DCS1800 CH885 1DL/4UL @ 26.94 dBm	455.80	mA
EDGE data transfer (GNSS OFF)	EGSM900 CH1 1DL/4UL @ 23.27 dBm	391.00	mA
	EGSM900 CH62 4DL/1UL @ 26.65 dBm	206.50	mA
	EGSM900 CH62 3DL/2UL @ 26.59 dBm	299.70	mA
	EGSM900 CH62 2DL/3UL @ 24.46 dBm	319.00	mA
	EGSM900 CH62 1DL/4UL @ 23.31 dBm	365.90	mA
	EGSM900 CH124 1DL/4UL @ 23.36 dBm	371.40	mA
	DCS1800 CH512 1DL/4UL @ 23.05 dBm	310.60	mA
	DCS1800 CH698 4DL/1UL @ 26.11 dBm	148.30	mA
	DCS1800 CH698 3DL/2UL @ 26.02 dBm	234.60	mA
	DCS1800 CH698 2DL/3UL @ 24.02 dBm	267.90	mA
	DCS1800 CH698 1DL/4UL @ 23.10 dBm	311.00	mA
	DCS1800 CH885 1DL/4UL @ 23.03 dBm	309.30	mA
5G SA data transfer (GNSS OFF)	n41A CH509202 @ 25.79 dBm	410.97	mA
	n41A CH518598 @ 26.01 dBm	415.76	mA
	n41A CH528000 @ 26.03 dBm	466.19	mA
	n78A CH623334 @ 25.79 dBm	410.79	mA
	n78A CH636666 @ 25.98 dBm	426.68	mA
	n78A CH650000 @ 26.01 dBm	409.30	mA
	n79A CH697094 @ 25.13 dBm	423.42	mA
	n79A CH713990 @ 26.31 dBm	459.48	mA
	n79A CH729468 @ 26.20 dBm	453.91	mA
	n1A CH426000 @ 23.20 dBm	708.15	mA
	n1A CH428000 @ 23.49 dBm	706.57	mA
	n1A CH430000 @ 23.46 dBm	716.22	mA
	n3A CH364000 @ 23.42 dBm	625.58	mA

	n3A CH368500 @ 23.31 dBm	607.94	mA
	n3A CH373000 @ 23.38 dBm	644.66	mA
	n28A CH154600 @ 23.48 dBm	497.17	mA
	n28A CH156100 @ 23.52 dBm	532.84	mA
	n28A CH157600 @ 23.56 dBm	467.06	mA
5G NSA data transfer (GNSS OFF)	3A_n41A CH509202 @ 25.97 dBm	1084.00	mA
	3A_n41A CH518598 @ 25.82 dBm	1086.00	mA
	3A_n41A CH528000 @ 25.72 dBm	1088.00	mA
	3A_n78A CH623334 @ 25.62 dBm	1010.00	mA
	3A_n78A CH636666 @ 25.90 dBm	1015.00	mA
	3A_n78A CH650000 @ 25.91 dBm	1009.00	mA
	3A_n79A CH697094 @ 23.56 dBm	870.67	mA
	3A_n79A CH713990 @ 23.73 dBm	864.48	mA
	3A_n79A CH729468 @ 23.66 dBm	865.31	mA
	39A_n41A CH509202 @ 26.52 dBm	673.32	mA
	39A_n41A CH518598 @ 26.47 dBm	674.46	mA
	39A_n41A CH528000 @ 26.56 dBm	699.83	mA
	8A_n41A CH509202 @ 23.60 dBm	662.83	mA
	8A_n41A CH518598 @ 23.71 dBm	664.44	mA
	8A_n41A CH528000 @ 23.74 dBm	682.92	mA
	1A_n78A CH623334 @ 23.45 dBm	787.10	mA
	1A_n78A CH636666 @ 23.46 dBm	797.87	mA
	1A_n78A CH650000 @ 23.60 dBm	791.08	mA
	5A_n78A CH623334 @ 23.88 dBm	673.61	mA
	5A_n78A CH636666 @ 23.64 dBm	678.25	mA
	5A_n78A CH650000 @ 23.74 dBm	675.11	mA

	1A_n79A CH697094 @ 23.60 dBm	820.97	mA
	1A_n79A CH713990 @ 23.63 dBm	817.81	mA
	1A_n79A CH729468 @ 23.65 dBm	823.63	mA
	38A_n78A CH623334 @ 23.43 dBm	588.05	mA
	38A_n78A CH636666 @ 23.54 dBm	595.16	mA
	38A_n78A CH650000 @ 23.43 dBm	590.28	mA
	39A_n79A CH697094 @ 26.54 dBm	715.66	mA
	39A_n79A CH713990 @ 26.60 dBm	712.76	mA
	39A_n79A CH729468 @ 26.53 dBm	713.59	mA
	40A_n41A CH509202 @ 23.58 dBm	543.65	mA
	40A_n41A CH518598 @ 23.55 dBm	544.04	mA
	40A_n41A CH528000 @ 23.60 dBm	561.54	mA
	40A_n78A CH623334 @ 23.51 dBm	587.20	mA
	40A_n78A CH636666 @ 23.49 dBm	586.92	mA
	40A_n78A CH650000 @ 23.39 dBm	580.83	mA
	41A_n79A CH697094 @ 26.47 dBm	720.59	mA
	41A_n79A CH713990 @ 26.56 dBm	720.35	mA
	41A_n79A CH729468 @ 26.50 dBm	737.11	mA
	5A_n41A CH509202 @ 23.68 dBm	658.25	mA
	5A_n41A CH518598 @ 23.73 dBm	658.95	mA
	5A_n41A CH528000 @ 23.79 dBm	677.01	mA
	7A_n78A CH623334 @ 23.53 dBm	783.31	mA
	7A_n78A CH636666 @ 23.37 dBm	787.52	mA
	7A_n78A CH650000 @ 23.49 dBm	780.64	mA
	8A_n78A CH623334 @ 23.64 dBm	679.07	mA
	8A_n78A CH636666 @ 23.66 dBm	683.93	mA

	8A_n78A CH650000 @ 23.65 dBm	679.19	mA

6.3.2. AG551Q-CN Power Consumption

Table 52: AG551Q-CN Power Consumption (25 °C, 3.8 V Power Supply)

Test Mode	Test Condition	Typ.	Unit
OFF state	Power down	20	μA
Sleep state	**AT+CFUN=0** (USB Disconnected)	1.23	mA
	AT+CFUN=4 (USB Disconnected)	1.34	mA
	EGSM900 @ DRX = 2	3.58	mA
	EGSM900 @ DRX = 5	2.36	mA
	EGSM900 @ DRX = 5 (USB Suspend)	5.61	mA
	EGSM900 @ DRX = 9	2.28	mA
	DCS1800 @ DRX = 2	3.90	mA
	DCS1800 @ DRX = 5	2.79	mA
	DCS1800 @ DRX = 5 (USB Suspend)	4.95	mA
	DCS1800 @ DRX = 9	2.13	mA
	WCDMA @ DRX = 0.64 s	2.93	mA
	WCDMA @ DRX = 0.64 s (USB Suspend)	6.31	mA
	WCDMA @ DRX = 1.28 s	2.27	mA
	WCDMA @ DRX = 2.56 s	2.04	mA
	WCDMA @ DRX = 5.12 s	1.78	mA
	LTE-FDD @ DRX = 0.32 s	4.99	mA
	LTE-FDD @ DRX = 0.64 s	3.34	mA
	LTE-FDD @ DRX = 0.64 s (USB Suspend)	6.69	mA
	LTE-FDD @ DRX = 1.28 s	2.41	mA
	LTE-FDD @ DRX = 2.56 s	2.29	mA

	LTE-TDD @ DRX = 0.32 s	5.15	mA
	LTE-TDD @ DRX = 0.64 s	3.48	mA
	LTE-TDD @ DRX = 0.64 s (USB Suspend)	6.71	mA
	LTE-TDD @ DRX = 1.28 s	2.52	mA
	LTE-TDD @ DRX = 2.56 s	2.32	mA
	5G NR FDD @ DRX = 0.32 s	13.06	mA
	5G NR FDD @ DRX = 0.64 s	7.21	mA
	5G NR FDD @ DRX = 0.64 s (USB Suspend)	10.45	mA
	5G NR FDD @ DRX = 1.28 s	4.30	mA
	5G NR FDD @ DRX = 2.56 s	3.16	mA
	5G NR TDD @ DRX = 0.32 s	13.42	mA
	5G NR TDD @ DRX = 0.64 s	7.36	mA
	5G NR TDD @ DRX = 0.64 s (USB Suspend)	10.79	mA
	5G NR TDD @ DRX = 1.28 s	4.48	mA
	5G NR TDD @ DRX = 2.56 s	4.01	mA
Idle state	EGSM900 CH62 @ DRX = 5	16.957	mA
	EGSM900 CH62 @ DRX = 5 (USB Active)	47.697	mA
	WCDMA @ DRX = 0.64 s	17.22	mA
	WCDMA @ DRX = 0.64 s (USB Active)	48.30	mA
	LTE-FDD @ DRX = 0.64 s	17.82	mA
	LTE-FDD @ DRX = 0.64 s (USB Active)	48.67	mA
	LTE-TDD @ DRX = 0.64 s	17.99	mA
	LTE-TDD @ DRX = 0.64 s (USB Active)	48.69	mA
	5G NR FDD @ DRX = 0.64 s	20.49	mA
	5G NR FDD @ DRX = 0.64 s (USB Active)	51.78	mA
	5G NR TDD @ DRX = 0.64 s	21.66	mA

	5G NR TDD @ DRX = 0.64 s (USB Active)	52.51	mA
WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA CH10562 @ 22.60 dBm	563.29	mA
	WCDMA B1 HSUPA CH10562 @ 22.59 dBm	563.92	mA
	WCDMA B1 HSDPA CH10700 @ 22.54 dBm	469.13	mA
	WCDMA B1 HSUPA CH10700 @ 22.55 dBm	476.21	mA
	WCDMA B1 HSDPA CH10838 @ 22.51 dBm	503.01	mA
	WCDMA B1 HSUPA CH10838 @ 22.57 dBm	507.48	mA
	WCDMA B8 HSDPA CH2937 @ 22.34 dBm	464.87	mA
	WCDMA B8 HSUPA CH2937 @ 22.37 dBm	467.04	mA
	WCDMA B8 HSDPA CH3012 @ 22.14 dBm	433.04	mA
	WCDMA B8 HSUPA CH3012 @ 22.44 dBm	433.76	mA
	WCDMA B8 HSDPA CH3088 @ 22.33 dBm	456.47	mA
	WCDMA B8 HSUPA CH3088 @ 22.35 dBm	455.54	mA
LTE data transfer (GNSS OFF)	LTE-FDD B1 CH18100 @ 23.12 dBm	736.00	mA
	LTE-FDD B1 CH18300 @ 23.22 dBm	682.81	mA
	LTE-FDD B1 CH18500 @ 23.05 dBm	643.14	mA
	LTE-FDD B3 CH19300 @ 23.22 dBm	760.99	mA
	LTE-FDD B3 CH19575 @ 23.25 dBm	733.38	mA
	LTE-FDD B3 CH19850 @ 23.19 dBm	742.74	mA
	LTE-FDD B5 CH20450 @ 23.93 dBm	549.74	mA
	LTE-FDD B5 CH20525 @ 23.97 dBm	527.67	mA
	LTE-FDD B5 CH20600 @ 23.95 dBm	543.46	mA
	LTE-FDD B7 CH20850 @ 23.07 dBm	678.76	mA
	LTE-FDD B7 CH21100 @ 23.06 dBm	630.87	mA
	LTE-FDD B7 CH21350 @ 23.08 dBm	678.95	mA
	LTE-FDD B8 CH21500 @ 23.80 dBm	557.21	mA

	LTE-FDD B8 CH21625 @ 23.83 dBm	519.70	mA
	LTE-FDD B8 CH21750 @ 23.83 dBm	528.07	mA
	LTE-TDD B34 CH36275 @ 22.10 dBm	254.58	mA
	LTE-TDD B38 CH37850 @ 23.10 dBm	348.17	mA
	LTE-TDD B38 CH38000 @ 23.07 dBm	351.28	mA
	LTE-TDD B38 CH38150 @ 23.05 dBm	360.54	mA
	LTE-TDD B39 CH38350 @ 23.26 dBm	344.79	mA
	LTE-TDD B39 CH38450 @ 23.26 dBm	324.09	mA
	LTE-TDD B39 CH38550 @ 23.32 dBm	314.73	mA
	LTE-TDD B40 CH38750 @ 23.01 dBm	323.13	mA
	LTE-TDD B40 CH39150 @ 23.04 dBm	347.90	mA
	LTE-TDD B40 CH39550 @ 22.90 dBm	310.43	mA
	LTE-TDD B41 CH40140 @ 23.01 dBm	346.77	mA
	LTE-TDD B41 CH40620 @ 22.97 dBm	327.25	mA
	LTE-TDD B41 CH41490 @ 22.81 dBm	342.76	mA
WCDMA voice call	WCDMA B1 CH10562 @ 23.12 dBm	564.91	mA
	WCDMA B1 CH10700 @ 23.13 dBm	476.48	mA
	WCDMA B1 CH10838 @ 23.00 dBm	506.32	mA
	WCDMA B8 CH2937 @ 23.39 dBm	499.94	mA
	WCDMA B8 CH3012 @ 23.40 dBm	457.99	mA
	WCDMA B8 CH3088 @ 23.32 dBm	488.18	mA
LTE Max. data rate	LTE-FDD B1 CH300 @ 20.89 dBm	588.19	mA
	LTE-FDD B3 CH1575 @ 20.83 dBm	611.87	mA
	LTE-FDD B5 CH2525 @ 22.01 dBm	504.27	mA
	LTE-FDD B7 CH3100 @ 20.42 dBm	585.76	mA
	LTE-FDD B8 CH3625 @ 21.75 dBm	486.51	mA

	LTE-FDD B34 CH36275 @ 19.70 dBm	300.60	mA
	LTE-TDD B38 CH38000 @ 20.53 dBm	396.28	mA
	LTE-TDD B39 CH38450 @ 20.84 dBm	361.19	mA
	LTE-TDD B40 CH39150 @ 20.44 dBm	374.00	mA
	LTE-TDD B41 CH40620 @ 20.52 dBm	373.86	mA
GSM voice call	EGSM900 CH1 PCL = 5 @ 32.46 dBm	348.70	mA
	EGSM900 CH62 PCL = 5 @ 32.69 dBm	326.00	mA
	EGSM900 CH62 PCL = 12 @ 18.27 dBm	103.40	mA
	EGSM900 CH62 PCL = 19 @ 4.10 dBm	89.80	mA
	EGSM900 CH124 PCL = 5 @ 32.49 dBm	319.20	mA
	DCS1800 CH512 PCL = 0 @ 29.25 dBm	220.80	mA
	DCS1800 CH698 PCL = 0 @ 29.47 dBm	221.30	mA
	DCS1800 CH698 PCL = 7 @ 15.59 dBm	96.30	mA
	DCS1800 CH698 PCL = 15 @ -0.09 dBm	89.70	mA
	DCS1800 CH885 PCL = 0 @ 29.32 dBm	218.50	mA
GPRS data transfer (GNSS OFF)	EGSM900 CH1 1DL/4UL @ 28.34 dBm	610.50	mA
	EGSM900 CH62 4DL/1UL @ 32.39 dBm	307.90	mA
	EGSM900 CH62 3DL/2UL @ 31.58 dBm	493.30	mA
	EGSM900 CH62 2DL/3UL @ 29.64 dBm	560.10	mA
	EGSM900 CH62 1DL/4UL @ 28.47 dBm	631.90	mA
	EGSM900 CH124 1DL/4UL @ 28.47 dBm	640.20	mA
	DCS1800 CH512 1DL/4UL @ 26.19 dBm	466.00	mA
	DCS1800 CH698 4DL/1UL @ 29.64 dBm	219.50	mA
	DCS1800 CH698 3DL/2UL @ 29.45 dBm	365.70	mA
	DCS1800 CH698 2DL/3UL @ 27.29 dBm	407.90	mA
	DCS1800 CH698 1DL/4UL @ 26.40 dBm	475.70	mA

	DCS1800 CH885 1DL/4UL @ 26.20 dBm	468.50	mA
EDGE data transfer (GNSS OFF)	EGSM900 CH1 1DL/4UL @ 23.31 dBm	367.40	mA
	EGSM900 CH62 4DL/1UL @ 26.80 dBm	179.50	mA
	EGSM900 CH62 3DL/2UL @ 26.73 dBm	292.40	mA
	EGSM900 CH62 2DL/3UL @ 24.38 dBm	326.50	mA
	EGSM900 CH62 1DL/4UL @ 23.33 dBm	370.90	mA
	EGSM900 CH124 1DL/4UL @ 23.50 dBm	380.70	mA
	DCS1800 CH512 1DL/4UL @ 22.37 dBm	317.60	mA
	DCS1800 CH698 4DL/1UL @ 25.60 dBm	158.20	mA
	DCS1800 CH698 3DL/2UL @ 25.47 dBm	242.90	mA
	DCS1800 CH698 2DL/3UL @ 23.19 dBm	274.90	mA
	DCS1800 CH698 1DL/4UL @ 22.49 dBm	323.50	mA
	DCS1800 CH885 1DL/4UL @ 22.27 dBm	319.10	mA
5G SA data transfer (GNSS OFF)	n1A CH426000 @ 23.17 dBm	748.67	mA
	n1A CH428000 @ 23.36 dBm	713.44	mA
	n1A CH430000 @ 23.12 dBm	709.59	mA
	n3A CH364000 @ 23.11 dBm	631.41	mA
	n3A CH368500 @ 23.03 dBm	597.49	mA
	n3A CH373000 @ 23.12 dBm	636.27	mA
	n28A CH154600 @ 23.12 dBm	511.23	mA
	n28A CH156100 @ 23.20 dBm	536.64	mA
	n28A CH157600 @ 23.09 dBm	474.42	mA
	n41A CH509202 @ 25.76 dBm	433.70	mA
	n41A CH518598 @ 25.99 dBm	443.61	mA
	n41A CH528000 @ 25.97 dBm	464.22	mA
	n78A CH623334 @ 25.92 dBm	439.16	mA

	n78A CH636666 @ 25.77 dBm	432.50	mA
	n78A CH650000 @ 26.28 dBm	443.71	mA
	n79A CH697094 @ 25.33 dBm	458.08	mA
	n79A CH713990 @ 26.61 dBm	504.48	mA
	n79A CH729468 @ 26.51 dBm	480.16	mA
5G NSA data transfer (GNSS OFF)	1A_n78A CH623334 @ 23.16 dBm	843.05	mA
	1A_n78A CH636666 @ 22.95 dBm	839.34	mA
	1A_n78A CH650000 @ 23.28 dBm	844.31	mA
	1A_n79A CH697094 @ 23.03 dBm	878.65	mA
	1A_n79A CH713990 @ 23.39 dBm	876.76	mA
	1A_n79A CH729468 @ 23.24 dBm	871.32	mA
	3A_n41A CH509202 @ 25.84 dBm	1055.00	mA
	3A_n41A CH518598 @ 25.89 dBm	1075.00	mA
	3A_n41A CH528000 @ 25.82 dBm	1112.00	mA
	3A_n78A CH623334 @ 26.00 dBm	1022.00	mA
	3A_n78A CH636666 @ 25.84 dBm	1027.00	mA
	3A_n78A CH650000 @ 25.69 dBm	1043.00	mA
	3A_n79A CH697094 @ 22.97 dBm	910.92	mA
	3A_n79A CH713990 @ 23.36 dBm	907.49	mA
	3A_n79A CH729468 @ 23.20 dBm	901.36	mA
	38A_n78A CH623334 @ 23.24 dBm	610.53	mA
	38A_n78A CH636666 @ 22.96 dBm	602.35	mA
	38A_n78A CH650000 @ 23.24 dBm	609.23	mA
	39A_n41A CH509202 @ 25.63 dBm	657.25	mA
	39A_n41A CH518598 @ 25.76 dBm	666.04	mA
	39A_n41A CH528000 @ 25.78 dBm	700.65	mA

	39A_n79A CH697094 @ 25.82 dBm	718.54	mA
	39A_n79A CH713990 @ 26.21 dBm	739.05	mA
	39A_n79A CH729468 @ 26.11 dBm	713.77	mA
	40A_n41A CH509202 @ 23.23 dBm	567.54	mA
	40A_n41A CH518598 @ 22.98 dBm	562.67	mA
	40A_n41A CH528000 @ 22.85 dBm	577.74	mA
	40A_n78A CH623334 @ 23.31 dBm	608.57	mA
	40A_n78A CH636666 @ 22.82 dBm	599.67	mA
	40A_n78A CH650000 @ 23.13 dBm	603.64	mA
	41A_n79A CH697094 @ 25.98 dBm	729.88	mA
	41A_n79A CH713990 @ 26.30 dBm	736.98	mA
	41A_n79A CH729468 @ 26.16 dBm	722.86	mA
	5A_n41A CH509202 @ 22.84 dBm	680.01	mA
	5A_n41A CH518598 @ 22.92 dBm	681.85	mA
	5A_n41A CH528000 @ 23.00 dBm	698.82	mA
	5A_n78A CH623334 @ 23.16 dBm	705.01	mA
	5A_n78A CH636666 @ 22.96 dBm	702.12	mA
	5A_n78A CH650000 @ 23.24 dBm	704.42	mA
	7A_n78A CH623334 @ 23.36 dBm	823.19	mA
	7A_n78A CH636666 @ 22.98 dBm	818.05	mA
	7A_n78A CH650000 @ 23.28 dBm	820.91	mA
	8A_n41A CH509202 @ 22.90 dBm	675.54	mA
	8A_n41A CH518598 @ 23.06 dBm	685.01	mA
	8A_n41A CH528000 @ 23.01 dBm	702.43	mA
	8A_n78A CH623334 @ 23.25 dBm	714.12	mA
	8A_n78A CH636666 @ 22.92 dBm	711.09	mA

	8A_n78A CH650000 @ 23.33 dBm	709.04	mA

6.3.3. AG550Q-EU Power Consumption

Table 53: AG550Q-EU Power Consumption (25 °C, 3.8 V Power Supply)

Test Mode	Test Condition	Typ.	Unit
OFF state	Power down	30	μA
Sleep state	**AT+CFUN=0** (USB Disconnected)	1.06	mA
	AT+CFUN=4 (USB Disconnected)	1.17	mA
	EGSM900 @ DRX = 2	3.10	mA
	EGSM900 @ DRX = 5	1.95	mA
	EGSM900 @ DRX = 5 (USB Suspend)	4.92	mA
	EGSM900 @ DRX = 9	1.95	mA
	DCS1800 @ DRX = 2	3.10	mA
	DCS1800 @ DRX = 5	1.96	mA
	DCS1800 @ DRX = 5 (USB Suspend)	5.39	mA
	DCS1800 @ DRX = 9	1.96	mA
	WCDMA @ DRX = 0.64 s	2.34	mA
	WCDMA @ DRX = 0.64 s (USB Suspend)	5.75	mA
	WCDMA @ DRX = 1.28 s	1.73	mA
	WCDMA @ DRX = 2.56 s	1.71	mA
	WCDMA @ DRX = 5.12 s	1.43	mA
	LTE-FDD @ DRX = 0.32 s	4.56	mA
	LTE-FDD @ DRX = 0.64 s	2.90	mA
	LTE-FDD @ DRX = 0.64 s (USB Suspend)	5.85	mA
	LTE-FDD @ DRX = 1.28 s	2.06	mA
	LTE-FDD @ DRX = 2.56 s	1.96	mA

	LTE-TDD @ DRX = 0.32 s	4.57	mA
	LTE-TDD @ DRX = 0.64 s	2.90	mA
	LTE-TDD @ DRX = 0.64 s (USB Suspend)	5.68	mA
	LTE-TDD @ DRX = 1.28 s	2.07	mA
	LTE-TDD @ DRX = 2.56 s	1.94	mA
	5G NR FDD @ DRX = 0.32 s	11.97	mA
	5G NR FDD @ DRX = 0.64 s	6.64	mA
	5G NR FDD @ DRX = 0.64 s (USB Suspend)	9.55	mA
	5G NR FDD @ DRX = 1.28 s	3.92	mA
	5G NR FDD @ DRX = 2.56 s	2.82	mA
	5G NR TDD @ DRX = 0.32 s	12.27	mA
	5G NR TDD @ DRX = 0.64 s	6.74	mA
	5G NR TDD @ DRX = 0.64 s（USB 挂起）	9.76	mA
	5G NR TDD @ DRX = 1.28 s	3.97	mA
	5G NR TDD @ DRX = 2.56 s	2.84	mA
Idle state	EGSM900 CH62 @ DRX = 5	16.04	mA
	EGSM900 CH62 @ DRX = 5 (USB Active)	45.85	mA
	WCDMA @ DRX = 0.64 s	16.30	mA
	WCDMA @ DRX = 0.64 s (USB Active)	46.55	mA
	LTE-FDD @ DRX = 0.64 s	16.70	mA
	LTE-FDD @ DRX = 0.64 s (USB Active)	48.12	mA
	LTE-TDD @ DRX = 0.64 s	17.15	mA
	LTE-TDD @ DRX = 0.64 s (USB Active)	49.53	mA
	5G NR FDD @ DRX = 0.64 s	19.70	mA
	5G NR FDD @ DRX = 0.64 s (USB Active)	49.96	mA
	5G NR TDD @ DRX = 0.64 s	19.95	mA

	5G NR TDD @ DRX = 0.64 s (USB Active)	50.08	mA
WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA CH9612 @ 23.36 dBm	642.49	mA
	WCDMA B1 HSUPA CH9612 @ 23.14 dBm	679.59	mA
	WCDMA B1 HSDPA CH9750 @ 23.34 dBm	566.63	mA
	WCDMA B1 HSUPA CH9750 @ 23.38 dBm	582.79	mA
	WCDMA B1 HSDPA CH9888 @ 23.27 dBm	584.03	mA
	WCDMA B1 HSUPA CH9888 @ 23.30 dBm	594.83	mA
	WCDMA B3 HSDPA CH937 @ 22.89 dBm	570.53	mA
	WCDMA B3 HSUPA CH937 @ 22.91 dBm	559.94	mA
	WCDMA B3 HSDPA CH1112 @ 22.84 dBm	569.01	mA
	WCDMA B3 HSUPA CH1112 @ 22.85 dBm	570.06	mA
	WCDMA B3 HSDPA CH1288 @ 22.64 dBm	783.89	mA
	WCDMA B3 HSUPA CH1288 @ 22.92 dBm	735.82	mA
	WCDMA B5 HSDPA CH4132 @ 22.48 dBm	442.45	mA
	WCDMA B5 HSUPA CH4132 @ 22.46 dBm	447.40	mA
	WCDMA B5 HSDPA CH4182 @ 22.47 dBm	442.45	mA
	WCDMA B5 HSUPA CH4182 @ 22.52 dBm	441.67	mA
	WCDMA B5 HSDPA CH4233 @ 22.40 dBm	473.85	mA
	WCDMA B5 HSUPA CH4233 @ 22.44 dBm	475.79	mA
	WCDMA B6 HSDPA CH4162 @ 22.52 dBm	430.6	mA
	WCDMA B6 HSUPA CH4162 @ 22.50 dBm	430.41	mA
	WCDMA B6 HSDPA CH4175 @ 22.51 dBm	439.35	mA
	WCDMA B6 HSUPA CH4175 @ 22.50 dBm	434.48	mA
	WCDMA B6 HSDPA CH4188 @ 22.49 dBm	439.45	mA
	WCDMA B6 HSUPA CH4188 @ 22.44 dBm	436.75	mA
	WCDMA B8 HSDPA CH2712 @ 22.46 dBm	480.07	mA

	WCDMA B8 HSUPA CH2712 @ 22.47 dBm	477.01	mA
	WCDMA B8 HSDPA CH2788 @ 22.45 dBm	438.80	mA
	WCDMA B8 HSUPA CH2788 @ 22.52 dBm	441.77	mA
	WCDMA B8 HSDPA CH2863 @ 22.45 dBm	462.02	mA
	WCDMA B8 HSUPA CH2863 @ 22.47 dBm	458.66	mA
LTE data transfer (GNSS OFF)	LTE-FDD B1 CH18100 @ 23.36 dBm	769.84	mA
	LTE-FDD B1 CH18300 @ 23.35 dBm	664.39	mA
	LTE-FDD B1 CH18500 @ 23.33dBm	729.13	mA
	LTE-FDD B2 CH18650 @ 23.47 dBm	652.84	mA
	LTE-FDD B2 CH18900 @ 23.44 dBm	610.43	mA
	LTE-FDD B2 CH19150 @ 23.47 dBm	605.88	mA
	LTE-FDD B3 CH19300 @ 23.41 dBm	741.51	mA
	LTE-FDD B3 CH19575 @ 23.43 dBm	764.43	mA
	LTE-FDD B3 CH19850 @ 23.47 dBm	798.90	mA
	LTE-FDD B4 CH20000 @ 23.51 dBm	648.37	mA
	LTE-FDD B4 CH20175 @ 23.52 dBm	610.18	mA
	LTE-FDD B4 CH20350 @ 23.49 dBm	605.52	mA
	LTE-FDD B5 CH20450 @ 23.58 dBm	507.54	mA
	LTE-FDD B5 CH20525 @ 23.64 dBm	481.95	mA
	LTE-FDD B5 CH20600 @ 23.6 dBm	492.41	mA
	LTE-FDD B7 CH20850 @ 23.13 dBm	668.30	mA
	LTE-FDD B7 CH21100 @ 23.12 dBm	638.26	mA
	LTE-FDD B7 CH21350 @ 23.11 dBm	659.75	mA
	LTE-FDD B8 CH21500 @ 23.65 dBm	524.63	mA
	LTE-FDD B8 CH21625 @ 23.58 dBm	499.89	mA
	LTE-FDD B8 CH21750 @ 23.6 dBm	497.12	mA

	LTE-FDD B20 CH24200 @ 23.6 dBm	524.66	mA
	LTE-FDD B20 CH24300 @ 23.6 dBm	496.27	mA
	LTE-FDD B20 CH24400 @ 23.6 dBm	486.33	mA
	LTE-FDD B28 CH27260 @ 23.6 dBm	513.18	mA
	LTE-FDD B28 CH27435 @ 23.6 dBm	480.85	mA
	LTE-FDD B28 CH27610 @ 23.6 dBm	461.91	mA
	LTE-TDD B38 CH37850 @ 23.02 dBm	385.16	mA
	LTE-TDD B38 CH38000 @ 23.14 dBm	379.28	mA
	LTE-TDD B38 CH38150 @ 23.09 dBm	366.50	mA
	LTE-TDD B40 CH38750 @ 23.15 dBm	339.53	mA
	LTE-TDD B40 CH39150 @ 23.09 dBm	338.36	mA
	LTE-TDD B40 CH39550 @ 23.1 dBm	318.10	mA
	LTE-TDD B41 CH40340 @ 23.01 dBm	361.20	mA
	LTE-TDD B41 CH40740 @ 23 dBm	344.75	mA
	LTE-TDD B41 CH41140 @ 22.74 dBm	354.73	mA
	LTE-TDD B42 CH41640 @ 23.01 dBm	370.78	mA
	LTE-TDD B42 CH41590 @ 23 dBm	378.26	mA
	LTE-TDD B42 CH43540 @ 22.74 dBm	380.45	mA
WCDMA voice call	WCDMA B1 CH9612 @ 22.98 dBm	604.74	mA
	WCDMA B1 CH9750 @ 23.02 dBm	531.68	mA
	WCDMA B1 CH9888 @ 23.03 dBm	550.13	mA
	WCDMA B3 CH937 @ 22.82 dBm	534.28	mA
	WCDMA B3 CH1112 @ 22.84 dBm	541.73	mA
	WCDMA B3 CH1288 @ 22.85 dBm	700.86	mA
	WCDMA B5 CH4132 @ 23.03 dBm	451.59	mA
	WCDMA B5 CH4182 @ 23.02 dBm	440.16	mA

	WCDMA B5 CH4233 @ 23.00 dBm	486.16	mA
	WCDMA B6 CH4162 @ 22.99 dBm	430.21	mA
	WCDMA B6 CH4175 @ 23.01 dBm	436.33	mA
	WCDMA B6 CH4188 @ 23.00 dBm	441.21	mA
	WCDMA B8 CH2712 @ 23.00 dBm	491.08	mA
	WCDMA B8 CH2788 @ 23.00 dBm	445.77	mA
	WCDMA B8 CH2863 @ 22.99 dBm	465.24	mA
GSM voice call	EGSM900 CH1 PCL = 5 @ 32.42 dBm	305.80	mA
	EGSM900 CH62 PCL = 5 @ 32.61 dBm	318.10	mA
	EGSM900 CH62 PCL = 12 @ 18.61 dBm	97.60	mA
	EGSM900 CH62 PCL = 19 @ 4.74 dBm	82.70	mA
	EGSM900 CH124 PCL = 5 @ 32.59 dBm	316.60	mA
	DCS1800 CH512 PCL = 0 @ 29.88 dBm	197.90	mA
	DCS1800 CH698 PCL=0 @ 30.13 dBm	201.90	mA
	DCS1800 CH698 PCL=7 @ 16.25 dBm	88.70	mA
	DCS1800 CH698 PCL 15 @ 0.56 dBm	83.20	mA
	DCS1800 CH885 PCL=0 @ 30.06 dBm	200.10	mA
	GSM850 CH128 PCL=0 @ 33.17 dBm	305.30	mA
	GSM850 CH188 PCL=5 @ 33.26 dBm	309.40	mA
	GSM850 CH188 PCL=5 @ 19.50 dBm	97.00	mA
	GSM850 CH188 PCL=12 @ 5.25 dBm	83.30	mA
	GSM850 CH251 PCL=19 @ 33.11 dBm	305.50	mA
	PCS1900 CH512 PCL=0 @ 29.28 dBm	201.90	mA
	PCS1900 CH661 PCL=0 @ 29.48 dBm	204.70	mA
	PCS1900 CH661 PCL=0 @ 15.52 dBm	87.40	mA
	PCS1900 CH661 PCL=7 @ 0.02 dBm	80.80	mA

	PCS1900 CH810 PCL=15 @ 29.52 dBm	205.50	mA
GPRS data transfer (GNSS OFF)	EGSM900 CH1 1DL/4UL @ 28.20 dBm	584.80	mA
	EGSM900 CH62 4DL/1UL @ 32.39 dBm	297.20	mA
	EGSM900 CH62 3DL/2UL @ 31.49 dBm	473.40	mA
	EGSM900 CH62 2DL/3UL @ 29.84 dBm	554.00	mA
	EGSM900 CH62 1DL/4UL @ 28.66 dBm	626.90	mA
	EGSM900 CH124 1DL/4UL @ 28.36 dBm	612.60	mA
	PCS1900 CH512 1DL4UL @ 26.66 dBm	417.30	mA
	PCS1900 CH661 4DL 1UL @ 29.99 dBm	196.10	mA
	PCS1900 CH661 3DL 2UL @ 29.95 dBm	328.40	mA
	PCS1900 CH661 2DL 3UL @ 28.11 dBm	377.60	mA
	PCS1900 CH661 1DL 4UL @ 28.18 dBm	483.90	mA
	PCS1900 CH810 1DL 4UL @ 26.93 dBm	437.90	mA
	GSM850 CH128 1DL 4UL @ 28.37 dBm	565.60	mA
	GSM850 CH188 4DL 1UL @ 32.58 dBm	298.20	mA
	GSM850 CH188 3DL 2UL @ 31.68 dBm	468.40	mA
	GSM850 CH188 2DL 3UL @ 29.76 dBm	528.70	mA
	GSM850 CH188 1DL 4UL @ 28.38 dBm	582.30	mA
	GSM850 CH251 1DL 4UL @ 28.31 dBm	583.20	mA
	DCS1800 CH512 1DL/4UL @ 26.97 dBm	414.50	mA
	DCS1800 CH698 3DL/2UL @ 30.25 dBm	197.20	mA
	DCS1800 CH698 2DL/3UL @ 28.13 dBm	329.90	mA
	DCS1800 CH698 1DL/4UL @ 27.21 dBm	367.80	mA
	DCS1800 CH885 1DL/4UL @ 27.00 dBm	427.90	mA
EDGE data transfer (GNSS OFF)	EGSM900 CH1 1DL/4UL @ 23.41 dBm	357.50	mA
	EGSM900 CH62 4DL/1UL @ 26.70 dBm	169.20	mA

	EGSM900 CH62 3DL/2UL @ 26.60 dBm	277.20	mA
	EGSM900 CH62 2DL/3UL @ 24.46 dBm	314.60	mA
	EGSM900 CH62 1DL/4UL @ 23.39 dBm	359.60	mA
	EGSM900 CH124 1DL/4UL @ 23.50 dBm	369.70	mA
	PCS1900 CH512 1DL 4UL @ 22.68 dBm	290.80	mA
	PCS1900 CH661 4DL 1UL @ 26.09 dBm	141.60	mA
	PCS1900 CH661 3DL 2UL @ 26.13 dBm	224.40	mA
	PCS1900 CH661 2DL 3UL @ 24.13 dBm	260.00	mA
	PCS1900 CH661 1DL 4UL @ 22.94 dBm	300.40	mA
	PCS1900 CH810 1DL 4UL @ 22.89 dBm	303.90	mA
	GSM850 CH128 1DL 4UL @ 23.48 dBm	349.80	mA
	GSM850 CH188 4DL 1UL @ 26.27 dBm	162.30	mA
	GSM850 CH188 3DL 2UL @ 26.25 dBm	261.50	mA
	GSM850 CH188 2DL 3UL @ 24.67 dBm	312.60	mA
	GSM850 CH188 1DL 4UL @ 23.47 dBm	353.70	mA
	GSM850 CH251 1DL 4UL @ 23.43 dBm	355.20	mA
	DCS1800 CH885 1DL 4UL @ 23.09 dBm	289.40	mA
	DCS1800 CH698 4DL/1UL @ 26.00 dBm	138.90	mA
	DCS1800 CH698 3DL/2UL @ 26.04 dBm	217.00	mA
	DCS1800 CH698 2DL/3UL @ 24.03 dBm	250.50	mA
	DCS1800 CH698 1DL/4UL @ 23.11 dBm	289.50	mA
	DCS1800 CH885 1DL/4UL @ 23.11 dBm	288.60	mA
5G SA data transfer (GNSS OFF)	n41A CH509202 @ 25.46 dBm	497.59	mA
	n41A CH518598 @ 26.19 dBm	470.88	mA
	n41A CH528000 @ 25.27 dBm	485.75	mA
	n78A CH623334 @ 25.57 dBm	380.00	mA

	n78A CH636666 @ 25.57 dBm	394.04	mA
	n78A CH650000 @ 25.43 dBm	380.33	mA
	n1A CH 385000 @ 23.46 dBm	717.26	mA
	n1A CH 390000 @ 23.42 dBm	731.34	mA
	n1A CH 395000 @ 23.48 dBm	768.28	mA
	n3A CH 343000 @ 23.50 dBm	692.05	mA
	n3A CH 349500 @ 23.42 dBm	604.92	mA
	n3A CH 356000 @ 23.44 dBm	658.83	mA
	n8A CH 177000 @ 22.91 dBm	502.93	mA
	n8A CH 179500 @ 22.87 dBm	470.27	mA
	n8A CH 182000 @ 22.86 dBm	470.02	mA
	n20A CH 167400 @ 23.08 dBm	451.41	mA
	n20A CH 169400 @ 23.01 dBm	437.38	mA
	n20A CH 171400 @ 23.92 dBm	441.07	mA
	n28A CH 142600 @ 23.37dBm	505.79	mA
	n28A CH 145100 @ 23.36 dBm	465.82	mA
	n28A CH 147600 @ 23.31 dBm	445.51	mA
5G NR NSA data transfer (GNSS OFF)	1A_n3A CH345000 @ 23.14 dBm	841.91	mA
	1A_n3A CH349500 @ 23.08 dBm	798.23	mA
	1A_n3A CH354000 @ 22.99 dBm	824.74	mA
	1A_n8A CH178000 @ 22.99 dBm	687.10	mA
	1A_n8A CH179500 @ 23 dBm	665.57	mA
	1A_n8A CH181000 @ 23 dBm	668.32	mA
	1A_n28A CH142600 @ 23.19 dBm	679.57	mA
	1A_n28A CH145100 @ 23.15 dBm	681.84	mA
	1A_n28A CH147600 @ 23.2 dBm	666.03	mA

	1A_n78A CH623334 @ 23.08 dBm	754.15	mA
	1A_n78A CH636666 @ 22.85 dBm	757.38	mA
	1A_n78A CH650000 @ 23.06 dBm	757.73	mA
	3A_n1A CH385000 @ 22.95 dBm	839.78	mA
	3A_n1A CH390000 @ 23.24 dBm	849.13	mA
	3A_n1A CH395000 @ 23.2 dBm	864.23	mA
	3A_n8A CH178000 @ 23.05 dBm	697.51	mA
	3A_n8A CH179500 @ 23.07 dBm	676.66	mA
	3A_n8A CH181000 @ 23.05 dBm	680.06	mA
	3A_n20A CH168400 @ 23.02 dBm	661.38	mA
	3A_n20A CH169400 @ 23.07 dBm	656.10	mA
	3A_n20A CH170400 @ 23.08 dBm	657.91	mA
	3A_n28A CH142600 @ 23.27 dBm	692.19	mA
	3A_n28A CH145100 @ 23.25 dBm	692.99	mA
	3A_n28A CH147600 @ 23.26 dBm	680.02	mA
	3A_n41A CH509202 @ 25.86 dBm	1076.00	mA
	3A_n41A CH518598 @ 25.89 dBm	1067.00	mA
	3A_n41A CH528000 @ 25.82 dBm	1074.00	mA
	3A_n78A CH623334 @ 25.67 dBm	1077.00	mA
	3A_n78A CH636666 @ 25.6 dBm	1066.00	mA
	3A_n78A CH650000 @ 25.67 dBm	1073.00	mA
	7A_n1A CH385000 @ 23.16 dBm	771.57	mA
	7A_n1A CH390000 @ 23.15 dBm	761.74	mA
	7A_n1A CH395000 @ 23.11 dBm	764.71	mA
	7A_n3A CH345000 @ 23.1 dBm	767.40	mA
	7A_n3A CH349500 @ 23.17 dBm	764.76	mA

	7A_n3A CH354000 @ 23.17 dBm	785.01	mA
	7A_n20A CH168400 @ 22.97 dBm	663.59	mA
	7A_n20A CH169400 @ 22.96 dBm	671.15	mA
	7A_n20A CH170400 @ 22.85 dBm	698.13	mA
	7A_n28A CH142600 @ 23 dBm	671.19	mA
	7A_n28A CH145100 @ 22.92 dBm	691.77	mA
	7A_n28A CH147600 @ 22.89 dBm	676.57	mA
	7A_n78A CH623334 @ 23.04 dBm	751.99	mA
	7A_n78A CH636666 @ 22.97 dBm	751.74	mA
	7A_n78A CH650000 @ 23.06 dBm	752.57	mA
	8A_n41A CH509202 @ 23.12 dBm	656.40	mA
	8A_n41A CH518598 @ 23.22 dBm	663.04	mA
	8A_n41A CH528000 @ 23.27 dBm	659.89	mA
	8A_n78A CH623334 @ 23.11 dBm	642.54	mA
	8A_n78A CH636666 @ 23.03 dBm	645.13	mA
	8A_n78A CH650000 @ 23.1 dBm	649.51	mA
	20A_n3A CH345000 @ 22.76 dBm	686.14	mA
	20A_n3A CH349500 @ 22.78 dBm	686.94	mA
	20A_n3A CH354000 @ 22.66 dBm	699.28	mA
	20A_n28A CH143600 @ 22.99 dBm	687.08	mA
	20A_n78A CH623334 @ 22.99 dBm	655.07	mA
	20A_n78A CH636666 @ 22.99 dBm	651.36	mA
	20A_n78A CH650000 @ 23.03 dBm	651.91	mA
	28A_n78A CH623334 @ 22.93 dBm	658.67	mA
	28A_n78A CH636666 @ 22.91 dBm	671.35	mA
	28A_n78A CH650000 @ 22.96 dBm	653.38	mA

	38A_n78A CH623334 @ 23.01 dBm	573.50	mA
	38A_n78A CH636666 @ 22.98 dBm	565.57	mA
	38A_n78A CH650000 @ 23.03 dBm	584.15	mA
	40A_n41A CH509202 @ 23.15 dBm	530.59	mA
	40A_n41A CH518598 @ 23.24 dBm	531.33	mA
	40A_n41A CH528000 @ 23.23 dBm	531.05	mA
	40A_n78A CH623334 @ 23.08 dBm	551.28	mA
	40A_n78A CH636666 @ 22.87 dBm	545.78	mA
	40A_n78A CH650000 @ 22.97 dBm	544.75	mA

6.3.4. AG551Q-EU Power Consumption

Table 54: AG551Q-EU Power Consumption (25 °C, 3.8 V Power Supply)

Test Mode	Test Condition	Typ.	Unit
OFF state	Power down	30	μA
Sleep state	**AT+CFUN=0** (USB Disconnected)	1.07	mA
	AT+CFUN=4 (USB Disconnected)	1.20	mA
	EGSM900 @ DRX = 2	3.16	mA
	EGSM900 @ DRX = 5	2.06	mA
	EGSM900 @ DRX = 5 (USB Suspend)	4.61	mA
	EGSM900 @ DRX = 9	2.03	mA
	DCS1800 @ DRX = 2	3.28	mA
	DCS1800 @ DRX = 5	2.05	mA
	DCS1800 @ DRX = 5 (USB Suspend)	4.63	mA
	DCS1800 @ DRX = 9	2.03	mA
	WCDMA @ DRX = 0.64 s	2.58	mA
	WCDMA @ DRX = 0.64 s (USB Suspend)	5.29	mA

	WCDMA @ DRX = 1.28 s	1.97	mA
	WCDMA @ DRX = 2.56 s	1.86	mA
	WCDMA @ DRX = 5.12 s	1.52	mA
	LTE-FDD @ DRX = 0.32 s	4.41	mA
	LTE-FDD @ DRX = 0.64 s	2.82	mA
	LTE-FDD @ DRX = 0.64 s (USB Suspend)	5.58	mA
	LTE-FDD @ DRX = 1.28 s	2.02	mA
	LTE-FDD @ DRX = 2.56 s	1.87	mA
	LTE-TDD @ DRX = 0.32 s	4.44	mA
	LTE-TDD @ DRX = 0.64 s	2.86	mA
	LTE-TDD @ DRX = 0.64 s (USB Suspend)	5.43	mA
	LTE-TDD @ DRX = 1.28 s	2.06	mA
	LTE-TDD @ DRX = 2.56 s	1.90	mA
	5G NR FDD @ DRX = 0.32 s	12.14	mA
	5G NR FDD @ DRX = 0.64 s	6.62	mA
	5G NR FDD @ DRX = 0.64 s (USB Suspend)	8.99	mA
	5G NR FDD @ DRX = 1.28 s	3.94	mA
	5G NR FDD @ DRX = 2.56 s	2.86	mA
	5G NR TDD @ DRX = 0.32 s	12.17	mA
	5G NR TDD @ DRX = 0.64 s	6.75	mA
	5G NR TDD @ DRX = 0.64 s（USB 挂起）	9.24	mA
	5G NR TDD @ DRX = 1.28 s	3.98	mA
	5G NR TDD @ DRX = 2.56 s	3.80	mA
Idle state	EGSM900 CH62 @ DRX = 5	15.16	mA
	EGSM900 CH62 @ DRX = 5 (USB Active)	46.34	mA
	WCDMA @ DRX = 0.64 s	15.74	mA

	WCDMA @ DRX = 0.64 s (USB Active)	46.60	mA
	LTE-FDD @ DRX = 0.64 s	16.16	mA
	LTE-FDD @ DRX = 0.64 s (USB Active)	46.88	mA
	LTE-TDD @ DRX = 0.64 s	16.24	mA
	LTE-TDD @ DRX = 0.64 s (USB Active)	47.10	mA
	5G NR FDD @ DRX = 0.64 s	19.05	mA
	5G NR FDD @ DRX = 0.64 s (USB Active)	49.77	mA
	5G NR TDD @ DRX = 0.64 s	19.27	mA
	5G NR TDD @ DRX = 0.64 s (USB Active)	49.88	mA
WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA CH9612 @ 23.02 dBm	696.48	mA
	WCDMA B1 HSUPA CH9612 @ 23.03 dBm	689.14	mA
	WCDMA B1 HSDPA CH9750 @ 23.07 dBm	590.20	mA
	WCDMA B1 HSUPA CH9750 @ 23.02 dBm	590.78	mA
	WCDMA B1 HSDPA CH9888 @ 23.04 dBm	599.80	mA
	WCDMA B1 HSUPA CH9888 @ 22.99 dBm	602.23	mA
	WCDMA B3 HSDPA CH937 @ 22.45 dBm	597.12	mA
	WCDMA B3 HSUPA CH937 @ 22.89 dBm	530.24	mA
	WCDMA B3 HSDPA CH1112 @ 22.91 dBm	574.33	mA
	WCDMA B3 HSUPA CH1112 @ 22.93 dBm	559.16	mA
	WCDMA B3 HSDPA CH1288 @ 22.86 dBm	732.87	mA
	WCDMA B3 HSUPA CH1288 @ 22.88 dBm	710.46	mA
	WCDMA B5 HSDPA CH4132 @ 22.66 dBm	453.94	mA
	WCDMA B5 HSUPA CH4132 @ 22.66 dBm	454.58	mA
	WCDMA B5 HSDPA CH4182 @ 22.74 dBm	447.63	mA
	WCDMA B5 HSUPA CH4182 @ 22.77 dBm	444.63	mA
	WCDMA B5 HSDPA CH4233 @ 22.7 dBm	488.34	mA

	WCDMA B5 HSUPA CH4233 @ 22.68 dBm	485.36	mA
	WCDMA B6 HSDPA CH4162 @ 22.73 dBm	437.55	mA
	WCDMA B6 HSUPA CH4162 @ 22.65 dBm	435.32	mA
	WCDMA B6 HSDPA CH4175 @ 22.73 dBm	441.06	mA
	WCDMA B6 HSUPA CH4175 @ 22.71 dBm	437.74	mA
	WCDMA B6 HSDPA CH4188 @ 22.72 dBm	445.77	mA
	WCDMA B6 HSUPA CH4188 @ 22.76 dBm	442.03	mA
	WCDMA B8 HSDPA CH2712 @ 22.67 dBm	485.09	mA
	WCDMA B8 HSUPA CH2712 @ 22.67 dBm	485.08	mA
	WCDMA B8 HSDPA CH2788 @ 22.73 dBm	446.46	mA
	WCDMA B8 HSUPA CH2788 @ 22.7 dBm	445.00	mA
	WCDMA B8 HSDPA CH2863 @ 22.64 dBm	468.43	mA
	WCDMA B8 HSUPA CH2863 @ 22.63 dBm	464.76	mA
LTE data transfer (GNSS OFF)	LTE-FDD B1 CH18100 @ 23.4 dBm	812.38	mA
	LTE-FDD B1 CH18300 @ 23.45 dBm	679.24	mA
	LTE-FDD B1 CH18500 @ 23.43 dBm	741.29	mA
	LTE-FDD B2 CH18650 @ 23.49 dBm	661.63	mA
	LTE-FDD B2 CH18900 @ 23.47 dBm	605.86	mA
	LTE-FDD B2 CH19150 @ 23.48 dBm	597.92	mA
	LTE-FDD B3 CH19300 @ 23.46 dBm	779.04	mA
	LTE-FDD B3 CH19575 @ 23.46 dBm	757.84	mA
	LTE-FDD B3 CH19850 @ 23.48 dBm	790.11	mA
	LTE-FDD B4 CH20000 @ 23.35 dBm	623.71	mA
	LTE-FDD B4 CH20175 @ 23.38 dBm	582.80	mA
	LTE-FDD B4 CH20350 @ 23.28 dBm	586.73	mA
	LTE-FDD B5 CH20450 @ 23.67 dBm	509.85	mA

	LTE-FDD B5 CH20525 @ 23.71 dBm	487.63	mA
	LTE-FDD B5 CH20600 @ 23.65 dBm	499.95	mA
	LTE-FDD B7 CH20850 @ 23.57 dBm	682.26	mA
	LTE-FDD B7 CH21100 @ 23.5 dBm	649.75	mA
	LTE-FDD B7 CH21350 @ 23.45 dBm	668.79	mA
	LTE-FDD B8 CH21500 @ 23.66 dBm	532.48	mA
	LTE-FDD B8 CH21625 @ 23.66 dBm	497.28	mA
	LTE-FDD B8 CH21750 @ 23.65 dBm	503.03	mA
	LTE-FDD B20 CH24200 @ 23.38 dBm	525.01	mA
	LTE-FDD B20 CH24300 @ 23.61 dBm	506.17	mA
	LTE-FDD B20 CH24400 @ 23.65 dBm	491.08	mA
	LTE-FDD B28 CH27260 @ 23.39 dBm	517.97	mA
	LTE-FDD B28 CH27435 @ 23.38 dBm	482.82	mA
	LTE-FDD B28 CH27610 @ 23.35 dBm	458.16	mA
	LTE-TDD B38 CH37850 @ 23.49 dBm	380.38	mA
	LTE-TDD B38 CH38000 @ 23.38 dBm	376.28	mA
	LTE-TDD B38 CH38150 @ 23.27 dBm	366.47	mA
	LTE-TDD B40 CH38750 @ 23.41 dBm	346.55	mA
	LTE-TDD B40 CH39150 @ 23.4 dBm	346.08	mA
	LTE-TDD B40 CH39550 @ 23.35 dBm	321.60	mA
	LTE-TDD B41 CH40340 @ 23.45 dBm	374.07	mA
	LTE-TDD B41 CH40740 @ 23.29 dBm	349.84	mA
	LTE-TDD B41 CH41140 @ 22.92 dBm	363.90	mA
	LTE-TDD B42 CH41640 @ 23.46 dBm	394.08	mA
	LTE-TDD B42 CH41590 @ 23.55 dBm	404.86	mA
	LTE-TDD B42 CH43540 @ 23.41 dBm	394.89	mA

WCDMA voice call	WCDMA B1 CH9612 @ 22.74 dBm	673.46	mA
	WCDMA B1 CH9750 @ 23.25 dBm	574.08	mA
	WCDMA B1 CH9888 @ 23.24 dBm	586.24	mA
	WCDMA B3 CH937 @ 23.11 dBm	596.47	mA
	WCDMA B3 CH1112 @ 23.11 dBm	600.69	mA
	WCDMA B3 CH1288 @ 23.15 dBm	701.70	mA
	WCDMA B5 CH4132 @ 23.18 dBm	454.33	mA
	WCDMA B5 CH4182 @ 23.26 dBm	442.82	mA
	WCDMA B5 CH4233 @ 23.18 dBm	490.58	mA
	WCDMA B6 CH4162 @ 23.22 dBm	433.56	mA
	WCDMA B6 CH4175 @ 23.26 dBm	436.65	mA
	WCDMA B6 CH4188 @ 23.24 dBm	442.24	mA
	WCDMA B8 CH2712 @ 23.24 dBm	491.80	mA
	WCDMA B8 CH2788 @ 23.25 dBm	447.06	mA
	WCDMA B8 CH2863 @ 23.18 dBm	469.33	mA
GSM voice call	EGSM900 CH1 PCL = 5 @ 32.45 dBm	336.90	mA
	EGSM900 CH62 PCL = 5 @ 32.61 dBm	346.70	mA
	EGSM900 CH62 PCL = 12 @ 18.78 dBm	116.40	mA
	EGSM900 CH62 PCL = 19 @ 4.71 dBm	82.60	mA
	EGSM900 CH124 PCL = 5 @ 32.43 dBm	302.20	mA
	DCS1800 CH512 PCL=0 @ 29.64 dBm	205.30	mA
	DCS1800 CH698 PCL=0 @ 29.83 dBm	205.70	mA
	DCS1800 CH698 PCL=7 @ 15.96 dBm	88.50	mA
	DCS1800 CH698 PCL 15 @ 0.31 dBm	82.60	mA
	DCS1800 CH885 PCL=0 @ 30.08 dBm	210.10	mA
	PCS1900 CH512 PCL=0 @ 29.67 dBm	203.20	mA

	PCS1900 CH661 PCL=0 @ 30.09 dBm	207.90	mA
	PCS1900 CH661 PCL=0 @ 30.34 dBm	214.00	mA
	PCS1900 CH661 PCL=7 @ 16.25 dBm	87.90	mA
	PCS1900 CH810 PCL=15 @ 0.73 dBm	80.40	mA
	GSM850 CH128 PCL=0 @ 32.54 dBm	296.60	mA
	GSM850 CH188 PCL=5 @ 32.5 dBm	297.90	mA
	GSM850 CH188 PCL=5 @ 18.92 dBm	96.80	mA
	GSM850 CH188 PCL=12 @ 4.72 dBm	83.00	mA
	GSM850 CH251 PCL=19 @ 32.43 dBm	292.10	mA
GPRS data transfer (GNSS OFF)	EGSM900 CH1 1DL/4UL @ 28.42 dBm	607.20	mA
	EGSM900 CH62 4DL/1UL @ 32.45 dBm	321.30	mA
	EGSM900 CH62 3DL/2UL @ 31.65 dBm	480.80	mA
	EGSM900 CH62 2DL/3UL @ 29.55 dBm	516.00	mA
	EGSM900 CH62 1DL/4UL @ 28.31 dBm	579.90	mA
	EGSM900 CH124 1DL/4UL @ 28.27 dBm	580.30	mA
	DCS1800 CH512 1DL/4UL @ 26.69 dBm	432.00	mA
	DCS1800 CH698 4DL/2UL @ 29.94 dBm	203.80	mA
	DCS1800 CH698 3DL/2UL @ 29.91 dBm	340.60	mA
	DCS1800 CH698 2DL/3UL @ 27.85 dBm	377.90	mA
	DCS1800 CH698 1DL/4UL @ 26.97 dBm	440.50	mA
	DCS1800 CH885 1DL/4UL @ 26.68 dBm	430.30	mA
	PCS1900 CH512 1DL4UL @ 27.39 dBm	479.80	mA
	PCS1900 CH661 4DL 1UL @ 30.25 dBm	233.80	mA
	PCS1900 CH661 3DL 2UL @ 30.21 dBm	355.30	mA
	PCS1900 CH661 2DL 3UL @ 28.35 dBm	391.60	mA
	PCS1900 CH661 1DL 4UL @ 28.11 dBm	485.70	mA

	PCS1900 CH810 1DL 4UL @ 27.09 dBm	446.90	mA
	GSM850 CH128 1DL 4UL @ 28.41 dBm	551.10	mA
	GSM850 CH188 4DL 1UL @ 32.7 dBm	295.20	mA
	GSM850 CH188 3DL 2UL @ 31.55 dBm	446.90	mA
	GSM850 CH188 2DL 3UL @ 29.68 dBm	505.30	mA
	GSM850 CH188 1DL 4UL @ 28.27 dBm	556.20	mA
	GSM850 CH251 1DL 4UL @ 28.27 dBm	560.30	mA
EDGE data transfer (GNSS OFF)	EGSM900 CH1 1DL/4UL @ 23.2 dBm	375.60	mA
	EGSM900 CH62 4DL/1UL @ 26.56 dBm	197.40	mA
	EGSM900 CH62 3DL/2UL @ 26.56 dBm	276.70	mA
	EGSM900 CH62 2DL/3UL @ 24.46 dBm	305.70	mA
	EGSM900 CH62 1DL/4UL @ 23.28 dBm	347.40	mA
	EGSM900 CH124 1DL/4UL @ 23.31 dBm	347.20	mA
	DCS1800 CH885 1DL 4UL @ 22.6 dBm	293.80	mA
	DCS1800 CH698 4DL/1UL @ 25.63 dBm	141.00	mA
	DCS1800 CH698 3DL/2UL @ 25.64 dBm	219.90	mA
	DCS1800 CH698 2DL/3UL @ 23.63 dBm	252.40	mA
	DCS1800 CH698 1DL/4UL @ 22.85 dBm	295.90	mA
	DCS1800 CH885 1DL/4UL @ 22.64 dBm	290.00	mA
	PCS1900 CH512 1DL 4UL @ 22.84 dBm	327.10	mA
	PCS1900 CH661 4DL 1UL @ 26.33 dBm	175.20	mA
	PCS1900 CH661 3DL 2UL @ 26.25 dBm	241.10	mA
	PCS1900 CH661 2DL 3UL @ 24.15 dBm	264.70	mA
	PCS1900 CH661 1DL 4UL @ 23.25 dBm	308.20	mA
	PCS1900 CH810 1DL 4UL @ 23.01 dBm	307.10	mA
	GSM850 CH128 1DL 4UL @ 23.41 dBm	338.30	mA

	GSM850 CH188 4DL 1UL @ 26.49 dBm	160.70	mA
	GSM850 CH188 3DL 2UL @ 26.46 dBm	259.30	mA
	GSM850 CH188 2DL 3UL @ 24.57 dBm	300.40	mA
	GSM850 CH188 1DL 4UL @ 23.53 dBm	345.70	mA
	GSM850 CH251 1DL 4UL @ 23.38 dBm	341.50	mA
5G NR SA data transfer (GNSS OFF)	n41A CH509202 @ 25.46 dBm	488.09	mA
	n41A CH518598 @ 25.89 dBm	505.28	mA
	n41A CH528000 @ 25.94 dBm	513.40	mA
	n78A CH623334 @ 25.61 dBm	415.51	mA
	n78A CH636666 @ 26.38 dBm	454.55	mA
	n78A CH650000 @ 25.07 dBm	398.54	mA
	n1A CH 385000 @ 23.31 dBm	700.67	mA
	n1A CH 390000 @ 23.35 dBm	706.38	mA
	n1A CH 395000 @ 23.37 dBm	730.74	mA
	n3A CH 343000 @ 23.50 dBm	692.05	mA
	n3A CH 349500 @ 23.42 dBm	604.92	mA
	n3A CH 356000 @ 23.44 dBm	658.83	mA
	n8A CH 177000 @ 23.15 dBm	536.08	mA
	n8A CH 179500 @ 23.08 dBm	493.08	mA
	n8A CH 182000 @ 23.01 dBm	497.83	mA
	n20A CH 167400 @ 22.77 dBm	460.68	mA
	n20A CH 169400 @ 22.63 dBm	440.25	mA
	n20A CH 171400 @ 22.74 dBm	452.69	mA
	n28A CH 142600 @ 23.89 dBm	549.36	mA
	n28A CH 145100 @ 24.02 dBm	561.46	mA
	n28A CH 147600 @ 23.34 dBm	491.54	mA

	1A_n3A CH345000 @ 22.81 dBm	849.06	mA
	1A_n3A CH349500 @ 22.78 dBm	800.95	mA
	1A_n3A CH354000 @ 22.82 dBm	816.38	mA
	1A_n8A CH178000 @ 23.60 dBm	748.92	mA
	1A_n8A CH179500 @ 23.60 dBm	723.78	mA
	1A_n8A CH181000 @ 23.39 dBm	721.80	mA
	1A_n28A CH142600 @ 23.47 dBm	767.32	mA
	1A_n28A CH145100 @ 23.52 dBm	775.62	mA
	1A_n28A CH147600 @ 23.04 dBm	728.45	mA
	1A_n78A CH623334 @ 23.00 dBm	837.29	mA
	1A_n78A CH636666 @ 22.77 dBm	829.23	mA
	1A_n78A CH650000 @ 22.81 dBm	829.87	mA
5G NR NSA data transfer (GNSS OFF)	3A_n1A CH385000 @ 23.21 dBm	888.70	mA
	3A_n1A CH390000 @ 23.14 dBm	895.24	mA
	3A_n1A CH395000 @ 23.14 dBm	910.15	mA
	3A_n8A CH178000 @ 23.35 dBm	762.10	mA
	3A_n8A CH179500 @ 23.3 dBm	736.47	mA
	3A_n8A CH181000 @ 23.31 dBm	736.61	mA
	3A_n20A CH168400 @ 23 dBm	716.60	mA
	3A_n20A CH169400 @ 23 dBm	715.09	mA
	3A_n20A CH170400 @ 23.01 dBm	716.26	mA
	3A_n28A CH142600 @ 23.16 dBm	770.58	mA
	3A_n28A CH145100 @ 23.23 dBm	765.70	mA
	3A_n28A CH147600 @ 23.23 dBm	758.40	mA
	3A_n41A CH509202 @ 25.89 dBm	1124.00	mA
	3A_n41A CH518598 @ 26.05 dBm	1130.00	mA

	3A_n41A CH528000 @ 26 dBm	1125.00	mA
	3A_n78A CH623334 @ 26.36 dBm	1038.00	mA
	3A_n78A CH636666 @ 26.07 dBm	1054.00	mA
	3A_n78A CH650000 @ 26.42 dBm	1064.00	mA
	7A_n1A CH385000 @ 23.41 dBm	806.13	mA
	7A_n1A CH390000 @ 23.33 dBm	810.73	mA
	7A_n1A CH395000 @ 23.31 dBm	829.96	mA
	7A_n3A CH345000 @ 23.09 dBm	801.51	mA
	7A_n3A CH349500 @ 23.14 dBm	801.68	mA
	7A_n3A CH354000 @ 23.12 dBm	822.96	mA
	7A_n20A CH168400 @ 23.04 dBm	714.79	mA
	7A_n20A CH169400 @ 22.93 dBm	731.04	mA
	7A_n20A CH170400 @ 22.94 dBm	754.39	mA
	7A_n28A CH142600 @ 23.47 dBm	772.95	mA
	7A_n28A CH145100 @ 23.38 dBm	764.25	mA
	7A_n28A CH147600 @ 23.37 dBm	755.24	mA
	7A_n78A CH623334 @ 23.66 dBm	823.79	mA
	7A_n78A CH636666 @ 23.3 dBm	820.82	mA
	7A_n78A CH650000 @ 23.56 dBm	821.60	mA
	8A_n41A CH509202 @ 23.02 dBm	730.01	mA
	8A_n41A CH518598 @ 23.12 dBm	729.16	mA
	8A_n41A CH528000 @ 23.11 dBm	732.22	mA
	8A_n78A CH623334 @ 23.53 dBm	719.40	mA
	8A_n78A CH636666 @ 23.03 dBm	711.63	mA
	8A_n78A CH650000 @ 23.33 dBm	707.74	mA
	20A_n3A CH345000 @ 23.06 dBm	721.74	mA

	20A_n3A CH349500 @ 23.00 dBm	728.99	mA
	20A_n3A CH354000 @ 23.01 dBm	743.08	mA
	20A_n28A CH143600 @ 23.09 dBm	709.82	mA
	20A_n78A CH623334 @ 23.40 dBm	719.71	mA
	20A_n78A CH636666 @ 23.10 dBm	716.87	mA
	20A_n78A CH650000 @ 22.95 dBm	708.72	mA
	28A_n78A CH623334 @ 23.39 dBm	722.69	mA
	28A_n78A CH636666 @ 23.11 dBm	715.22	mA
	28A_n78A CH650000 @ 22.97 dBm	712.73	mA
	38A_n78A CH623334 @ 23.25 dBm	614.08	mA
	38A_n78A CH636666 @ 22.99 dBm	605.87	mA
	38A_n78A CH650000 @ 22.81 dBm	604.64	mA
	40A_n41A CH509202 @ 23.19 dBm	581.03	mA
	40A_n41A CH518598 @ 23.25 dBm	584.85	mA
	40A_n41A CH528000 @ 23.24 dBm	584.20	mA
	40A_n78A CH623334 @ 23.66 dBm	583.12	mA
	40A_n78A CH636666 @ 22.87 dBm	588.24	mA
	40A_n78A CH650000 @ 22.79 dBm	581.01	mA

6.3.5. AG550Q-NA Power Consumption

Table 55: AG550Q-NA Power Consumption (25 °C, 3.8 V Power Supply)

Test Mode	Test Condition	Typ.	Unit
OFF state	Power down	30	μA
Sleep state	**AT+CFUN=0** (USB Disconnected)	1.21	mA
	AT+CFUN=4 (USB Disconnected)	1.35	mA
	PCS1900 @ DRX = 2	3.14	mA

	PCS1900 @ DRX = 5	1.83	mA
	PCS1900 @ DRX = 5 (USB Suspend)	5.01	mA
	PCS1900 @ DRX = 9	2.03	mA
	LTE-FDD @ DRX = 0.32 s	4.41	mA
	LTE-FDD @ DRX = 0.64 s	2.81	mA
	LTE-FDD @ DRX = 0.64 s (USB Suspend)	5.64	mA
	LTE-FDD @ DRX = 1.28 s	1.98	mA
	LTE-FDD @ DRX = 2.56 s	1.91	mA
	LTE-TDD @ DRX = 0.32 s	4.50	mA
	LTE-TDD @ DRX = 0.64 s	2.84	mA
	LTE-TDD @ DRX = 0.64 s (USB Suspend)	5.66	mA
	LTE-TDD @ DRX = 1.28 s	2.03	mA
	LTE-TDD @ DRX = 2.56 s	1.87	mA
	5G NR FDD @ DRX = 0.32 s	11.73	mA
	5G NR FDD @ DRX = 0.64 s	6.47	mA
	5G NR FDD @ DRX = 0.64s (USB Suspend)	9.15	mA
	5G NR FDD @ DRX = 1.28 s	3.82	mA
	5G NR FDD @ DRX = 2.56 s	2.83	mA
	5G NR TDD @ DRX = 0.32 s	11.90	mA
	5G NR TDD @ DRX = 0.64 s	6.42	mA
	5G NR TDD @ DRX = 0.64 s (USB Suspend)	9.17	mA
	5G NR TDD @ DRX = 1.28 s	3.68	mA
	5G NR TDD @ DRX = 2.56 s	2.69	mA
Idle state	PCS1900 CH661 @ DRX = 5	15.63	mA
	PCS1900 CH661 @ DRX = 5 (USB Active)	46.81	mA
	LTE-FDD @ DRX = 0.64 s	16.68	mA

	LTE-FDD @ DRX = 0.64 s (USB Active)	46.09	mA
	LTE-TDD @ DRX = 0.64 s	16.55	mA
	LTE-TDD @ DRX = 0.64 s (USB Active)	46.09	mA
	5G NR FDD @ DRX = 0.64 s	18.86	mA
	5G NR FDD @ DRX = 0.64 s (USB Active)	48.99	mA
	5G NR TDD @ DRX = 0.64 s	19.48	mA
	5G NR TDD @ DRX = 0.64 s (USB Active)	49.29	mA
LTE data transfer (GNSS OFF)	LTE-FDD B2 CH18700 @ 23.15 dBm	675.35	mA
	LTE-FDD B2 CH18900 @ 23.1 dBm	620.95	mA
	LTE-FDD B2 CH19100 @ 23.17 dBm	629.29	mA
	LTE-FDD B4 CH20050 @ 23.16 dBm	651.72	mA
	LTE-FDD B4 CH20175 @ 23.21 dBm	623.89	mA
	LTE-FDD B4 CH20300 @ 23.1 dBm	611.28	mA
	LTE-FDD B5 CH20450 @ 23.23 dBm	507.87	mA
	LTE-FDD B5 CH20525 @ 23.28 dBm	481.68	mA
	LTE-FDD B5 CH20600 @ 23.25 dBm	492.89	mA
	LTE-FDD B7 CH20850 @ 23.18 dBm	647.62	mA
	LTE-FDD B7 CH21100 @ 23.19 dBm	620.69	mA
	LTE-FDD B7 CH21350 @ 23.15 dBm	622.82	mA
	LTE-FDD B12 CH23060 @ 23.23 dBm	460.78	mA
	LTE-FDD B12 CH23095 @ 23.31 dBm	468.50	mA
	LTE-FDD B12 CH23130 @ 23.3 dBm	460.78	mA
	LTE-FDD B13 CH23230 @ 23.08 dBm	514.02	mA
	LTE-FDD B14 CH23330 @ 23.21 dBm	462.59	mA
	LTE-FDD B17 CH23780 @ 23.26 dBm	469.79	mA
	LTE-FDD B17 CH23790 @ 23.28 dBm	465.99	mA

	LTE-FDD B17 CH23800 @ 23.31 dBm	460.52	mA
	LTE-FDD B25 CH26140 @ 23.16 dBm	699.31	mA
	LTE-FDD B25 CH26365 @ 23.17 dBm	648.20	mA
	LTE-FDD B25 CH26590 @ 23.15 dBm	633.62	mA
	LTE-FDD B26 CH26765 @ 23.17 dBm	526.86	mA
	LTE-FDD B26 CH26865 @ 23.24 dBm	512.12	mA
	LTE-FDD B26 CH26965 @ 23.18 dBm	502.90	mA
	LTE-FDD B28 CH27310 @ 23.32 dBm	506.65	mA
	LTE-FDD B28 CH27435 @ 23.29 dBm	478.05	mA
	LTE-FDD B28 CH27560 @ 23.31 dBm	453.78	mA
	LTE-FDD B66 CH132072 @ 23.09 dBm	650.70	mA
	LTE-FDD B66 CH132322 @ 23 dBm	612.61	mA
	LTE-FDD B66 CH132572 @ 23.03 dBm	617.16	mA
	LTE-FDD B71 CH133222 @ 23.08 dBm	500.09	mA
	LTE-FDD B71 CH133322 @ 23.08 dBm	464.67	mA
	LTE-FDD B71 CH133372 @ 23.09 dBm	460.03	mA
	LTE-TDD B41 CH39750 @ 22.99 dBm	353.54	mA
	LTE-TDD B41 CH40620 @ 23.01 dBm	338.94	mA
	LTE-TDD B41 CH41490 @ 22.83 dBm	360.87	mA
	LTE-TDD B48 CH55340 @ 23.49 dBm	402.97	mA
	LTE-TDD B48 CH55990 @ 23.42 dBm	402.59	mA
	LTE-TDD B48 CH56640 @ 23.36 dBm	401.68	mA
GSM voice call	PCS1900 CH512 PCL = 0 @ 28.89 dBm	234.70	mA
	PCS1900 CH661 PCL = 0 @ 29.16 dBm	200.40	mA
	PCS1900 CH661 PCL = 0 @ 15.20 dBm	87.00	mA
	PCS1900 CH661 PCL = 7 @ 0.26 dBm	80.60	mA

	PCS1900 CH810 PCL = 15 @ 29.17 dBm	199.90	mA
GPRS data transfer (GNSS OFF)	PCS1900 CH512 1DL4UL @ 25.80 dBm	407.90	mA
	PCS1900 CH661 4DL 1UL @ 28.86 dBm	184.00	mA
	PCS1900 CH661 3DL 2UL @ 28.78 dBm	308.10	mA
	PCS1900 CH661 2DL 3UL @ 27.16 dBm	363.70	mA
	PCS1900 CH661 1DL 4UL @ 27.33 dBm	470.10	mA
	PCS1900 CH810 1DL 4UL @ 26.14 dBm	422.90	mA
EDGE data transfer (GNSS OFF)	PCS1900 CH512 1DL 4UL @ 21.76 dBm	286.90	mA
	PCS1900 CH661 4DL 1UL @ 25.23 dBm	138.90	mA
	PCS1900 CH661 3DL 2UL @ 25.23 dBm	217.80	mA
	PCS1900 CH661 2DL 3UL @ 23.03 dBm	250.80	mA
	PCS1900 CH661 1DL 4UL @ 21.89 dBm	288.80	mA
	PCS1900 CH810 1DL 4UL @ 22.09 dBm	291.60	mA
5G NR SA data transfer (GNSS OFF)	n2A CH372000 @ 23.21 dBm	550.59	mA
	n2A CH376000 @ 23.02 dBm	528.34	mA
	n2A CH380000 @ 23.01 dBm	527.64	mA
	n5A CH166800 @ 22.98 dBm	464.24	mA
	n5A CH167300 @ 22.87 dBm	462.07	mA
	n5A CH167800 @ 22.81 dBm	466.99	mA
	n25A CH372000 @ 23.52 dBm	617.97	mA
	n25A CH376500 @ 23.36 dBm	598.61	mA
	n25A CH381000 @ 23.4 dBm	614.90	mA
	n66A CH346000 @ 23.54 dBm	586.32	mA
	n66A CH349000 @ 23.48 dBm	598.42	mA
	n66A CH352000 @ 23.55 dBm	605.93	mA
	n71A CH134600 @ 23.13 dBm	441.01	mA

	n71A CH136100 @ 23.11 dBm	432.08	mA
	n71A CH137600 @ 23.16 dBm	454.12	mA
	n41A CH509202 @ 25.79 dBm	470.93	mA
	n41A CH518598 @ 26.47 dBm	514.89	mA
	n41A CH528000 @ 25.75 dBm	491.33	mA
	n48A CH638000 @ 23.14 dBm	323.00	mA
	n48A CH641666 @ 23.32 dBm	314.00	mA
	n48A CH645332 @ 23.02 dBm	317.00	mA
	n77A CH623334 @ 25.29 dBm	407.00	mA
	n77A CH650000 @ 25.21 dBm	398.00	mA
	n77A CH676666 @ 24.83 dBm	413.00	mA
	n78A CH623334 @ 25.27 dBm	396.06	mA
	n78A CH636666 @ 26.19 dBm	451.13	mA
	n78A CH650000 @ 25.29 dBm	415.01	mA
5G NR NSA data transfer (GNSS OFF)	2A_n5A CH166800 @ 22.83 dBm	663.60	mA
	2A_n5A CH167300 @ 22.73 dBm	667.59	mA
	2A_n5A CH167800 @ 22.71 dBm	670.97	mA
	2A_n41A CH509202 @ 23.12 dBm	739.72	mA
	2A_n41A CH518598 @ 23.18 dBm	746.42	mA
	2A_n41A CH528000 @ 23.09 dBm	744.79	mA
	2A_n48A CH638000 @ 23.01 dBm	713.00	mA
	2A_n48A CH641666 @ 23.10 dBm	710.00	mA
	2A_n48A CH645332 @ 22.96 dBm	709.00	mA
	2A_n66A CH346000 @ 23.01 dBm	781.74	mA
	2A_n66A CH349000 @ 23.05 dBm	793.87	mA
	2A_n66A CH352000 @ 23.01 dBm	783.88	mA

	2A_n71A CH134600 @ 22.9 dBm	662.70	mA
	2A_n71A CH136100 @ 22.72 dBm	650.11	mA
	2A_n71A CH137600 @ 22.76 dBm	666.40	mA
	2A_n77A CH623334 @ 22.94 dBm	784.00	mA
	2A_n77A CH650000 @ 23.08 dBm	779.00	mA
	2A_n77A CH676666 @ 23.07 dBm	802.00	mA
	2A_n78A CH623334 @ 23.23 dBm	762.43	mA
	2A_n78A CH636666 @ 23.08 dBm	769.71	mA
	2A_n78A CH650000 @ 23.16 dBm	766.80	mA
	5A_n2A CH372000 @ 22.7 dBm	686.27	mA
	5A_n2A CH376000 @ 22.79 dBm	683.57	mA
	5A_n2A CH380000 @ 22.79 dBm	647.80	mA
	5A_n41A CH509202 @ 23.21 dBm	660.77	mA
	5A_n41A CH518598 @ 23.28 dBm	659.12	mA
	5A_n41A CH528000 @ 23.26 dBm	661.28	mA
	5A_n48A CH638000 @ 23.26 dBm	599.00	mA
	5A_n48A CH641666 @ 23.02 dBm	597.00	mA
	5A_n48A CH645332 @ 22.78 dBm	591.00	mA
	5A_n66A CH346000 @ 23.3 dBm	705.36	mA
	5A_n66A CH349000 @ 23.18 dBm	709.62	mA
	5A_n66A CH352000 @ 23.18 dBm	703.62	mA
	5A_n77A CH623334 @ 23.10 dBm	674.00	mA
	5A_n77A CH650000 @ 23.18 dBm	690.00	mA
	5A_n77A CH676666 @ 23.14 dBm	673.00	mA
	5A_n78A CH623334 @ 23.04 dBm	653.65	mA
	5A_n78A CH636666 @ 23.23 dBm	660.59	mA

	5A_n78A CH650000 @ 23.26 dBm	656.70	mA
	7A_n77A CH623334 @ 23.12 dBm	791.00	mA
	7A_n77A CH650000 @ 23.37 dBm	795.00	mA
	7A_n77A CH676666 @ 23.40 dBm	804.00	mA
	12A_n2A CH372000 @ 23.04 dBm	740.17	mA
	12A_n2A CH376000 @ 22.88 dBm	723.94	mA
	12A_n2A CH380000 @ 22.91 dBm	714.09	mA
	12A_n25A CH372000 @ 23.28 dBm	814.73	mA
	12A_n25A CH376500 @ 23.25 dBm	812.93	mA
	12A_n25A CH381000 @ 23.28 dBm	819.87	mA
	12A_n66A CH346000 @ 23.32 dBm	766.82	mA
	12A_n66A CH349000 @ 23.24 dBm	769.59	mA
	12A_n66A CH352000 @ 23.19 dBm	767.25	mA
	12A_n77A CH623334 @ 23.01 dBm	666.00	mA
	12A_n77A CH650000 @ 22.88 dBm	664.00	mA
	12A_n77A CH676666 @ 23.07 dBm	678.00	mA
	13A_n2A CH372000 @ 23.08 dBm	666.65	mA
	13A_n2A CH376000 @ 22.66 dBm	662.34	mA
	13A_n2A CH380000 @ 23.02 dBm	675.32	mA
	13A_n66A CH346000 @ 23.15 dBm	693.91	mA
	13A_n66A CH349000 @ 23.17 dBm	687.35	mA
	13A_n66A CH352000 @ 23.12 dBm	699.42	mA
	12A_n78A CH623334 @ 23.24 dBm	637.24	mA
	12A_n78A CH636666 @ 23.12 dBm	643.01	mA
	12A_n78A CH650000 @ 23.09 dBm	639.93	mA
	25A_n41A CH509202 @ 22.94 dBm	733.89	mA

	25A_n41A CH518598 @ 23.17 dBm	743.84	mA
	25A_n41A CH528000 @ 23.1 dBm	743.37	mA
	66A_n2A CH372000 @ 22.92 dBm	746.34	mA
	66A_n2A CH376000 @ 22.78 dBm	758.65	mA
	66A_n2A CH380000 @ 22.8 dBm	749.81	mA
	66A_n5A CH166800 @ 22.69 dBm	674.73	mA
	66A_n5A CH167300 @ 22.66 dBm	673.71	mA
	66A_n5A CH167800 @ 22.75 dBm	675.85	mA
	66A_n25A CH372000 @ 23.11 dBm	835.71	mA
	66A_n25A CH376500 @ 23.08 dBm	837.82	mA
	66A_n25A CH381000 @ 23.05 dBm	846.44	mA
	66A_n41A CH509202 @ 23.27 dBm	741.53	mA
	66A_n41A CH518598 @ 23.23 dBm	746.54	mA
	66A_n41A CH528000 @ 23.21 dBm	742.54	mA
	66A_n48A CH638000 @ 23.10 dBm	701.00	mA
	66A_n48A CH641666 @ 23.15 dBm	701.00	mA
	66A_n48A CH645332 @ 23.04 dBm	700.00	mA
	66A_n71A CH134600 @ 23.04 dBm	667.87	mA
	66A_n71A CH136100 @ 22.96 dBm	656.82	mA
	66A_n71A CH137600 @ 22.95 dBm	669.82	mA
	66A_n77A CH623334 @ 22.96 dBm	780.00	mA
	66A_n77A CH650000 @ 23.16 dBm	781.00	mA
	66A_n77A CH676666 @ 23.14 dBm	795.00	mA
	66A_n78A CH623334 @ 23.29 dBm	750.79	mA
	66A_n78A CH636666 @ 23.25 dBm	770.55	mA
	66A_n78A CH650000 @ 23.34 dBm	762.80	mA

	71A_n2A CH372000 @ 23.01 dBm	695.76	mA
	71A_n2A CH376000 @ 23.04 dBm	683.49	mA
	71A_n2A CH380000 @ 22.93 dBm	672.32	mA
	71A_n66A CH346000 @ 23.24 dBm	724.66	mA
	71A_n66A CH349000 @ 23.25 dBm	729.19	mA
	71A_n66A CH352000 @ 23.21 dBm	728.32	mA

6.3.6. AG551Q-NA Power Consumption

Table 56: AG551Q-NA Power Consumption (25 °C, 3.8 V Power Supply)

Test Mode	Test Condition	Typ.	Unit
OFF state	Power down	30	μA
Sleep state	**AT+CFUN = 0** (USB Disconnected)	1.11	mA
	AT+CFUN = 4 (USB Disconnected)	1.26	mA
	PCS1900 @ DRX = 2	3.08	mA
	PCS1900 @ DRX = 5	2.00	mA
	PCS1900 @ DRX = 5 (USB Suspend)	4.71	mA
	PCS1900 @ DRX = 9	1.94	mA
	LTE-FDD @ DRX = 0.32 s	4.31	mA
	LTE-FDD @ DRX = 0.64 s	2.77	mA
	LTE-FDD @ DRX = 0.64 s (USB Suspend)	5.72	mA
	LTE-FDD @ DRX = 1.28s	2.04	mA
	LTE-FDD @ DRX = 2.56 s	1.91	mA
	LTE-TDD @ DRX = 0.32 s	4.36	mA
	LTE-TDD @ DRX = 0.64 s	2.79	mA
	LTE-TDD @ DRX = 0.64 s (USB Suspend)	5.78	mA
	LTE-TDD @ DRX = 1.28 s	2.09	mA

	LTE-TDD @ DRX = 2.56 s	1.94	mA
	5G NR FDD @ DRX = 0.32 s	12.38	mA
	5G NR FDD @ DRX = 0.64 s	6.80	mA
	5G NR FDD @ DRX = 0.64 s (USB Suspend)	10.09	mA
	5G NR FDD @ DRX = 1.28 s	3.91	mA
	5G NR FDD @ DRX = 2.56 s	2.88	mA
	5G NR TDD @ DRX = 0.32 s	12.36	mA
	5G NR TDD @ DRX = 0.64 s	6.75	mA
	5G NR TDD @DRX = 0.64 s (USB Suspend)	10.11	mA
	5G NR TDD @ DRX = 1.28 s	3.88	mA
	5G NR TDD @ DRX = 2.56 s	3.41	mA
Idle state	PCS1900 CH62 @ DRX = 5	15.79	mA
	PCS1900 CH62 @ DRX = 5 (USB Active)	46.68	mA
	LTE-FDD @ DRX = 0.64 s	16.63	mA
	LTE-FDD @ DRX = 0.64 s (USB Active)	47.46	mA
	LTE-TDD @ DRX = 0.64 s	16.63	mA
	LTE-TDD @ DRX = 0.64 s (USB Active)	47.48	mA
	5G NR FDD @ DRX = 0.64 s	21.10	mA
	5G NR FDD @ DRX = 0.64 s (USB Active)	51.80	mA
	5G NR TDD @ DRX = 0.64 s	20.13	mA
	5G NR TDD @ DRX = 0.64 s (USB Active)	50.72	mA
LTE data transfer (GNSS OFF)	LTE-FDD B2 CH18700 @ 23.33 dBm	702.80	mA
	LTE-FDD B2 CH18900 @ 23.31 dBm	635.64	mA
	LTE-FDD B2 CH19100 @ 23.31 dBm	647.25	mA
	LTE-FDD B4 CH20050 @ 23.28 dBm	668.57	mA
	LTE-FDD B4 CH20175 @ 23.35 dBm	613.74	mA

	LTE-FDD B4 CH20300 @ 23.28 dBm	652.09	mA
	LTE-FDD B5 CH20450 @ 23.33 dBm	521.63	mA
	LTE-FDD B5 CH20525 @ 23.37 dBm	495.34	mA
	LTE-FDD B5 CH20600 @ 23.34 dBm	504.46	mA
	LTE-FDD B7 CH20850 @ 23.22 dBm	660.95	mA
	LTE-FDD B7 CH21100 @ 23.21 dBm	628.49	mA
	LTE-FDD B7 CH21350 @ 23.25 dBm	647.65	mA
	LTE-FDD B12 CH23060 @ 23.36 dBm	466.06	mA
	LTE-FDD B12 CH23095 @ 23.37 dBm	473.13	mA
	LTE-FDD B12 CH23130 @ 23.44 dBm	463.79	mA
	LTE-FDD B13 CH23230 @ 23.39 dBm	535.74	mA
	LTE-FDD B14 CH23330 @ 23.33 dBm	460.06	mA
	LTE-FDD B17 CH23780 @ 23.4 dBm	469.45	mA
	LTE-FDD B17 CH23790 @ 23.36 dBm	460.93	mA
	LTE-FDD B17 CH23800 @ 23.48 dBm	458.54	mA
	LTE-FDD B25 CH26140 @ 23.33 dBm	718.96	mA
	LTE-FDD B25 CH26365 @ 23.34 dBm	658.90	mA
	LTE-FDD B25 CH26590 @ 23.36 dBm	639.72	mA
	LTE-FDD B26 CH26765 @ 23.2 dBm	529.26	mA
	LTE-FDD B26 CH26865 @ 23.26 dBm	513.15	mA
	LTE-FDD B26 CH26965 @ 23.23 dBm	503.69	mA
	LTE-FDD B28 CH27310 @ 23.34 dBm	516.95	mA
	LTE-FDD B28 CH27435 @ 23.47 dBm	484.49	mA
	LTE-FDD B28 CH27560 @ 23.37 dBm	456.29	mA
	LTE-FDD B66 CH132072 @ 23.31 dBm	669.24	mA
	LTE-FDD B66 CH132322 @ 23.31 dBm	717.27	mA

	LTE-FDD B66 CH132572 @ 23.32 dBm	651.04	mA
	LTE-FDD B71 CH133222 @ 23.38 dBm	526.19	mA
	LTE-FDD B71 CH133322 @ 23.36 dBm	480.66	mA
	LTE-FDD B71 CH133372 @ 23.4 dBm	476.60	mA
	LTE-TDD B41 CH39750 @ 23.12 dBm	358.98	mA
	LTE-TDD B41 CH40620 @ 23.11 dBm	339.28	mA
	LTE-TDD B41 CH41490 @ 22.94 dBm	354.41	mA
	LTE-TDD B48 CH55340 @ 23.09 dBm	417.14	mA
	LTE-TDD B48 CH55990 @ 23.02 dBm	417.33	mA
	LTE-TDD B48 CH56640 @ 22.99 dBm	416.35	mA
GSM voice call	PCS1900 CH512 PCL = 0 @ 29.51 dBm	206.10	mA
	PCS1900 CH661 PCL = 0 @ 29.64 dBm	210.20	mA
	PCS1900 CH661 PCL = 0 @ 15.77 dBm	87.90	mA
	PCS1900 CH661 PCL = 7 @ 0.12 dBm	81.20	mA
	PCS1900 CH810 PCL = 15 @ 29.67 dBm	207.70	mA
GPRS data transfer (GNSS OFF)	PCS1900 CH512 1DL4UL @ 26.36 dBm	432.20	mA
	PCS1900 CH661 4DL 1UL @ 29.45 dBm	197.50	mA
	PCS1900 CH661 3DL 2UL @ 29.36 dBm	329.00	mA
	PCS1900 CH661 2DL 3UL @ 27.56 dBm	383.30	mA
	PCS1900 CH661 1DL 4UL @ 27.76 dBm	497.60	mA
	PCS1900 CH810 1DL 4UL @ 26.61 dBm	445.90	mA
EDGE data transfer (GNSS OFF)	PCS1900 CH512 1DL 4UL @ 22.30 dBm	302.50	mA
	PCS1900 CH661 4DL 1UL @ 25.69 dBm	146.60	mA
	PCS1900 CH661 3DL 2UL @ 25.62 dBm	230.80	mA
	PCS1900 CH661 2DL 3UL @ 23.65 dBm	268.40	mA
	PCS1900 CH661 1DL 4UL @ 22.24 dBm	302.10	mA

	PCS1900 CH810 1DL 4UL @ 22.69 dBm	311.30	mA
5G NR SA data transfer (GNSS OFF)	n2A CH372000 @ 23.11 dBm	528.96	mA
	n2A CH376000 @ 23.15 dBm	532.29	mA
	n2A CH380000 @ 22.85 dBm	515.28	mA
	n5A CH166800 @ 22.72 dBm	432.00	mA
	n5A CH167300 @ 22.64 dBm	432.54	mA
	n5A CH167800 @ 22.73 dBm	429.63	mA
	n25A CH372000 @ 23.61 dBm	637.22	mA
	n25A CH376500 @ 23.59 dBm	621.70	mA
	n25A CH381000 @ 23.54 dBm	654.72	mA
	n66A CH346000 @ 22.97 dBm	539.33	mA
	n66A CH349000 @ 23.04 dBm	580.52	mA
	n66A CH352000 @ 22.97 dBm	566.05	mA
	n71A CH134600 @ 22.84 dBm	418.54	mA
	n71A CH136100 @ 22.69 dBm	403.92	mA
	n71A CH137600 @ 22.67 dBm	429.08	mA
	n41A CH509202 @ 25.98 dBm	510.75	mA
	n41A CH518598 @ 26.31 dBm	530.13	mA
	n41A CH528000 @ 26.18 dBm	531.25	mA
	n48A CH638000 @ 23.27 dBm	332.00	mA
	n48A CH641666 @ 23.28 dBm	328.00	mA
	n48A CH645332 @ 23.14 dBm	328.00	mA
	n77A CH623334 @ 25.11 dBm	411.00	mA
	n77A CH650000 @ 25.83 dBm	427.00	mA
	n77A CH676666 @ 25.51 dBm	434.00	mA
	n78A CH623334 @ 25.19 dBm	418.83	mA

	n78A CH636666 @ 25.81 dBm	451.43	mA
	n78A CH650000 @ 25.48 dBm	424.73	mA
5G NR NSA data transfer (GNSS OFF)	2A_n5A CH166800 @ 22.52 dBm	661.92	mA
	2A_n5A CH167300 @ 22.53 dBm	666.21	mA
	2A_n5A CH167800 @ 22.44 dBm	667.53	mA
	2A_n41A CH509202 @ 22.85 dBm	769.37	mA
	2A_n41A CH518598 @ 23.17 dBm	783.62	mA
	2A_n41A CH528000 @ 23.27 dBm	776.22	mA
	2A_n48A CH638000 @ 23.08 dBm	734.00	mA
	2A_n48A CH641666 @ 22.91 dBm	730.00	mA
	2A_n48A CH645322 @ 22.78 dBm	728.00	mA
	2A_n66A CH344000 @ 23.04 dBm	777.96	mA
	2A_n66A CH349000 @ 22.74 dBm	735.50	mA
	2A_n66A CH354000 @ 22.57 dBm	733.65	mA
	2A_n71A CH134600 @ 22.75 dBm	661.73	mA
	2A_n71A CH136100 @ 22.74 dBm	674.82	mA
	2A_n71A CH137600 @ 22.65 dBm	665.88	mA
	2A_n77A CH623334 @ 22.79 dBm	808.00	mA
	2A_n77A CH650000 @ 22.96 dBm	813.00	mA
	2A_n77A CH676666 @ 22.82 dBm	827.00	mA
	2A_n78A CH623334 @ 23.03 dBm	759.79	mA
	2A_n78A CH636666 @ 23.16 dBm	765.98	mA
	2A_n78A CH650000 @ 22.81 dBm	751.70	mA
	5A_n2A CH372000 @ 23.1 dBm	669.48	mA
	5A_n2A CH376000 @ 22.83 dBm	660.21	mA
	5A_n2A CH380000 @ 22.83 dBm	667.46	mA

	5A_n41A CH509202 @ 22.92 dBm	693.82	mA
	5A_n41A CH518598 @ 23.16 dBm	713.39	mA
	5A_n41A CH528000 @ 23.23 dBm	707.53	mA
	5A_n48A CH638000 @ 23.33 dBm	615.00	mA
	5A_n48A CH641666 @ 22.86 dBm	610.00	mA
	5A_n48A CH645322 @ 22.75 dBm	610.00	mA
	5A_n66A CH344000 @ 23.21 dBm	703.80	mA
	5A_n66A CH349000 @ 22.69 dBm	666.34	mA
	5A_n66A CH354000 @ 22.76 dBm	675.70	mA
	5A_n77A CH623334 @ 22.93 dBm	701.00	mA
	5A_n77A CH650000 @ 22.91 dBm	695.00	mA
	5A_n77A CH676666 @ 22.76 dBm	699.00	mA
	5A_n78A CH623334 @ 23.07 dBm	696.08	mA
	5A_n78A CH636666 @ 23.01 dBm	705.99	mA
	5A_n78A CH650000 @ 22.92 dBm	694.05	mA
	7A_n77A CH623334 @ 22.97 dBm	813.00	mA
	7A_n77A CH650000 @ 23.31 dBm	828.00	mA
	7A_n77A CH676666 @ 23.37 dBm	836.00	mA
	12A_n2A CH372000 @ 23.01 dBm	675.08	mA
	12A_n2A CH376000 @ 22.71 dBm	653.88	mA
	12A_n2A CH380000 @ 22.75 dBm	662.43	mA
	12A_n25A CH372000 @ 23.05 dBm	902.25	mA
	12A_n25A CH376500 @ 23.15 dBm	912.16	mA
	12A_n25A CH381000 @ 23.09 dBm	877.99	mA
	12A_n66A CH344000 @ 23.14 dBm	698.42	mA
	12A_n66A CH349000 @ 22.72 dBm	657.17	mA

	12A_n66A CH354000 @ 22.7 dBm	666.29	mA
	12A_n77A CH623334 @ 22.87 dBm	687.00	mA
	12A_n77A CH650000 @ 23.20 dBm	688.00	mA
	12A_n77A CH676666 @ 23.10 dBm	696.00	mA
	13A_n2A CH372000 @ 22.79 dBm	727.34	mA
	13A_n2A CH376000 @ 23.02 dBm	723.29	mA
	13A_n2A CH380000 @ 22.84 dBm	734.58	mA
	13A_n66A CH344000 @ 23.15 dBm	761.19	mA
	13A_n66A CH349000 @ 23.3 dBm	757.53	mA
	13A_n66A CH354000 @ 22.6 dBm	812.99	mA
	12A_n78A CH623334 @ 22.85 dBm	688.07	mA
	12A_n78A CH636666 @ 23.22 dBm	694.63	mA
	12A_n78A CH650000 @ 22.83 dBm	685.89	mA
	25A_n41A CH509202 @ 22.87 dBm	770.60	mA
	25A_n41A CH518598 @ 23.12 dBm	790.93	mA
	25A_n41A CH528000 @ 23.2 dBm	782.61	mA
	66A_n2A CH372000 @ 23.25 dBm	735.06	mA
	66A_n2A CH376000 @ 22.87 dBm	735.84	mA
	66A_n2A CH380000 @ 22.9 dBm	747.61	mA
	66A_n5A CH166800 @ 22.61 dBm	660.96	mA
	66A_n5A CH167300 @ 22.66 dBm	662.12	mA
	66A_n5A CH167800 @ 22.62 dBm	663.00	mA
	66A_n25A CH372000 @ 22.93 dBm	913.32	mA
	66A_n25A CH376500 @ 22.7 dBm	924.72	mA
	66A_n25A CH381000 @ 22.74 dBm	932.42	mA
	66A_n41A CH509202 @ 22.74 dBm	764.44	mA

	66A_n41A CH518598 @ 23.26 dBm	783.58	mA
	66A_n41A CH528000 @ 23.22 dBm	781.59	mA
	66A_n48A CH638000 @ 23.13 dBm	722.00	mA
	66A_n48A CH641666 @ 23.12 dBm	718.00	mA
	66A_n48A CH645322 @ 22.84 dBm	719.00	mA
	66A_n71A CH134600 @ 22.82 dBm	655.43	mA
	66A_n71A CH136100 @ 22.81 dBm	664.98	mA
	66A_n71A CH137600 @ 22.73 dBm	659.81	mA
	66A_n77A CH623334 @ 22.78 dBm	806.00	mA
	66A_n77A CH650000 @ 22.97 dBm	811.00	mA
	66A_n77A CH676666 @ 22.82 dBm	818.00	mA
	66A_n78A CH623334 @ 22.95 dBm	761.37	mA
	66A_n78A CH636666 @ 23.21 dBm	769.42	mA
	66A_n78A CH650000 @ 22.83 dBm	757.18	mA
	71A_n2A CH372000 @ 23.12 dBm	687.47	mA
	71A_n2A CH376000 @ 22.98 dBm	681.45	mA
	71A_n2A CH380000 @ 22.97 dBm	689.48	mA
	71A_n66A CH344000 @ 23.18 dBm	725.66	mA
	71A_n66A CH349000 @ 22.85 dBm	690.42	mA
	71A_n66A CH354000 @ 22.78 dBm	695.59	mA

NOTE

The power consumption data of AG553Q-EU will be provided in a future version of the document.

6.4. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

The following table shows the module electrostatic discharge characteristics.

Table 57: Electrostatic Discharge Characteristics (Temperature: 25–30 ºC, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±6	±10	kV
Antenna Interfaces	±6	±10	kV
Other Interfaces	±0.5	±1	kV

6.5. Operating and Storage Temperatures

Table 58: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [37]	-35	+25	+75	ºC
Extended Temperature Range [38]	-40	-	+85	ºC
eCall Temperature Range [39]	-40	-	+95	ºC
Storage Temperature Range	-40	-	+95	ºC

[37] Within the operating temperature range, the module meets 3GPP specifications.
[38] Within the extended temperature range, the module remains fully functional and the ability to establish and maintain functions such as voice, SMS, data transmission, emergency call, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.
[39] Within eCall temperature range, the emergency call function must be functional until the module is broken. When the ambient temperature is between 75 °C and 95 °C and the module temperature has reached the threshold value, the module will trigger protective measures (such as reduce power, decrease throughput, unregister the device, etc.) to ensure the full function of emergency call.

6.6. Thermal Dissipation

To achieve better performance of the module, it is recommended to comply with the following principles for thermal consideration:

- On your PCB design, please keep placement of the module away from heating sources, especially high-power components such as ARM processor, audio power amplifier, power supply, etc.
- Do not place components on the opposite side of the PCB area where the module is mounted, in order to facilitate adding of heatsink when necessary.
- Do not apply solder mask on the opposite side of the PCB area where the module is mounted, so as to ensure better heat dissipation performance.
- The reference ground of the area where the module is mounted should be complete, and add ground vias as many as possible for better heat dissipation. Through-holes will create better heat dissipation performance.
- Ensure the ground pads of the module and PCB are fully connected.
- According to customers' application demands, the heatsink can be mounted on the top of the module, or the opposite side of the PCB area where the module is mounted, or both of them [40].
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between the heatsink and module/PCB.

The following shows two kinds of heatsink designs for reference and customers can choose one or both of them according to their application structure.

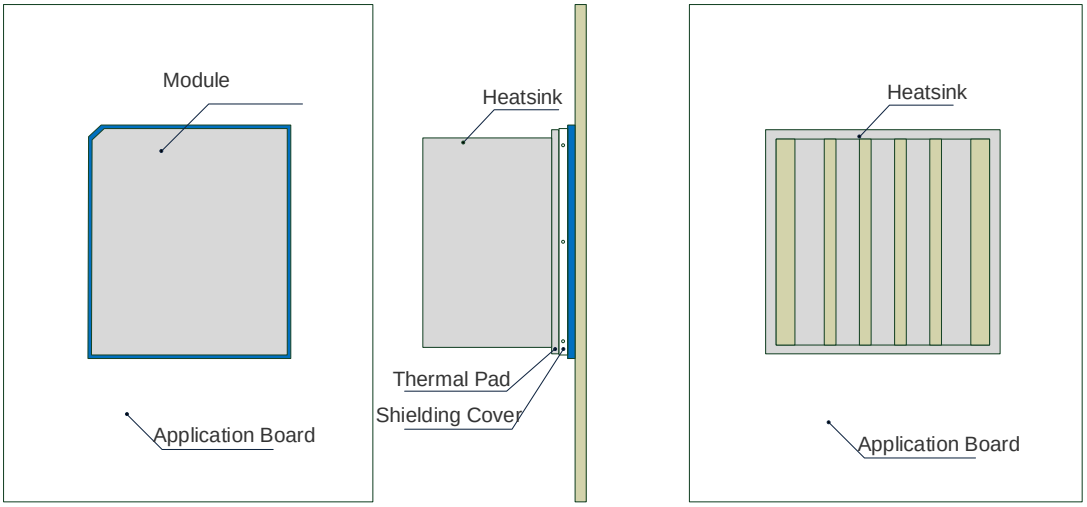


Figure 45: Referenced Heatsink Design (Heatsink at the Top of the Module)

[40] It is recommended to add the heat sink on the top of the module.

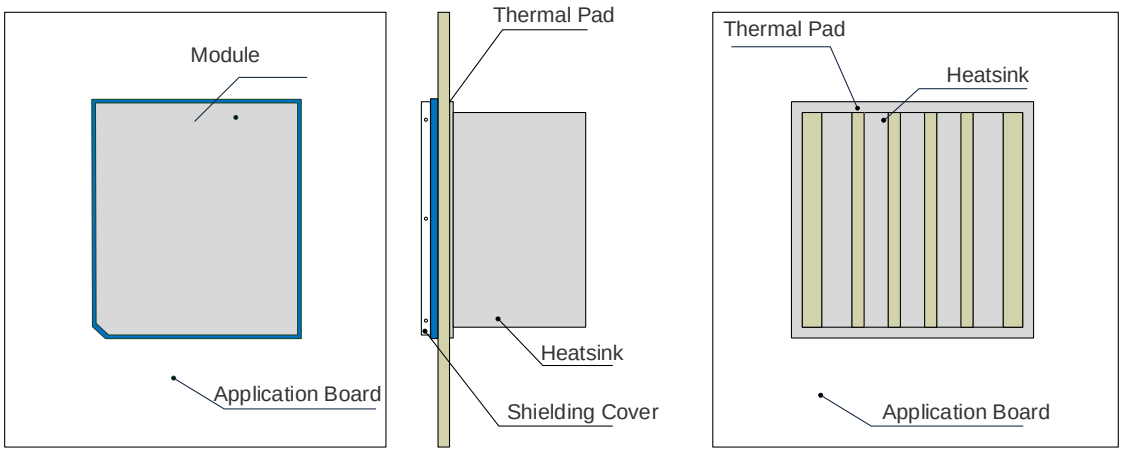


Figure 46: Referenced Heatsink Design (Heatsink at the Backside of Customers' PCB)

NOTE

1. When the BB chip temperature reaches the set thresholds, the module will implement corresponding thermal management solutions, such as data rate fallback, transmitting power reduction, and Limited Service Mode, to protect the module. When the BB chip temperature exceeds 105 °C, the module detaches from the network and enters Limited Service Mode in which only emergency call is available. Therefore, the thermal design should be maximally optimized to ensure normal module performance. See ***document [14]*** for detailed information on software thermal management.
2. For more detailed introduction on hardware thermal design, see ***document [15]*** and thermal simulation report of AG55xQ family.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

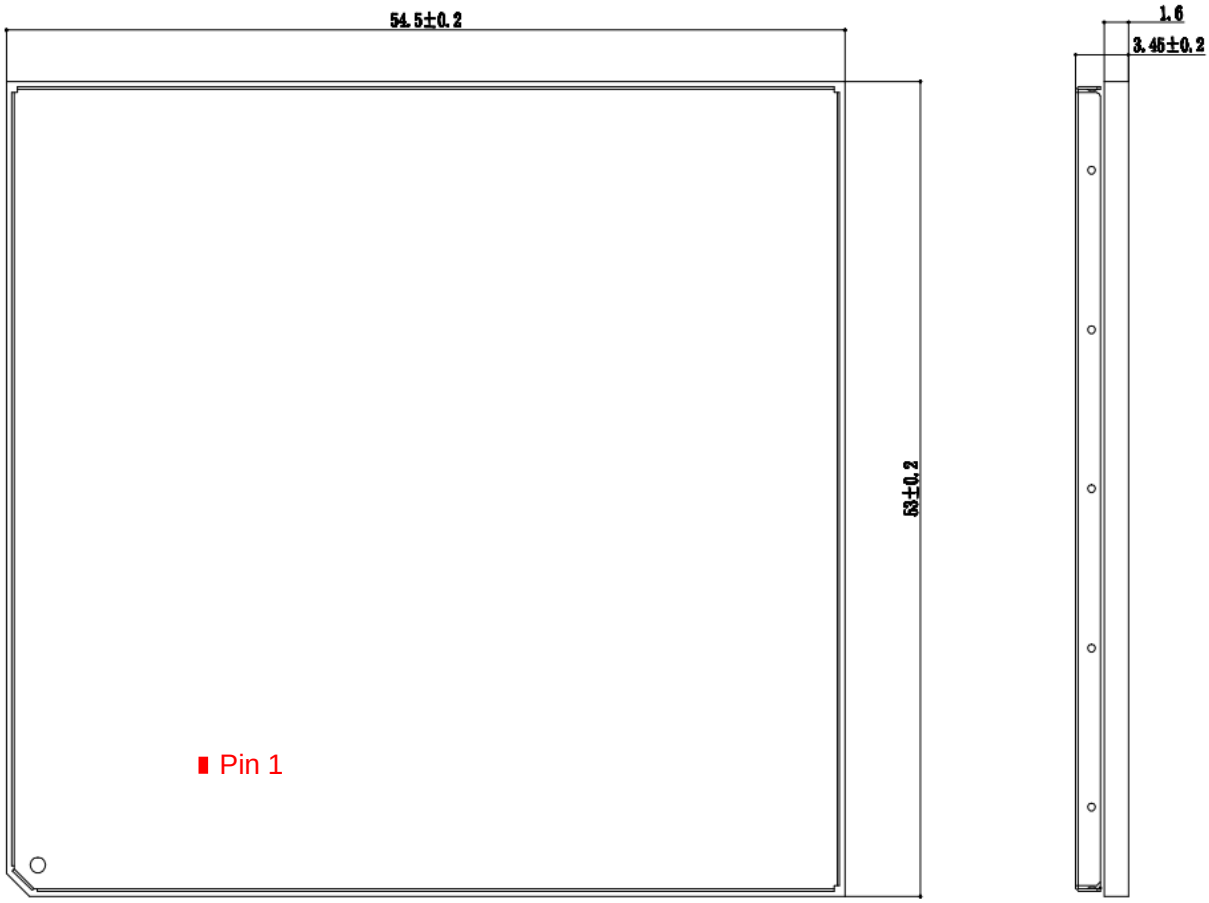


Figure 47: Module Top and Side Dimensions

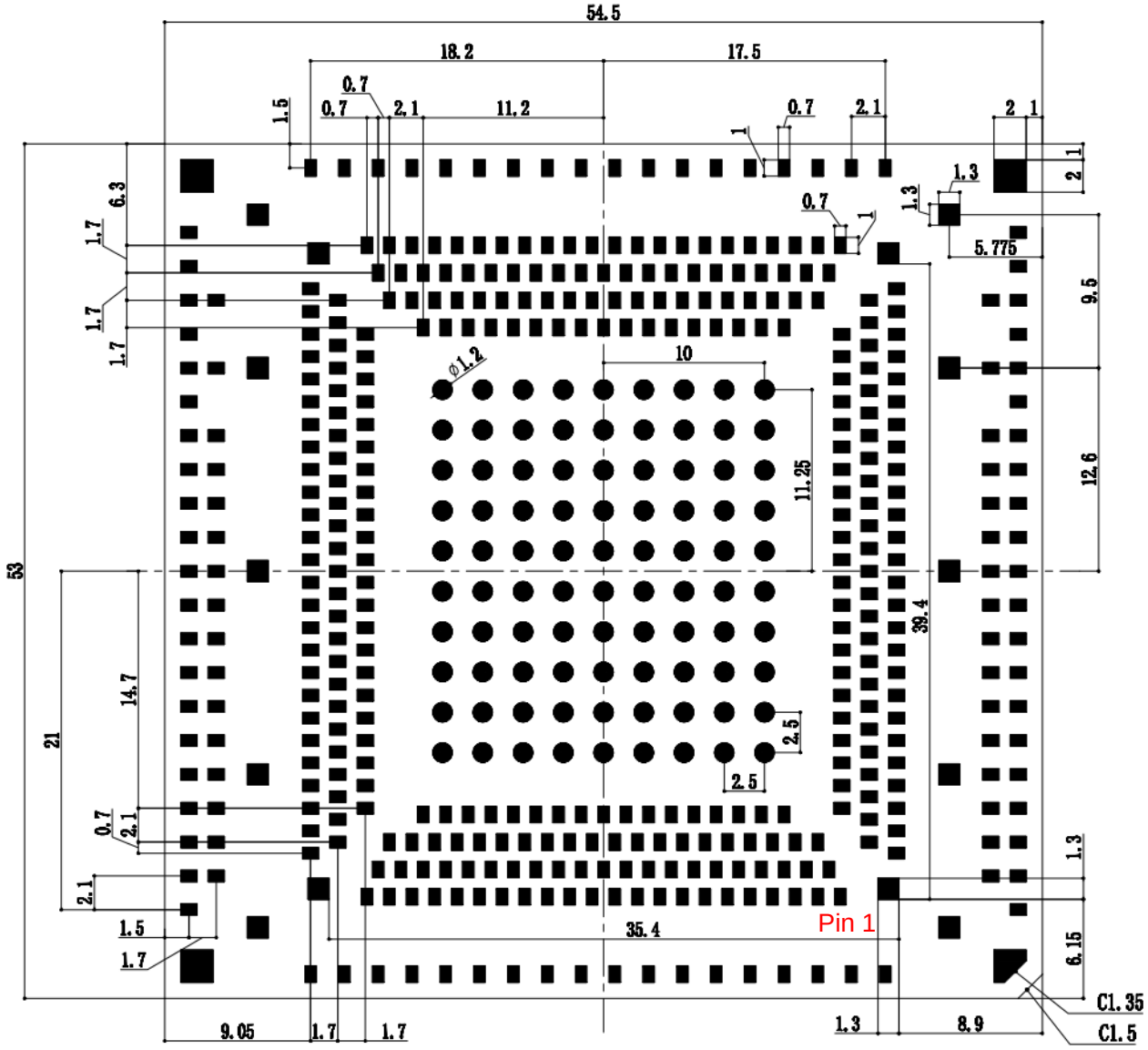


Figure 48: Module Bottom Dimensions (Unit: mm)

NOTE

The package warpage level of the module conforms to *JEITA ED-7306* standard.

7.2. Recommended Footprint

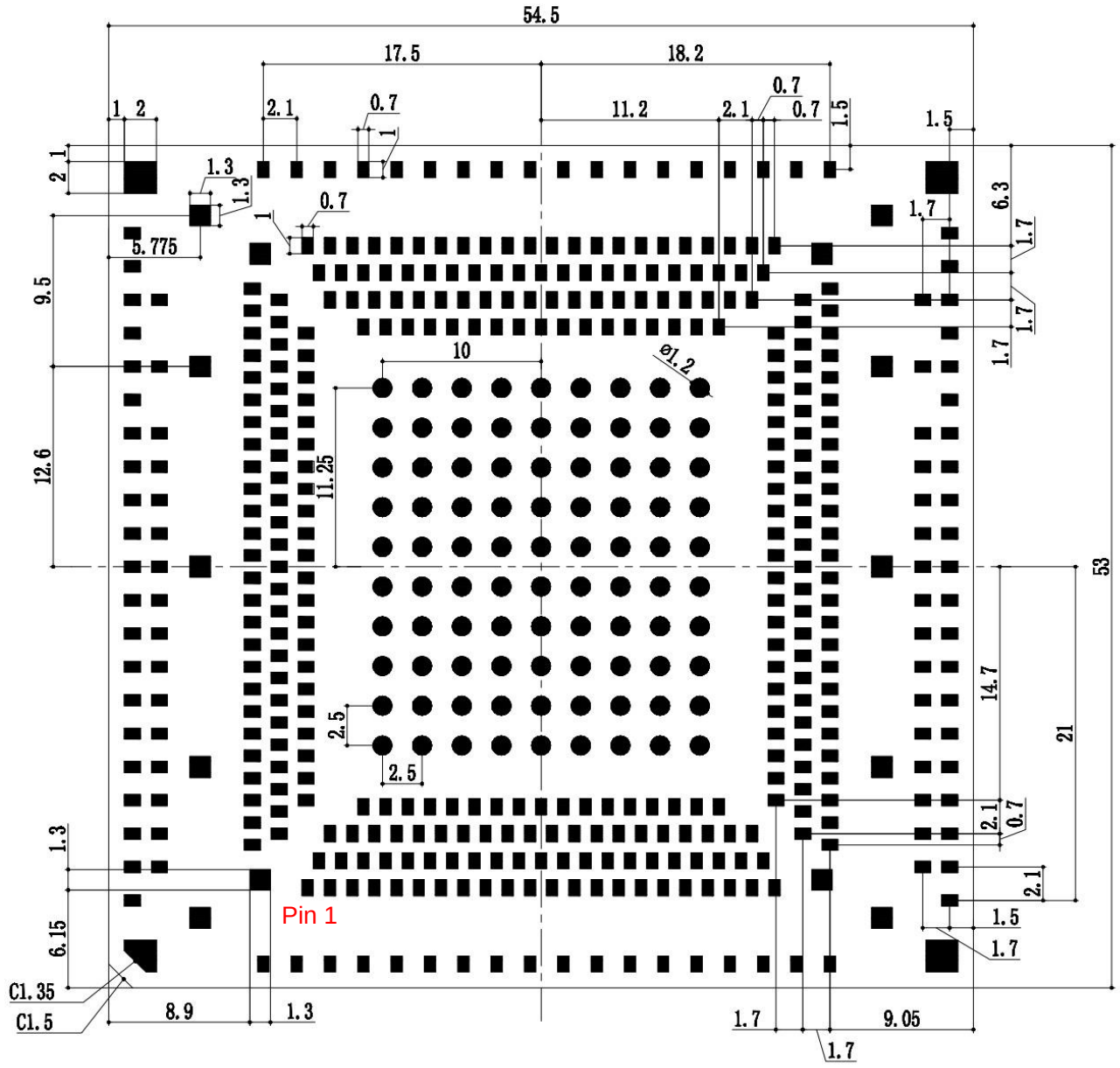


Figure 49: Recommended Footprint (Perspective View) (Unit: mm)

NOTE

1. For easy maintenance of the module, keep about 3 mm between the module and other components on the motherboard.
2. Non-Solder Mask Defined (NSMD) pads preferred.

7.3. Top and Bottom Views

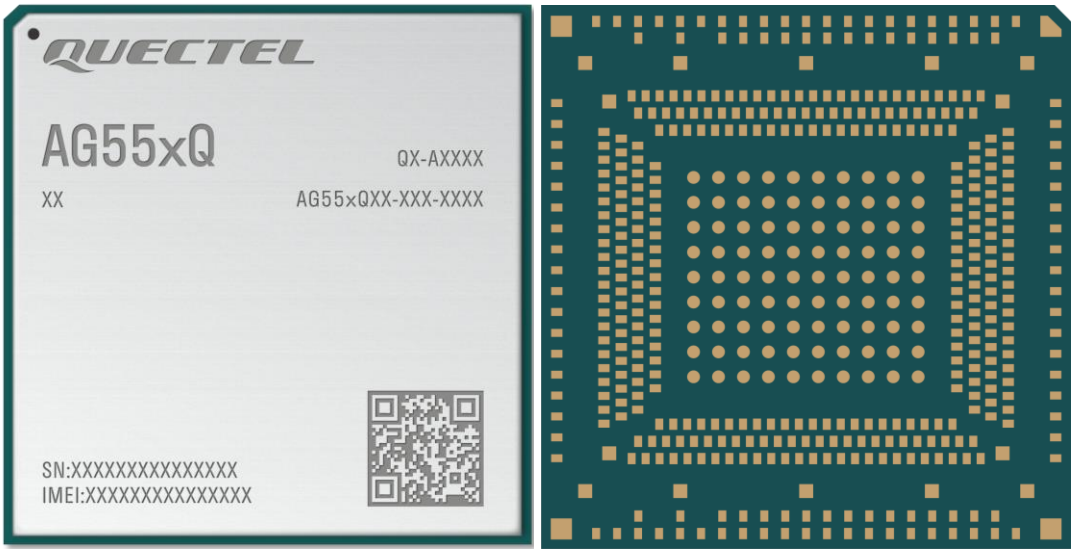


Figure 50: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours[41] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

[41] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [16]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

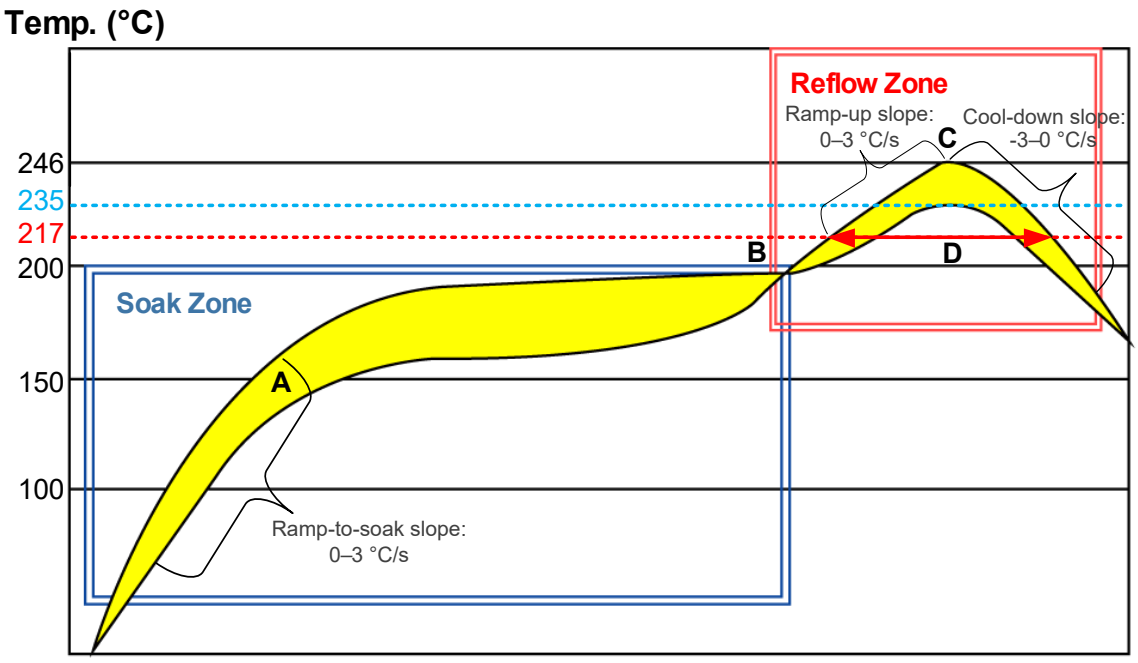


Figure 51: Recommended Reflow Soldering Thermal Profile

Table 59: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
3. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
4. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [16]***.

8.3. Packaging Specification

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and one reel is 12.24 meters long. The packaging details are

as follow.

8.3.1. Carrier Tape

Dimension details are as follow:

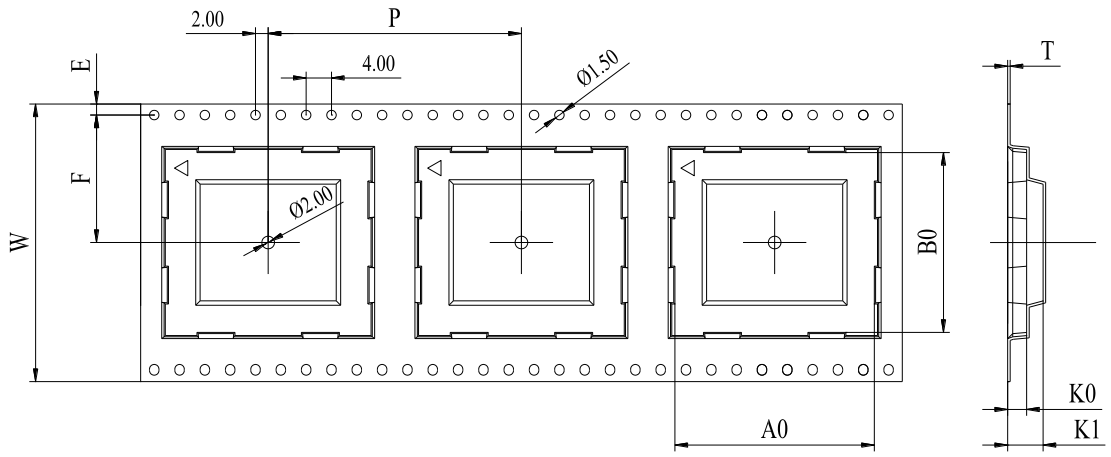


Figure 52: Carrier Tape Dimension Drawing

Table 60: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
72	72	0.4	53.7	55.2	4.85	5.35	34.2	1.75

8.3.2. Plastic Reel

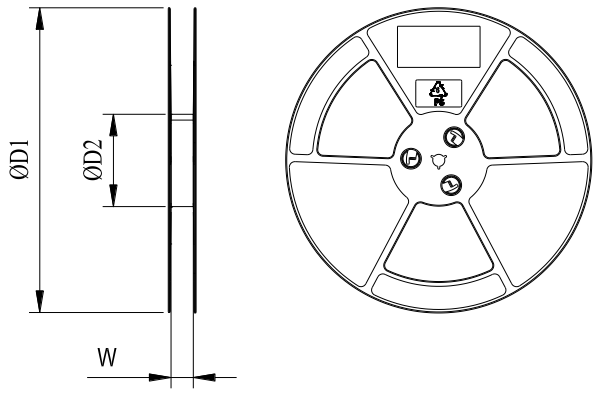
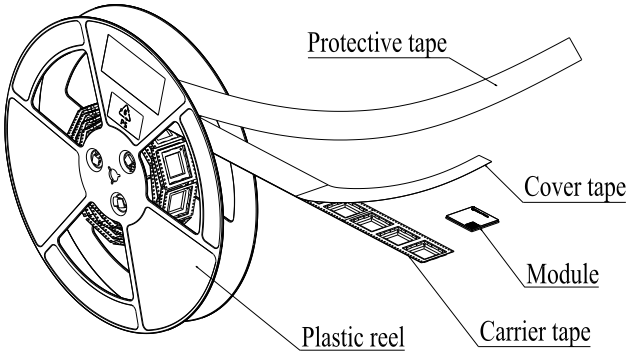


Figure 53: Plastic Reel Dimension Drawing

Table 61: Plastic Reel Dimension Table (Unit: mm)

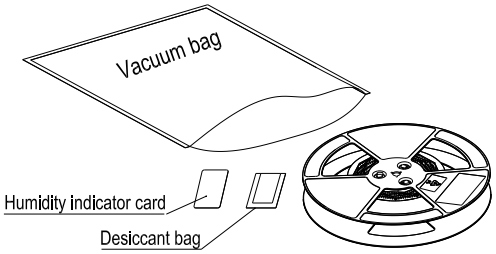
øD1	øD2	W
380	178	72.5

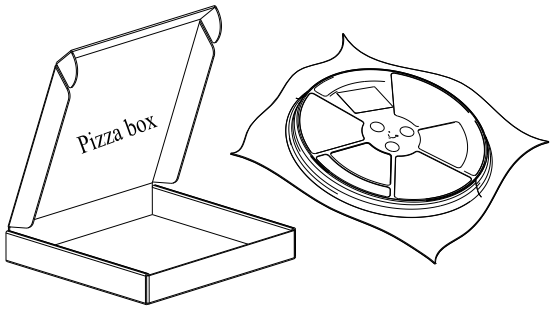
8.3.3. Packaging Process



Place the modules into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 150 modules.

Place the packaged plastic reel, a humidity indicator card and a desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 600 modules.

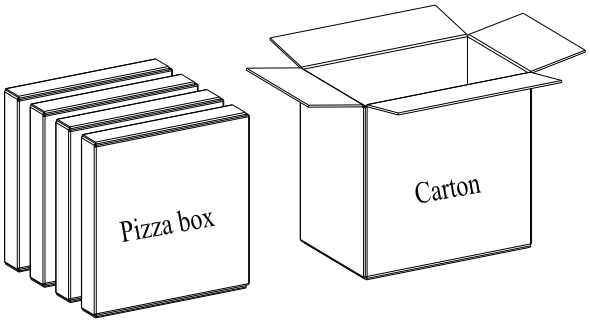


Figure 54: Packaging Process

8.3.4. Packaging Specification

Table 62: Packaging Specification

Model Name	MOQ for MP	Minimum Package: 150 pcs	Minimum Package × 4 = 600 pcs
AG55xQ family	150 pcs	Size (mm): 405 × 390 × 83	Size (mm): 425 × 358 × 410

9 Appendix References

Table 63: Related Documents

Document Name
[1] Quectel_AG55xQ_Series_QuecOpen_GPIO_Configuration
[2] Quectel_V2X&5G_EVB_User_Guide
[3] Quectel_AG55xQ&AG57xQ_Series_QuecOpen_Device_Management_API_Reference_Design
[4] Quectel_AG553Q-EU_QuecOpen_Device_Management_API_Reference_Design
[5] Quectel_AG55xQ&AG57xQ_Series_QuecOpen_AT_Commands_Manual
[6] Quectel_AG55xQ&AG57xQ_Series_QuecOpen_Low_Power_Mode_Application_Note
[7] Quectel_AG55xQ&AG57xQ_Series_QuecOpen_Audio_Development_Guide
[8] Quectel_AG55xQ_Series_QuecOpen_Reference_Design
[9] Quectel_AG55xQ&AG57xQ_Series_QuecOpen_ADC_Development_Guide
[10] Quectel_AG55xQ&AG57xQ_Series_QuecOpen_QDR&PPE_Application_Note
[11] Quectel_AG55xQ&AG57xQ_Series_QuecOpen_GNSS_API_Reference_Manual
[12] Quectel_AG55xQ_Series_QuecOpen_CA&EN-DC_Features
[13] Quectel_RF_Layout_Application_Note
[14] Quectel_AG55xQ&AG57xQ_Series_QuecOpen_Software_Thermal_Management_Guide
[15] Quectel_Module_Thermal_Design_Guide
[16] Quectel_Module_SMT_Application_Note

Table 64: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
5G NR	5G New Radio
AC	Alternating Current
ADC	Analog-to-Digital Converter
ADAS	Advanced Driver-assistant Systems
AMR	Adaptive Multi-rate
AP	Application Processor
API	Application Program Interface
AVTP	Audio/Video Transport Protocol
bps	Bits Per Second
BLSP	BAM Low-Speed Peripheral
BPSK	Binary Phase Shift Keying
BT	Bluetooth
CS	Coding Scheme
CTS	Clear to Send
C-V2X	Cellular Vehicle-to-Everything
DCE	Data Communications Equipment
DC-HSDPA	Dual Carrier High Speed Packet Access Plus
DCS	Data Communications Equipment
DFOTA	Delta Firmware Upgrade Over the Air
DL	Downlink
DR	Dead Reckoning
DRX	Discontinuous Reception

DSDA	Dual SIM Dual Active
DSSS	Dual SIM Single Standby
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EAVB	Ethernet Audio Video Bridging
EDGE	Enhanced Data Rates for GSM Evolution
EFR	Enhanced Full Rate
EGSM	Extended GSM900 Band (including standard GSM900 band)
EMI	Electromagnetic Interference
eMMC	Embedded Multimedia Card
EN-DC	E-UTRA-NR Dual Connectivity
EP	PCIe Endpoint
ESD	Electrostatic Discharge
EVB	Evaluation Board
EOS	Electrical Over Stress
FDD	Frequency Division Duplex
FEM	Front-End Module
FR	Full Rate
FTP	File Transfer Protocol
FQTSS	Forwarding and Queuing of Time Sensitive Streams
Galileo	Galileo satellite navigation system
GLONASS	Russian Global Navigation Satellite System
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPIO	General-purpose Input/Output

GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications
gPTP	General Precise Time Protocol
HPUE	High Power User Equipment
HR	Half Rate
HSDPA	High Speed Down Link Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
Imax	Maximum Load Current
IMEI	International Mobile Equipment Identity
IMU	Inertial Measurement Unit
I/O	Input/Output
ITS	Intelligent Transportation System
Inom	Normal Current
LAA	License Assisted Access
LDO	Low-dropout Regulator
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPM	Low Power Mode
LTE	Long Term Evolution
MAC	Medium Access Control
MCS	Modulation and Coding Scheme

MDIO	Management Data Input/Output
ME	Mobile Equipment
MIMO	Multiple Input Multiple Output
MMS	Multimedia Messaging Service
MHB	Middle/High Band
MO	Mobile Originated
MLCC	Multi-layer Ceramic Chip Capacitor
MT	Mobile Terminated
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
NSA	Non-Standalone
NTP	Network Time Protocol
OBU	On-board Units
PA	Power Amplifier
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PING	Packet Internet Groper
PMIC	Power Management IC
PPP	Point-to-Point Protocol
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RC	PCIe Root Complex

RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RSU	Roadside Units
RTC	Real-Time Clock
RTS	Ready To Send/Request to Send
RoHS	Restriction of Hazardous Substances
Rx	Receive
SA	Standalone
SCS	Sub-Carrier Space
SDIO	Secure Digital Input/Output
SIM	Subscriber Identity Module
SMD	Surface Mount Device
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SPI	Serial Peripheral Interface
SPK	Speaker
SSL	Secure Sockets Layer
SRP	Stream Reservation Protocol
TCP	Transmission Control Protocol
TCU	Telematics Control Units
TDD	Time Division Duplexing
TLS	Transport Layer Security
Tx	Transmitting Direction
XFEM	Extended Finite Element Method
t(ch)	Clock high

t(cl)	Clock low
t(mov)	Master output valid
t(mis)	Master input setup
t(mih)	Master input hold
UART	Universal Asynchronous Receiver & Transmitter
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
V_{I}max	Absolute Maximum Input Voltage
V_{I}min	Absolute Minimum Input Voltage
V_{OH}max	Maximum High-level Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio

V2I	Vehicle-to-Infrastructure
V2P	Vehicle-to-Pedestrian
V2V	Vehicle-to-Vehicle
WAN	Wide Area Network
WCDMA	Wideband Code Division Multiple Access
Wi-Fi	Wireless Fidelity
WLAN	Wireless Local Area Network

Product Marketing Name：Quectel AG550Q-NA

FCC Certification Requirements.

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.

And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source based timeaveraging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion

Requirements of 2.1091.

2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

3. A label with the following statements must be attached to the host end product: This device contains FCC ID: XMR2022AG550QNA

4. To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

radiation, maximum antenna gain (including cable loss) must not exceed: Operating Band	FCC Max Antenna Gain（dBi）
GSM1900	1.00
LTE B2/n2	8.00
LTE B4	5.00
LTE B5/n5	9.41
LTE B7	8.00
LTE B12	8.70
LTE B13	9.16
LTE B14	9.23
LTE B17	8.74
LTE B25/n25	8.00
LTE B26 (814-824)	9.36
LTE B26 (824-849)	9.41
LTE B41	8.00

LTE B48	-2.00
LTE B66/n66	5.00
NR Band n41	6.00
LTE B71/n71	8.48
NR Band n77	3.00
NR Band n78	3.00

5. This module must not transmit simultaneously with any other antenna or transmitter
6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

For this device, OEM integrators must be provided with labeling instructions of finished products.

Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: XMR2022AG550QNA" or "Contains FCC ID: XMR2022AG550QNA" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier's Declaration of Conformity procedure without

a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

IC Statement

IRSS-GEN

"This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device."The transmitter module may not be co-located with any other transmitter orantenna. or "Le présentappareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence.L'exploitation est autorisée aux deux conditions suivantes :

1) l'appareil ne doit pas produire de brouillage; 2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Déclaration sur l'exposition aux rayonnements RF

L'autre utilisépour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.

The host product shall be properly labeled to identify the modules within the host product.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word "Contains" or similar wording expressing the same meaning, as follows: "Contains IC: 10224A-2022AG550NA" or "where: 10224A-2022AG550NA is the module's certification number".

Le produit hôte doit être correctement étiquetép our identifier les modules dans le produit hôte.

L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installédans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, préc édéd u mot «Contient»o u d'un libellés emblable exprimant la même signification, comme suit:

"Contient IC: 10224A-2022AG550NA " ou "où: 10224A-2022AG550NA est le numéro de certification du module".