EC200U Series

Hardware Design

LTE Standard Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

About the Document

Revision History

Version	Date	Author	Description
-	2021-10-08	King MA/ Nathan LIU	Creation of the document
1.0	2021-11-05	King MA/ Nathan LIU	First official release
1.1.0	2022-03-01	Reuben WANG/ Nathan LIU	Added the related content of EC200U-AU

Contents

Table Index

Figure Index

1 Introduction

This document defines the EC200U series module and describes its air interface and hardware interfaces which are connected with your applications.

This document can help you quickly understand module interface specifications, electrical and mechanical details, as well as other related information of EC200U series module. To facilitate its application in different fields, relevant reference design is also provided for customers' reference. Associated with application note and user guide, you can use EC200U series module to design and set up wireless applications easily.

This document is applicable to the following variants:

- EC200U-CN
- EC200U-EU
- EC200U-AU

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	When an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin name, AT command, or argument is under development and currently not supported, unless otherwise specified.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO1_DATA[0:3] refers to all four SDIO1_DATA pins: SDIO1_DATA0, SDIO1_DATA1, SDIO1_DATA2 and SDIO1_DATA3.

2 Product Overview

2.1. General Description

EC200U series is a wireless communication module, which supports LTE-FDD, LTE-TDD, GSM/GPRS network data connection. It provides voice function for your special applications and also supports GNSS. The following table shows the frequency bands of the module.

Table 2: Frequency Bands of EC200U-CN Module

Network Mode	Frequency Band
LTE-FDD	B1/B3/B5/B8
LTE-TDD	B34/B38/B39/B40/B41
GSM [1]	GSM900/DCS1800
GNSS [2]	GPS, GLONASS, BeiDou, Galileo, QZSS
Bluetooth and Wi-Fi Scan [3]	Support

Table 3: Frequency Bands of EC200U-EU Module

Network Mode	Frequency Band
LTE-FDD	B1/B3/B5/B7/B8/B20/B28
LTE-TDD	B38/B40/B41
GSM [1]	GSM850/GSM900/DCS1800/PCS1900

[1] GSM is optional.
[2] GNSS function is optional.
[3] EC200U series supports Bluetooth and Wi-Fi Scan functions. Due to the shared antenna interface, the two functions cannot be used at the same time; Bluetooth and Wi-Fi Scan functions are optional (supported or not supported simultaneously), please contact Quectel Technical Supports for details.

GNSS [2]	GPS, GLONASS, BeiDou, Galileo, QZSS
Bluetooth and Wi-Fi Scan [3]	Support

Table 4: Frequency Bands of EC200U-AU Module

Network Mode	Frequency Band
LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B28/B66
LTE-TDD	B38/B40/B41
GSM [1]	GSM850/GSM900/DCS1800/PCS1900
GNSS [2]	GPS, GLONASS, BeiDou, Galileo, QZSS
Bluetooth and Wi-Fi Scan [3]	Support

With a compact profile of 28.0 mm × 31.0 mm × 2.4 mm, EC200U series can meet almost all requirements for M2M applications such as automotive, metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, tablet PC, etc.

EC200U series is an SMD type module which can be embedded into applications through 144 pins, including 80 LCC pins and 64 LGA pins.

2.2. Key Features

Table 5: Key Features of EC200U Series Module

Feature	Details
Power Supply	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	● Class 4 for EGSM850 ● Class 4 for EGSM900 ● Class 1 for DCS1800 ● Class 1 for PCS1900 ● Class 3 for LTE-FDD bands ● Class 3 for LTE-TDD bands
LTE Features	● Supports Cat 1 FDD and TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth

	● FDD: Max. 10 Mbps (DL), Max. 5 Mbps (UL) ● TDD: Max. 8.96 Mbps (DL), Max. 3.1 Mbps (UL)
GSM Features	**GPRS:** ● Supports GPRS multi-slot class 12 ● Coding scheme: CS-1, CS-2, CS-3 and CS-4 ● Max. 85.6 kbps (DL)/Max. 85.6 kbps (UL)
Internet Protocol Features	● Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS/ FTPS/SSL/FILE/MQTT/MMS protocols ● Supports PAP and CHAP for PPP connections
SMS	● Text and PDU mode ● Point to point MO and MT ● SMS cell broadcast ● SMS storage: Stored in (U) SIM card and ME, stored in ME by default
(U)SIM Interface	● Supports USIM/SIM card: 1.8/3.0 V ● Supports DSDS
Audio Features	● Supports one analog audio input and one analog audio output ● GSM: HR/FR/EFR/AMR/AMR-WB ● Supports echo cancellation and noise suppression
USB Interface	● Compliant with USB 2.0 specification (slave mode only); the data transfer rate can reach up to 480 Mbps ● Used for AT command communication, data transmission, software debugging, firmware upgrade ● Supports USB serial drivers for Windows 7/8/8.1/10, Linux 2.6–5.12, Android 4.x–11.x, etc.
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rates reach up to 921600 bps; 115200 bps by default ● Support MAIN_RTS and MAIN_CTS hardware flow control **Debug UART:** ● Used for Linux console and log output ● 921600 bps baud rates ● Can only be used as a debugging UART, not a general UART **Auxiliary UART**
I2C Interfaces	● Two I2C interfaces
SPI Interface	● SPI interface only supports master mode
SD Card Interface	● SD 2.0 protocol compliant
WLAN Application Interface*	● Supports SDIO 1.1 interface for WLAN function
LCD Interface	● LCD interface supporting SPI mode
Matrix keyboard	● Support 4 × 4 matrix keyboard

Interfaces	
ADC Interfaces	● Three ADC interfaces
USB_BOOT Interface	● Forced download interface
AT Commands	● Compliant with 3GPP TS 27.007, 3GPP TS 27.005 and Quectel enhanced AT commands
Network Indication	● NET_MODE and NET_STATUS to indicate network connectivity status
Antenna Interfaces	● Main antenna interface (ANT_MAIN), Wi-Fi Scan/Bluetooth antenna interface (ANT_BT/WIFI_SCAN) and GNSS [7] antenna interface (ANT_GNSS) ● 50 Ω impedance
Location	● Supports Wi-Fi Scan/GNSS [7]
Physical Characteristics	● Size: (28.0 ±0.15) mm × (31.0 ±0.15) mm × (2.4 ±0.2) mm ● Weight: approx. 4.1 g
Temperature Ranges	● Operating temperature range: -35 °C to +75 °C [8] ● Extended temperature range: -40 °C to +85 °C [9] ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	● USB interface or FOTA
RoHS	● All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of EC200U series and illustrates the major functional parts.

- Power management
- Baseband
- Flash
- Radio frequency
- Peripheral interfaces

[7] GNSS function is optional.
[8] Within operating temperature range, the module is 3GPP compliant.
[9] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

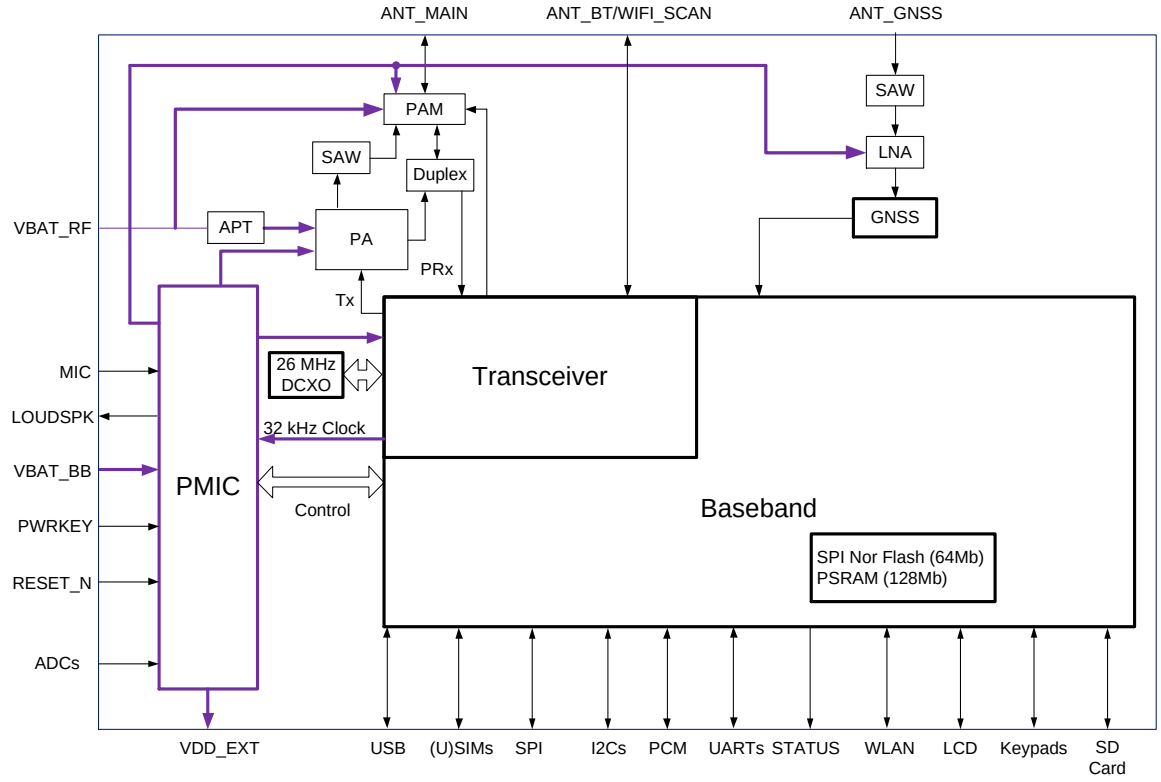


Figure 1: Functional Diagram

2.4. EVB

In order to help customers to develop applications with EC200U series, Quectel provides an evaluation board (UMTS & LTE EVB), USB to RS-232 converter cable, earphone, antennas and other peripherals to control or test the module. For more details, please refer to ***document [1]***.

3 Application Interfaces

3.1. General Description

EC200U series is equipped with 80 LCC pins plus 64 LGA pins that can be connected to cellular application platform. The subsequent chapters will provide detailed descriptions of the following interfaces.

- Power supply
- (U)SIM interfaces
- USB interface
- UART interfaces
- SPI interface
- PCM and I2C interfaces
- Analog audio interfaces
- LCD interface
- Matrix keyboard interface
- SD card interface
- WLAN application interface*
- ADC interfaces
- Status indications
- USB_BOOT interface

3.2. Pin Assignment

The following figure shows the pin assignment of EC200U series module.

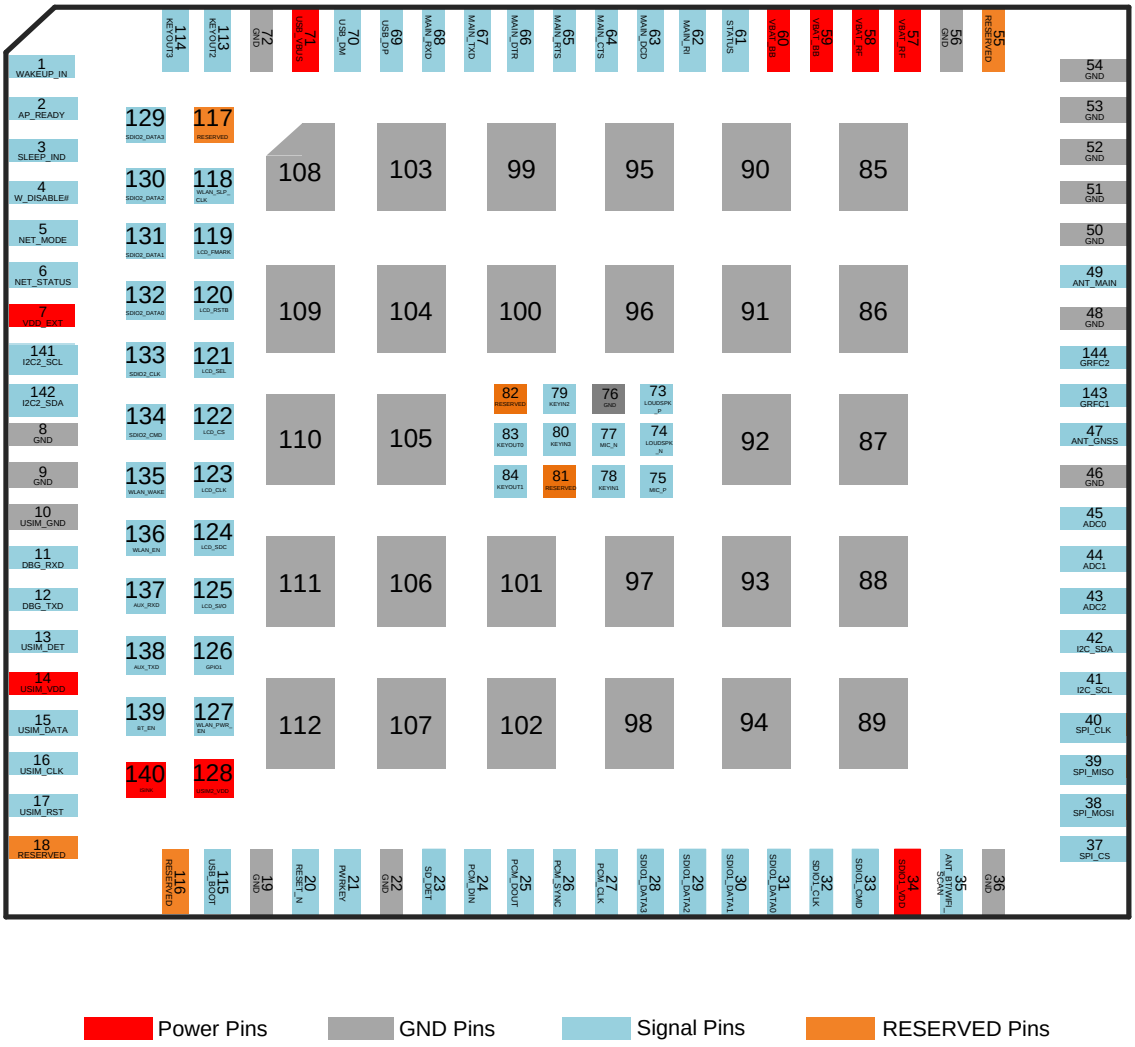


Figure 2: Pin Assignment (Top View)

NOTE

1. USB_BOOT and KEYIN1 cannot be pulled up before the module's successful startup.
2. Please keep all RESERVED and unused pins unconnected, and all GND pins are connected to the ground.
3. Pin 85–112 should be connected to the ground.

3.3. Pin Description

The following tables show the pin definition of EC200U series module.

Table 6: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

Table 7: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	59, 60	PI	Power supply for module's baseband part and RF part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 1.5 A.
VBAT_RF	57, 58	PI	Power supply for module's RF part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 2 A.
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 76, 85–112				
Module Output Power					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

VDD_EXT	7	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. Add 2.2 μF capacitor if used. If unused, keep it open.
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	21	DI	Turn on/off the module	V_{IL}max = 0.5 V	VBAT power domain
RESET_N	20	DI	Reset the module	V_{IL}max = 0.5 V	VBAT power domain. If unused, keep it open. Active low.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	61	DO	Indicate module's operating status		1.8 V power domain. If unused, keep it open.
NET_MODE	5	DO	Indicate the module's network activity status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
NET_STATUS	6	DO	Indicate the module's network registration mode	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	71	AI	Used for USB detection	Vmax = 5.25 V Vmin = 3.5 V Vnom = 5.0 V	Typical: 5.0 V If unused, keep it open.
USB_DP	69	AIO	USB differential data bus (+)		Require differential impedance of 90 Ω. USB 2.0 compliant. If unused, keep it open.
USB_DM	70	AIO	USB differential data bus (-)		Require differential impedance of 90 Ω. USB 2.0 compliant. If

					unused, keep it open.
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	10		(U)SIM1 card GND		Connect to the GND of (U)SIM card connector.
USIM_VDD	14	PO	(U)SIM1 card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V can be recognized by the module automatically.
USIM_DATA	15	DIO	(U)SIM1 card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{IL}max =1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_CLK	16	DO	(U)SIM1 card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_RST	17	DO	(U)SIM1 card reset	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_DET	13	DI	(U)SIM card	V_{IL}min = -0.3 V	1.8 V power domain.

			hot-plug detect	V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	If unused, keep it open.
USIM2_VDD	128	PO	(U)SIM2 card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V can be recognized by the module automatically.
AP_READY	2	DIO	(U)SIM card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	The (U)SIM2 function is optional. If the firmware version of the module supports the function of the (U)SIM2 card, the relevant functions of the (U)SIM2 card can be realized by multiplexing AP_READY, WAKEUP_IN, SLEEP_IND, and W_DISABLE#. For details, please consult Quectel Technical Supports.
WAKEUP_IN	1	DO	(U)SIM2 card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
SLEEP_IND	3	DI	(U)SIM2 card hot-plug detect	V_{IL}min = -0.3 V	
W_DISABLE#	4	DO	(U)SIM2 card reset	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

MAIN_RI	62	DO	Main UART ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_DCD	63	DO	Main UART data carrier detect	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
MAIN_CTS	64	DO	DTE clear to send signal from DCE	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	Connect to DTE's CTS. 1.8 V power domain. If unused, keep it open.
MAIN_RTS	65	DI	DTE request to send signal to DCE	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	Connect to DTE's RTS. 1.8 V power domain. If unused, keep it open.
MAIN_DTR	66	DI	Main UART data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Pull-up by default. Low level wakes up the module. If unused, keep it open.
MAIN_TXD	67	DO	Main UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_RXD	68	DI	Main UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	12	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
DBG_RXD	11	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
Auxiliary UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
AUX_RXD	137	DI	Auxiliary UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V	1.8 V power domain. If unused, keep it open.

				V_{IH}max = 2.0 V	
AUX_TXD	138	DO	Auxiliary UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC2	43	AI	General-purpose ADC interface	Voltage range: 0–VBAT_BB	Use 1 kΩ resistor in series. If unused, keep it open. The external resistor should be less than 100 kΩ when the voltage divider resistor applies.
ADC1	44	AI	General-purpose ADC interface	Voltage range: 0–VBAT_BB	
ADC0	45	AI	General-purpose ADC interface	Voltage range: 0–VBAT_BB	
Analog Audio Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LOUDSPK_P	73	AO	Loudspeaker differential output (+)		If unused, keep them open.
LOUDSPK_N	74	AO	Loudspeaker differential output (-)		
MIC_P	75	AI	Microphone analog input (+)		
MIC_N	77	AI	Microphone analog input (-)		
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	41	OD	I2C serial clock		Require external pull-up to 1.8 V if used. If unused, keep it open.
I2C_SDA	42	OD	I2C serial data		
I2C2_SCL	141	OD	I2C serial clock		
I2C2_SDA	142	OD	I2C serial data		
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

PCM_DIN	24	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
PCM_DOUT	25	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PCM_SYNC	26	DI	PCM data frame sync	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open. The PCM function only supports slave mode, not master mode.
PCM_CLK	27	DI	PCM clock	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CS	37	DO	SPI chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	If you use a module model that supports GNSS function, the SPI function of Pin 37–40 cannot be used and needs to be left unconnected.
SPI_MOSI	38	DO	SPI master mode output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SPI_MISO	39	DI	SPI master mode input		
SPI_CLK	40	DO	SPI clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCD Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD_FMARK	119	DI	LCD frame synchronization	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open.
LCD_RSTB	120	DO	LCD reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCD_SEL	121	-	Reserved	-	
LCD_CS	122	DO	LCD chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCD_CLK	123	DO	LCD clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCD_SDC	124	DO	LCD register selection	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCD_SI/O	125	DIO	LCD data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
ISINK	140	PI	Sink current input.	Imax = 200 mA	It is driven by the

			Backlight adjustment	Configurable current	current sink method, and connected to the backlight cathode, the brightness can be adjusted with current control.
Matrix Keyboard Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	115	DI	Matrix key input0		It can be multiplexed as KEYIN0 after startup.
KEYIN1	78	DI	Matrix key input1		1.8 V power domain. If unused, keep it open. The KEYIN1 cannot be pulled up before startup.
KEYIN2	79	DI	Matrix key input2		1.8 V power domain. If unused, keep them open.
KEYIN3	80	DI	Matrix key input3		
KEYOUT0	83	DO	Matrix key output0		
KEYOUT1	84	DO	Matrix key output1		
KEYOUT2	113	DO	Matrix key output2		
KEYOUT3	114	DO	Matrix key output3		
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_DET	23	DI	SD card detect		1.8 V power domain. If unused, keep it open.
SDIO1_DATA3	28	DIO	SDIO data bit 3		1.8/3.2 V power domain. If unused, keep them open.
SDIO1_DATA2	29	DIO	SDIO data bit 2		
SDIO1_DATA1	30	DIO	SDIO data bit 1		
SDIO1_DATA0	31	DIO	SDIO data bit 0		
SDIO1_CLK	32	DO	SDIO clock		

SDIO1_CMD	33	DIO	SDIO command		
SDIO1_VDD	34	PO	SDIO power supply		
WLAN Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_SLP_CLK	118	DO	WLAN sleep clock		If unused, keep it open.
WLAN_PWR_EN	127	DO	WLAN power supply enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
SDIO2_DATA3	129	DIO	WLAN SDIO data bit 3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open.
SDIO2_DATA2	130	DIO	WLAN SDIO data bit 2	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
SDIO2_DATA1	131	DIO	WLAN SDIO data bit 1	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
SDIO2_DATA0	132	DIO	WLAN SDIO data bit 0	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
SDIO2_CLK	133	DO	WLAN SDIO CLK	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SDIO2_CMD	134	DO	WLAN SDIO command	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
WLAN_WAKE	135	DI	Wake up the module by an external Wi-Fi module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V	1.8 V power domain. If unused, keep it open.

				V_{IH}max = 2.0 V	
WLAN_EN	136	DO	WLAN function enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_BT/WIFI_SCAN	35	AIO	The shared antenna interface of Bluetooth and Wi-Fi Scan		Bluetooth and Wi-Fi Scan cannot be used simultaneously; Wi-Fi Scan antenna can only receive but not transmit. 50 Ω characteristic impedance. If unused, keep it open.
ANT_GNSS	47	AI	GNSS antenna interface		50 Ω characteristic impedance. If unused, keep it open.
ANT_MAIN	49	AIO	Main antenna interface		50 Ω characteristic impedance.
USB_BOOT					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	115	DI	Control pin for the module to enter download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain, a circuit design for entering download mode should be reserved.
Other Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WAKEUP_IN	1	DI	Wake up the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Pull-up by default. If unused, keep it open.
AP_READY	2	DI	Application processor ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V	1.8 V power domain. If unused, keep it

				V_{IH}min = 1.26 V V_{IH}max = 2.0 V	open.
SLEEP_IND	3	DO	Sleep indicator	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
W_DISABLE#	4	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Pull-up by default. Driving the pin low can make the module enter the airplane mode. If unused, keep it open.
GPIO1	126	DO	CP log		It can output CP log, and only 8 Mbps baud rate is supported, and test points should be reserved.
BT_EN	139		Reserved		
GRFC1	143	DIO	Generic RF controller		
GRFC2	144	DIO	Generic RF controller		
Reserved Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	18, 55, 81, 82, 116, 117				Keep these pins open.

3.4. Operating Modes

Table 8: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.

Minimum Functionality Mode	**AT+CFUN=0** can set the module to a minimum functionality mode without removing the power supply. In this case, RF function will be invalid.
Airplane Mode	**AT+CFUN=4** or W_DISABLE# can set the module to airplane mode. In this case, RF function will be invalid.
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level. In this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.
Power Down Mode	In this mode, the power management unit (PMU) shuts down the power supply. Software is not active, the serial interface is not accessible, while operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.

3.5. Power Saving

3.5.1. Sleep Mode

The module is able to reduce its current consumption to a minimum value in sleep mode. The following section describes power saving procedures of the module.

3.5.1.1. UART Application

If the host communicates with module via UART interface, the following preconditions should be met to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive MAIN_DTR to high level.

The following figure shows the connection between the module and the host.

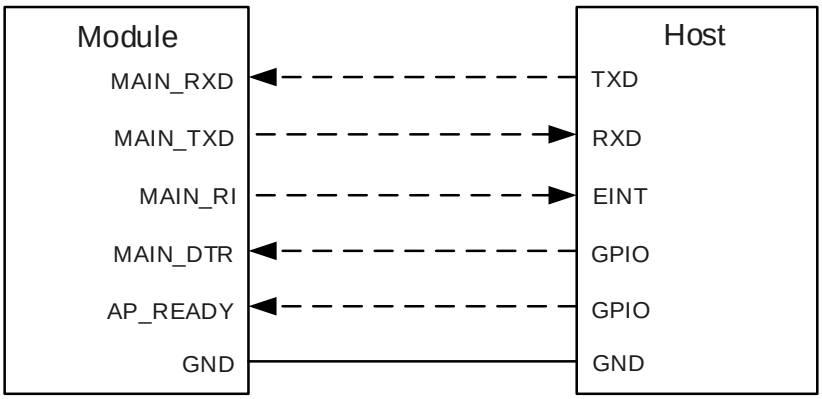


Figure 3: Sleep Mode Application via UART

- Driving MAIN_DTR to low level by the host can wake up the module.
- When the module has a URC to report, the URC will trigger the behavior of MAIN_RI pin. Please refer to ***Chapter 3.22*** for details about MAIN_RI behavior.

3.5.1.2. USB Application with USB Remote Wakeup Function*

If the host supports USB suspend/resume and remote wakeup functions, the following three preconditions must be met to make the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the MAIN_DTR is held at high level, or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters suspended state.

The following figure shows the connection between the module and the host.

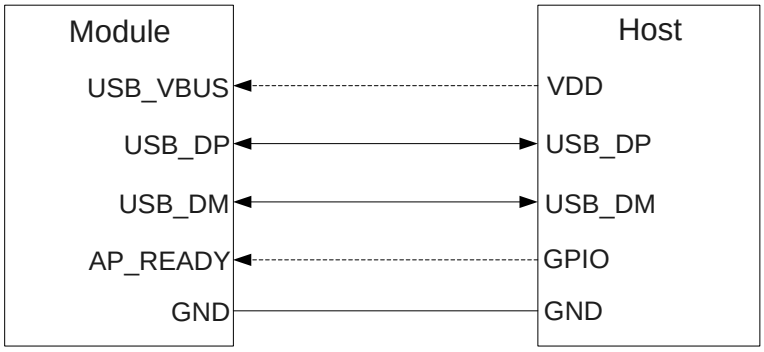


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to the module through USB can wake up the module.
- When the module has a URC to report, the module will send remote wakeup signals via USB bus so as to wake up the host.

NOTE

1. USB suspend is supported on Linux system but not supported on Windows system.
2. Pay attention to the level match shown in dotted line between the module and the host.

3.5.1.3. USB Application with USB Suspend/Resume and MAIN_RI Function*

If the host supports USB suspend/resume but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host.

In this case, three preconditions can make the module enter the sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the MAIN_DTR is held at high level, or keep it open.
- Ensure the host's USB bus, which is connected with the module's USB interface, enters suspended state.

The following figure shows the connection between the module and the host.

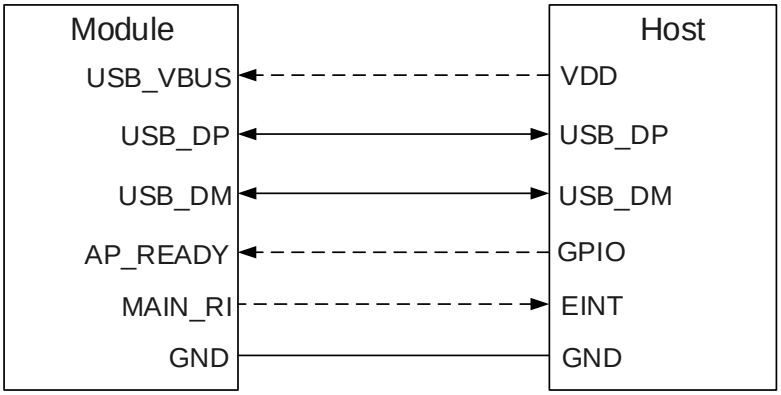


Figure 5: Sleep Mode Application with MAIN_RI

- Sending data to the module through USB can wake up the module.
- When the module has a URC to report, the URC will trigger the behaviors of MAIN_RI pin.

NOTE

1. USB suspend is supported on Linux system but not supported on Windows system.
2. Pay attention to the level match shown in dotted line between the module and the host.

3.5.1.4. USB Application

If the host does not support USB suspend function, USB_VBUS should be disconnected via an external control circuit of USB_VBUS to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the MAIN_DTR is held at high level, or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

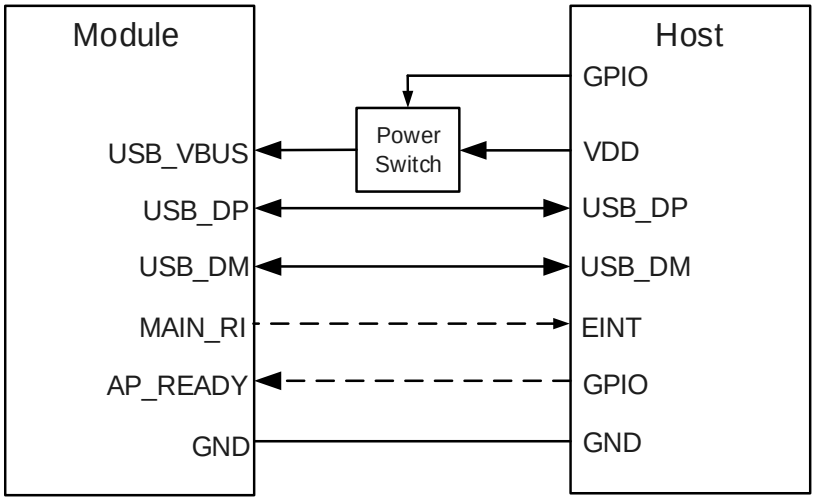


Figure 6: Sleep Mode Application without Suspended Function

The module will be wakened up when USB_VBUS is restored to be powered.

NOTE

Please pay attention to the level match shown in dotted line between the module and the host.

3.5.2. Airplane Mode

When the module enters airplane mode, the RF function does not work, and all AT commands related to RF function will be not accessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# is pulled up by default. Its control function for airplane mode, which is disabled by default in software, can be enabled through **AT+QCFG="airplanecontrol",1**. When such a control function is enabled, you can drive W_DISABLE# to low level to make the module enter airplane mode.

Software:

AT+CFUN = <fun> provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode (RF functions are disabled).
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** RF function is disabled (Airplane mode).

3.6. Power Supply

3.6.1. Power Supply Pins

The module provides four VBAT pins for connection with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part.
- Two VBAT_BB pins for module's baseband part and RF part.

Table 9: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	57, 58	Power supply for module's RF part	3.3	3.8	4.3	V
VBAT_BB	59, 60	Power supply for module's baseband part and RF part	3.3	3.8	4.3	V
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 76, 85–112					

3.6.2. Voltage Stability Requirements

The power supply range of the module is from 3.3 V to 4.3 V. Please make sure that the input voltage will never drop below 3.3 V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 4G networks.

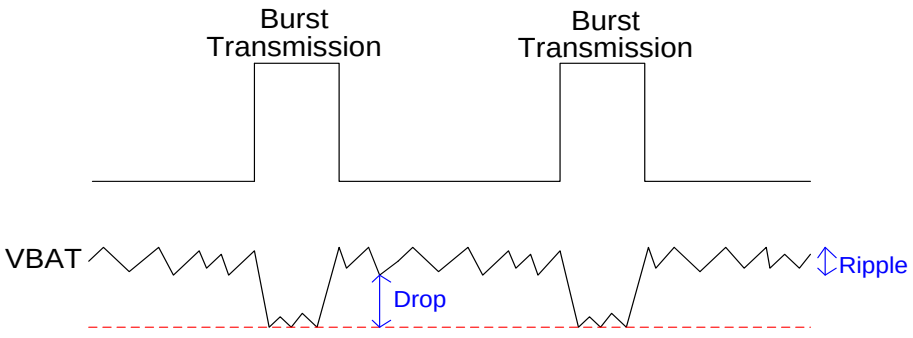


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100 μF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT_BB and VBAT_RF. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star configuration routing. The width of VBAT_BB trace should be no less than 2 mm; and the width of VBAT_RF trace should be no less than 2.5 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to ensure the stability of power source, it is suggested that a TVS diode of which reverse stand-off voltage is 4.7 V and peak pulse power is up to 2550 W should be used.

The following figure shows the star configuration routing of the power supply.

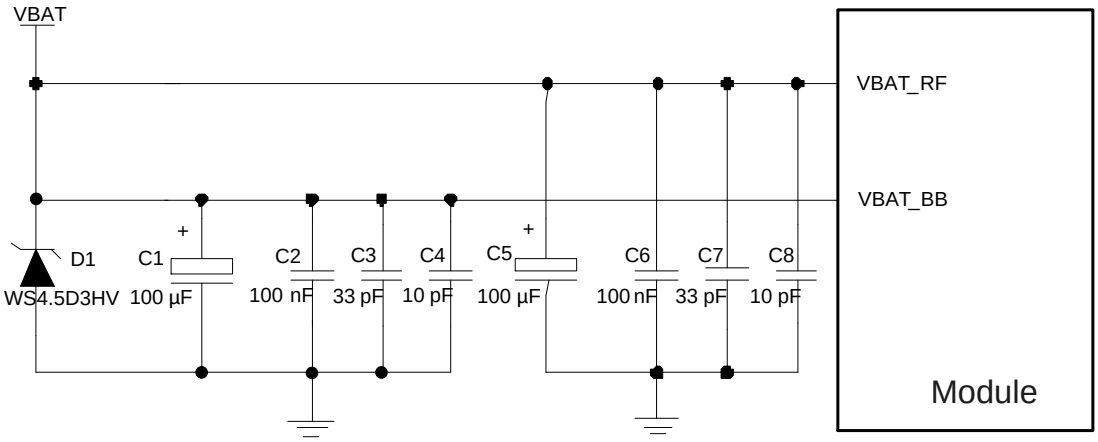


Figure 8: Star Configuration Routing of Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current up to 2.0 A to the module that only supports LTE network, while 3 A at least should be provided for GSM network. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), use a buck converter as the power supply.

The following figure shows a reference design for +5 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.5 A.

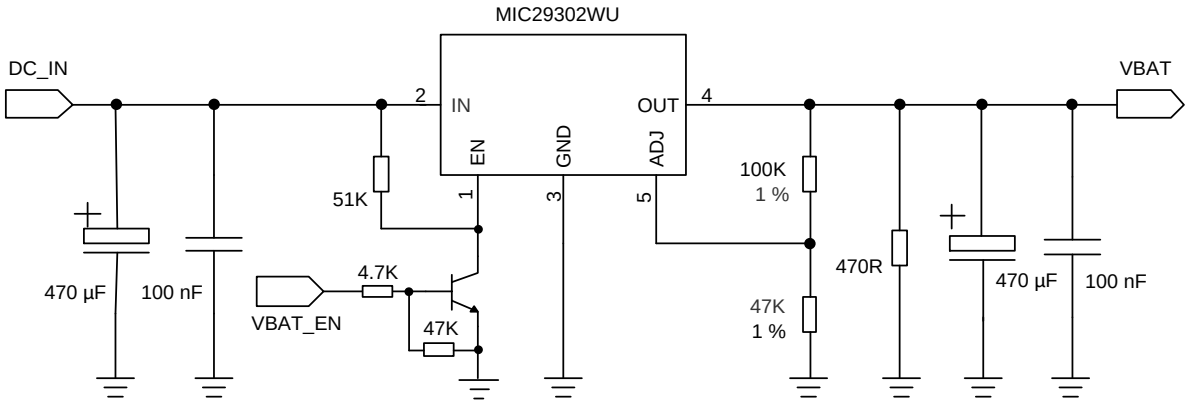


Figure 9: Reference Circuit of Power Supply

3.6.4. Monitor the Power Supply

You can use **AT+CBC** to monitor the VBAT_BB voltage value. For more details, see ***document [2]***.

3.7. Turn on/Turn off/Reset

3.7.1. Turn on Module with PWRKEY

Table 10: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	21	DI	Turn on/off the module	VBAT power domain

When the module is in power-off mode, it can be turned on to normal mode by driving PWRKEY to a low level for at least 2 s. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

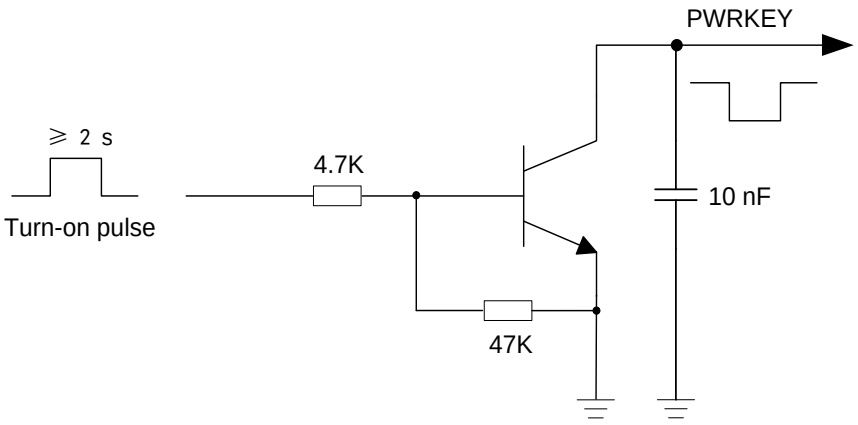


Figure 10: Turn on Module by Using Driving Circuit

Another way to control the PWRKEY is to use a button directly. When pressing the button, electrostatic strike may generate from finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection.

A reference circuit is shown in the following figure.

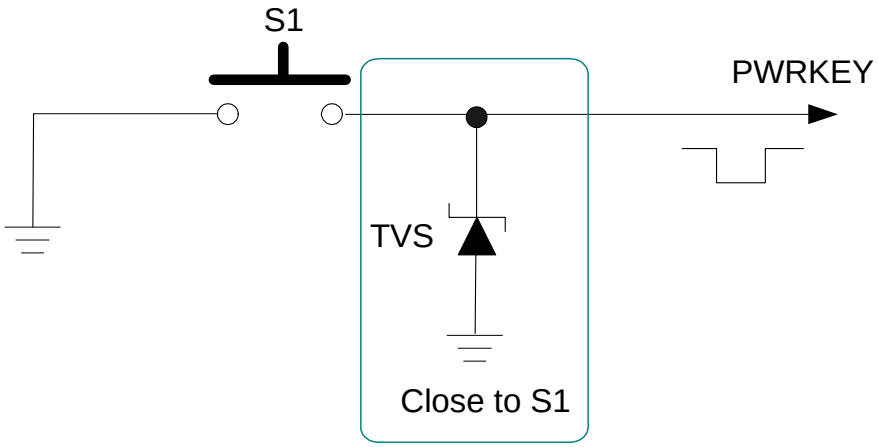


Figure 11: Turn on Module by Using Button

The power-up scenario is illustrated in the following figure.

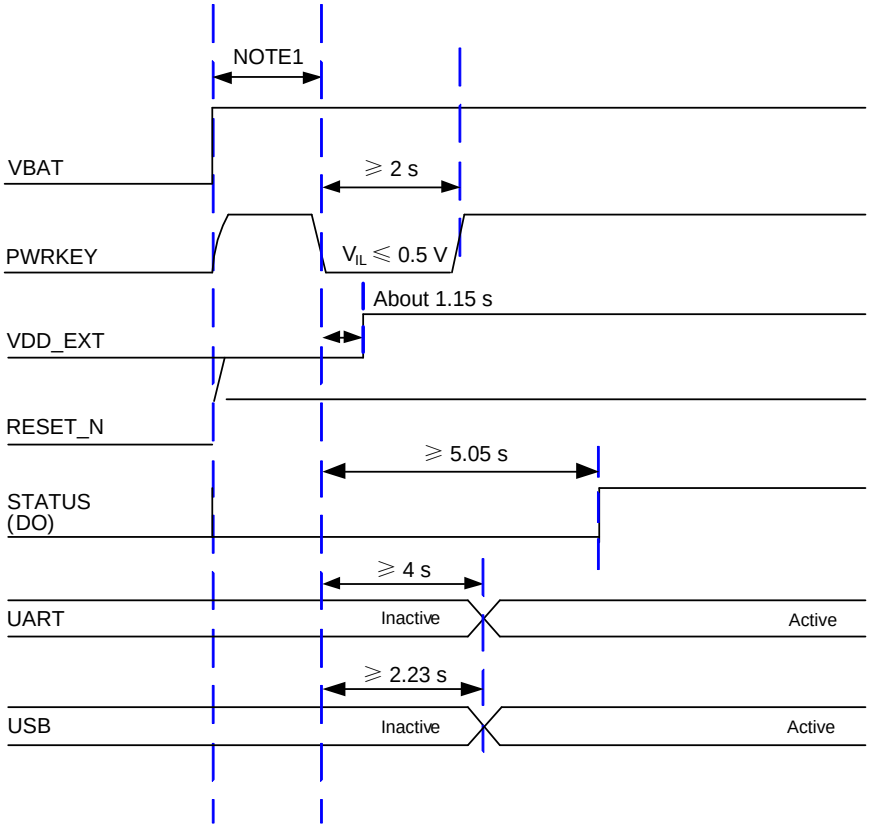


Figure 12: Power-up Timing

NOTE

1. Please make sure that VBAT is stable before PWRKEY is pulled down. It is recommended that the time interval between powering up VBAT and pulling down PWRKEY is no less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 1 kΩ resistor if the module needs being powered on automatically and shutdown is not needed.

3.7.2. Turn off Module

The following ways can be used to turn off the module:

- Turn off the module with PWRKEY.
- Turn off the module by using **AT+QPOWD**.

3.7.2.1. Turn off Module with PWRKEY

Driving PWRKEY low for at least 3 s and releasing it, the module executes power-down procedure.

The power-down scenario is illustrated in the following figure.

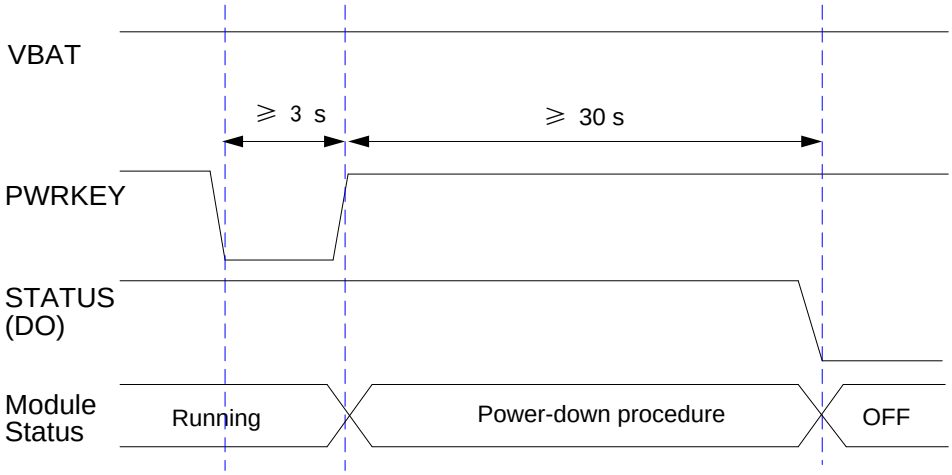


Figure 13: Power-down Timing

3.7.2.2. Turn off Module with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to the procedure of turning off the module via PWRKEY.

Please refer to ***document [2]*** for details about **AT+QPOWD**.

NOTE

1. In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, can the power supply be cut off.
2. When keeping the PWRKEY to the ground, the module can only be forced to turn off by cutting off the VBAT power supply considering that the module cannot be turned off with AT command. Therefore, it is recommended that you can turn on or turn off the module by pulling up and pulling down the PWEKEY instead of keeping the PWRKEY to the ground.
3. When being turned off, the module will log out of the network. The time for logging out relates to its network status. Thus, please pay attention to the shutdown time in your design because the actual shutdown time varies with the network status.

3.7.3. Reset the Module

The RESET_N can be used to reset the module. The module can be reset by driving RESET_N low for at least 100 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 11: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	20	DI	Reset the module	VBAT power domain

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

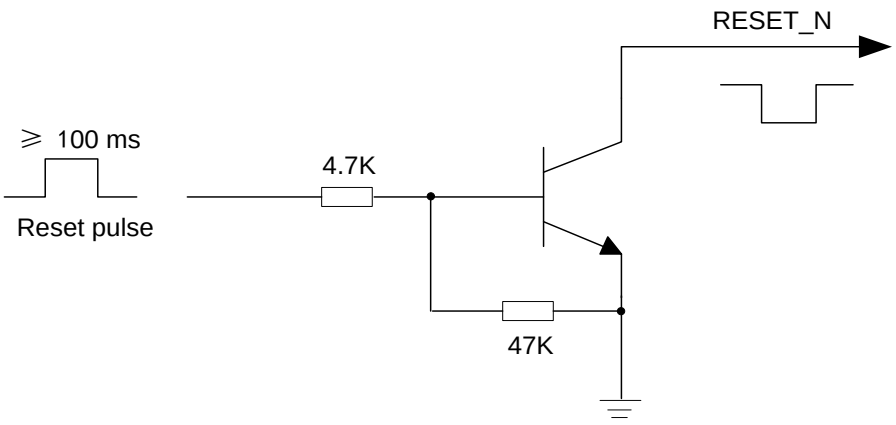


Figure 14: Reference Circuit of RESET_N by Using Driving Circuit

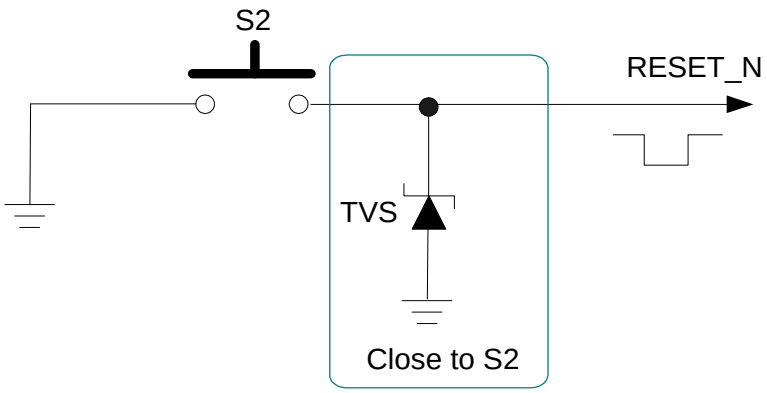


Figure 15: Reference Circuit of RESET_N by Using Button

The timing of resetting module is illustrated in the following figure.

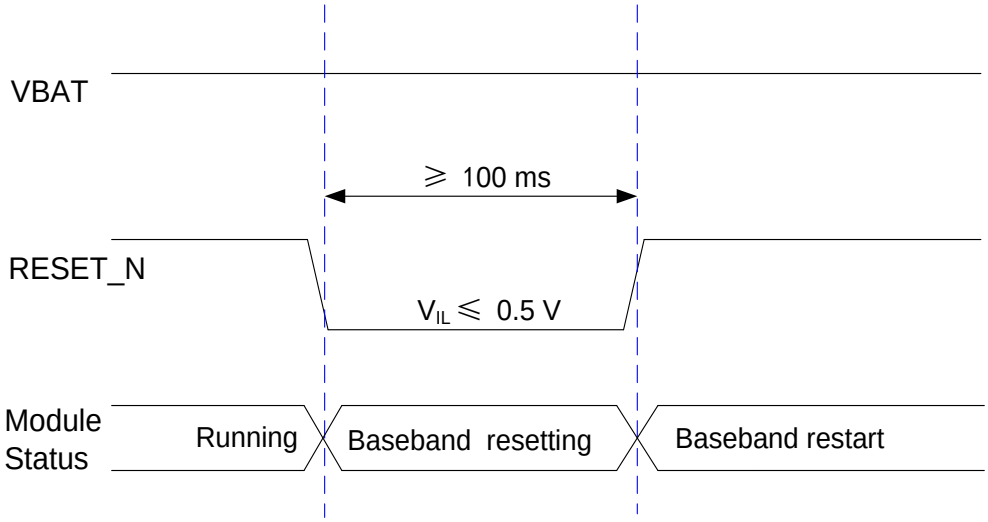


Figure 16: Timing of Resetting Module

NOTE

1. Ensure that there is no large capacitance exceeding 10 nF on PWRKEY and RESET_N.
2. It is recommended to use RESET_N only when the module cannot be turned off by **AT+QPOWD** or PWRKEY.

3.8. (U)SIM Interfaces

The module provides two (U)SIM interfaces, and it supports DSDS function. The (U)SIM interfaces meet ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported.

Table 12: Pin Definition of (U)SIM1 Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	14	PO	(U)SIM card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM_DATA	15	DIO	(U)SIM card data	
USIM_CLK	16	DO	(U)SIM card clock	
USIM_RST	17	DO	(U)SIM card reset	

USIM_DET	13	DI	(U)SIM card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM_GND	10		(U)SIM card GND	

Table 13: Pin Definition of (U)SIM2 Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM2_VDD	128	PO	(U)SIM2 card power supply	The (U)SIM2 function is optional. If the firmware version of the module supports the function of the (U)SIM2 card, the relevant functions of the (U)SIM2 card can be realized by multiplexing AP_READY, WAKEUP_IN, SLEEP_IND, and W_DISABLE# pins. For details, please consult Quectel Technical Supports.
AP_READY	2	DIO	(U)SIM2 card data	
WAKEUP_IN	1	DO	(U)SIM2 card clock	
W_DISABLE#	4	DO	(U)SIM2 card reset	
SLEEP_IND	3	DI	(U)SIM2 card hot-plug detect	

The module supports (U)SIM card hot-plug via the USIM_DET, and both high and low level detections are supported. By default, the function is disabled, and it can be enabled by **AT+QSIMDET**. Please see ***document [2]*** for more details about the **AT+QSIMDET**.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

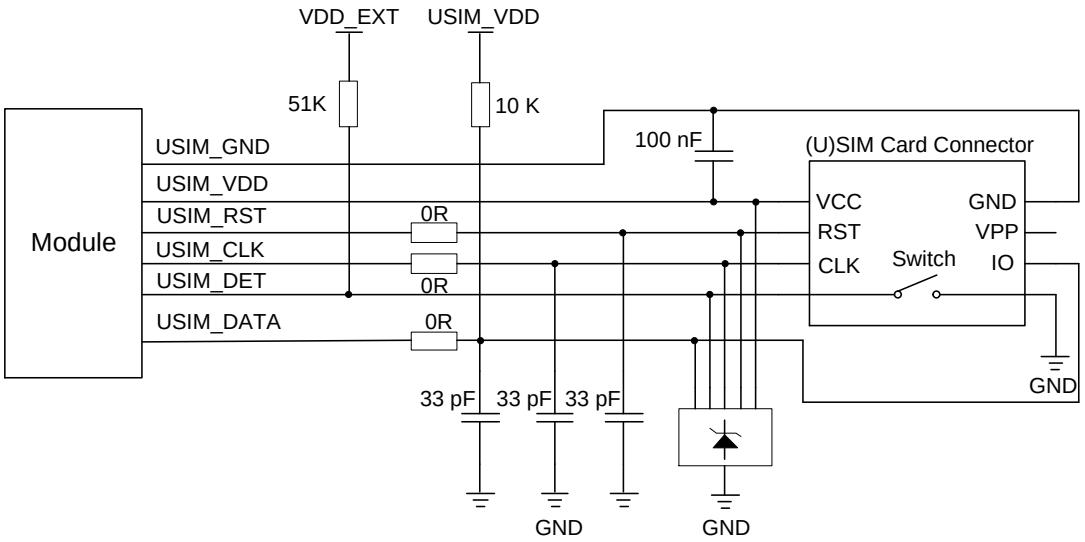


Figure 17: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

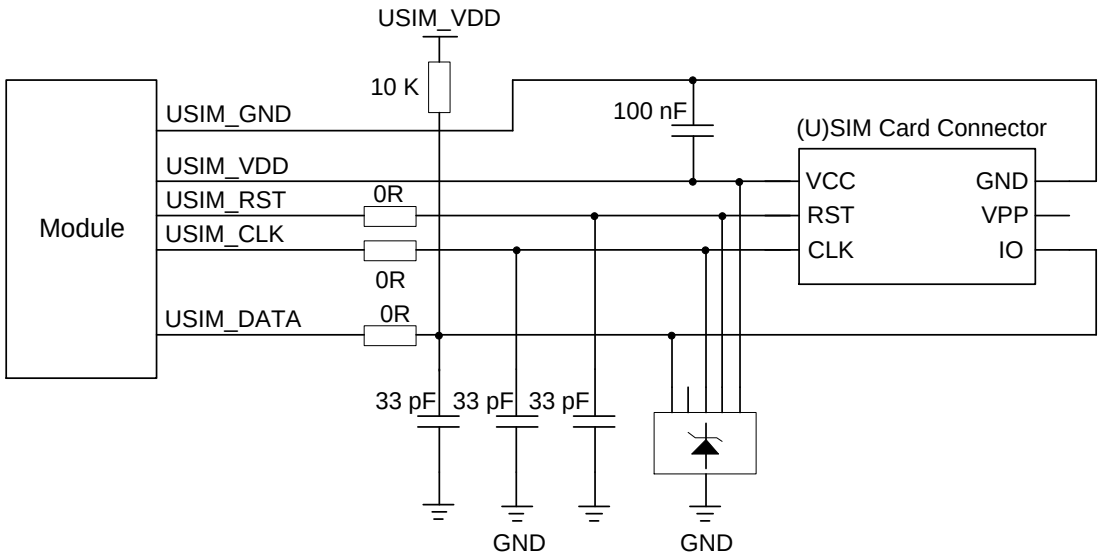


Figure 18: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in your applications, please follow the criteria below in (U)SIM circuit design:

- Place (U)SIM card connector as close to the module as possible. Keep the trace length less than 200 mm as far as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Keep the trace between the ground of (U)SIM card connector and USIM_GND short and wide. Keep the trace width of USIM_GND and USIM_VDD no less than 0.5 mm to maintain the same electric potential. If the ground is complete on your PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not be more than 15 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors on USIM_DATA, USIM_CLK and USIM_RST are used for filtering interference of EGSM900. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to
- add a pull-up resistor near the (U)SIM card connector.

3.9. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480 Mbps) and full-speed (12 Mbps) modes. The USB

interface only supports USB slave mode and it can be used for AT command communication, data transmission, software debugging and firmware upgrade.

Table 14: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	69	AIO	USB differential data bus (+)	Require differential impedance of 90 Ω
USB_DM	70	AIO	USB differential data bus (-)	Require differential impedance of 90 Ω
USB_VBUS	71	AI	USB connection detect	Typical 5.0 V, Minimum 3.5 V
GND	72		Ground	

For more details about the USB 2.0 specifications, please visit http://www.usb.org/home.

Reserve test points for debugging and firmware upgrade in your design. The following figure shows a reference circuit of USB interface.

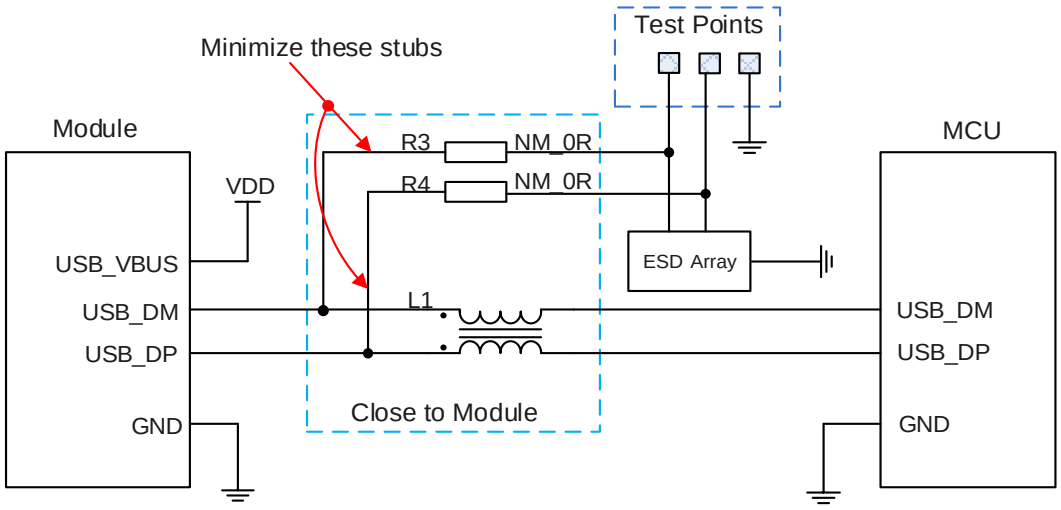


Figure 19: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and your MCU in order to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data line signal, L1, R3 and R4 components must be placed close to the module, and also these resistors should be placed close to each other. The

extra stubs of trace must be as short as possible.

The following principles should be complied with when designing the USB interface, so as to meet USB 2.0 specification.

- Route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic device and RF signal traces. It is recommended to route the USB differential traces in inner-layer of the PCB and to surround the traces with ground on that layer and with ground planes above and below.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 2.0 pF, and keep the ESD protection components to the USB connector as close as possible.

3.10. UART Interfaces

The module provides three UART interfaces: the main UART interface, the debug UART interface and auxiliary UART Interface. The following shows their features.

- Main UART interface: The main UART interface supports 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800 and 921600 bps baud rates, and the default is 115200 bps. This interface is used for data transmission and AT command communication and supports RTS and CTS hardware flow control.
- Debug UART interface: Only supports 921600 bps baud rate, used for the output of partial logs.
- Auxiliary UART Interface

Table 15: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_RI	62	DO	Main UART ring indication	1.8 V power domain. If unused, keep them open.
MAIN_DCD	63	DO	Main UART data carrier detect	
MAIN_CTS	64	DO	DTE clear to send signal from DCE (Connect to DTE's CTS)	
MAIN_RTS	65	DI	DTE request to send signal to DCE (Connect to DTE's RTS)	
MAIN_DTR	66	DI	Main UART data terminal ready	

MAIN_TXD	67	DO	Main UART transmit
MAIN_RXD	68	DI	Main UART receive

Table 16: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	12	DO	Debug UART transmit	1.8 V power domain. If unused, keep them open.
DBG_RXD	11	DI	Debug UART receive	

Table 17: Pin Definition of Auxiliary UART Interface

Pin Name	Pin No.	I/O	Description	Comment
AUX_TXD	138	DO	Auxiliary UART transmit	1.8 V power domain. If unused, keep them open.
AUX_RXD	137	DI	Auxiliary UART receive	

The module provides 1.8 V UART interface. Use a level shifter if the application is equipped with a 3.3 V UART interface. A level shifter TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure shows a reference design.

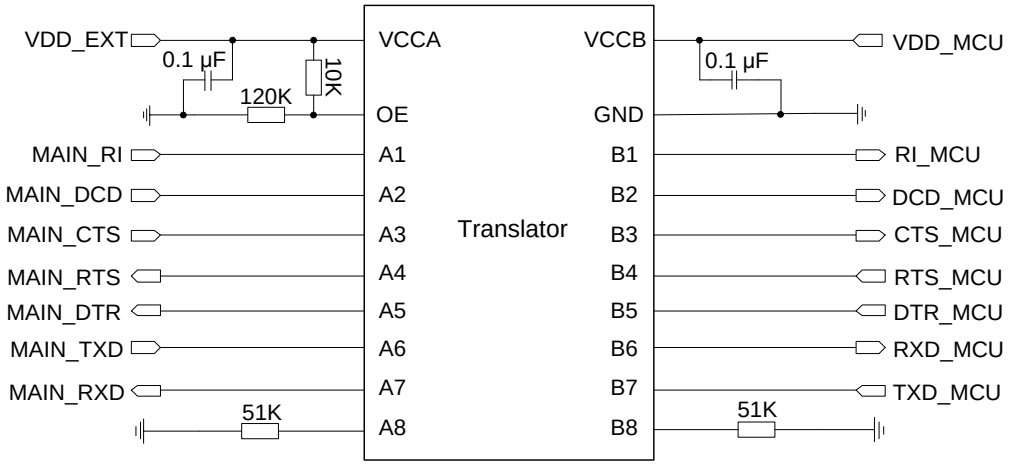


Figure 20: Reference Circuit with Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

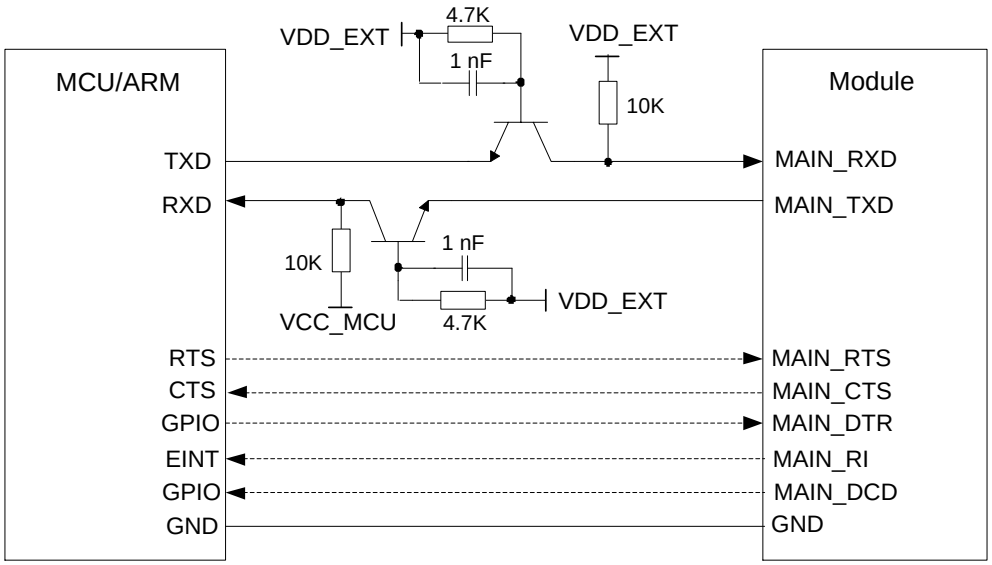


Figure 21: Reference Circuit with Transistor Circuit

NOTE

1. Triode level transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS.

3.11. SPI Interface

The SPI interface of EC200U series module only supports master mode. It allows the full duplex synchronous communication between module and peripherals. Its working voltage is 1.8 V, and the maximum clock frequency is 25 MHz. If a universal 4-wire SPI interface is used to connect to Nor Flash, it provides the basic Flash operation including reading, writing and erasing, and does not support the file system.

Table 18: Pin Definition of SPI interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CS	37	DO	SPI chip select	If you use a module model

SPI_MOSI	38	DO	SPI master mode output	that supports GNSS function, the SPI function of Pin 37–40 cannot be used and needs to be left unconnected.
SPI_MISO	39	DI	SPI master mode input	
SPI_CLK	40	DO	SPI clock	

3.12. I2C Interfaces

The module provides two I2C interfaces.

Table 19: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	41	OD	I2C serial clock	Require external pull-up to 1.8 V if used. If unused, keep it open.
I2C_SDA	42	OD	I2C serial data	
I2C2_SCL	141	OD	I2C serial clock	
I2C2_SDA	142	OD	I2C serial data	

NOTE

The I2C bus supports simultaneous connection of multiple peripherals except for codec IC. In other words, if a codec IC has been mounted on the I2C bus, no other peripherals can be mounted. If there is no codec IC on the bus, multiple peripherals can be mounted.

3.13. PCM Interface

The module provides one PCM interface which only supports slave mode.

Table 20: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	24	DI	PCM data input	1.8 V power domain. If unused, keep it open.

PCM_DOUT	25	DO	PCM data output	1.8 V power domain. If unused, keep it open.
PCM_SYNC	26	DI	PCM data frame sync	1.8 V power domain. If unused, keep it open. The PCM function only supports slave mode.
PCM_CLK	27	DI	PCM clock	

The following figure shows the reference design of PCM and I2C interface with external Codec chip:

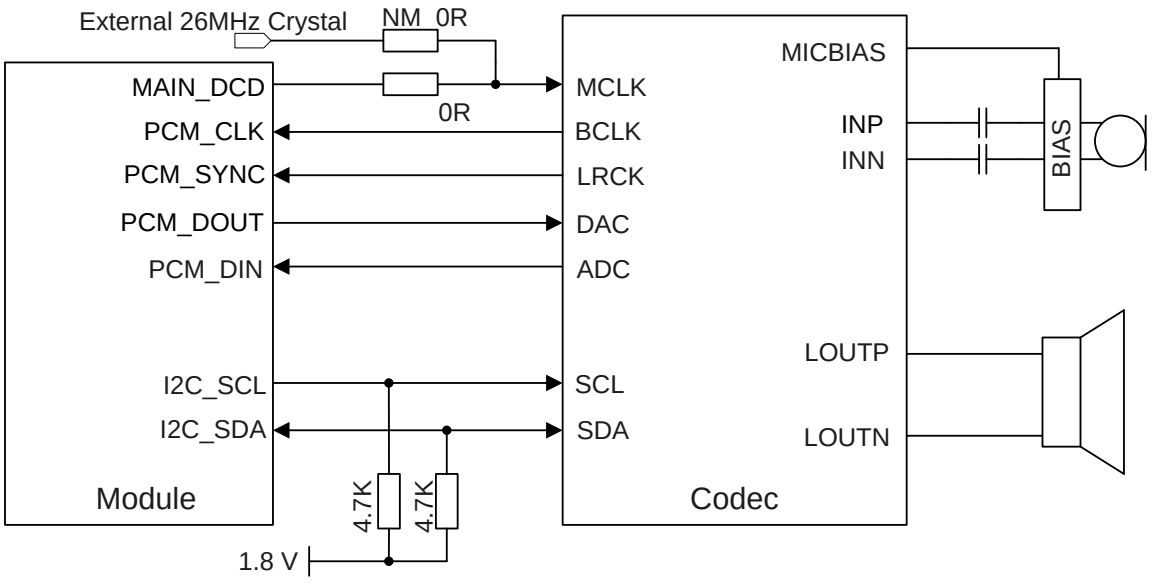


Figure 22: Reference Circuit of I2C and PCM Application with External Codec Chip

NOTE

It is recommended to reserve an RC (R = 22 Ω, C = 22 pF) circuit on the PCM traces, especially for PCM_CLK.

3.14. Analog Audio Interfaces

The module provides one analog audio input channel and one analog audio output channel. The pin definition is shown in the table below.

Table 21: Pin Definition of Analog Audio Interfaces

Interface	Pin Name	Pin No.	I/O	Description
AOUT	LOUDSPK_P	73	AO	Loudspeaker differential

				output (+)
	LOUDSPK_N	74	AO	Loudspeaker differential output (-)
AIN	MIC_P	75	AI	Microphone analog input (+)
	MIC_N	77	AI	Microphone analog input (-)

- AIN channel is a differential input channel, which can be applied for input of microphone (usually an electret microphone).
- The AOUT channel is a differential output with a built-in power amplifier. The default configuration of power amplifier is Class AB and the maximum driving power is 500 mW for 8 Ω load. When PA is configured as Class D, the maximum driving power is 800 mW for 8 Ω load.

3.14.1. Notes on Audio Interface Design

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10 pF and 33 pF) for filtering out RF interference, thus reducing TDD noise. The 33 pF capacitor is applied for filtering out RF interference when the module is transmitting at EGSM900. Without placing this capacitor, TDD noise could be heard. The 10 pF capacitor here is used for filtering out RF interference at DCS1800. Please note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you would have to discuss with their capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. In some cases, EGSM900 TDD noise is more severe; while in other cases, DCS1800 TDD noise is more obvious. Therefore, a suitable capacitor can be selected based on the test results. The filter capacitors on the PCB should be placed as close to the audio devices or audio interfaces as possible, and the traces should be as short as possible. They should go through the filter capacitors before arriving at other connection points.

In order to decrease radio or other signal interference, RF antennas should be placed away from audio interfaces and audio traces. Power traces cannot be parallel with and also should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

3.14.2. Microphone Interface Circuit

The reference circuit of the microphone interface is shown in the figure below:

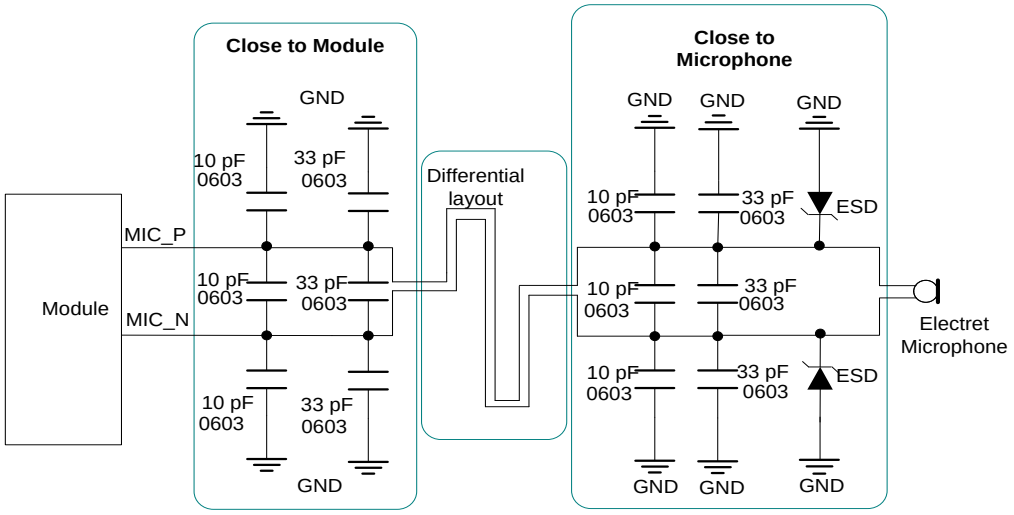


Figure 23: Reference Circuit of Microphone Interface

NOTE

MIC channel is sensitive to ESD, so it is not recommended to remove the ESD components used for protecting the MIC.

3.14.3. Loudspeaker Interface Circuit

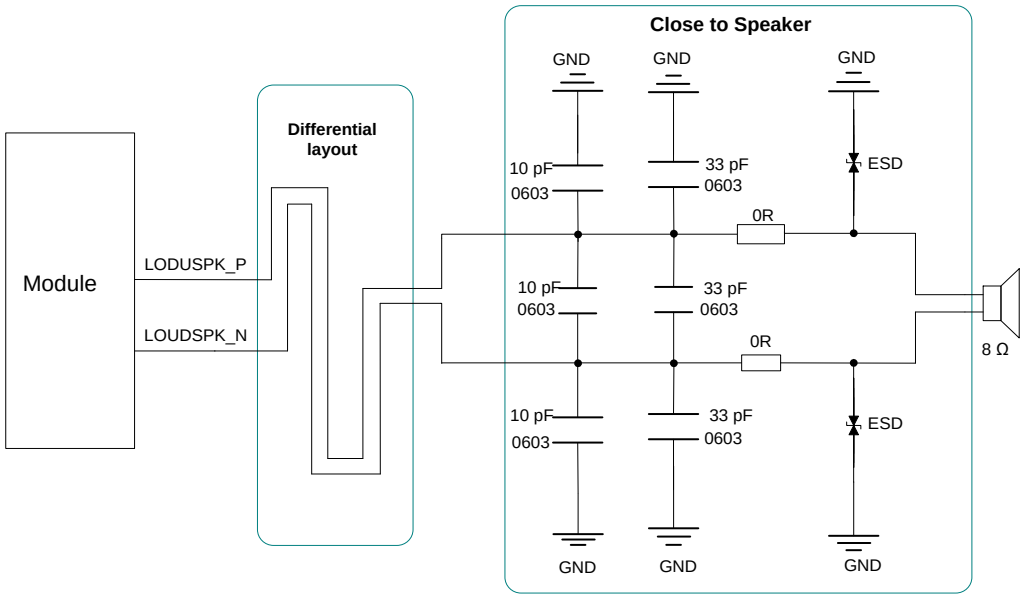


Figure 24: Reference Circuit of Loudspeaker Interface

3.15. LCD Interface

The LCD interface of the module supports a liquid crystal display with a maximum resolution of 320 × 240 and DMA transmission, 16-bit RGB565 and YUV formats.

Table 22: Pin Definition of LCD Interface

Pin Name	Pin No.	I/O	Description	Comment
LCD_FMARK	119	DI	LCD frame synchronization	1.8 V power domain. If unused, keep them open.
LCD_RSTB	120	DO	LCD reset	
LCD_SEL	121	-	Reserved	
LCD_CS	122	DO	LCD chip select	
LCD_CLK	123	DO	LCD clock	
LCD_SDC	124	DO	LCD register selection	
LCD_SI/O	125	DIO	LCD data	
ISINK	140	PI	Sink current input. Backlight adjustment	Imax = 200 mA It is driven by the current sink method, and connected to the backlight cathode, the brightness can be adjusted with current control.

3.16. Matrix Keyboard Interface

The module provides one keyboard interface. It supports 4 × 4 matrix keyboard.

Table 23: Pin Definition of Matrix Keyboard Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Matrix keyboard input0	1.8 V power domain. If unused, keep it open. The USB_BOOT cannot be pulled up before startup and

				it can be used as KEYIN0 after startup.
KEYIN1	78	DI	Matrix keyboard input1	1.8 V power domain. If unused, keep it open. The KEYIN1 cannot be pulled up before startup.
KEYIN2	79	DI	Matrix keyboard input2	1.8 V power domain. If unused, keep them open.
KEYIN3	80	DI	Matrix keyboard input3	
KEYOUT0	83	DO	Matrix keyboard output0	
KEYOUT1	84	DO	Matrix keyboard output1	
KEYOUT2	113	DO	Matrix keyboard output2	
KEYOUT3	114	DO	Matrix keyboard output3	

3.17. SD Card Interface

The module supports SDIO 2.0 interface for SD card.

Table 24: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_DET	23	DI	SD card detect	1.8 V power domain. If unused, keep it open.
SDIO1_DATA3	28	DIO	SDIO data bit 3	1.8/3.2V power domain. If unused, keep them open.
SDIO1_DATA2	29	DIO	SDIO data bit 2	
SDIO1_DATA1	30	DIO	SDIO data bit 1	
SDIO1_DATA0	31	DIO	SDIO data bit 0	
SDIO1_CLK	32	DO	SDIO clock	
SDIO1_CMD	33	DIO	SDIO command	
SDIO1_VDD	34	PO	SDIO power supply	

The following figure shows a reference design of SD card interface.

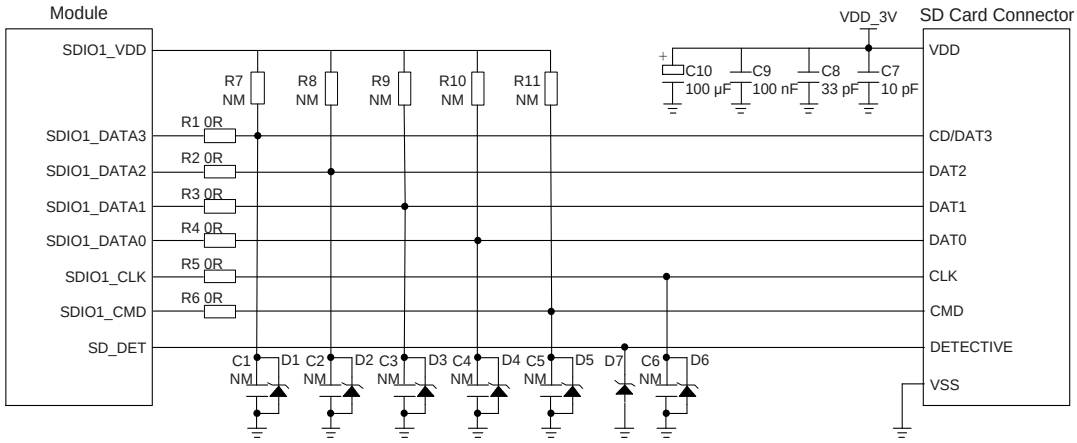


Figure 25: Reference Circuit of SD Card Interface

In SD card interface design, in order to ensure good communication performance with SD card, the following design principles should be complied with:

- The voltage range of SD card power supply VDD_3 V is 2.7–3.6 V and a sufficient current up to 0.8 A should be provided. As the maximum output current of SDIO1_VDD is 150 mA which can only be used for SDIO pull-up resistors, an externally power supply is needed for SD card.
- To avoid jitter of bus, resistors R7–R11 are needed to pull up the SDIO to SDIO1_VDD. Value of these resistors is among 10–100 kΩ and the recommended value is 100 kΩ. SDIO1_VDD should be used as the pull-up power.
- In order to adjust signal quality, it is recommended to add 0 Ω resistors R1–R6 in series between the module and the SD card. The bypass capacitors C1–C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- In order to offer good ESD protection, it is recommended to add a TVS diode on SD card pins near the SD card connector with junction capacitance less than 15 pF.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is important to route the SDIO signal surrounded with ground on the layer and ground planes above and below. The impedance of SDIO data trace is 50 Ω ±10 %.
- Make sure the adjacent trace spacing is more than two times of the trace width and the load capacitance of SDIO bus should be less than 15 pF.
- It is recommended to keep the trace length difference between SDIO1_CLK and SDIO1_DATA [0:3]/ SDIO1_CMD less than 1 mm and the total routing length less than 50 mm.

3.18. WLAN Application Interface*

The module provides an SDIO 1.1 standard WLAN application interface.

Table 25: Pin Definition of WLAN Interface

Pin Name	Pin No.	I/O	Description	Comment
WLAN_SLP_CLK	118	DO	WLAN sleep clock	If unused, keep it open.
WLAN_PWR_EN	127	DO	WLAN power supply enable control	1.8 V power domain. If unused, keep them open.
SDIO2_DATA3	129	DIO	WLAN SDIO data bit 3	
SDIO2_DATA2	130	DIO	WLAN SDIO data bit 2	
SDIO2_DATA1	131	DIO	WLAN SDIO data bit 1	
SDIO2_DATA0	132	DIO	WLAN SDIO data bit 0	
SDIO2_CLK	133	DO	WLAN SDIO CLK	
SDIO2_CMD	134	DO	WLAN SDIO command	
WLAN_WAKE	135	DI	Wake up the module by an external Wi-Fi module	1.8 V power domain. If unused, keep them open.
WLAN_EN	136	DO	WLAN function enable control	

The SDIO interface rate is very high. To ensure that the interface design complies with the SDIO 1.1 specification, the following principles are recommended:

- It is important to route the SDIO signal surrounded with ground on the layer and ground planes above and below. The impedance of SDIO data trace is 50 Ω ±10 %.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is recommended to keep the trace length difference between WLAN_SDIO_CLK and WLAN_SDIO_DATA [0:3]/ WLAN_SDIO_CMD less than 1 mm and the total routing length less than 50 mm.
- Make sure the adjacent trace spacing is more than two times of the trace width and the load capacitance of SDIO bus should be less than 15 pF.

NOTE

WLAN application interface conflicts with other functions, and please consult Quectel Technical Supports for details.

3.19. ADC Interfaces

The module provides three ADC interfaces. **AT+QADC=0** can be used to read the voltage value on ADC0 pin. **AT+QADC=1** can be used to read the voltage value on ADC1 pin. **AT+QADC=2** can be used to read the voltage value on ADC2 pin. For more details about **AT+QADC**, please refer to ***document [2]***.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded with ground.

Table 26: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description	Comment
ADC0	45	General-purpose ADC interface	Use a 1 kΩ resistor in series if used. If unused, keep them open.
ADC1	44	General-purpose ADC interface	
ADC2	43	General-purpose ADC interface	

Table 27: Characteristic of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0	-	VBAT_BB	V
ADC1 Voltage Range	0	-	VBAT_BB	V
ADC1 Voltage Range	0	-	VBAT_BB	V
ADC Resolution	-	12	-	bits

NOTE

The external resistor should be less than 100 kΩ when the voltage divider resistor applies.

3.20. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module has NET_MODE and NET_STATUS for network status indication. The following tables describe pin definition and logic level changes in different network status.

Table 28: Pin Definition of Network Connection Status/Activity Indicator

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	5	DO	Indicate the module's network activity status	1.8 V power domain. If unused, keep them open.
NET_STATUS	6	DO	Indicate the module's network registration mode	

Table 29: Working State of Network Connection Status/Activity Indicator

Pin Name	Logic Level Changes	Network Status
NET_STATUS	Always high	Registered on LTE network
	Always low	Others
NET_MODE	Flicker slowly (200 ms high/1800 ms low)	Network searching
	Flicker quickly (234 ms high/266 ms low)	Idle
	Flicker rapidly (62 ms high/63 ms low)	Data transfer is ongoing
	Always high	Voice calling

A reference circuit is shown in the following figure.

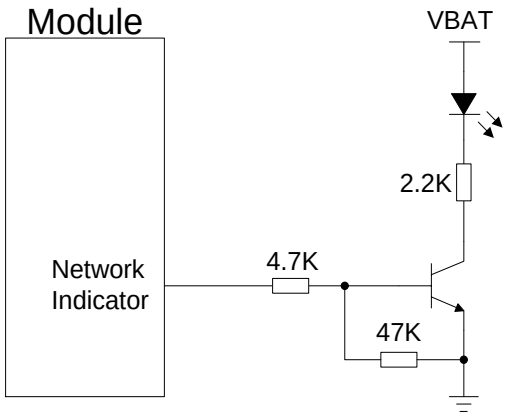


Figure 26: Reference Circuit of Network Indicator

3.21. STATUS

The STATUS pin is an output for module's operation status indication. When the module is turned on normally, the STATUS outputs high level.

Table 30: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	61	DO	Indicate the module's operation status	1.8 V power domain. If unused, keep it open.

A reference circuit is shown in the following figure.

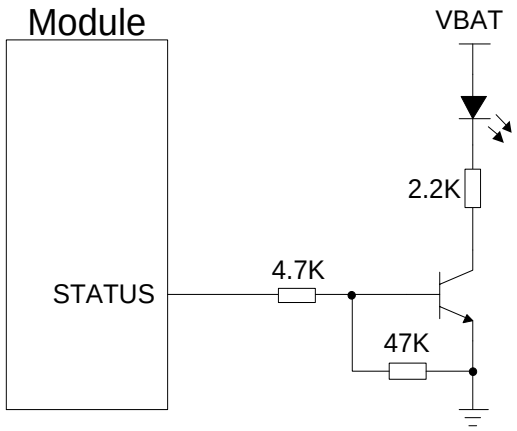


Figure 27: Reference Circuit of STATUS

NOTE

The STATUS cannot be used as the indication of power-down state when VBAT doesn't supply power to the module.

3.22. Behaviors of MAIN_RI

AT+QCFG="risignaltype","physical" can be used to configure MAIN_RI behaviors.

No matter on which port a URC is presented, the URC will trigger the behavior of MAIN_RI pin.

NOTE

The **AT+QURCCFG** allows you to set the main UART, USB AT port or USB modem port as the URC output port. The USB AT port is used to send AT commands by default.

In addition, MAIN_RI behaviors can be configured flexibly. The default behaviors of the MAIN_RI are shown as below.

Table 31: Behaviors of the MAIN_RI

State	Response
Idle	MAIN_RI keeps at high level
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns

The MAIN_RI behavior can be configured by **AT+QCFG="urc/MAIN_RI/ring"** and see ***document [2]*** for details.

3.23. USB_BOOT Interface

The module provides a USB_BOOT pin. You can pull up USB_BOOT to 1.8 V before VDD_EXT is powered up, and the module will enter download mode when it is powered on. In this mode, the module can upgrade firmware over USB interface.

If your application has a scan key, you can also press the "USB_BOOT + KEYOUT0" scan key before powering on the module, and the module will enter the download mode when it is turned on.

Table 32: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Control pin for the module to enter download mode	1.8 V power domain. Active high. The download control circuit must be reserved.

The following figure shows a reference circuit of USB_BOOT interface.

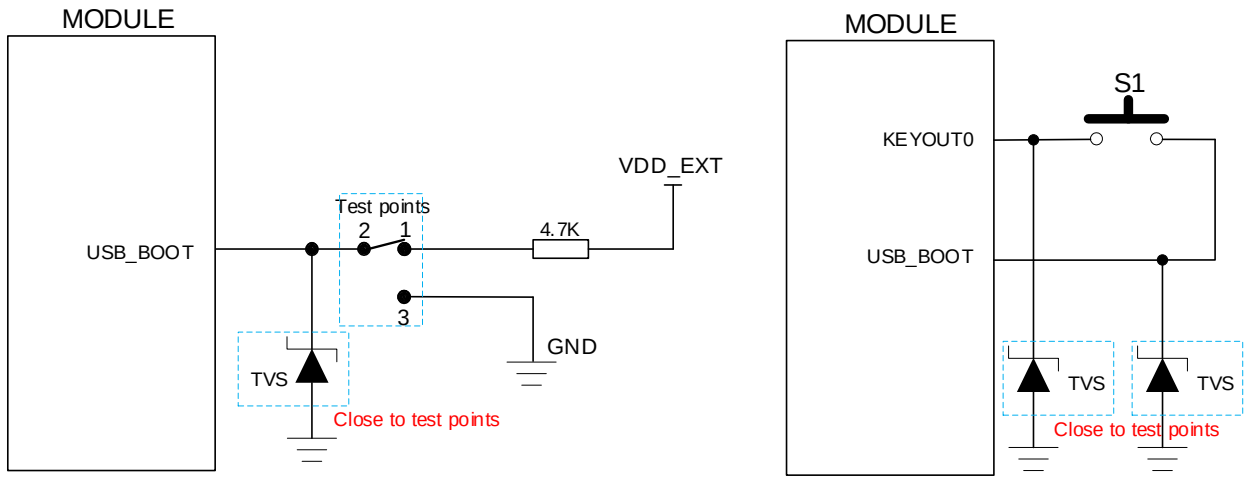


Figure 28: Reference Circuit of USB_BOOT Interface

NOTE

Please make sure that VBAT is stable before PWRKEY is pulled down. It is recommended that the time interval between powering up VBAT and pulling down PWRKEY is no less than 30 ms.

4 Antenna Interfaces

EC200U series module provides a main antenna interface, a Wi-Fi Scan/Bluetooth antenna interface and a GNSS antenna interface. The antenna ports have an impedance of 50 Ω.

4.1. Main Antenna and Wi-Fi Scan/Bluetooth Antenna Interfaces

4.1.1. Pin Definition

The pin definition of main antenna and Wi-Fi Scan/Bluetooth antenna interfaces is shown below.

Table 33: Pin Definition of Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	49	AIO	Main antenna interface	50 Ω impedance.
ANT_BT/WIFI_SCAN	35	AIO	The shared antenna interface of Wi-Fi Scan/Bluetooth; Bluetooth and Wi-Fi Scan cannot be used simultaneously; Wi-Fi Scan antenna can only receive but not transmit.	50 Ω impedance. If unused, keep it open.

NOTE

EC200U series supports Bluetooth and Wi-Fi Scan functions. Due to the shared antenna interface, the two functions cannot be used at the same time; Bluetooth and Wi-Fi Scan functions are optional (supported or not supported simultaneously), please contact Quectel Technical Supports for details.

4.1.2. Operating Frequency

Table 34: EC200U-CN Operating Frequencies

3GPP Band	Transmit	Receive	Unit
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-TDD B34	2010–2025	2010–2025	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B39	1880–1920	1880–1920	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2535–2675	2535–2675	MHz

NOTE

The GSM network access technology of EC200U-CN is optional. If the module that you select doesn't support GSM network access technology, there is no corresponding frequency band.

Table 35: EC200U-EU Operating Frequencies

3GPP Band	Transmit	Receive	Unit
GSM850	824–849	869–894	MHz
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
PCS1900	1850–1910	1930–1990	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz

LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B20	832–862	791–821	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz

Table 36: EC200U-AU Operating Frequencies

3GPP Band	Transmit	Receive	Unit
GSM850	824–849	869–894	MHz
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
PCS1900	1850–1910	1930–1990	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B2	1850–1910	1930-1990	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B4	1710–1755	2110–2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-FDD B66	1710–1780	2110–2180	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz

4.1.3. Reference Design of RF Antenna Interfaces

A reference design of ANT_MAIN and ANT_BT/WIFI_SCAN is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

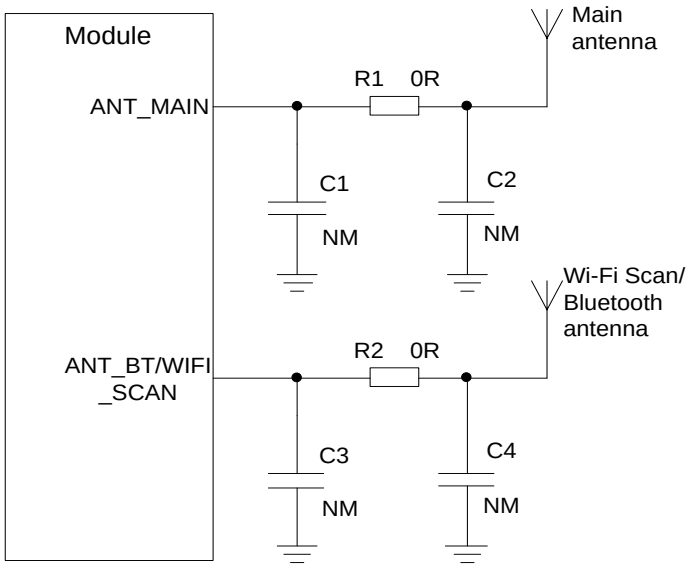


Figure 29: Reference Circuit of RF Antenna Interfaces

NOTE

1. In order to improve the receiving sensitivity, it is necessary to ensure the proper distance between the main antenna and Wi-Fi Scan/Bluetooth receiving antenna.
2. Place the π-type matching components (R1 & C1 & C2 and R2 & C3 & C4) as close to the antenna as possible.

4.2. GNSS Antenna Interface

The following tables list the pin definition and frequency characteristics of the GNSS antenna interface respectively.

Table 37: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment

ANT_GNSS	47	AI	GNSS antenna interface	50 Ω impedance. If unused, keep it open.

Table 38: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BeiDou (Compass)	1561.098 ±2.046	MHz
QZSS	1575.42	MHz

A reference design of GNSS antenna is shown as below:

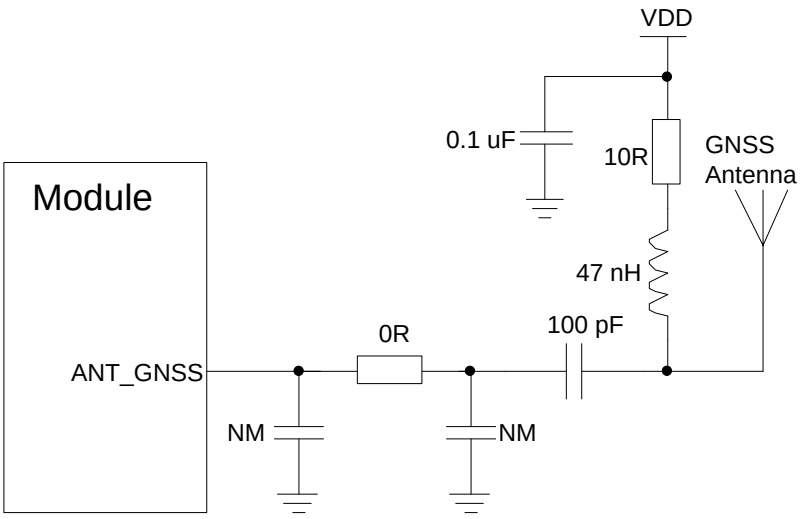


Figure 30: Reference Circuit of GNSS Antenna

NOTE

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. The VDD circuit is not needed if you select a passive antenna.

4.3. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the space between the RF trace and the ground (S). Microstrip and coplanar waveguide are typically used in RF layout to control characteristic impedance. The following figures are reference designs of microstrip or coplanar waveguide with different PCB structures.

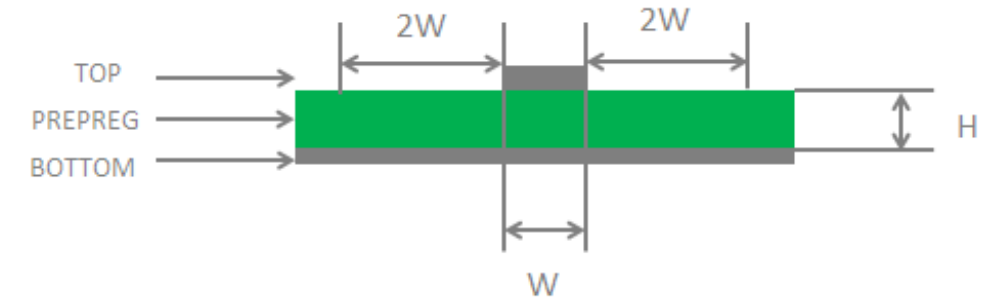


Figure 31: Microstrip Design on a 2-layer PCB

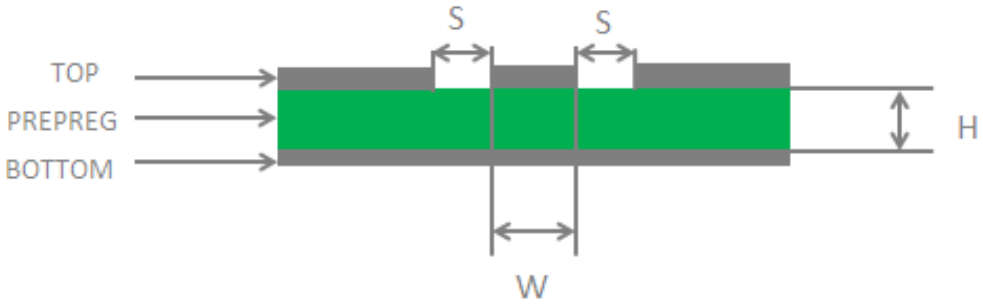


Figure 32: Coplanar Waveguide Design on a 2-layer PCB

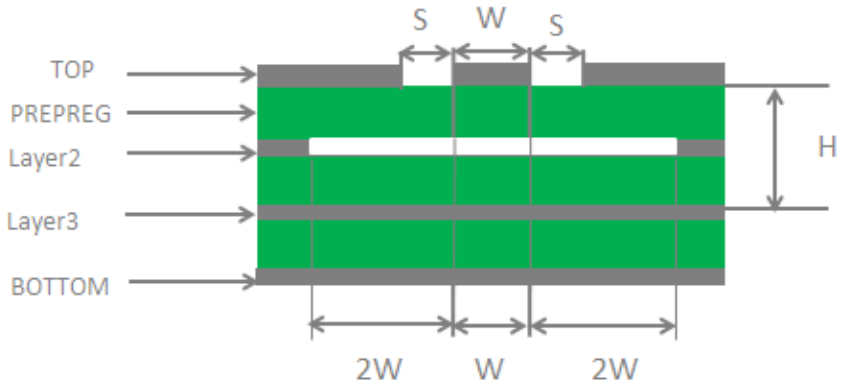


Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

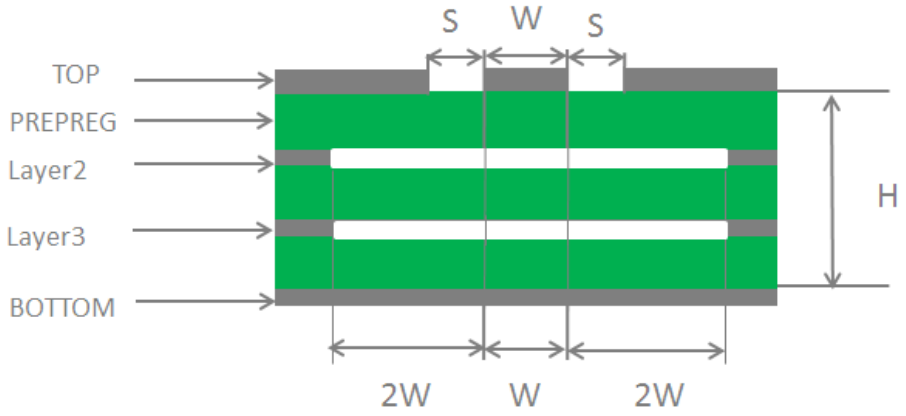


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, please refer to ***document [3]***.

4.4. Antenna Installation

4.4.1. Antenna Requirement

The following table shows the requirements of main antenna.

Table 39: Antenna Requirements

Type	Requirements
GNSS	Frequency range: 1559–1609 MHz Polarization: RHCP or linear VSWR: < 2 (typ.) Passive antenna gain: > 0 dBi Active antenna noise factor: < 1.5 dB Active antenna gain: > 0 dBi Active antenna internal LNA gain: < 17 dB
GSM/LTE	VSWR: ≤ 2 Efficiency: > 30 % Max input power: 50 W Input impedance: 50 Ω < 1 dB: LB (< 1 GHz) < 1.5 dB: MB (1–2.3 GHz) < 2 dB: HB (> 2.3 GHz)

4.4.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

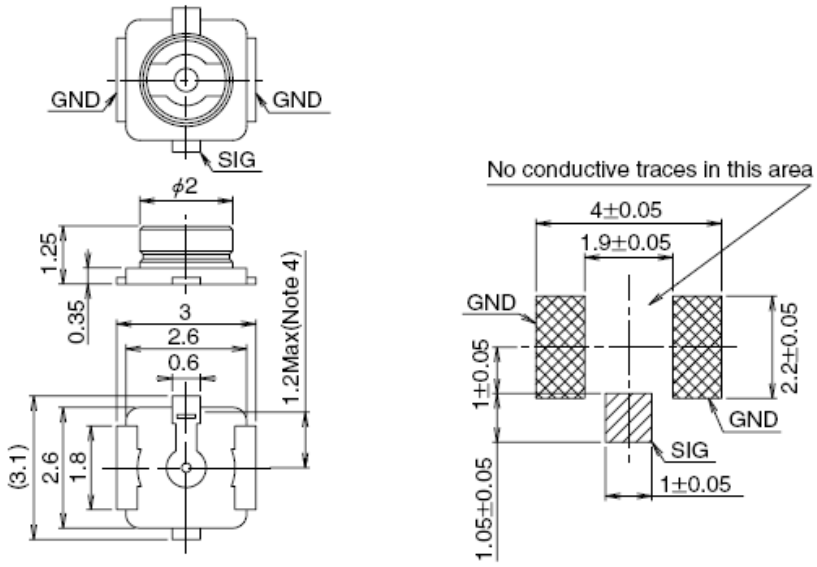


Figure 35: Dimensions of U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

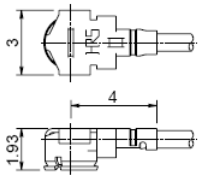
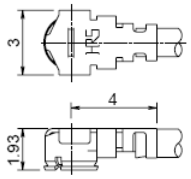
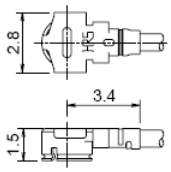
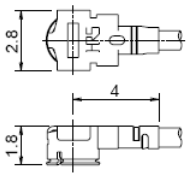
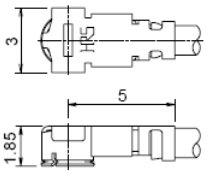
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 36: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

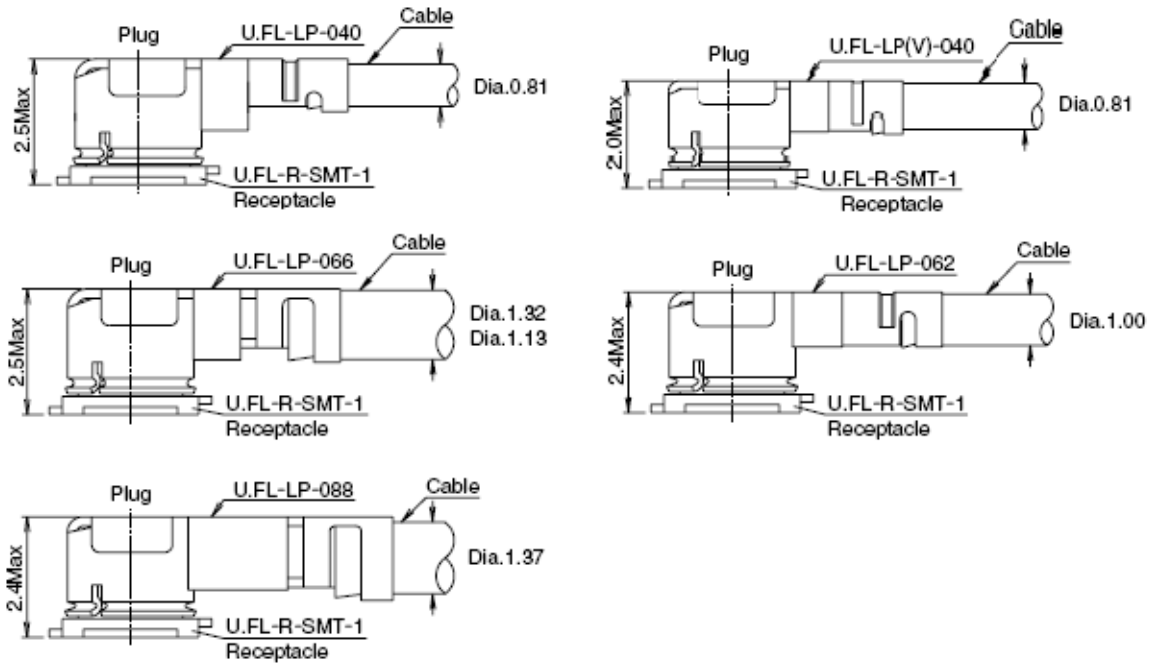


Figure 37: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://hirose.com.

5 Electrical Characteristics, Radio and Reliability

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 40: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	1.5	A
Peak Current of VBAT_RF	-	2.0	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V
Voltage at ADC1	0	VBAT_BB	V
Voltage at ADC2	0	VBAT_BB	V

5.2. Power Supply Ratings

Table 41: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum value.	3.3	3.8	4.3	V
	Voltage drop during burst transmission	Maximum power control level on EGSM900.			400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on EGSM900.		1.8	2.0/3.0	A
USB_VBUS	USB detection		3.5	5.0	5.25	V

NOTE

The power supply should be able to provide sufficient current up to 2.0 A to the module that only supports LTE network, while 3.0 A at least should be provided for GSM network.

5.3. Operating and Storage Temperatures

The operating and storage temperatures are listed in the following table.

Table 42: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [10]	-35	+25	+75	ºC
Extended Temperature Range [11]	-40		+85	ºC
Storage Temperature Range	-40		+90	ºC

5.4. Power Consumption

Table 43: EC200U-CN Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	31	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.126	mA
	EGSM900 @ DRX = 2 (USB disconnected)	3.271	mA
	EGSM900 @ DRX = 5 (USB disconnected)	2.637	mA
	EGSM900 @ DRX = 5 (USB suspend)	4.105	mA
	EGSM900 @ DRX = 9 (USB disconnected)	2.448	mA
	DCS1800 @ DRX = 2 (USB disconnected)	3.265	mA
	DCS1800 @ DRX = 5 (USB disconnected)	2.637	mA
	DCS1800 @ DRX = 5 (USB suspend)	4.206	mA
	DCS1800 @ DRX = 9 (USB disconnected)	2.457	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.515	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.832	mA

[10] Within the operating temperature range, the module meets 3GPP specifications.
[11] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

	LTE-FDD @ PF = 64 (USB suspend)	3.152	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.487	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.314	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.581	mA
	LTE-TDD @ PF = 64 (USB disconnected)	1.868	mA
	LTE-TDD @ PF = 64 (USB suspend)	3.217	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.510	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.329	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	21.10	mA
	EGSM900 @ DRX = 5 (USB connected)	29.89	mA
	LTE-FDD @ PF = 64 (USB disconnected)	21.07	mA
	LTE-FDD @ PF = 64 (USB connected)	29.88	mA
	LTE-TDD @ PF = 64 (USB disconnected)	21.16	mA
	LTE-TDD @ PF = 64 (USB connected)	29.88	mA
GPRS data transfer	EGSM900 4DL/1UL @ 33.2 dBm	231	mA
	EGSM900 3DL/2UL @ 31.3 dBm	344.7	mA
	EGSM900 2DL/3UL @ 29.2 dBm	395.6	mA
	EGSM900 1DL/4UL @ 28.3 dBm	406.9	mA
	DCS1800 4DL/1UL @ 30.1 dBm	156	mA
	DCS1800 3DL/2UL @ 28.5 dBm	213.7	mA
	DCS1800 2DL/3UL @ 26.4 dBm	244.9	mA
	DCS1800 1DL/4UL @ 25.1 dBm	252	mA
LTE data transfer	LTE-FDD B1 @ 23.2 dBm	662.1	mA
	LTE-FDD B3 @ 23.5 dBm	566	mA
	LTE-FDD B5 @ 23.4 dBm	570.9	mA

	LTE-FDD B8 @ 23.1 dBm	545.5	mA
	LTE-TDD B34 @ 23.01 dBm	287.1	mA
	LTE-TDD B38 @ 23.1 dBm	343.9	mA
	LTE-TDD B39 @ 22.95 dBm	294.6	mA
	LTE-TDD B40 @ 23.12 dBm	306.4	mA
	LTE-TDD B41 @ 23.37 dBm	393.3	mA
GSM voice call	EGSM900 PCL = 5 @ 33.27 dBm	250	mA
	EGSM900 PCL = 12 @ 19.42 dBm	92.2	mA
	EGSM900 PCL = 19 @ 6.21 dBm	62.8	mA
	DCS1800 PCL = 0 @ 30.24 dBm	175	mA
	DCS1800 PCL = 7 @ 16.2 dBm	75.4	mA
	DCS1800 PCL = 15 @ 0.87 dBm	57.7	mA

NOTE

The GSM network access technology of EC200U-CN is optional. If the module that you select doesn't support GSM network access technology, there is no corresponding current consumption.

Table 44: EC200U-EU Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	40	μA
Sleep state	**AT+CFUN = 0** (USB disconnected)	1.139	mA
	GSM850 @ DRX = 2 (USB disconnected)	2.078	mA
	GSM850 @ DRX = 5 (USB disconnected)	1.555	mA
	GSM850 @ DRX = 5 (USB suspend)	2.739	mA
	GSM850 @ DRX = 9 (USB disconnected)	1.392	mA
	DCS1800 @ DRX = 2 (USB disconnected)	2.085	mA

	DCS1800 @ DRX = 5 (USB disconnected)	1.551	mA
	DCS1800 @ DRX = 5 (USB suspend)	2.778	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.381	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.535	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.848	mA
	LTE-FDD @ PF = 64 (USB suspend)	3.099	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.490	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.311	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.584	mA
	LTE-TDD @ PF = 64 (USB disconnected)	1.871	mA
	LTE-TDD @ PF = 64 (USB suspend)	3.086	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.503	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	13.01	mA
	EGSM900 @ DRX = 5 (USB connected)	28.94	mA
	LTE-FDD @ PF = 64 (USB disconnected)	12.68	mA
	LTE-FDD @ PF = 64 (USB connected)	27.92	mA
	LTE-TDD @ PF = 64 (USB disconnected)	12.70	mA
	LTE-TDD @ PF = 64 (USB connected)	27.95	mA
GPRS data transfer	GSM850 4DL/1UL @ 32.89 dBm	254	mA
	GSM850 3DL/2UL @ 30.9 dBm	383	mA
	GSM850 2DL/3UL @ 28.67 dBm	431	mA
	GSM850 1DL/4UL @ 26.54 dBm	448	mA
	EGSM900 4DL/1UL @ 32.55 dBm	231	mA
	EGSM900 3DL/2UL @ 31.3 dBm	344.7	mA
	EGSM900 2DL/3UL @ 29.2 dBm	395.6	mA

	EGSM900 1DL/4UL @ 28.3 dBm	406.9	mA
	DCS1800 4DL/1UL @ 30.1 dBm	156	mA
	DCS1800 3DL/2UL @ 28.5 dBm	213.7	mA
	DCS1800 2DL/3UL @ 26.4 dBm	244.9	mA
	DCS1800 1DL/4UL @ 25.1 dBm	252	mA
	PCS1900 4DL/1UL @ 29.93 dBm	153	mA
	PCS1900 3DL/2UL @ 27.99 dBm	219	mA
	PCS1900 2DL/3UL @ 25.94 dBm	249	mA
	PCS1900 1DL/4UL @ 23.87 dBm	261	mA
LTE data transfer	LTE-FDD B1 @ 23.4 dBm	607	mA
	LTE-FDD B3 @ 22.96 dBm	508	mA
	LTE-FDD B5 @ 23 dBm	492	mA
	LTE-FDD B7 @ 22.8dBm	709	mA
	LTE-FDD B8 @ 23.1 dBm	558	mA
	LTE-FDD B20 @ 23 dBm	576	mA
	LTE-FDD B28 @ 23.3 dBm	586	mA
	LTE-TDD B38 @ 23.1 dBm	320.9	mA
	LTE-TDD B40 @ 23.12 dBm	286	mA
	LTE-TDD B41 @ 23.37 dBm	317	mA
GSM voice call	GSM850 PCL = 5 @ 33 dBm	246	mA
	GSM850 PCL = 12 @ 19.8 dBm	95	mA
	GSM850 PCL = 19 @ 6.7 dBm	64	mA
	EGSM900 PCL = 5 @ 33.27 dBm	250	mA
	EGSM900 PCL = 12 @ 19.42 dBm	92.2	mA
	EGSM900 PCL = 19 @ 6.21 dBm	62.8	mA

	DCS1800 PCL = 0 @ 30.24 dBm	175	mA
	DCS1800 PCL = 7 @ 16.2 dBm	75.4	mA
	DCS1800 PCL = 15 @ 0.87 dBm	57.7	mA
	PCS1900 PCL = 0 @ 29.8 dBm	168	mA
	PCS1900 PCL = 7 @ 16.6 dBm	78	mA
	PCS1900 PCL = 15 @ 0.8 dBm	59	mA

Table 45: EC200U-AU Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	TBD	μA
Sleep state	**AT+CFUN = 0** (USB disconnected)	TBD	mA
	GSM850 @ DRX = 2 (USB disconnected)	TBD	mA
	GSM850 @ DRX = 5 (USB disconnected)	TBD	mA
	GSM850 @ DRX = 5 (USB suspend)	TBD	mA
	GSM850 @ DRX = 9 (USB disconnected)	TBD	mA
	DCS1800 @ DRX = 2 (USB disconnected)	TBD	mA
	DCS1800 @ DRX = 5 (USB disconnected)	TBD	mA
	DCS1800 @ DRX = 5 (USB suspend)	TBD	mA
	DCS1800 @ DRX = 9 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 32 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 64 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 64 (USB suspend)	TBD	mA
	LTE-FDD @ PF = 128 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 256 (USB disconnected)	TBD	mA
	LTE-TDD @ PF = 32 (USB disconnected)	TBD	mA

	LTE-TDD @ PF = 64 (USB disconnected)	TBD	mA
	LTE-TDD @ PF = 64 (USB suspend)	TBD	mA
	LTE-TDD @ PF = 128 (USB disconnected)	TBD	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	TBD	mA
	EGSM900 @ DRX = 5 (USB connected)	TBD	mA
	LTE-FDD @ PF = 64 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 64 (USB connected)	TBD	mA
	LTE-TDD @ PF = 64 (USB disconnected)	TBD	mA
	LTE-TDD @ PF = 64 (USB connected)	TBD	mA
GPRS data transfer	GSM850 4DL/1UL @ 32.89 dBm	TBD	mA
	GSM850 3DL/2UL @ 30.9 dBm	TBD	mA
	GSM850 2DL/3UL @ 28.67 dBm	TBD	mA
	GSM850 1DL/4UL @ 26.54 dBm	TBD	mA
	EGSM900 4DL/1UL @ 32.55 dBm	TBD	mA
	EGSM900 3DL/2UL @ 31.3 dBm	TBD	mA
	EGSM900 2DL/3UL @ 29.2 dBm	TBD	mA
	EGSM900 1DL/4UL @ 28.3 dBm	TBD	mA
	DCS1800 4DL/1UL @ 30.1 dBm	TBD	mA
	DCS1800 3DL/2UL @ 28.5 dBm	TBD	mA
	DCS1800 2DL/3UL @ 26.4 dBm	TBD	mA
	DCS1800 1DL/4UL @ 25.1 dBm	TBD	mA
	PCS1900 4DL/1UL @ 29.93 dBm	TBD	mA
	PCS1900 3DL/2UL @ 27.99 dBm	TBD	mA
	PCS1900 2DL/3UL @ 25.94 dBm	TBD	mA
	PCS1900 1DL/4UL @ 23.87 dBm	TBD	mA

LTE data transfer	LTE-FDD B1 @ 23.4 dBm	TBD	mA
	LTE-FDD B2 @ 23.4 dBm	TBD	mA
	LTE-FDD B3 @ 22.96 dBm	TBD	mA
	LTE-FDD B4 @ 22.96 dBm	TBD	mA
	LTE-FDD B5 @ 23 dBm	TBD	mA
	LTE-FDD B7 @ 22.8dBm	TBD	mA
	LTE-FDD B8 @ 23.1 dBm	TBD	mA
	LTE-FDD B28 @ 23.3 dBm	TBD	mA
	LTE-FDD B66 @ 23.3 dBm	TBD	mA
	LTE-TDD B38 @ 23.1 dBm	TBD	mA
	LTE-TDD B40 @ 23.12 dBm	TBD	mA
	LTE-TDD B41 @ 23.37 dBm	TBD	mA
GSM voice call	GSM850 PCL = 5 @ 33 dBm	TBD	mA
	GSM850 PCL = 12 @ 19.8 dBm	TBD	mA
	GSM850 PCL = 19 @ 6.7 dBm	TBD	mA
	EGSM900 PCL = 5 @ 33.27 dBm	TBD	mA
	EGSM900 PCL = 12 @ 19.42 dBm	TBD	mA
	EGSM900 PCL = 19 @ 6.21 dBm	TBD	mA
	DCS1800 PCL = 0 @ 30.24 dBm	TBD	mA
	DCS1800 PCL = 7 @ 16.2 dBm	TBD	mA
	DCS1800 PCL = 15 @ 0.87 dBm	TBD	mA
	PCS1900 PCL = 0 @ 29.8 dBm	TBD	mA
	PCS1900 PCL = 7 @ 16.6 dBm	TBD	mA
	PCS1900 PCL = 15 @ 0.8 dBm	TBD	mA

5.5. Tx Power

The following table shows the RF output power of EC200U series module.

Table 46: EC200U-CN RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B5/B8	23 dBm ±2 dB	< -39 dBm
LTE-TDD B34/B38/B39/B40/B41	23 dBm ±2 dB	< -39 dBm

NOTE

The GSM network access technology of EC200U-CN is optional. If the module that you select doesn't support GSM network access technology, there is no corresponding RF output power.

Table 47: EC200U-EU RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
GSM850	33 dBm ±2 dB	5 dBm ±5 dB
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B5/B7/B8/B20/B28	23 dBm ±2 dB	< -39 dBm
LTE-TDD B38/B40/B41	23 dBm ±2 dB	< -39 dBm

Table 48: EC200U-AU RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
GSM850	33 dBm ±2 dB	5 dBm ±5 dB

EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B1/B2/B3/B4/B5/B7/B8/B28/B66	23 dBm ±2 dB	< -39 dBm
LTE-TDD B38/B40/B41	23 dBm ±2 dB	< -39 dBm

NOTE

In GPRS 4 slots TX mode, the maximum output power is reduced by 6 dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

5.6. Rx Sensitivity

The following tables show conducted RF receiving sensitivity of EC200U series module.

Table 49: EC200U-CN Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)	3GPP
	Primary	
EGSM900	-109.5 dBm	-102.0 dBm
DCS1800	-109.5 dBm	-102.0 dBm
LTE-FDD B1 (10 MHz)	-98.5 dBm	-96.3 dBm
LTE-FDD B3 (10 MHz)	-99.6 dBm	-93.3 dBm
LTE-FDD B5 (10 MHz)	-99.2 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98.7 dBm	-93.3 dBm
LTE-TDD B34 (10 MHz)	-99.2 dBm	-96.3 dBm
LTE-TDD B38 (10 MHz)	-98.8 dBm	-96.3 dBm
LTE-TDD B39 (10 MHz)	-99.5 dBm	-96.3 dBm

LTE-TDD B40 (10 MHz)	-99.4 dBm	-96.3 dBm
LTE-TDD B41 (10 MHz)	-98.9 dBm	-94.3 dBm

NOTE

The GSM network access technology of EC200U-CN is optional. If the module that you select doesn't support GSM network access technology, there is no corresponding RF receiving sensitivity data.

Table 50: EC200U-EU Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)	3GPP
	Primary	
GSM850	-109.5 dBm	-102.0 dBm
EGSM900	-109.5 dBm	-102.0 dBm
DCS1800	-109 dBm	-102.0 dBm
PCS1900	-109 dBm	-102.0 dBm
LTE-FDD B1 (10 MHz)	-97.8 dBm	-96.3 dBm
LTE-FDD B3 (10 MHz)	-98.5 dBm	-93.3 dBm
LTE-FDD B5 (10 MHz)	-99.2 dBm	-94.3 dBm
LTE-FDD B7 (10 MHz)	-97 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98.7 dBm	-93.3 dBm
LTE-FDD B20 (10 MHz)	-98 dBm	-93.3 dBm
LTE-FDD B28 (10 MHz)	-98.8 dBm	-94.8 dBm
LTE-TDD B38 (10 MHz)	-98.3 dBm	-96.3 dBm
LTE-TDD B40 (10 MHz)	-98.5 dBm	-96.3 dBm
LTE-TDD B41 (10 MHz)	-98 dBm	-94.3 dBm

Table 51: EC200U-AU Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)	3GPP
	Primary	
GSM850	TBD	-102.0 dBm
EGSM900	TBD	-102.0 dBm
DCS1800	TBD	-102.0 dBm
PCS1900	TBD	-102.0 dBm
LTE-FDD B1 (10 MHz)	TBD	-96.3 dBm
LTE-FDD B2 (10 MHz)	TBD	-94.3 dBm
LTE-FDD B3 (10 MHz)	TBD	-93.3 dBm
LTE-FDD B4 (10 MHz)	TBD	-96.3 dBm
LTE-FDD B5 (10 MHz)	TBD	-94.3 dBm
LTE-FDD B7 (10 MHz)	TBD	-94.3 dBm
LTE-FDD B8 (10 MHz)	TBD	-93.3 dBm
LTE-FDD B28 (10 MHz)	TBD	-94.8 dBm
LTE-FDD B66 (10 MHz)	TBD	-96.3 dBm
LTE-TDD B38 (10 MHz)	TBD	-96.3 dBm
LTE-TDD B40 (10 MHz)	TBD	-96.3 dBm
LTE-TDD B41 (10 MHz)	TBD	-94.3 dBm

5.7. ESD

If the static electricity generated by various ways discharges to the module, the module maybe damaged to a certain extent. Thus, please take proper ESD countermeasures and handling methods. For example, wearing anti-static gloves during the development, production, assembly and testing of the module; adding ESD protective components to the ESD sensitive interfaces and points in the product design.

The following table shows the module electrostatics discharge characteristics.

Table 52: Electrostatics Discharge Characteristics (25 ºC, 45 % Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter. The tolerances for dimensions without tolerance values are ±0.2 mm.

6.1. Mechanical Dimensions

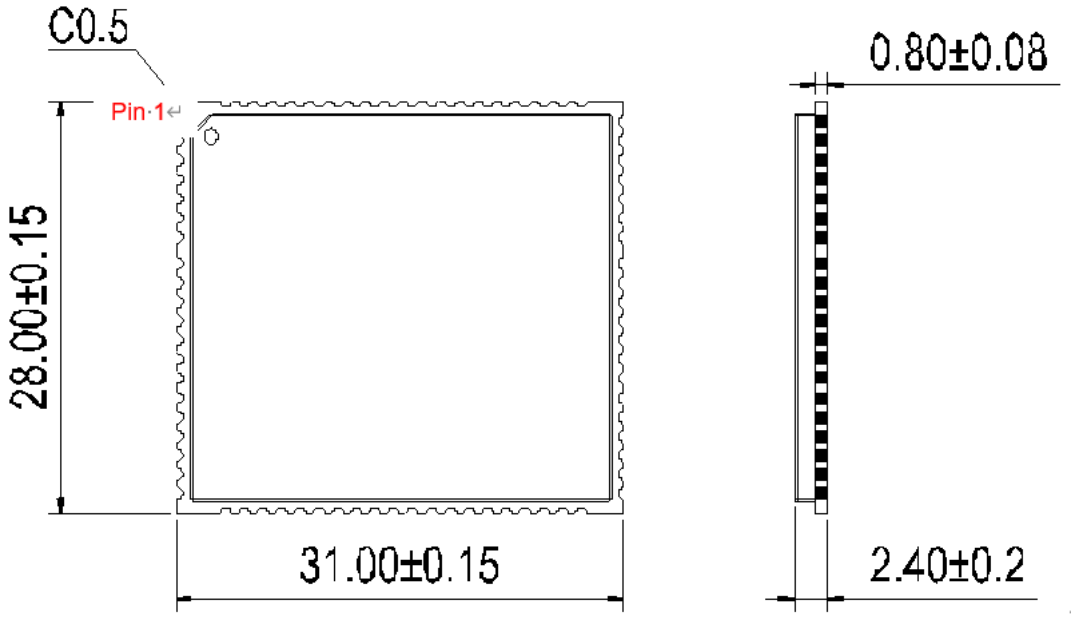


Figure 38: Module Top and Side Dimensions

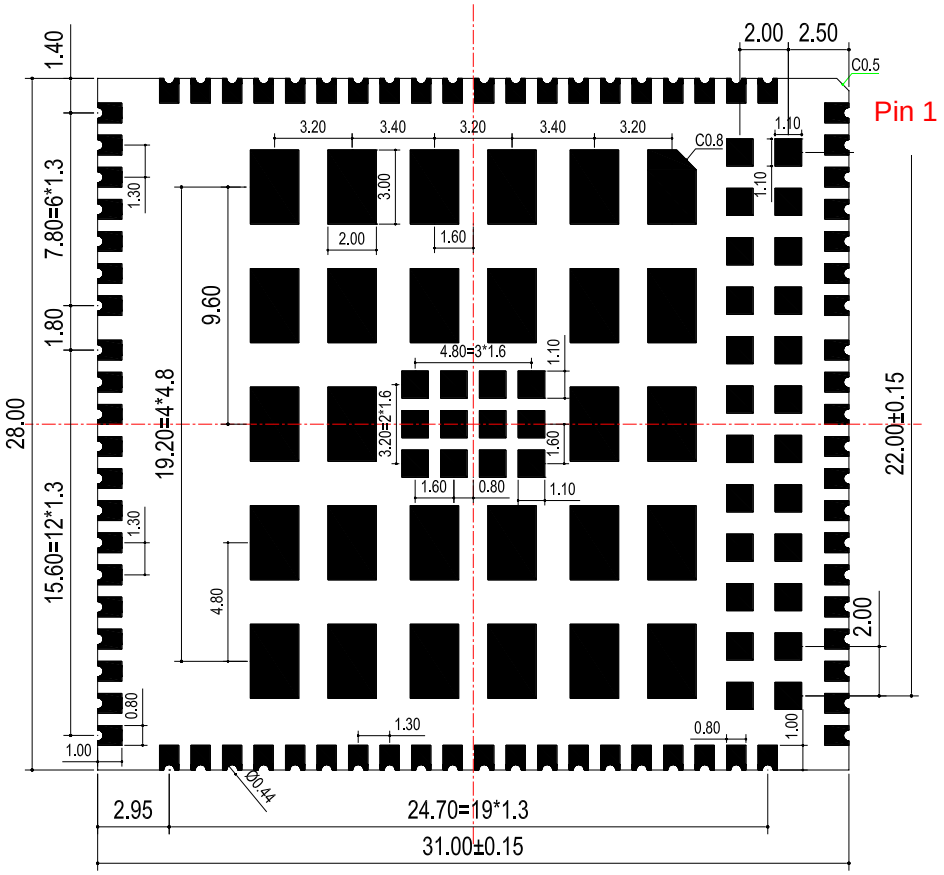


Figure 39: Module Bottom Dimensions

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

6.2. Recommended Footprint

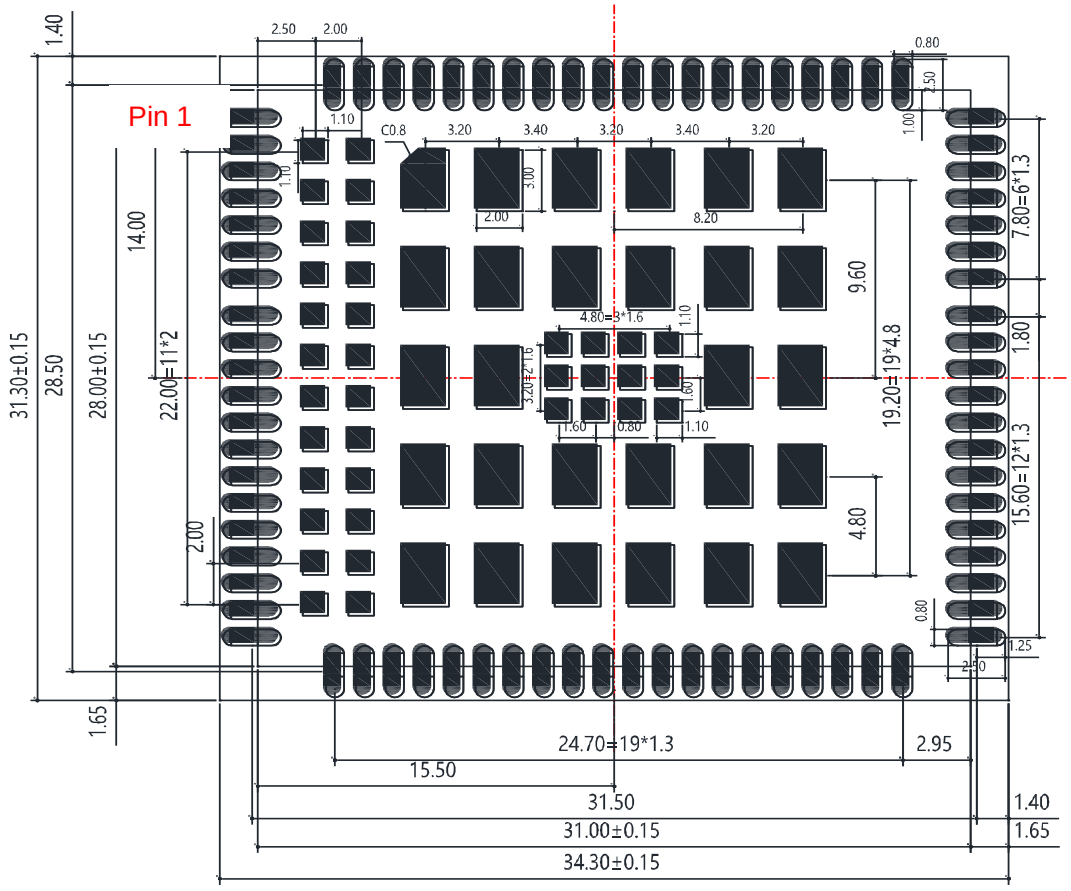


Figure 40: Recommended Footprint (Top View)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

6.3. Top and Bottom Views

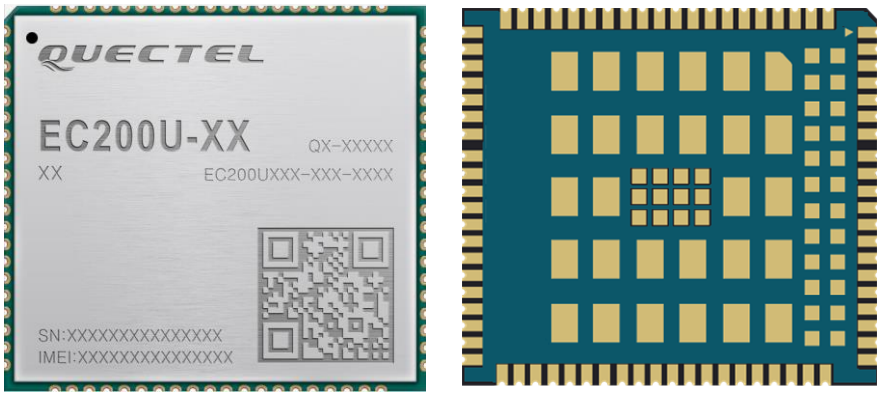


Figure 41: Top & Bottom View of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

7 Storage, Manufacturing & Packaging

7.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours[12] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:
   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

[12] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20 mm. For more details, please refer to ***document [4]***.

It is suggested that the peak reflow temperature is 235–246 ºC, and the absolute maximum reflow temperature is 246 ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

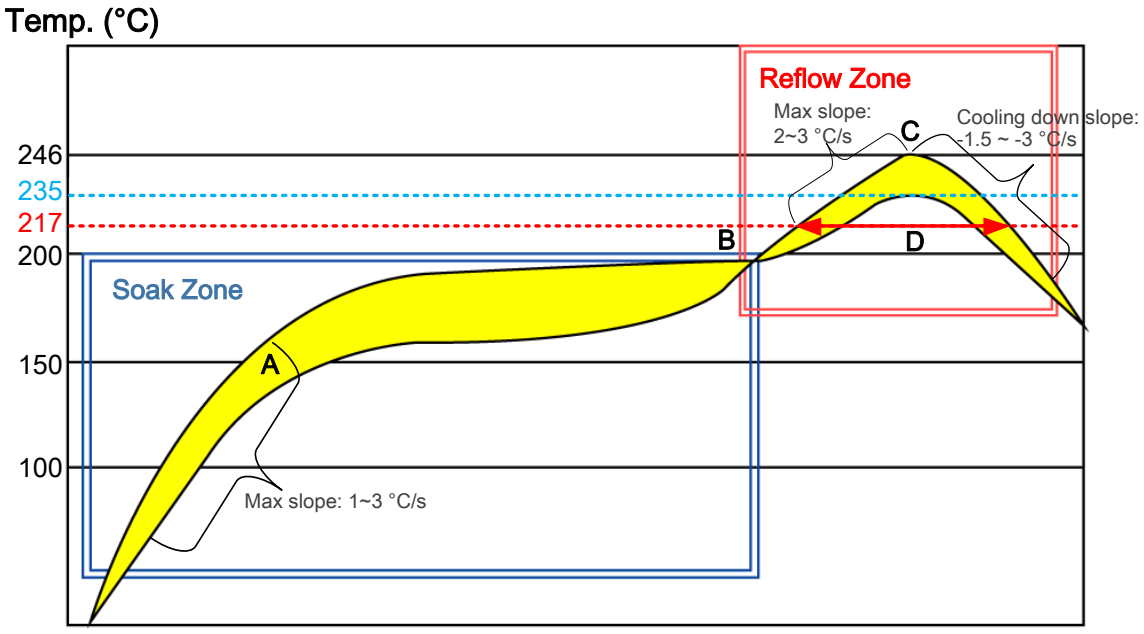


Figure 42: Reflow Soldering Thermal Profile

Table 53: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max. slope	1 to 3 °C/sec
Soak time (between A and B: 150 °C and 200 °C)	70 to 120 sec
Reflow Zone	
Max. slope	2 to 3 °C/sec
Reflow time (D: over 217 °C)	40 to 70 sec
Max. temperature	235 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [4]***.

7.3. Packaging Specifications

The module adopts carrier tape packaging and details are as follow:

7.3.1. Carrier Tape

Dimension details are as follow:

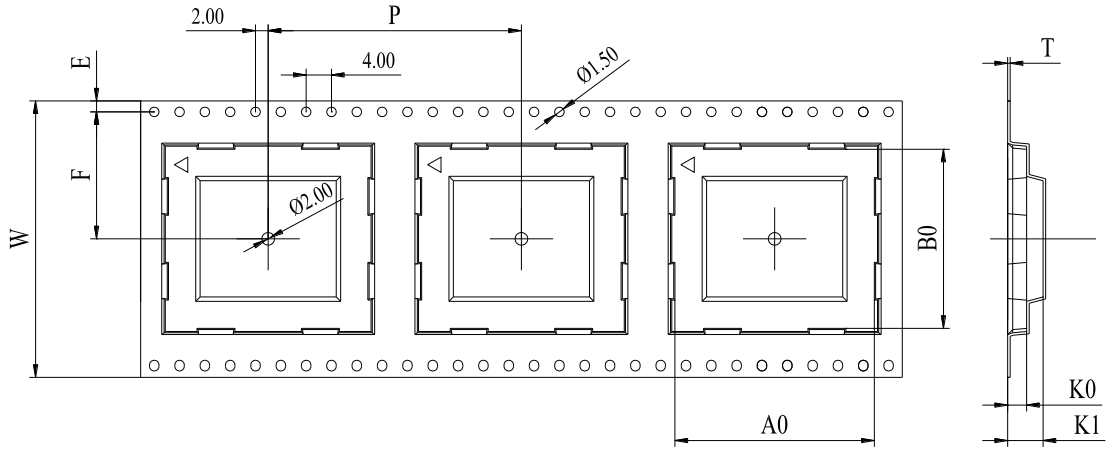


Figure 43: Carrier Tape Dimension Drawing

Table 54: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	40	0.4	31.5	28.5	3.0	5.6	20.2	1.75

7.3.2. Plastic Reel

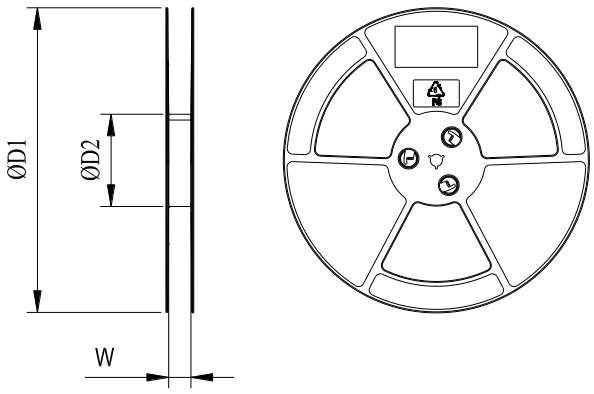
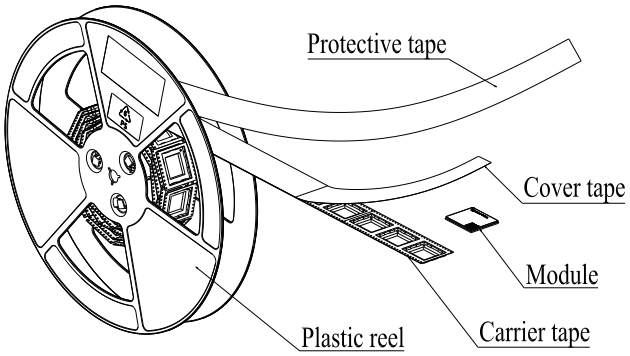


Figure 44: Plastic Reel Dimension Drawing

Table 55: Plastic Reel Dimension Table (Unit: mm)

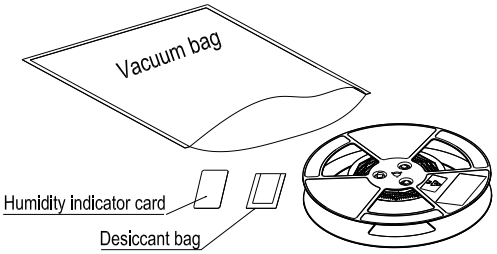
øD1	øD2	W
330	100	44.5

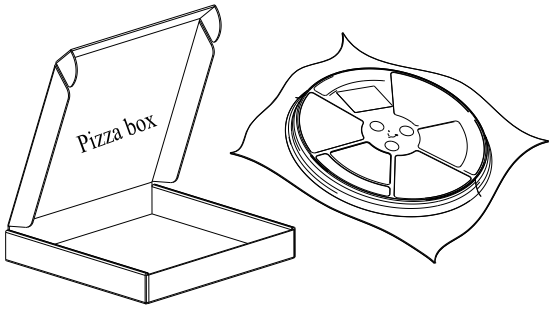
7.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 1000 modules.

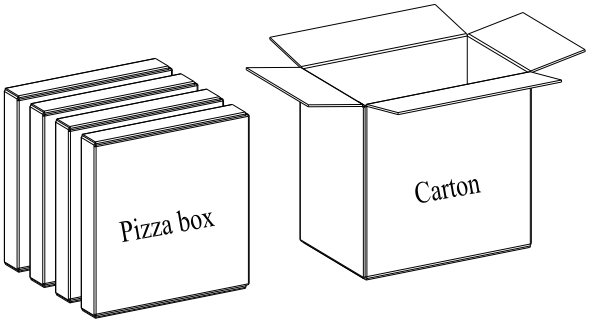


Figure 45: **Packaging Process**

8 Appendix References

Table 56: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EC200U&EG915U_Series_AT_Commands_Manual
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_SMT_User_Guide

Table 57: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection Multiplexing
CS	Coding Scheme
CTS	Clear to Send
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DMA	Direct Memory Access
DSDS	Dual SIM Dual Standby
DTE	Data Terminal Equipment

DTR	Data Terminal Ready
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
EVB	Evaluation Board
FDD	Frequency Division Duplex
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP-over-SSL
GND	Ground
GSM	Global System for Mobile Communications
HR	Half Rate
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
LED	Light Emitting Diode
LTE	Long Term Evolution
MCU	Microcontroller Unit/Microprogrammed Control Unit
ME	Mobile Equipment
MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport
MSL	Moisture Sensitivity Level
NITZ	Network Identity and Time Zone
NTP	Network Time Protocol

PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PF	Paging Frame
POS	Point of Sale
PPP	Point-to-Point Protocol
RF	Radio Frequency
RGB	Red, Green, Blue
SM	Smart Media
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver &Transmitter
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnom	Nominal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum High-level Input Voltage

V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
V_{OH}max	Maximum High-level Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network