EG915U Series

Hardware Design

LTE Standard Module Series

Version: 1.0

Date: 2021-11-23

Status: Released

At Quectel, our aim is to provide timely and comprehensive services to our customers. If you require any assistance, please contact our headquarters:

Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local offices. For more information, please visit:
http://www.quectel.com/support/sales.htm.

For technical support, or to report documentation errors, please visit:
http://www.quectel.com/support/technical.htm.
Or email us at: support@quectel.com.

Legal Notices

We offer information as a service to you. The provided information is based on your requirements and we make every effort to ensure its quality. You agree that you are responsible for using independent analysis and evaluation in designing intended products, and we provide reference designs for illustrative purposes only. Before using any hardware, software or service guided by this document, please read this notice carefully. Even though we employ commercially reasonable efforts to provide the best possible experience, you hereby acknowledge and agree that this document and related services hereunder are provided to you on an “as available” basis. We may revise or restate this document from time to time at our sole discretion without any prior notice to you.

Use and Disclosure Restrictions

License Agreements

Documents and information provided by us shall be kept confidential, unless specific permission is granted. They shall not be accessed or used for any purpose except as expressly provided herein.

Copyright

Our and third-party products hereunder may contain copyrighted material. Such copyrighted material shall not be copied, reproduced, distributed, merged, published, translated, or modified without prior written consent. We and the third party have exclusive rights over copyrighted material. No license shall be granted or conveyed under any patents, copyrights, trademarks, or service mark rights. To avoid ambiguities, purchasing in any form cannot be deemed as granting a license other than the normal non-exclusive, royalty-free license to use the material. We reserve the right to take legal action for noncompliance with abovementioned requirements, unauthorized use, or other illegal or malicious use of the material.

Trademarks

Except as otherwise set forth herein, nothing in this document shall be construed as conferring any rights to use any trademark, trade name or name, abbreviation, or counterfeit product thereof owned by Quectel or any third party in advertising, publicity, or other aspects.

Third-Party Rights

This document may refer to hardware, software and/or documentation owned by one or more third parties ("third-party materials"). Use of such third-party materials shall be governed by all restrictions and obligations applicable thereto.

We make no warranty or representation, either express or implied, regarding the third-party materials, including but not limited to any implied or statutory, warranties of merchantability or fitness for a particular purpose, quiet enjoyment, system integration, information accuracy, and non-infringement of any third-party intellectual property rights with regard to the licensed technology or use thereof. Nothing herein constitutes a representation or warranty by us to either develop, enhance, modify, distribute, market, sell, offer for sale, or otherwise maintain production of any our products or any other hardware, software, device, tool, information, or product. We moreover disclaim any and all warranties arising from the course of dealing or usage of trade.

Privacy Policy

To implement module functionality, certain device data are uploaded to Quectel's or third-party's servers, including carriers, chipset suppliers or customer-designated servers. Quectel, strictly abiding by the relevant laws and regulations, shall retain, use, disclose or otherwise process relevant data for the purpose of performing the service only or as permitted by applicable laws. Before data interaction with third parties, please be informed of their privacy and data security policy.

Disclaimer

a) We acknowledge no liability for any injury or damage arising from the reliance upon the information.
b) We shall bear no liability resulting from any inaccuracies or omissions, or from the use of the information contained herein.
c) While we have made every effort to ensure that the functions and features under development are free from errors, it is possible that they could contain errors, inaccuracies, and omissions. Unless otherwise provided by valid agreement, we make no warranties of any kind, either implied or express, and exclude all liability for any loss or damage suffered in connection with the use of features and functions under development, to the maximum extent permitted by law, regardless of whether such loss or damage may have been foreseeable.
d) We are not responsible for the accessibility, safety, accuracy, availability, legality, or completeness of information, advertising, commercial offers, products, services, and materials on third-party websites and third-party resources.

Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.

Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.

The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.

In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2021-11-23	Len CHEN/Reuben WANG/ Frank WANG/Ailsa WANG	Creation of the document
1.0	2021-11-23	Len CHEN/Reuben WANG/ Frank WANG/Ailsa WANG	First official release

Contents

Table Index

Figure Index

1 Introduction

This document defines the EG915U series module and describes its air interfaces and hardware interfaces which are connected with relate to customers' applications.

It can help customers quickly understand interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, customers can use this module to design and to set up mobile applications easily.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable.

2 Product Overview

EG915U series module is an LTE-FDD, LTE-TDD and GSM wireless communication module, which provides data connectivity on LTE-FDD, LTE-TDD and GPRS networks. It also provides voice functionality, Bluetooth and Wi-Fi Scan [1] to meet your specific application demands. Related information and details are listed in the table below:

Table 2: Brief Introduction of the Module

Categories	
Packaging and pins number	126-pin; LGA
Dimensions	(23.6 ±0.2) mm × (19.9 ±0.2) mm × (2.4±0.2)mm
Weight	2.5 ±0.2 g
Wireless network functions	LTE/GSM/Bluetooth/Wi-Fi Scan [1]
Variants	EG915U-CN [2]; EG915U-EU; EG915U-LA

2.1. Frequency Bands and Functions

Table 2: Wireless Network Type

Wireless Network Type	EG915U-CN	EG915U-EU	EG915U-LA
LTE-FDD	B1/B3/B5/B8	B1/B3/B5/B7/B8/B20/B28	B2/B3/B4/B5/B7/B8/B28 /B66
LTE-TDD	B34/B38/B39/B40/B41	-	-
GSM	900/1800 MHz	850/900/1800/1900 MHz	850/900/1800/1900 MHz
Bluetooth and Wi-Fi Scan [1]	2.4 GHz	2.4 GHz	2.4 GHz

[1] EG915U series support Bluetooth and Wi-Fi Scan functions. Due to the shared antenna interface, the two functions cannot be used simultaneously. Bluetooth and Wi-Fi Scan functions are optional (both supported or not), please contact Quectel Technical Support for details.
[2] Only EG915U-CN provides LTE-TDD, please consult Quectel Technical Support for details.

2.2. Key Features

The following table describes the detailed features of EG915U series module.

Table 4: Key Features of EG915U Series Module

Features	Description
Power Supply	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	**EG915U-CN:** ● EGSM900: Class 4 (33 dBm ±2 dB) ● DCS1800: Class 1 (30 dBm ±2 dB) ● LTE-FDD: Class 3 (23 dBm ±2 dB) ● LTE-TDD: Class 3 (23 dBm ±2 dB) **EG915U-EU:** ● GSM850/EGSM900: Class 4 (33 dBm ±2 dB) ● DCS1800/PCS1900: Class 1 (30 dBm ±2 dB) ● LTE-FDD: Class 3 (23 dBm ±2 dB) **EG915U-LA:** ● GSM850/EGSM900: Class 4 (33 dBm ±2 dB) ● DCS1800/PCS1900: Class 1 (30 dBm ±2 dB) ● LTE-FDD: Class 3 (23 dBm ±2 dB)
LTE Features	**EG915U-CN:** ● Supports up to Cat 1 FDD/TDD. ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth. ● Supports uplink QPSK, 16QAM. ● Supports downlink QPSK, 16QAM and 64QAM. ● FDD: Max 10 Mbps (DL)/5 Mbps (UL). ● TDD: Max 8.96 Mbps (DL)/3.1 Mbps (UL). **EG915U-EU:** ● Supports up to Cat 1 FDD. ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth. ● Supports uplink QPSK, 16QAM. ● Supports downlink QPSK, 16QAM and 64QAM. ● FDD: Max 10 Mbps (DL)/5 Mbps (UL). **EG915U-LA:** ● Supports up to Cat 1 FDD. ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth. ● Supports uplink QPSK, 16QAM. ● Supports downlink QPSK, 16QAM and 64QAM.

	● FDD: Max 10 Mbps (DL)/5 Mbps (UL).
GSM Features	**GPRS:** ● Supports GPRS multi-slot class 12 ● Coding scheme: CS-1/CS-2/CS-3/CS-4 ● Max 85.6 Kbps (DL)/85.6 Kbps (UL)
Internet Protocol Features	● Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS/ FTPS/SSL/FILE/MQTT/MMS protocols ● Support PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) protocols which are usually used for PPP connection
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: Stored in (U)SIM card and ME, stored in ME by default
(U)SIM Interface	● Supports USIM/SIM card: 1.8/3.0 V
UART Interfaces	**Main UART** ● Used for AT command communication and data transmission ● Baud rates reach up to 921600 bps; 115200 bps by default ● Supports RTS and CTS hardware flow control **Debug UART** ● Used for the output of partial logs ● Baud rate: 921600 bps ● Only used for debug UART, cannot be used for universal UART **Auxiliary UART**
SPI Interface	● Supports one SPI Interface (master mode only)
I2C Interface	● Supports one I2C Interface
PCM Interface	● Supports one PCM Interface
Audio Features	● Supports one analog audios input and one analog audios output ● GSM: HR/FR/EFR/AMR/AMR-WB ● Supports echo cancellation and noise suppression
ADC Interfaces	● Supports two ADC Interfaces
Network Indication	● NET_STATUS used to indicate the network connectivity status
AT Commands	● Compliant with *3G PP TS 27.007, 27.005* and Quectel enhanced AT commands
USB_BOOT Interface	● Supports one download control interface
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● Bluetooth and Wi-Fi Scan antenna interface (ANT_BT/WIFI_SCAN) ● 50 Ω impedance

Position Fixing	●	Support Wi-Fi Scan
Temperature Range	●	Operation temperature range: -35 to +75 °C [4] ● Extended temperature range: -40 to +85 °C [5] ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	●	USB interface and DFOTA
RoHS	●	All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- Flash
- Radio frequency
- Peripheral interfaces

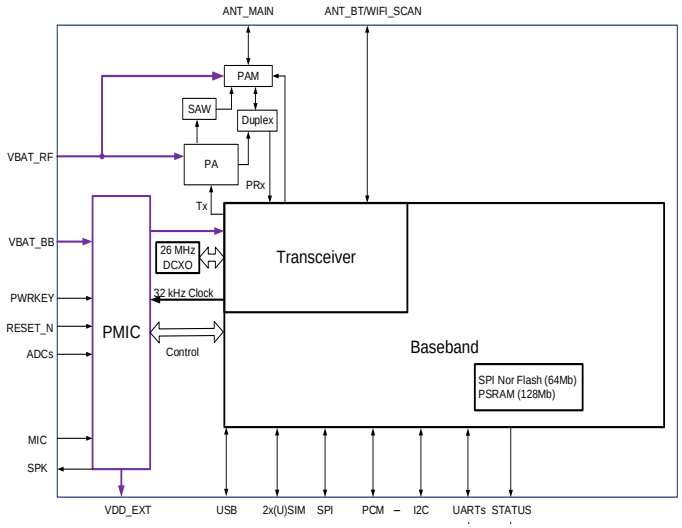


Figure 1: Functional Diagram

[4] Within operating temperature range, the module meets 3GPP specifications.
[5] Within extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

2.4. Pin Assignment

The following figure illustrates the pin assignment of the module.

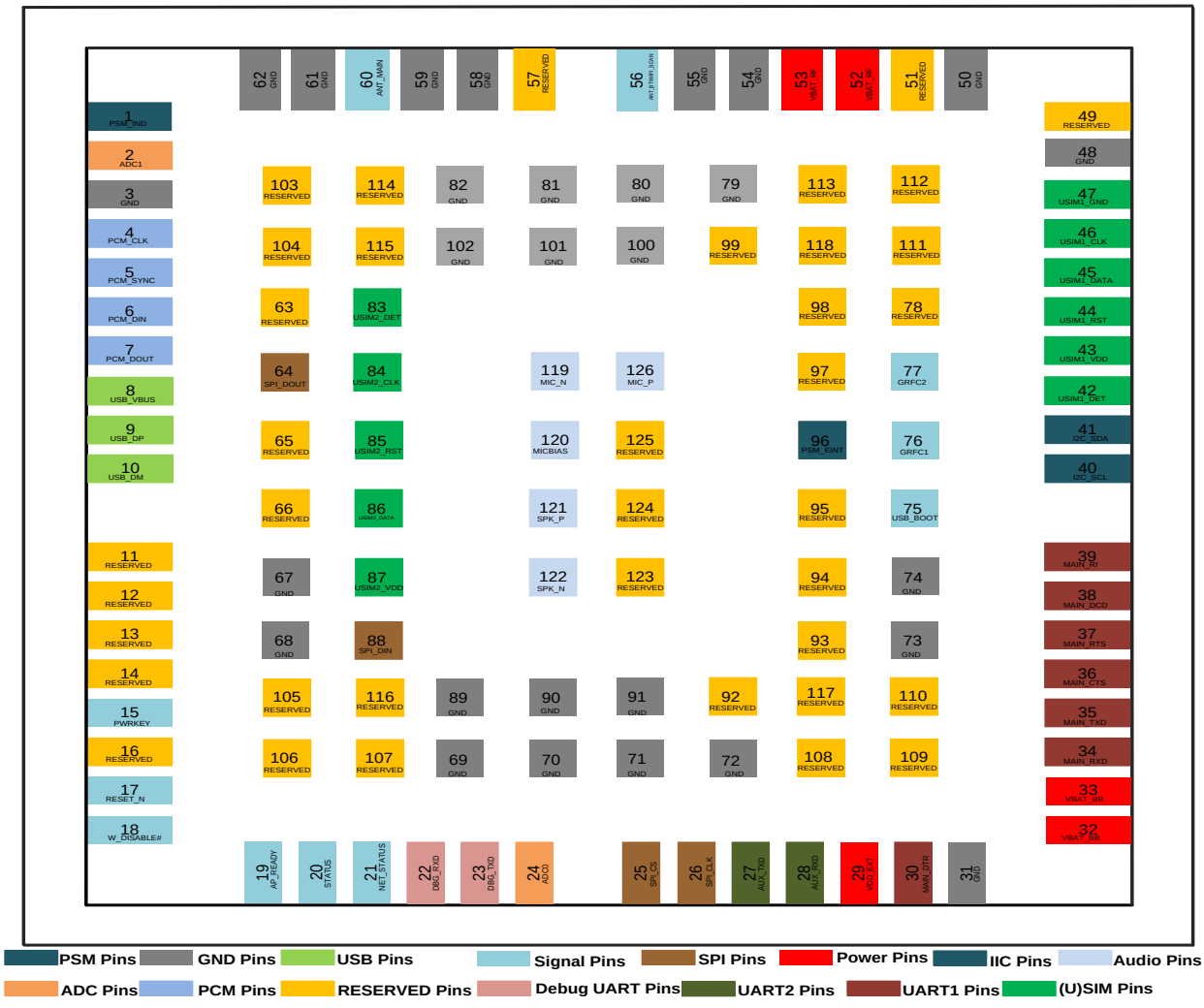


Figure 2: EG915U Series Module Pin Assignment (Top View)

NOTE

1. USB_BOOT cannot be pulled up before startup.
2. Keep NC and RESERVED pins unconnected, all GND pins shall be connected to the ground.
3. The function of PSM is under development and it is not recommended to use it right now.
4. The module supports dual-SIM single stand by. For details, please contact Quectel Technical Support.

2.5. Pin Description

The following tables show the pin definition of the module.

Table 3: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 1 A
VBAT_RF	52, 53	PI	Power supply for the module's RF part		It must be provided with sufficient current up to 2.5 A
VDD_EXT	29	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. Add 2.2 µF bypass capacitor when in use.

					If unused, keep it open.
Power On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turn on/off the module	V_{IL}max = 0.5 V	VBAT power domain.
RESET_N	17	DI	Reset the module		VBAT power domain. If unused, keep it open.
Indication Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	20	DO	Indicate the module's operation status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open
NET_STATUS	21	DO	Indicate the module's network activity status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	8	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.5 V Vnom = 5.0 V	Typical: 5.0 V If unused, keep it open.
USB_DP	9	AIO	USB differential data (+)		USB 2.0 compliant. Require differential impedance of 90 Ω. If unused, keep it open.
USB_DM	10	AIO	USB differential data (-)		
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	43	PO	(U)SIM1 card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V	Either 1.8 V or 3.0 V (U)SIM card is supported and

				Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	can be identified automatically by the module.
USIM1_DATA	45	DIO	(U)SIM1 card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_CLK	46	DO	(U)SIM1 card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_RST	44	DO	(U)SIM1 card reset	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open
USIM1_GND	47	-	Ground	-	Specified ground for (U)SIM1 card
USIM2_VDD	87	PO	(U)SIM2 card power supply	Iomax = 50 mA **1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.

USIM2_DATA	86	DIO	(U)SIM2 card data	**1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_CLK	84	DO	(U)SIM2 card clock	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_RST	85	DO	(U)SIM2 card reset	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_DET	83	DI	(U)SIM2 card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_CTS	36	DO	DTE clear to send signal to DCE (connect to DTE's CTS)	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open. MAIN_DTR& MAIN_DCD& MAIN_RI will have a period of time when the module is powered on.
MAIN_RTS	37	DI	DTE request to send signal to DCE (connect to DTE's RTS)	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
MAIN_RXD	34	DI	Main UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	

MAIN_DCD	38	DO	Main UART data carrier detect	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
MAIN_TXD	35	DO	Main UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
MAIN_RI	39	DO	Main UART ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
MAIN_DTR	30	DI	Main UART data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
Auxiliary UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**comment**
AUX_TXD	27	DO	Auxiliary UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
AUX_RXD	28	DI	Auxiliary UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	22	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
DBG_TXD	23	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C _SCL	40	OD	I2C serial clock		External pull-up resistor is required. 1.8 V only. If unused, keep it open.
I2C _SDA	41	OD	I2C serial data		The I2 C interface supports simultaneous

					connection of multiple peripherals except for codec IC
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	5	DI	PCM data frame sync	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open. Support slave mode only.
PCM_CLK	4	DI	PCM clock	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
PCM_DIN	6	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
PCM_DOUT	**7**	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
RF Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	60	AIO	Main antenna interface		50 Ω impedance
ANT_BT/ WIFI_SCAN	56	AIO	The shared interface for Bluetooth and Wi-Fi Scan		50 Ω impedance. If unused, keep it open
GRFC Antenna Tuner Control Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	76	DO	Generic RF Controller		If unused, keep it open.
GRFC2	77	DO			
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CLK	26	DO	SPI clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	Master mode only.
SPI_CS	25	DO	SPI chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	

SPI_DIN	88	DI	SPI master mode input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
SPI_DOUT	64	DO	SPI master mode output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	24	AI	General-purpose ADC interface	Voltage range: 0.1 V to VBAT	If unused, keep it open.
ADC1	2	AI			
Analog Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC_N	119	AI	Microphone analog input (-)		
MICBIAS	120	PO	Bias voltage output for microphone	Vo = 2.2–3.0 V Vnom = 2.2 V	
SPK_P	121	AO	Analog audio differential output (+)		
SPK_N	122	AO	Analog audio differential output (-)		
MIC_P	126	AI	Microphone analog input (+)		
USB_BOOT					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	75	DI	Control pin for module to enter download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Active high. A circuit that enables the module to enter the download mode must be reserved.
PSM Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

PSM_IND	1	DO	Indicate the module's power saving mode		
PSM_EINT	96	DI	External interrupt pin; wake up the module from PSM		
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
W_DISABLE#	18	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Pulled up by default. When it is in low voltage level, the module can enter airplane mode. If unused, keep it open. When the pin is powered on, there will be a period of time when the level status is uncertain.
AP_READY	19	DI	Application processor ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open. When the PIN pin is powered on, there will be a period of time when the level status is uncertain.
GND					
Pin Name	**Pin No.**				
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67, 68, 69, 70, 71, 72, 73, 74, 79, 80, 81, 82, 89, 90, 91, 100, 101, 102				
RESERVED					
Pin Name	**Pin No.**				

NOTE	11, 12, 13, 14, 16, 49, 51, 57, 65, 66, 78, 92, 93, 94, 95, 97, 98, 99, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 123, 124, 125

1. The functions of PSM and GRFC are under development and it is not recommended to use them right now, please consult Quectel Technical Support for details.

5. PIN18(MAIN_W_DISABLE)&PIN19(AP_READY)&PIN30(MAIN_DTR) &PIN38(MAIN_DCD)&PIN39(MAIN_RI) When the module is powered on, there will be a period of time when the power level is indeterminate. First, high level 3V lasts for 2 seconds, then low power Ping lasts for 1.2 seconds, and then it is configured as 1.8V input/output. According to specific usage scenarios and circuit design, please evaluate whether the output stage that is indeterminate when the power is just turned on meets the customer's application design requirements.

2.6. EVB

In order to help customers develop applications with EG915U series moduel. Quectel provides an evaluation board (UMTS&LTE EVB), USB to RS-232 converter cable, earphone, antennas and other peripherals to control or test the module. For more details, please refer to ***document [1]***.

3 Operating Characteristics

EG915U series module have a total of 126 pins, The subsequent chapters will provide detailed descriptions of the following interfaces.

- Power supply
- (U)SIM interface
- USB interface
- UART interfaces
- SPI interface
- PCM and I2C interfaces
- Analog audio interfaces
- ADC interfaces
- PSM interface*
- Status indication
- USB_BOOT interface

3.1. Operating Modes

The following table briefly outlines the operating modes to be mentioned in the following chapters.

Table 5: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module is registered on the network and ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** command can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** command or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, current consumption of the module will be reduced to the minimal	

	level. In this mode, the module can still receive paging, SMS, voice call and TCP/UDP data from network normally.
Power Down Mode	In this mode, the VBAT power supply is constantly turned on and the software stops working.

3.2. Sleep Mode

The module is able to reduce its current consumption to an ultra-low value in the sleep mode. The following section describes power saving procedures of EG915U series module.

3.2.1 UART Application Scenario

If the host communicates with module via UART interface, the following preconditions should be met to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive MAIN_DTR to high level.

The following figure shows the connection between the module and the host.

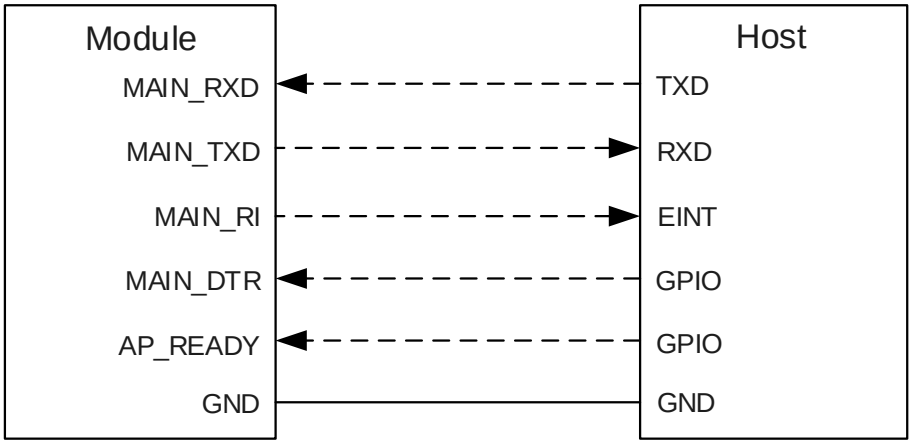


Figure 3: Sleep Mode Application via UART

- Driving MAIN_DTR low will wake up the module.
- When EG915U series has a URC to report, the URC will trigger the behavior of MAIN_RI pin. See ***Chapter 4.10.3*** for details about MAIN_RI behavior.

3.2.2. USB Application Scenario

If the host supports USB suspend/resume and remote wakeup functions, the following three preconditions can make the module enter the sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the MAIN_DTR is kept at high level or kept open.
- Ensure the host's USB Bus, which is connected with the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

3.2.2.1.USB Application with USB Remote Wakeup Function

The host supports USB Suspend/Resume and remote wakeup function.
The following figure illustrates the connection between the module and the host.

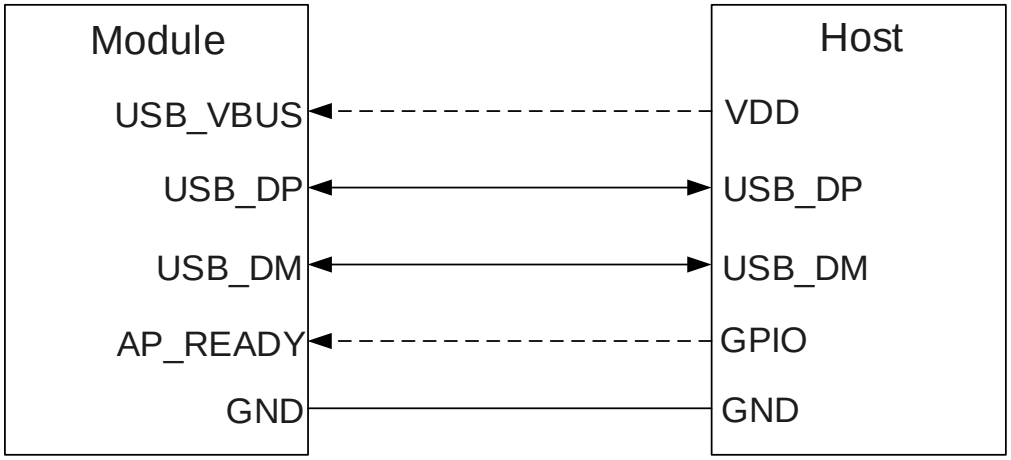


Figure 4: Sleep Mode Application with USB Remote Wakeup

- You can wake up the module by sending data to it through USB.
- When the module has a URC to report, the module will send remote wakeup signals via USB bus so as to wake up the host.

NOTE

1. Under Linux OS, USB support Suspend, under Windows OS nonsupport Suspend.
2. Pay attention to the level match shown in dotted line between the module and the host.

3.2.2.2.USB Application with USB Suspend/Resume and MAIN_RI Wakeup Function

If the host supports USB Suspend/Resume, but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host.
The following figure shows the connection between the module and the host.

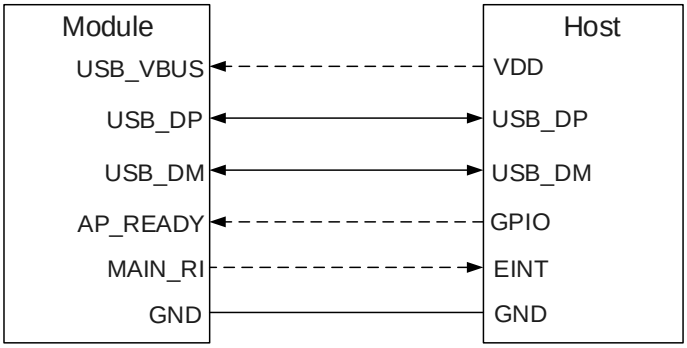


Figure 5: Sleep Mode Application with MAIN_RI

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the URC will trigger the behavior of MAIN_RI pin.

3.3. Airplane Mode

When the module enters into airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

3.3.1. Hardware

The W_DISABLE# pin is pulled up by default. Its control function for airplane mode is disabled by default and **AT+QCFG="airplanecontrol",1** can be used to enable the function. Driving it low will set the module enter airplane mode.

3.3.2. Software

AT+CFUN=<fun> provides choices of the functionality level through setting <fun> into 0, 1 or 4.

- **AT+CFUN=0**: Minimum functionality (disable RF function and (U)SIM function).
- **AT+CFUN=1**: Full functionality (default).
- **AT+CFUN=4**: Airplane mode (disable RF function).

3.4. Power Supply

3.4.1. Power Supply Pins

The module provides 4 VBAT pins for connection with an external power supply.

- Two VBAT_RF pins for RF part.
- Two VBAT_BB pins for BB part.

Table 6: Pin Definition of Power Supply

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	3.3	3.8	4.3	V
VBAT_RF	52, 53	PI	Power supply for the module's RF part	3.3	3.8	4.3	V
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67, 68, 69, 70, 71, 72, 73, 74, 79, 80, 81, 82, 89, 90,						

	91, 100, 101, 102

3.4.2. Reference Design for Power Supply

The power design for the module is very important, as the performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of 3.0 A at least. If the voltage drops between input and output is not too high, it is suggested that an LDO should be used to supply power to the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is recommended.

The following figure illustrates a reference design for +5 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

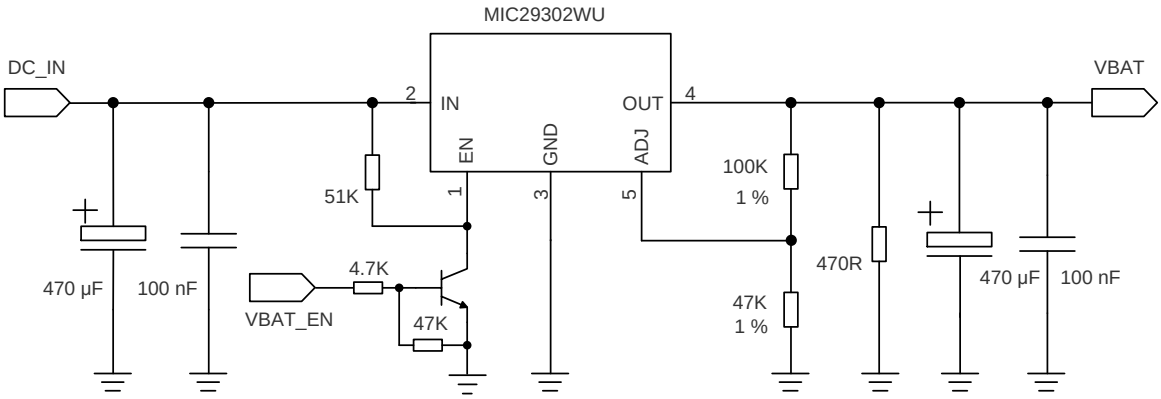


Figure 6: Reference Design of Power Supply

3.4.3. Requirements for Voltage Stability

The power supply range of the module is from 3.3 V to 4.3 V. Please make sure the input voltage will never drop below 3.3 V.

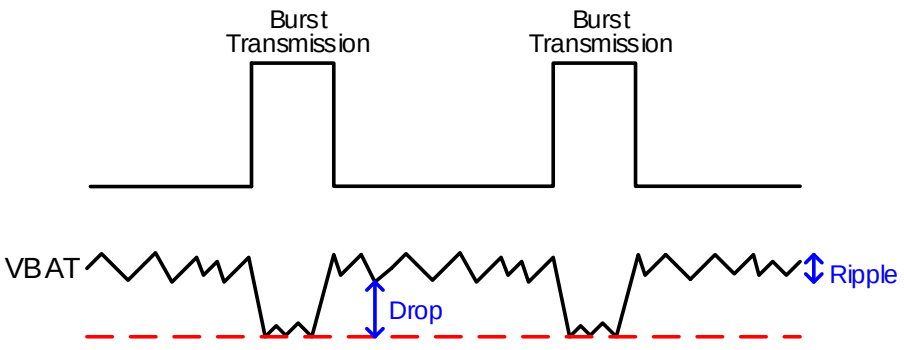


Figure 7: Power Supply Limits during Burst Transmission

To decrease the voltage drop, use bypass capacitors of about 100 µF with low ESR (ESR = 0.7 Ω) and reserve a multi-layer ceramic chip (MLCC) capacitor array due to their ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT_SENSE and VBAT_RF pins. When the external power supply is connected to the module, VBAT_SENSE and VBAT_RF need to be routed in star structure. The width of the VBAT_RF trace should not be less than 2.5 mm. When used as a power supply pin (that is, without charging function), the width of the VBAT_SENSE trace should not be less than 1 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, to avoid the surge, use a TVS diode of which reverse working voltage is 4.7 V and peak pulse power is up to 2550 W. The reference circuit is shown as below:

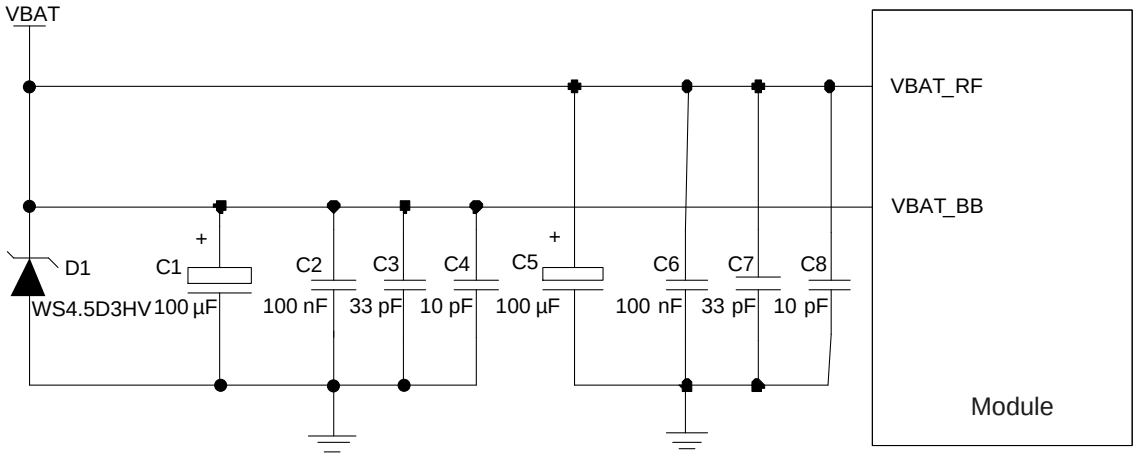


Figure 8: Power Supply

3.5. Turn on

3.5.1. Turn on with PWPKEY

Table 7: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turn on/off the module	VBAT power domain.

When the module is in power down mode, you can turn it on to normal mode by driving the PWRKEY pin low for at least 2 s. It is recommended to use an open drain/collector driver to control the PWRKEY. A

simple reference circuit is illustrated in the following figure.

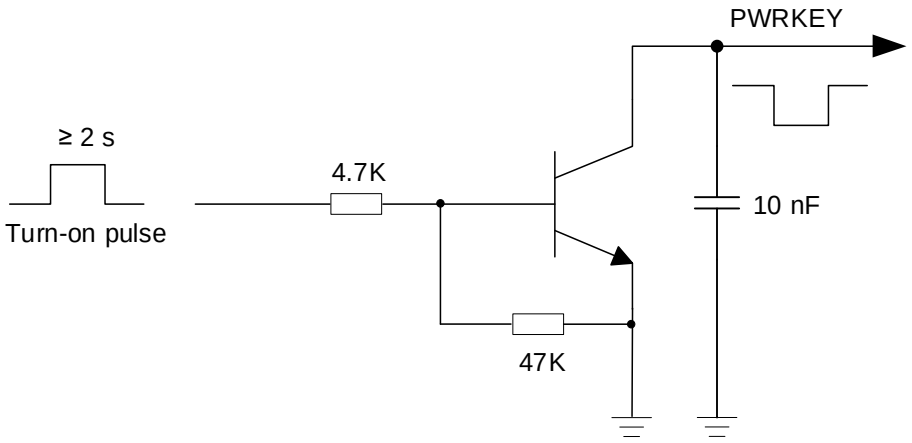


Figure 9: Turing on the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When you are pressing the key, electrostatic strike may be generated from finger. Therefore, you must place a TVS component nearby the button for ESD protection. A reference circuit is shown in the following figure.

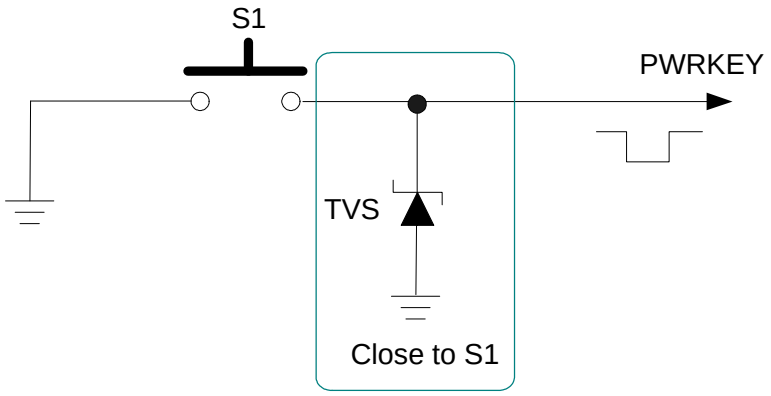


Figure 10: Turing on the Module Using Button

The power-up scenario is illustrated in the following figure.

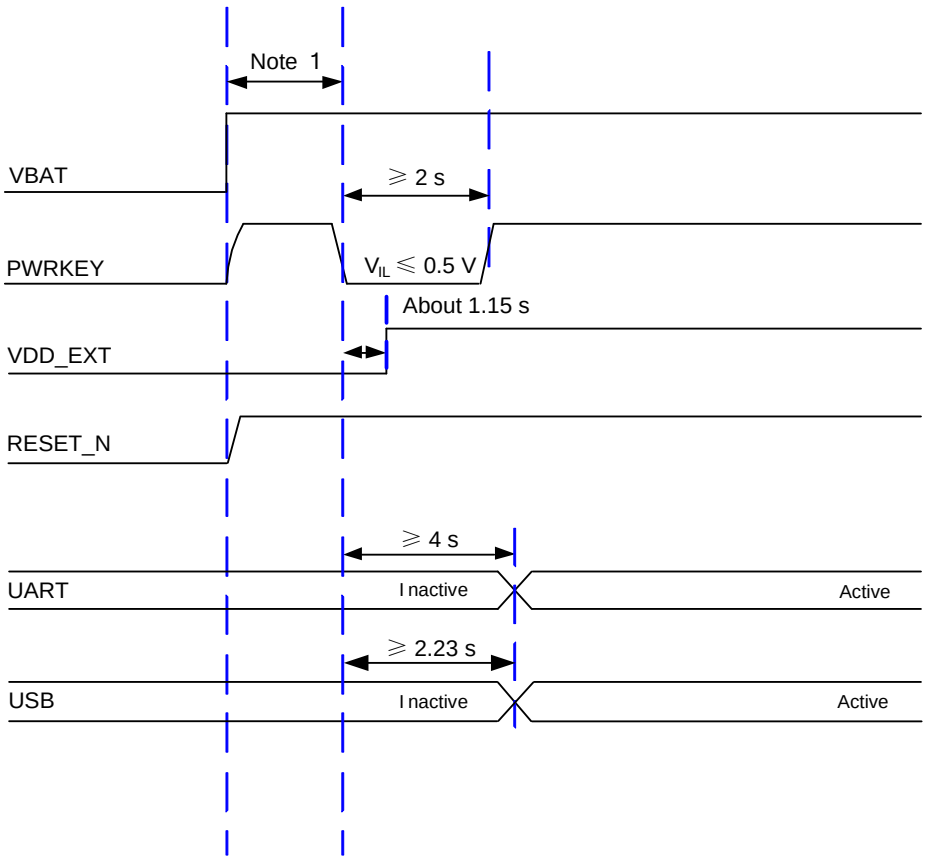


Figure 11: Power-up Timing

NOTE

1. Make sure that the VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 1 kΩ resistor if the module needs to be powered on automatically and shutdown is not needed.

3.6. Turn off

The following procedures can be used to turn off the module:

- Using the PWRKEY pin.
- Using **AT+QPOWD**.

3.6.1. Turn off with PWPKEY

Drive the PWRKEY pin low for at least 3 s and then release PWRKEY. After this, the module executes power-down procedure. The power-down scenario is illustrated in the following figure.

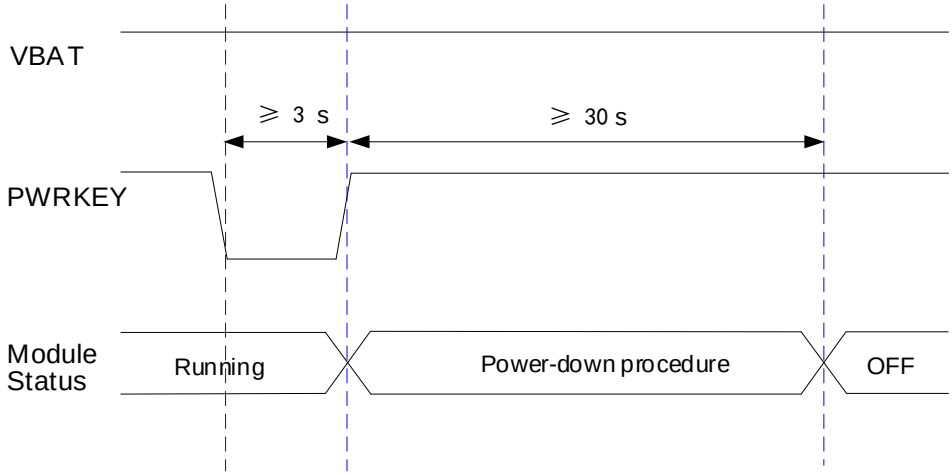


Figure 12: Timing of Turning off Module

3.6.2. Turn off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to turning off the module via the PWRKEY pin.

Please refer to ***document [2]*** for details about **AT+QPOWD** command.

NOTE

1. To avoid damaging internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut off the power supply.
2. When keeping the PWRKEY to the ground and the AT command cannot be used to turn off, the module can only be forced to turn off by cutting off the VBAT power supply. Therefore, we recommend that you can turn on or turn off the module by pulling up and pulling down the PWEKEY instead of keeping the PWRKEY to the ground.
3. The time for the module to log out of the network is related to the current network status, so the specific shutdown time is related to the network status, please pay attention to the shutdown time in the design.

3.7. Reset

The RESET_N pin can be used to reset the module. The module can be reset by pulling the RESET_N pin low for at least 100 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 8: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	17	DI	Reset the module	VBAT power domain. If unused, keep it open.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

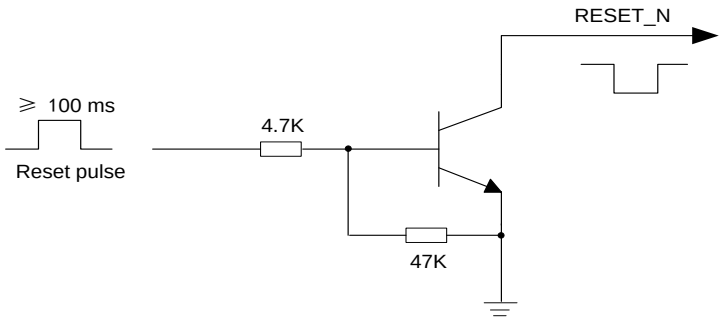


Figure 13: Reference Circuit of RESET_N by Using Driving Circuit

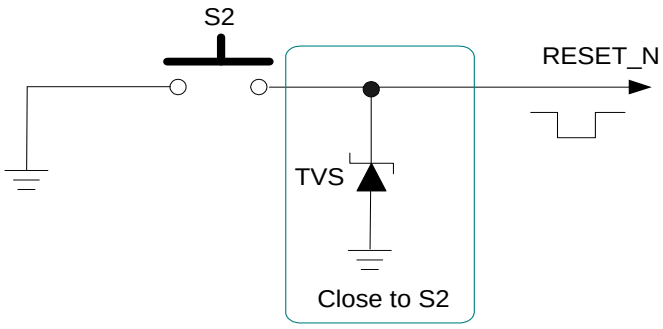


Figure 14: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the following figure.

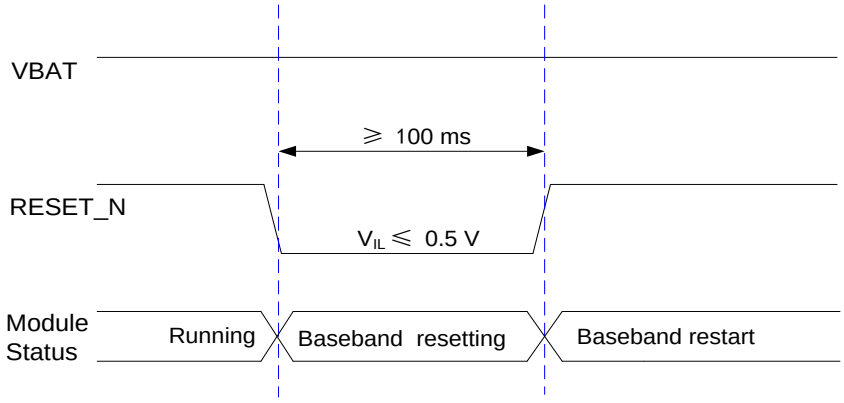


Figure 15: Timing of Resetting the Module

NOTE

1. Ensure that there is no large capacitance exceeding 10 nF on PWRKEY and RESET_N pins.
2. It is recommended to use RESET_N only when you fail to turn off the module with the **AT+QPOWD** or PWRKEY pin.

4 Application Interfaces

4.1. Analog Audio Interfaces

The module provides one analog audio input channel and one analog audio output channel. The pin definitions are shown in the following table.

Table 9: Pin Definition of Analog Audio Interfaces

Pin Name	Pin No.	I/O	Description
MIC_N	119	AI	Microphone analog input (-)
MICBIAS	120	PO	Bias voltage output for microphone
SPK_P	121	AO	Analog audio differential output (+)
SPK_N	122	AO	Analog audio differential output (-)
MIC_P	126	AI	Microphone analog input (+)

- AI channels are differential input channels, which can be applied for input of microphone (usually an electret microphone is used).
- AO channels are differential output channels, which can be applied for output receiver.
- The module's internal audio amplifier is configured as a class AB amplifier by default.

4.1.1. Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g., 10 pF and 33 pF) for filtering out RF interference, thus reducing TDD noise. The 33 pF capacitor is applied for filtering out RF interference when the module is transmitting at EGSM900. Without placing this capacitor, TDD noise could be heard. The 10 pF capacitor here is used for filtering out RF interference at DCS1800. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you would have to discuss with your capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The filter capacitors on the PCB board should be placed as close to the audio devices or audio interfaces

as possible, and the traces should be as short as possible. They should go through the filter capacitors before arriving at other connection points.

To reduce radio or other signal interference, RF antennas should be placed away from audio interfaces and audio traces. Power traces should not be parallel with and also should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

4.1.2. Microphone Interface Design

The microphone channel reference circuit is shown in the following figure.

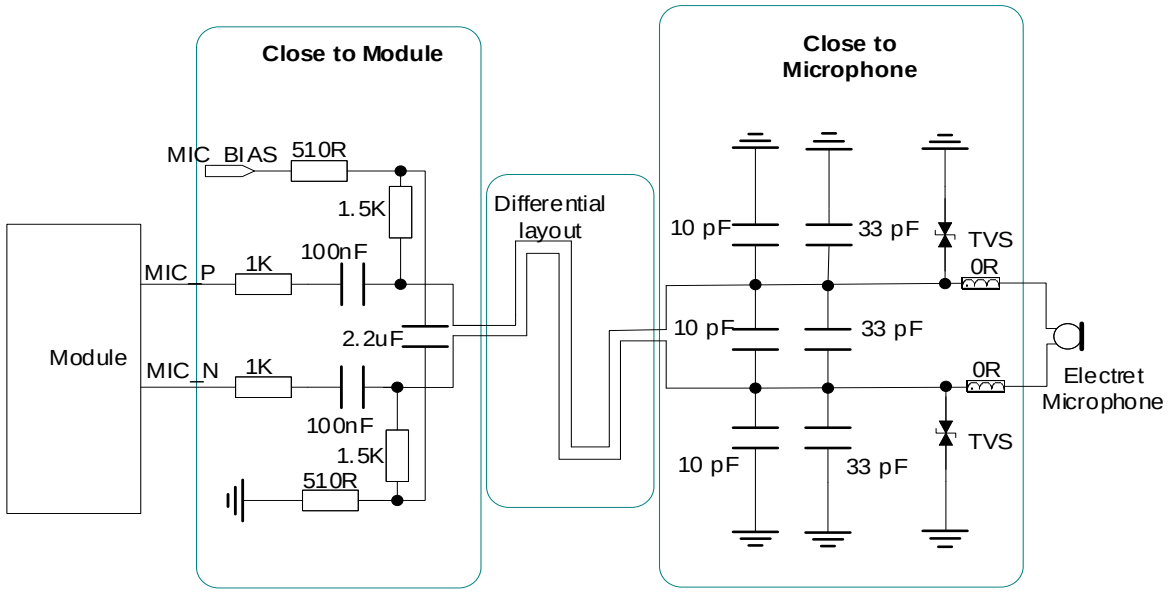


Figure 16: Reference Design for Microphone Interface

NOTE

MIC channel is sensitive to ESD, so it is not recommended to remove the ESD components used for protecting the MIC.

4.1.3. Receiver Interface Design

The receiver channel reference circuit is shown in the following figure:

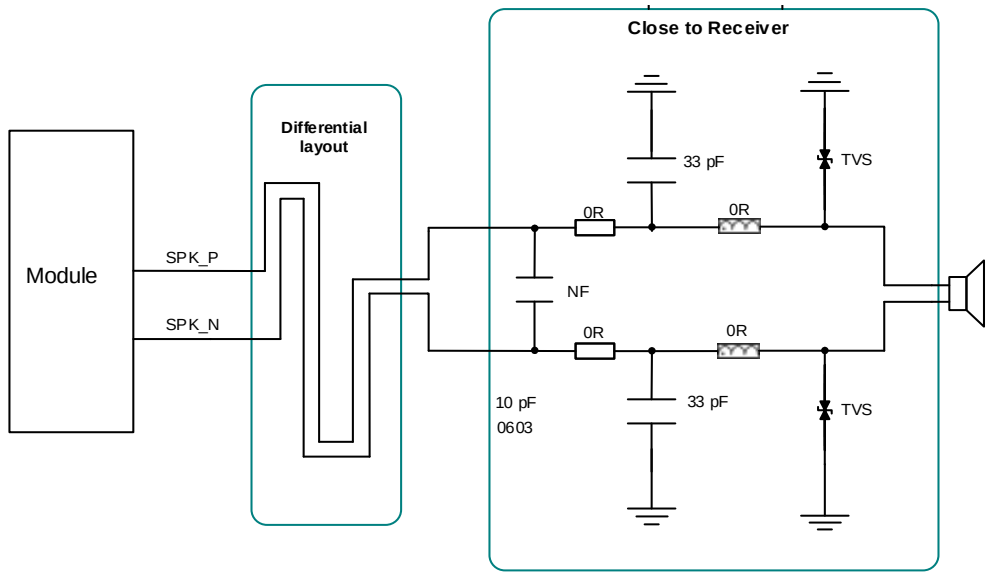


Figure 17: Reference Design for Receiver Interface

4.2. USB Interface

EG915U series module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports full-speed (12 Mbps) and high-speed (480 Mbps) modes. The USB interface can only serve as a slave device and is used for AT command communication, data transmission, software debugging and firmware upgrade.

Table 10: Functions of the USB Interface

Functions	
Data communication with external AP	Y
AT command communication	Y
Data transmission	Y
GNSS NMEA output	N
Software debugging	Y
Firmware upgrade	Y
Voice over USB	N

Table 11: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	Typical 5.0 V Minimum 3.5 V
USB_DP	9	AIO	USB differential data (+)	USB 2.0 compliant. Require differential impedance of 90 Ω. If unused, keep it open.
USB_DM	10	AIO	USB differential data (-)	

For more details about the USB 2.0 specifications, visit http://www.usb.org/home.

It is recommended to reserve test points for debugging and firmware upgrade in your design. The following figure shows a reference circuit of USB interface.

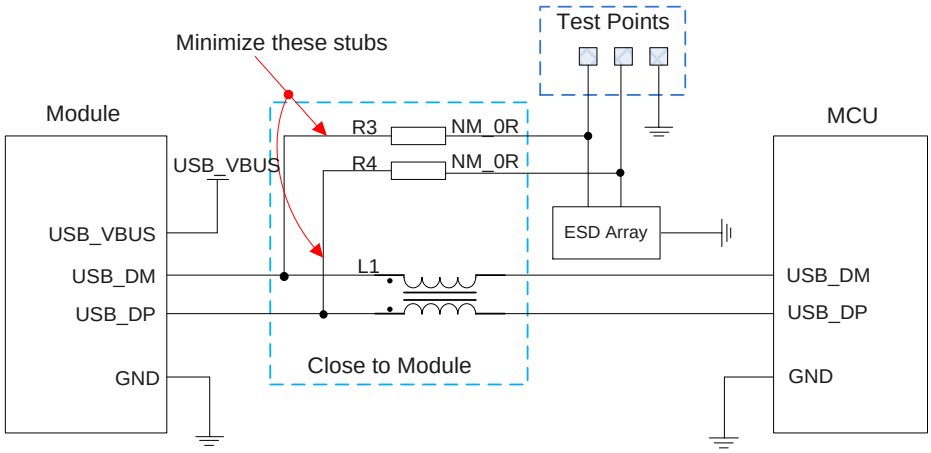


Figure 18: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. To ensure the signal integrity of USB data lines, L1, R3 and R4 must be placed close to the module, and resistors R3 and R4 should be placed close to each other. The extra stubs of trace must be as short as possible.

When designing the USB interface, you should follow the following principles to meet USB 2.0 specification.

- Route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. Route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that

layer and ground planes above and below.

- Pay attention to the selection of the ESD component on the USB data line. Its stray capacitance should not exceed 2 pF and should be placed as close as possible to the USB connector.

4.3. USB_BOOT Interface

The module provides a USB_BOOT pin. You can pull up USB_BOOT to VDD_EXT before power-up and the module will enter download mode when it is turned on. In this mode, the module supports firmware upgrade over USB interface.

Table 12: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Control pin for module to enter download mode	1.8 V power domain. Active high. A circuit that enables the module to enter the download mode must be reserved.

The following figure shows a reference circuit of USB_BOOT interface.

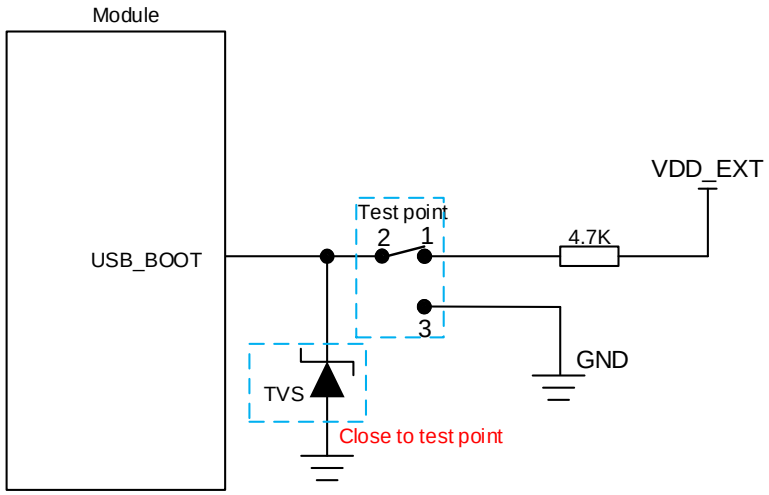


Figure 19: Reference Circuit of USB_BOOT Interface

4.4. (U)SIM Interface

The module provides 2 (U)SIM interfaces, dual SIM single stand by. The (U)SIM interfaces circuitry meets ETSI requirement. Both 1.8 V and 3.0 V (U)SIM cards are supported.

Table 15: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	43	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_DATA	45	DIO	(U)SIM1 card data	
USIM1_CLK	46	DO	(U)SIM1 card clock	
USIM1_RST	44	DO	(U)SIM1 card reset	
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep this pin open
USIM1_GND	47			Specified ground for (U)SIM1 card
USIM2_VDD	87	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM2_DATA	86	IO	(U)SIM2 card data	
USIM2_CLK	84	DO	(U)SIM2 card clock	
USIM2_RST	85	DO	(U)SIM2 card reset	
USIM2_DET	83	DI	(U)SIM2 card hot-plug detect	1.8 V power domain. If unused, keep it open

EG915U series module supports (U)SIM card hot-plug via the USIM_DET pin and both high and low level detections are supported. By default, the function is disabled, please see **AT+QSIMDET** in ***document [2]*** for more details.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

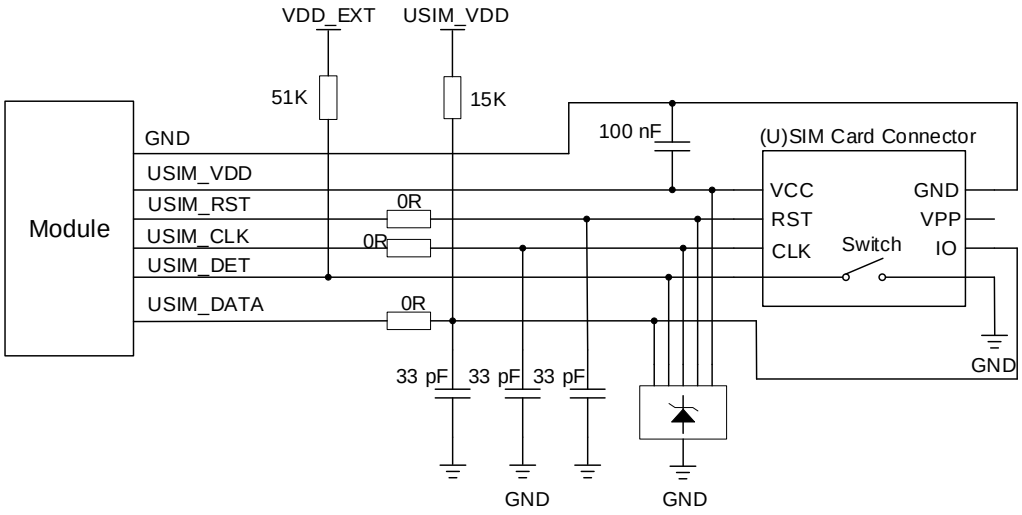


Figure 20: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

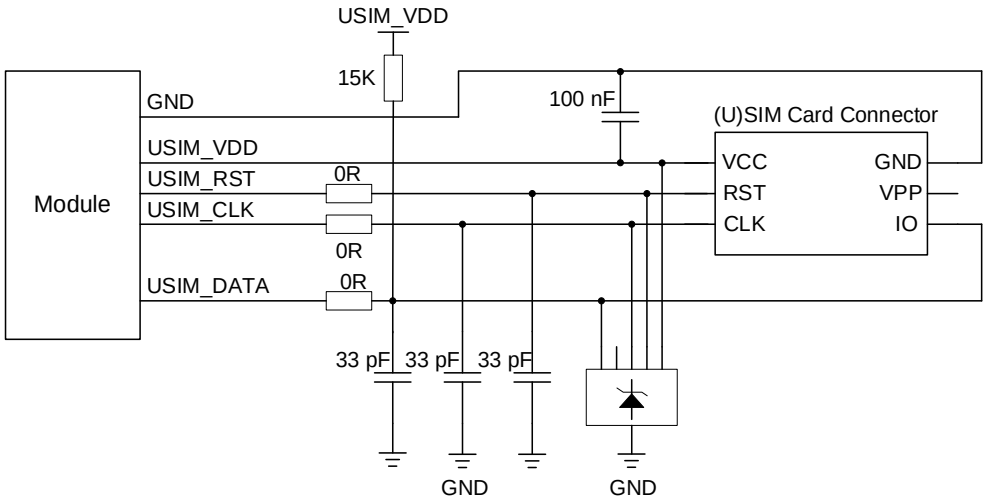


Figure 21: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in (U)SIM circuit design:

- Place (U)SIM card connector as close to the module as possible. Keep the trace length less than 200 mm as far as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Ensure the USIM_VDD has a bypass capacitor less than 1 μF, and the capacitor should be close to the (U)SIM card connector.

- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer good ESD protection, it is recommended to add a TVS diode array of which the parasitic capacitance should be less than 15 pF. Add 0 Ω resistors in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors are used for filtering interference of EGSM900. Additionally, keep the (U)SIM peripheral circuit close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

4.5. I2C and PCM Interfaces

The module provides one I2C interface and one pulse code modulation (PCM) interface. The PCM interface of the module only supports slave mode; therefore, the clock signal of the codec IC needs to be provided externally.

Table 13: Pin Definition of I2C and PCM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C _SCL	40	OD	I2C serial clock	External pull-up resistor is required. 1.8 V only. If unused, keep it open. If the I2C interface is used to connect to external codec, it cannot connect to other external devices.
I2C _SDA	41	OD	I2C serial data	
PCM_DIN	6	DI	PCM data input	1.8 V power domain. If unused, keep it open. Support slave mode only.
PCM_DOUT	7	DO	PCM data output	
PCM_SYNC	5	DI	PCM data frame sync	
PCM_CLK	4	DI	PCM clock	

The following figure shows a reference design of PCM interface with external codec IC.

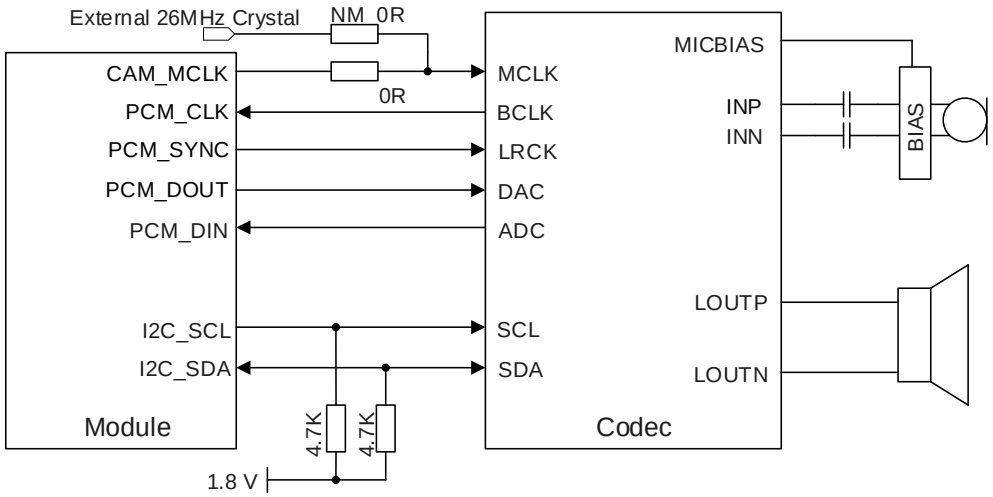


Figure 22: Reference Circuit of I2 C and PCM Application with Audio Codec

NOTE

1. It is recommended to reserve an RC (R = 22 Ω, C = 22 pF) circuit on the PCM traces, especially for PCM_CLK.
2. The I2 C interface supports simultaneous connection of multiple peripherals except for codec IC. In other words, if a codec IC has been mounted on the I2 C bus, no other peripherals can be mounted; if there is no codec IC on the bus, multiple peripherals can be mounted.

4.6. UART Interfaces

The module provides three UART interfaces: the main UART interface and the debug UART interface and auxiliary UART. Their features are described as follows.

- Main UART interface supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps and 921600 bps baud rates, and the default is 115200 bps. This interface is used for data transmission and AT command communication.
- Debug UART interface supports 921600 bps baud rate. It is used for the output of partial logs.
- Auxiliary UART.

Table 14: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	36	DO	DTE clear to send signal to DCE (connect to DTE's CTS)	1.8 V power domain. If unused, keep it

MAIN_RTS	37	DI	DTE request to send signal to DCE (connect to DTE's RTS)	open.
MAIN_RXD	34	DI	Main UART receive	
MAIN_DCD	38	DO	Main UART data carrier detect	
MAIN_TXD	35	DO	Main UART transmit	
MAIN_RI	39	DO	Main UART ring indication	
MAIN_DTR	30	DI	Main UART data terminal ready	

Table 15: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	22	DI	Debug UART receive	1.8 V power domain. If unused, keep it open.
DBG_TXD	23	DO	Debug UART transmit	

Table 16: Auxiliary UART

Pin Name	Pin No.	I/O	Description	Comment
AUX_TXD	27	DO	Auxiliary UART transmit	1.8 V power domain. If unused, keep it open.
AUX_RXD	28	DI	Auxiliary UART receive	

The module provides 1.8 V UART interfaces. Use a level shifter if the application is equipped with a 3.3 V UART interface. A level shifter TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

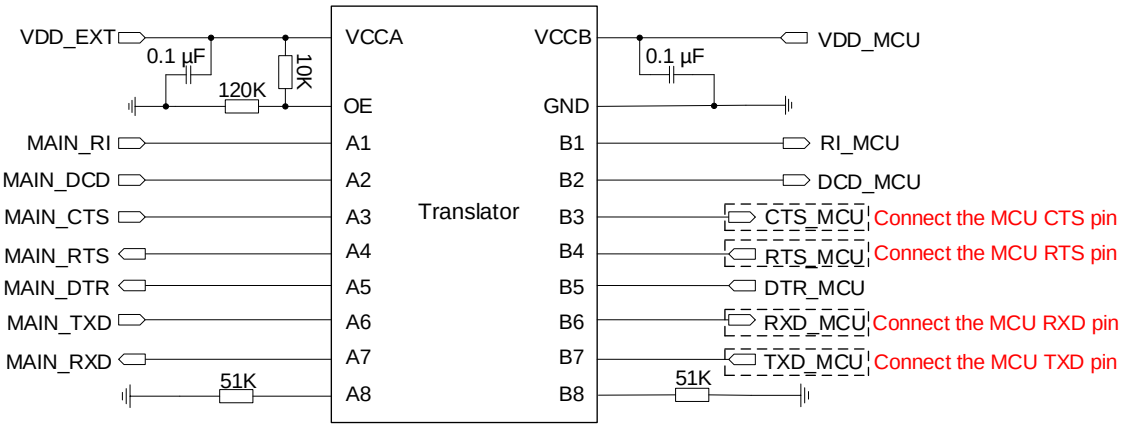


Figure 23: Reference Circuit with Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as follows. For the design of circuits in dotted lines, please refer to that of the circuits in solid lines, but please pay attention to the direction of connection.

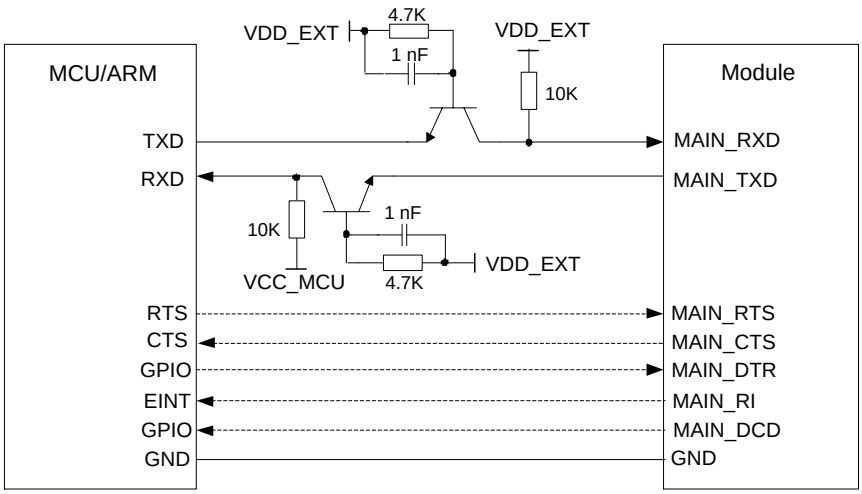


Figure 24: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS.

4.7. ADC Interface

The module provides two analog-to-digital converter (ADC) interfaces. You can use **AT+QADC=0** to read the voltage value on ADC0 pin, **AT+QADC=1** to read the voltage value on ADC1, See ***document [2]*** for more details.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 17: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	General-purpose ADC interface	A 1 kΩ series resistor is required for use. If unused, keep it open.
ADC1	2	AI		

Table 21: Characteristics of ADC Interface

Name	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0.1	-	VBAT	V
ADC1 Voltage Range	0.1	-	VBAT	V
ADC Resolution	-	12	-	bits

NOTE

1. The input voltage of ADC should not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC pin when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.
4. If input voltage of ADC interface is designed with a resistor divider circuit, the resistance value of the external divider resistor must be less than 100 kΩ, otherwise the measurement accuracy of the ADC will be reduced significantly.

4.8. SPI Interface

The module provides one SPI interface that only supports master mode. It has a working voltage of 1.8 V and a maximum clock frequency of 25 MHz.

Table 22: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	26	DO	SPI clock	Just master mode only. 1.8 V power domain. If unused, keep it open.
SPI_CS	25	DO	SPI chip select	
SPI_DIN	88	DI	SPI master mode input	
SPI_DOUT	64	DO	SPI master mode output	

NOTE

When the universal 4-wire SPI interface is connected to NOR Flash, it supports basic Flash reading, writing, erasing and other operations, but you need to perform wear leveling. It does not support file system and can only be used for storage purpose.

4.9. PSM Interface*

The module supports power saving mode (PSM). It enters the PSM mode through the following AT commands when working normally.

- **AT+CFUN=4:** Enter airplane mode.
- **AT+QSCLK=3:** Enable PSM.
- **AT+CFUN=1:** Exit airplane mode.

Pulling the PSM_EINT pin up externally or setting the timer in software will enable the module to exit PSM.

Table 18: Pin Definition of PSM Interface

Pin Name	Pin No.	I/O	Description	Comment
PSM_IND	1	DO	Indicate the module's power saving mode	VRTC power domain
PSM_EINT	96	DI	External interrupt pin; Wake up the module from PSM.	VRTC power domain

A reference circuit is shown in the following figure.

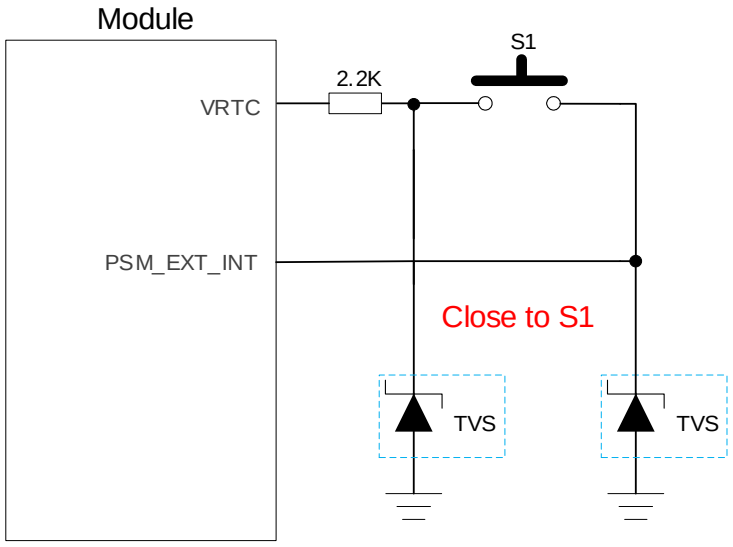


Figure 25: Reference Circuit of Wake up Module from PSM

4.10. Indication Signal

Table 19: Pin Definition of Indication Signal

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module's operation status	1.8 V power domain. If unused, keep it open.
AP_READY	19	DI	Application processor ready	
NET_STATUS	21	DO	Indicate the module's network activity status	

4.10.1. Network Status Indication

The network indication pins NET_STATUS can drive the network status indicators. The following tables describe pin definition and logic level changes in different network status.

Table 20: Working State of Network Connection Status/Activity Indication

Pin Name	Status	Network Status
NET_STATUS	Flicker slowly (200 ms high/1800 ms low)	Network searching
	Flicker quickly (234 ms high/266 ms low)	Idle
	Flicker rapidly (63 ms low /62 ms high)	Data transfer is ongoing
	Always high	Voice calling

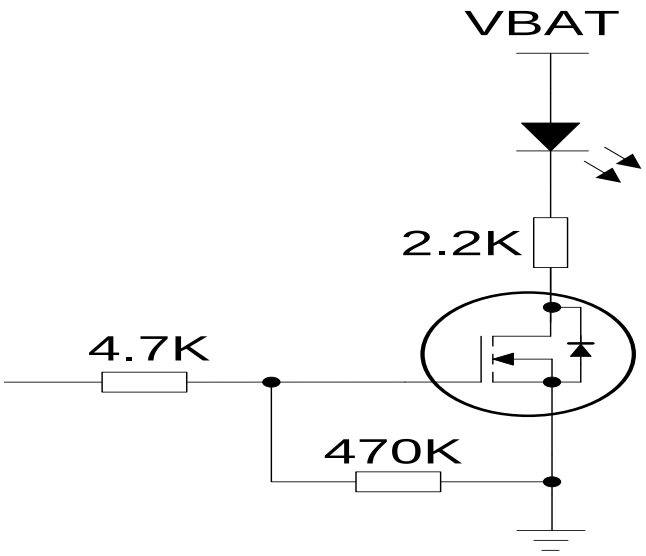


Figure 26: Reference Circuit of Network Status Indication

4.10.2. STATUS

The STATUS pin is an open drain output for indicating the module's operation status. It will output high level when module is powered ON successfully.

Table 21: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment

A reference circuit is shown as below.

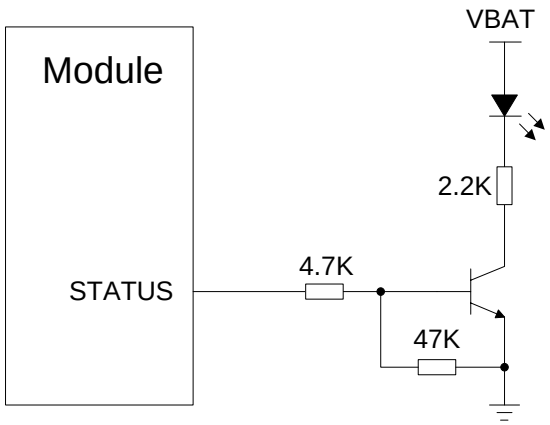


Figure 27: Reference Circuits of STATUS

NOTE

4.10.3. MAIN_RI

AT+QCFG= "risignaltype", "physical" command can be used to configure MAIN_RI behavior. No matter on which port a URC is presented, the URC will trigger the behavior of MAIN_RI.

NOTE

The URC can be outputted via UART port, USB AT port and USB modem port, which can be set by **AT+QURCCFG** command. The default port is USB AT port.

In addition, MAIN_RI behavior can be configured flexibly. The default behavior of the MAIN_RI is shown as below.

Table 22: Behaviors of the MAIN_RI

State	Response
Idle	MAIN_RI keeps at high level.
URC	MAIN_RI outputs 120 ms low pulse when a new URC return.

The MAIN_RI behavior can be changed via **AT+QCFG="urc/ri/ring"*** . Please refer to ***document [2]*** for details.

4.11. Control Signal

Table 23: Pin Definition of Control Signal

Pin Name	Pin No.	I/O	Description	Comment
W_DISABLE#	18	DI	Airplane mode control	1.8 V power domain. Pulled up by default. When it is in low voltage level, the module can enter airplane mode. If unused, keep this pin open.

The module provides a W_DISABLE# pin to enable or disable airplane mode through hardware operation. W_DISABLE# is pulled up by default, and driving it low will set the module to airplane mode. Its control function for airplane mode is disabled by default and **AT+QCFG= "airplanecontrol", 1** can be used to enable the function.

AT+CFUN=<fun> command provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4.

- AT+CFUN=0: Minimum functionality mode (RF functions are disabled).
- AT+CFUN=1: Full functionality mode (by default).
- AT+CFUN=4: RF function is disabled (Airplane mode).

5 Antenna Interfaces

EG915U series module provides a main antenna interface, a Bluetooth/Wi-Fi Scan antenna interface. The impedance of antenna ports is 50 Ω.

5.1. Main Antenna Interface

5.1.1. Pin Definition

Table 24: Pin Definition of RF Antennas

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance.
ANT_BT/WIFI_SCAN	56	AIO	The shared interface for Bluetooth and Wi-Fi Scan	Bluetooth and Wi-Fi Scan cannot be used simultaneously; Wi-Fi Scan can only receive but not transmit. 50 Ω impedance. If unused, keep it open.

NOTE

Only passive antennas are supported.

5.1.2. Operating Frequency

Table 25: Operating Frequency of EG915U-CN

Operating Frequency	Transmit (MHz)	Receive (MHz)

EGSM900	880-915	925-960
DCS1800	1710-1785	1805-1880
LTE-B1	1920-1980	2110-2170
LTE-B3	1710-1785	1805-1880
LTE-B5	824-849	869-894
LTE-B8	880-915	925-960
LTE-B34	2010-2025	2010-2025
LTE-B38	2570-2620	2570-2620
LTE-B39	1880-1920	1880-1920
LTE-B40	2300-2400	2300-2400
LTE-B41	2535-2675	2535-2675

Table 26: Operating Frequency of EG915U-EU

Operating Frequency	Transmit (MHz)	Receive (MHz)
GSM850	824-849	869-894
PCS1900	1850-1910	1930-1990
EGSM900	880-915	925-960
DCS1800	1710-1785	1805-1880
LTE-B1	1920-1980	2110-2170
LTE-B3	1710-1785	1805-1880
LTE-B5	824-849	869-894
LTE-B7	2500-2570	2620-2690
LTE-B8	880-915	925-960
LTE-B20	832-862	791-821
LTE-B28	703-748	758-803

Table 27: Operating Frequency of EG915U-LA

Operating Frequency	Transmit (MHz)	Receive (MHz)
GSM850	824-849	869-894
PCS1900	1850-1910	1930-1990
EGSM900	880-915	925-960
DCS1800	1710-1785	1805-1880
LTE-B2	1850-1910	1930-1990
LTE-B3	1710-1785	1805-1880
LTE-B4	1710-1755	2110-2155
LTE-B5	824-849	869-894
LTE-B7	2500-2570	2620-2690
LTE-B8	880-915	925-960
LTE-B28	703-748	758-803
LTE-B66	1710-1780	2110-2200

NOTE

Only EG915U-CN supports LTE-TDD.

5.1.3. Reference Design of Antenna Interface

A reference design of ANT_MAIN pin and ANT_BT/WIFI_SACN pin are shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

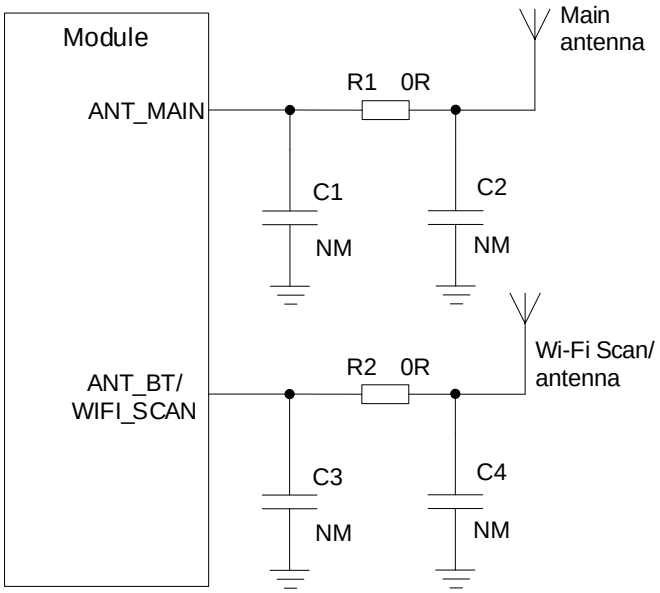


Figure 28: Reference Circuit of RF Antenna

5.1.4. Operating Frequency

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between the RF traces and the ground (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

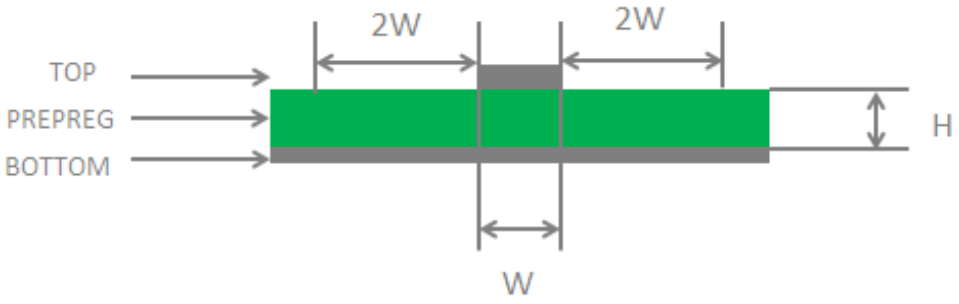


Figure 29: Microstrip Design on a 2-layer PCB

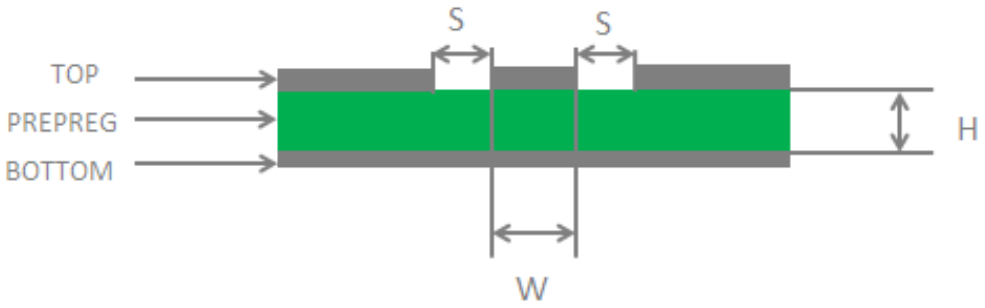


Figure 30: Coplanar Waveguide Design on a 2-layer PCB

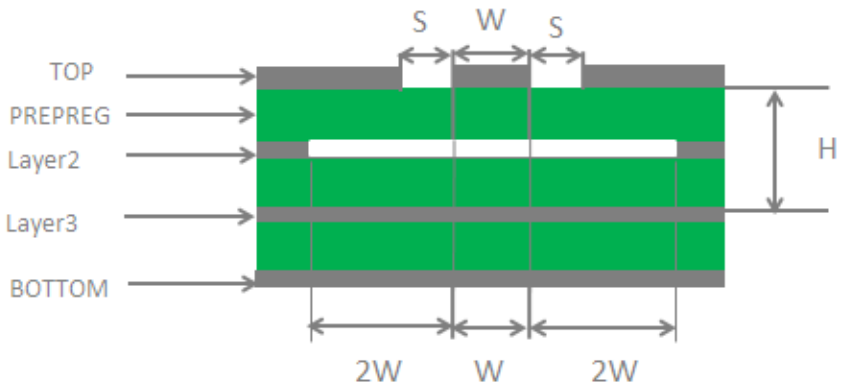


Figure 31: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

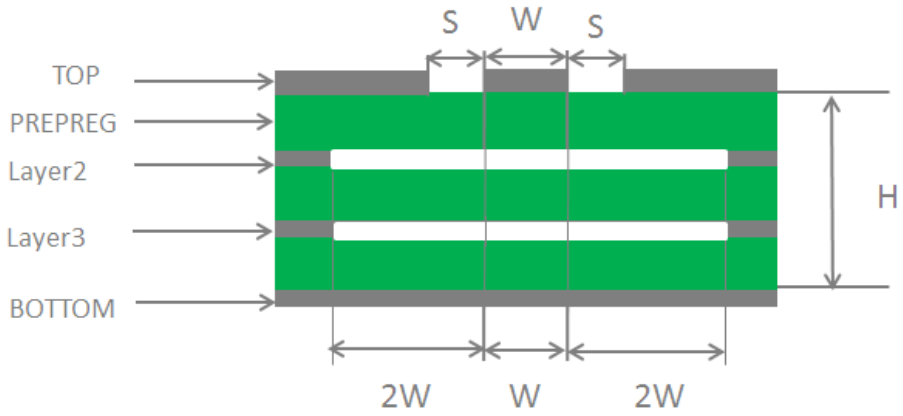


Figure 32: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [3]***.

5.2. Antenna Installation

5.2.1. Antenna Design Requirement

Table 28: Requirements for Antenna Design

Type	Requirements
GSM/LTE	VSWR: ≤ 2 Efficiency: > 30 % Max input power: 50 W Input impedance: 50 Ω Cable insertion loss: < **1 dB**：LB（< 1 GHz） < **1.5 dB**：MB（1–2.3 GHz） < **2 dB**：HB（> 2.3 GHz）

5.2.2. RF Connector Recommendtion

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by *Hirose*.

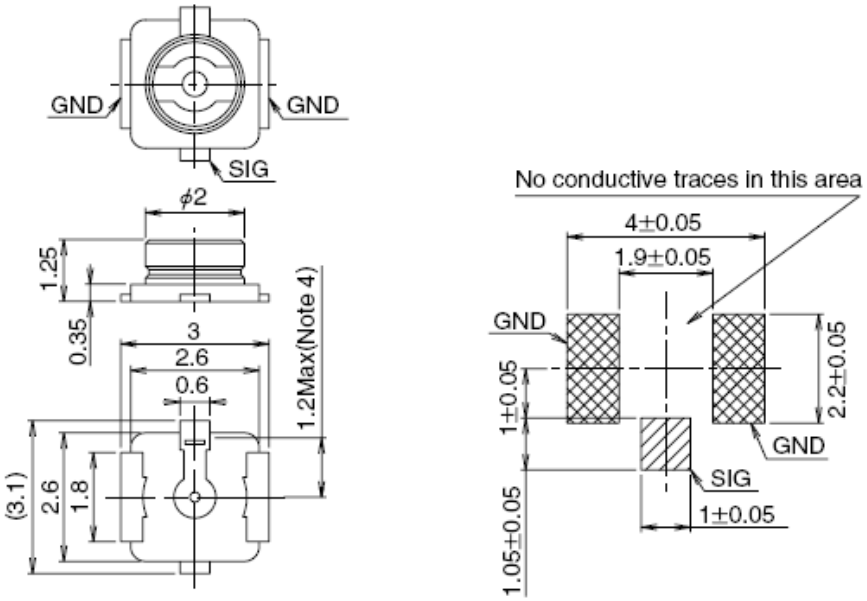


Figure 33: Dimensions of U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

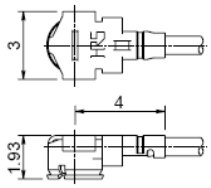
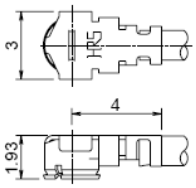
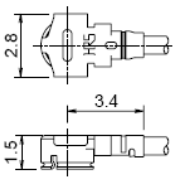
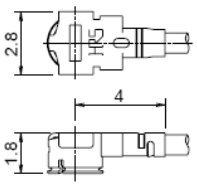
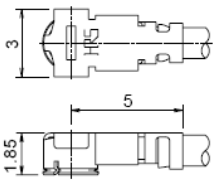
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 34: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

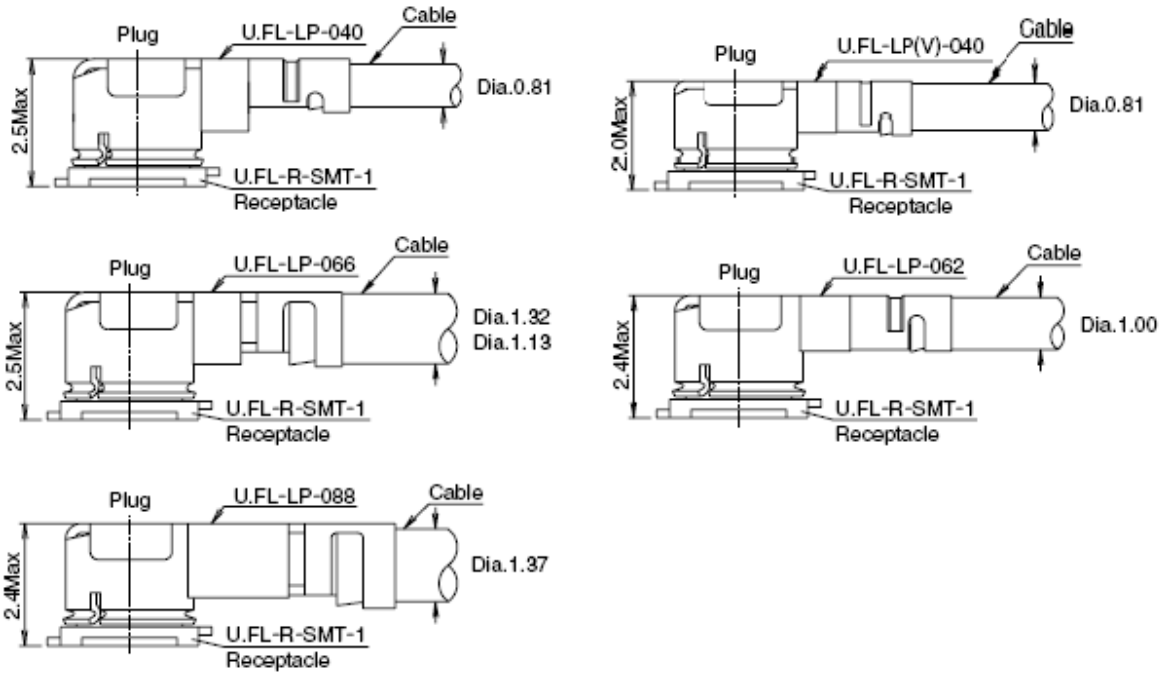


Figure 35: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://hirose.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 32: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	1.0	A
Peak Current of VBAT_RF	0	2.5	A
Voltage on Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT	V
Voltage at ADC1	0	VBAT	V

6.2. Power Supply Ratings

Table 29: The Module's Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during transmitting burst	Maximum power control level at EGSM 900	-	-	400	mV

	Voltage drop during peak data rate	-	-	-	-	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level at EGSM 900	-	1.7	2.5	A
USB_VBUS	USB connection detection	-	3.5	5.0	5.25	V

6.3. Operation and Storage Temperatures

Table 30: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [6]	-35	+25	+75	ºC
Extended Operation Range [7]	-40	+25	+85	ºC
Storage Temperature Range	-40	+25	+90	ºC

6.4. Power Consumption

Table 31: EG915U-CN Current Consumption

EG915U-CN			
Description	**Conditions**	**Typ.**	**Unit**
OFF state	Power down	32	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.0	mA
	AT+CFUN=0 (USB connected)	2.2	mA
	AT+CFUN=4 (USB disconnected)	1.0	mA

[6] Within operating temperature range, the module is 3GPP compliant.
[7] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

	AT+CFUN=4 (USB connected)	2.3	mA
	EGSM @ DRX = 2 (USB disconnected)	2.0	mA
	EGSM @ DRX = 5 (USB disconnected)	1.5	mA
	EGSM @ DRX = 5 (USB connected)	2.7	mA
	EGSM @ DRX = 9 (USB disconnected)	1.3	mA
	DCS @ DRX = 2 (USB disconnected)	2.0	mA
	DCS @ DRX = 5 (USB disconnected)	1.5	mA
	DCS @ DRX = 5 (USB connected)	2.7	mA
	DCS @ DRX = 9 (USB disconnected)	1.3	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.5	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.8	mA
	LTE-FDD @ PF = 64 (USB connected)	3.0	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.4	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.2	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.5	mA
	LTE-TDD @ PF = 64 (USB disconnected)	1.8	mA
	LTE-TDD @ PF = 64 (USB connected)	3.1	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.4	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.2	mA
Idle state	EGSM @ DRX = 5 (USB disconnected)	12.2	mA
	EGSM @ DRX = 5 (USB connected)	28.5	mA
	LTE-FDD @ PF = 64 (USB disconnected)	12.5	mA
	LTE-FDD @ PF = 64 (USB connected)	29.0	mA
	LTE-TDD @ PF = 64 (USB disconnected)	12.5	mA
	LTE-TDD @ PF = 64 (USB connected)	29.0	mA
LTE data transfer	LTE-FDD B1 @ 22.93 dBm	571	mA

	LTE-FDD B3 @ 22.86 dBm	583	mA
	LTE-FDD B5 @ 23.51 dBm	527	mA
	LTE-FDD B8 @ 22.79 dBm	568	mA
	LTE-FDD B34 @ 23.32 dBm	268	mA
	LTE-FDD B38 @ 23.29 dBm	300	mA
	LTE-FDD B39 @ 23.15 dBm	241	mA
	LTE-FDD B40 @ 22.97 dBm	284	mA
	LTE-FDD B41 @ 23.06 dBm	296	mA
GPRS data transfer	GSM900 4DL/1UL @ 32.86 dBm	226	mA
	GSM900 3DL/2UL @ 30.86 dBm	343	mA
	GSM900 2DL/3UL @ 28.81 dBm	392	mA
	GSM900 1DL/4UL @ 26.63 dBm	405	mA
	DCS1800 4DL/1UL @ 30.13 dBm	160	mA
	DCS1800 3DL/2UL @ 28.12 dBm	221	mA
	DCS1800 2DL/3UL @ 26.01 dBm	249	mA
	DCS1800 1DL/4UL @ 23.94 dBm	258	mA
GSM voice call	GSM900 PCL=5 @ 32.83 dBm	245	mA
	GSM900 PCL=12 @ 18.94 dBm	90	mA
	GSM900 PCL=19 @ 6.18 dBm	63	mA
	DCS1800P CL=0 @ 30.12 dBm	176	mA
	DCS1800P CL=7 @ 15.97 dBm	75	mA
	DCS1800P CL=15 @ 0.28 dBm	57	mA
GSM voice call (Max. Current)	GSM900 PCL=5 @ 32.83 dBm	1.77	A
	GSM900 PCL=12 @ 18.94 dBm	0.44	A
	GSM900 PCL=19 @ 6.18 dBm	0.18	A
	DCS1800P CL=0 @ 30.12 dBm	1.18	A

	DCS1800P CL=7 @ 15.97 dBm	0.3	A
	DCS1800P CL=15 @ 0.28 dBm	0.15	A

Table 32: EG915U-EU Current Consumption

EG915U-EU			
Description	**Conditions**	**Typ.**	**Unit**
OFF state	Power down	43	μA
	AT+CFUN=0 (USB disconnected)	1.01	mA
	AT+CFUN=0 (USB connected)	2.2	mA
	AT+CFUN=4 (USB disconnected)	1.02	mA
	AT+CFUN=4 (USB connected)	2.21	mA
	EGSM @ DRX = 2 (USB disconnected)	2.09	mA
	EGSM @ DRX = 5 (USB disconnected)	1.55	mA
	EGSM @ DRX = 5 (USB connected)	2.67	mA
	EGSM @ DRX = 9 (USB disconnected)	1.39	mA
Sleep state	DCS @ DRX = 2 (USB disconnected)	2.1	mA
	DCS @ DRX = 5 (USB disconnected)	1.5	mA
	DCS @ DRX = 5 (USB connected)	2.78	mA
	DCS @ DRX = 9 (USB disconnected)	1.36	mA
	LTE-FDD @ PF = 32 (USB disconnected)	3.49	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.22	mA
	LTE-FDD @ PF = 64 (USB connected)	3.48	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.63	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.34	mA
Idle state	EGSM @ DRX = 5 (USB disconnected)	12.05	mA

	EGSM @ DRX = 5 (USB connected)	27.3	mA
	LTE-FDD @ PF = 64 (USB disconnected)	12.38	mA
	LTE-FDD @ PF = 64 (USB connected)	27.58	mA
LTE data transfer	LTE-FDD B1 @ 22.29 dBm	638	mA
	LTE-FDD B3 @ 22.88 dBm	617	mA
	LTE-FDD B5 @ 23.01 dBm	637	mA
	LTE-FDD B7 @ 22.95 dBm	793	mA
	LTE-FDD B8 @ 23.17 dBm	696	mA
	LTE-FDD B20 @ 23.05 dBm	516	mA
	LTE-FDD B28 @ 23.06 dBm	559	mA
GPRS data transfer	GSM850 4DL/1UL @ 32.96 dBm	266	mA
	GSM850 3DL/2UL @ 30.7 dBm	394	mA
	GSM850 2DL/3UL @ 28.66 dBm	457	mA
	GSM850 1DL/4UL @ 26.41 dBm	464	mA
	GSM900 4DL/1UL @ 32.31 dBm	245	mA
	GSM900 3DL/2UL @ 30.7 dBm	371	mA
	GSM900 2DL/3UL @ 28.66 dBm	445	mA
	GSM900 1DL/4UL @ 26.63 dBm	452	mA
	DCS1800 4DL/1UL @ 29.84 dBm	171	mA
	DCS1800 3DL/2UL @ 27.89 dBm	242	mA
	DCS1800 2DL/3UL @ 25.85 dBm	269	mA
	DCS1800 1DL/4UL @ 23.78 dBm	279	mA
	PCS1900 4DL/1UL @ 29.68 dBm	171	mA
	PCS1900 3DL/2UL @ 27.74 dBm	247	mA
	PCS1900 2DL/3UL @ 25.66 dBm	279	mA

	PCS1900 1DL/4UL @ 23.59 dBm	295	mA
GSM voice call	GSM850 PCL=5 @ 32.82 dBm	289	mA
	GSM850 PCL=12 @ 19.08 dBm	111	mA
	GSM850 PCL=19 @ 6.12 dBm	80	mA
	GSM900 PCL=5 @ 32.34 dBm	261	mA
	GSM900 PCL=12 @ 19.06 dBm	109	mA
	GSM900 PCL=19 @ 5.39 dBm	79	mA
	DCS1800P CL=0 @ 29.89 dBm	196	mA
	DCS1800P CL=7 @ 15.96 dBm	91	mA
	DCS1800P CL=15 @ 0.95 dBm	75	mA
	PCS1900P CL=0 @ 29.66 dBm	193	mA
	PCS1900P CL=7 @ 15.59 dBm	93	mA
	PCS1900P CL=15 @ 0.58 dBm	75	mA
GSM voice call (Max. Current)	GSM850 PCL=5 @ 32.82 dBm	1.88	A
	GSM850 PCL=12 @ 19.08 dBm	0.46	A
	GSM850 PCL=19 @ 6.12 dBm	0.19	A
	GSM900 PCL=5 @ 32.34 dBm	1.72	A
	GSM900 PCL=12 @ 19.06 dBm	0.44	A
	GSM900 PCL=19 @ 5.39 dBm	0.19	A
	DCS1800P CL=0 @ 29.89 dBm	1.13	A
	DCS1800P CL=7 @ 15.96 dBm	0.30	A
	DCS1800P CL=15 @ 0.95 dBm	0.16	A
	PCS1900P CL=0 @ 29.66 dBm	1.10	A
	PCS1900P CL=7 @ 15.59 dBm	0.33	A
	PCS1900P CL=15 @ 0.58 dBm	0.15	A

Table 33: EG915U-LA Current Consumption

EG915U-LA			
Description	**Conditions**	**Typ.**	**Unit**
OFF state	Power down	40	uA
Sleep state	**AT+CFUN=0** (USB disconnected)	0.98	mA
	AT+CFUN=0 (USB connected)	2.38	mA
	AT+CFUN=4 (USB disconnected)	1.06	mA
	AT+CFUN=4 (USB connected)	2.43	mA
	EGSM @ DRX = 2 (USB disconnected)	2.20	mA
	EGSM @ DRX = 5 (USB disconnected)	1.65	mA
	EGSM @ DRX = 5 (USB connected)	3.07	mA
	EGSM @ DRX = 9 (USB disconnected)	1.47	mA
	DCS @ DRX = 2 (USB disconnected)	2.22	mA
	DCS @ DRX = 5 (USB disconnected)	1.63	mA
	DCS @ DRX = 5 (USB connected)	3.03	mA
	DCS @ DRX = 9 (USB disconnected)	1.48	mA
	LTE-FDD @ PF = 32 (USB disconnected)	3.54	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.25	mA
	LTE-FDD @ PF = 64 (USB connected)	3.74	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.61	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.32	mA
Idle state	EGSM @ DRX = 5 (USB disconnected)	13.06	mA
	EGSM @ DRX = 5 (USB connected)	28.73	mA
	LTE-FDD @ PF = 64 (USB disconnected)	13.05	mA
	LTE-FDD @ PF = 64 (USB connected)	28.61	mA
LTE data transfer	LTE-FDD B2 @ 22.63d Bm	694	mA

	LTE-FDD B3 @ 22.88 dBm	667	mA
	LTE-FDD B4 @ 22.94d Bm	718	mA
	LTE-FDD B5 @ 23.01 dBm	622	mA
	LTE-FDD B7 @ 22.95 dBm	797	mA
	LTE-FDD B8 @ 23.17 dBm	644	mA
	LTE-FDD B28 @ 23.06 dBm	627	mA
	LTE-FDD B66 @ 22.81d Bm	725	mA
GPRS data transfer	GSM850 4DL/1UL @ 32.96 dBm	269	mA
	GSM850 3DL/2UL @ 30.7 dBm	394	mA
	GSM850 2DL/3UL @ 28.66 dBm	463	mA
	GSM850 1DL/4UL @ 26.41 dBm	473	mA
	GSM900 4DL/1UL @ 32.31 dBm	257	mA
	GSM900 3DL/2UL @ 30.7 dBm	372	mA
	GSM900 2DL/3UL @ 28.66 dBm	456	mA
	GSM900 1DL/4UL @ 26.63 dBm	452	mA
	DCS1800 4DL/1UL @ 29.84 dBm	174	mA
	DCS1800 3DL/2UL @ 27.89 dBm	244	mA
	DCS1800 2DL/3UL @ 25.85 dBm	270	mA
	DCS1800 1DL/4UL @ 23.78 dBm	280	mA
	PCS1900 4DL/1UL @ 29.68 dBm	179	mA
	PCS1900 3DL/2UL @ 27.74 dBm	250	mA
	PCS1900 2DL/3UL @ 25.66 dBm	289	mA
	PCS1900 1DL/4UL @ 23.59 dBm	295	mA
GSM voice call	GSM850 PCL=5 @ 32.82 dBm	288	mA
	GSM850 PCL=12 @ 19.08 dBm	113	mA
	GSM850 PCL=19 @ 6.12 dBm	80	mA

	GSM900 PCL=5 @ 32.34 dBm	261	mA
	GSM900 PCL=12 @ 19.06 dBm	112	mA
	GSM900 PCL=19 @ 5.39 dBm	79	mA
	DCS1800P CL=0 @ 29.89 dBm	187	mA
	DCS1800P CL=7 @ 15.96 dBm	91	mA
	DCS1800P CL=15 @ 0.95 dBm	72	mA
	PCS1900P CL=0 @ 29.66 dBm	196	mA
	PCS1900P CL=7 @ 15.59 dBm	94	mA
	PCS1900P CL=15 @ 0.58 dBm	72	mA

6.5. Tx Power

Table 34: EG915U-CN RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD	23 dBm ±2 dB	< -39 dBm
LTE-TDD	23 dBm ±2 dB	< -39 dBm

Table 35: EG915U-EU RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
GSM850/EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B5/B7/B8/B20/B28	23 dBm ±2 dB	< -39 dBm

Table 36: EG915U-LA RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
GSM850/EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B2/B3/B4/B5/B7/B8/B28/B66	23 dBm ±2 dB	< -39 dBm

6.6. Rx Sensitivity

Table 37: EG915U-CN Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)	3GPP (SIMO)
	Primary	Primary+ Diversity
EGSM900	-108.0	-102 dBm
DCS1800	-107.5	-102 dBm
LTE-FDD B1 (10 MHz)	-97.3	-96.3 dBm
LTE-FDD B3 (10 MHz)	-98	-93.3 dBm
LTE-FDD B5 (10 MHz)	-99	-94.3 dBm
LTE-FDD B8 (10 MHz)	-99	-93.3 dBm
LTE-TDD B34 (10 MHz)	-98	-96.3 dBm
LTE-TDD B38 (10 MHz)	-97.6	-96.3 dBm
LTE-TDD B39 (10 MHz)	-98.4	-96.3 dBm
LTE-TDD B40 (10 MHz)	-98.3	-96.3 dBm
LTE-TDD B41 (10 MHz)	-97	-94.3 dBm

Table 38: EG915U-EU Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)	3GPP (SIMO)
	Primary	Primary+ Diversity
GSM850	-108	-102 dBm
EGSM900	-106.5	-102 dBm
DCS1800	-107.5	-102 dBm
PCS1900	-107	-102 dBm
LTE-FDD B1 (10 MHz)	-97	-96.3 dBm
LTE-FDD B3 (10 MHz)	-98.3	-93.3 dBm
LTE-FDD B5 (10 MHz)	-97.4	-94.3 dBm
LTE-FDD B7 (10 MHz)	-96.1	-94.3 dBm
LTE-FDD B8 (10 MHz)	-97	-93.3 dBm
LTE-FDD B20 (10 MHz)	-98.3	-93.3 dBm
LTE-FDD B28 (10 MHz)	-98.6	-94.8 dBm

Table 39: EG915U-LA Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)	3GPP (SIMO)
	Primary	Primary+ Diversity
GSM850	-108	-102 dBm
EGSM900	-106.8	-102 dBm
DCS1800	-107.5	-102 dBm
PCS1900	-107.2	-102 dBm
LTE-FDD B2 (10 MHz)	-98.1	-94.3 dBm
LTE-FDD B3 (10 MHz)	-98.2	-93.3 dBm
LTE-FDD B4 (10 MHz)	-97.5	-96.3 dBm

LTE-FDD B5 (10 MHz)	-97.4	-94.3 dBm
LTE-FDD B7 (10 MHz)	-96.1	-94.3 dBm
LTE-FDD B8 (10 MHz)	-97.5	-93.3 dBm
LTE-TDD B28 (10 MHz)	-99.4	-93.3 dBm
LTE-TDD B66 (10 MHz)	-97.9	-95.8 dBm

6.7. ESD

If the static electricity generated by various ways discharges to the module, the module maybe damaged to a certain extent. Thus, please take proper ESD countermeasures and handling methods. For example, wearing anti-static gloves during the development, production, assembly and testing of the module; adding ESD protective component to the ESD sensitive interfaces and points in the product design of the module.

The following table shows the electrostatics discharge characteristics of the module.

Table 40: Electrostatics Discharge Characteristics (25 °C, 45 % Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.2 Mechanical Dimensions

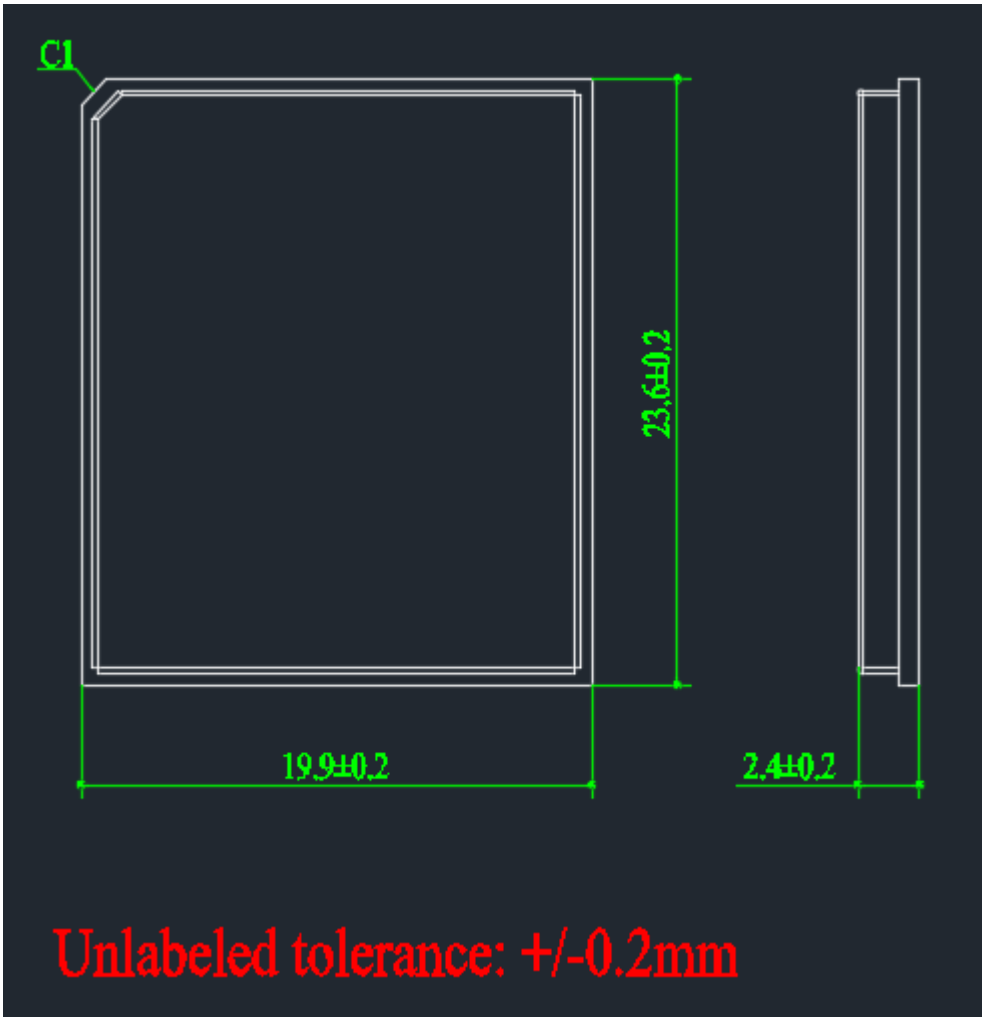


Figure 36: Module Top and Side Dimensions (Unit: mm)

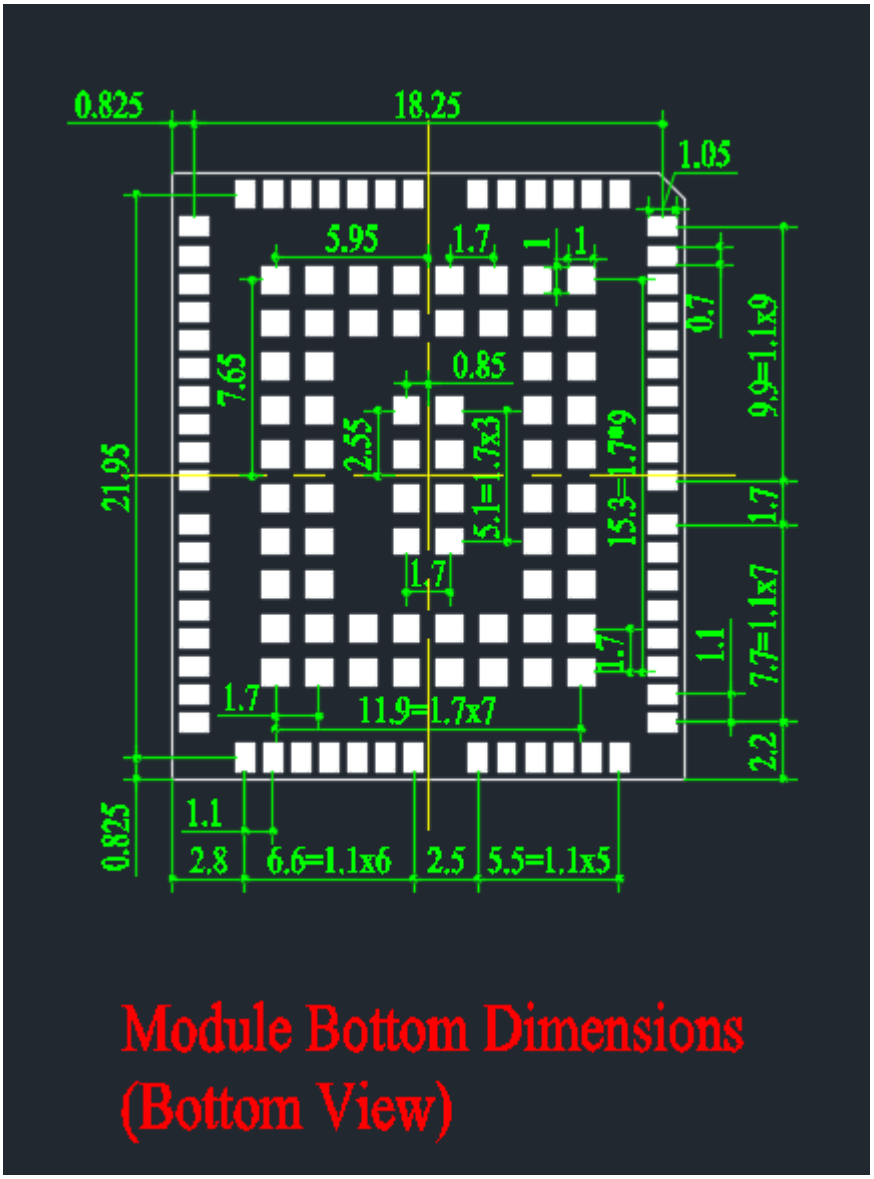


Figure 37: Module Bottom Dimensions

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.3 Recommended Footprint

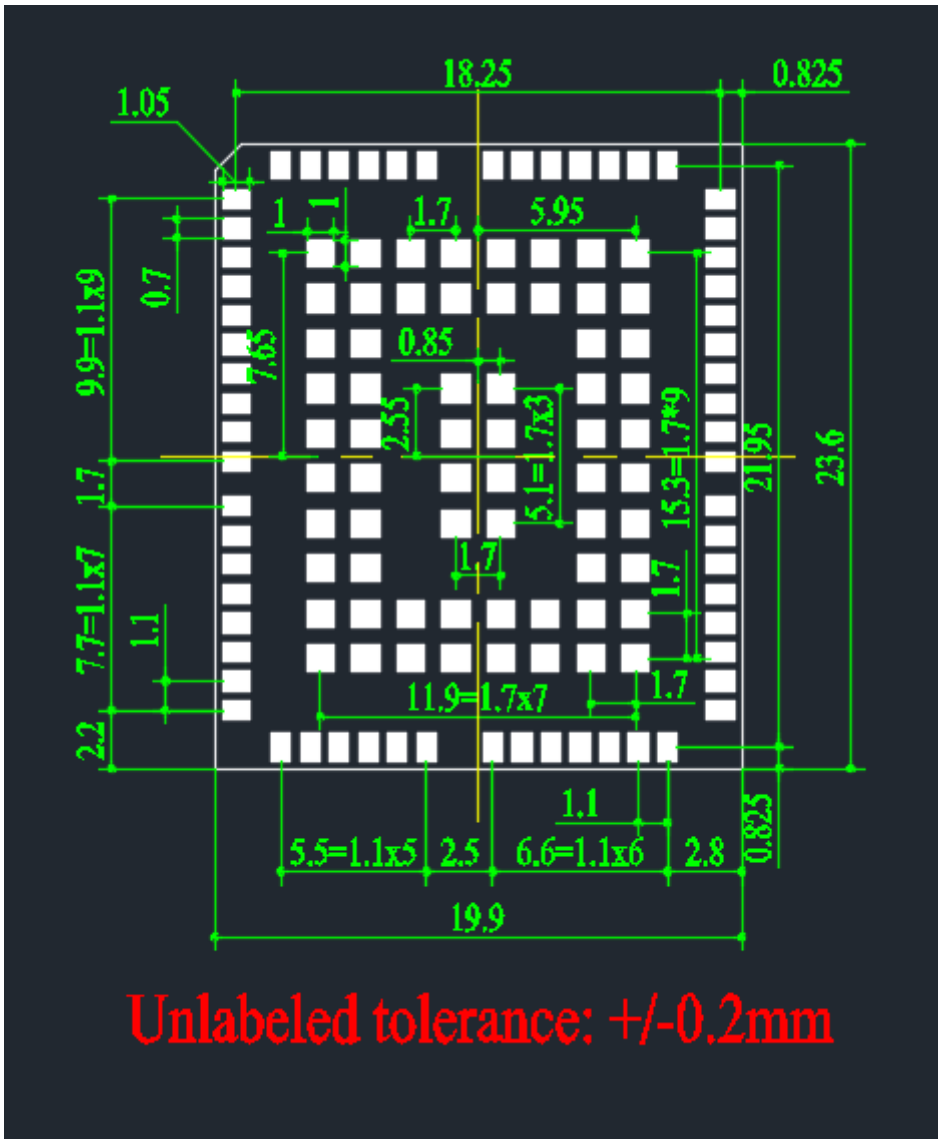


Figure 38: Recommended Footprint (TOP View)

NOTE

1. For easy maintenance of the module, keep about 3 mm between the module and other components on the motherboard.
2. To keep the reliability of the mounting and soldering, keep the motherboard thickness as at least 1.2 mm

7.3 Top and Bottom Views

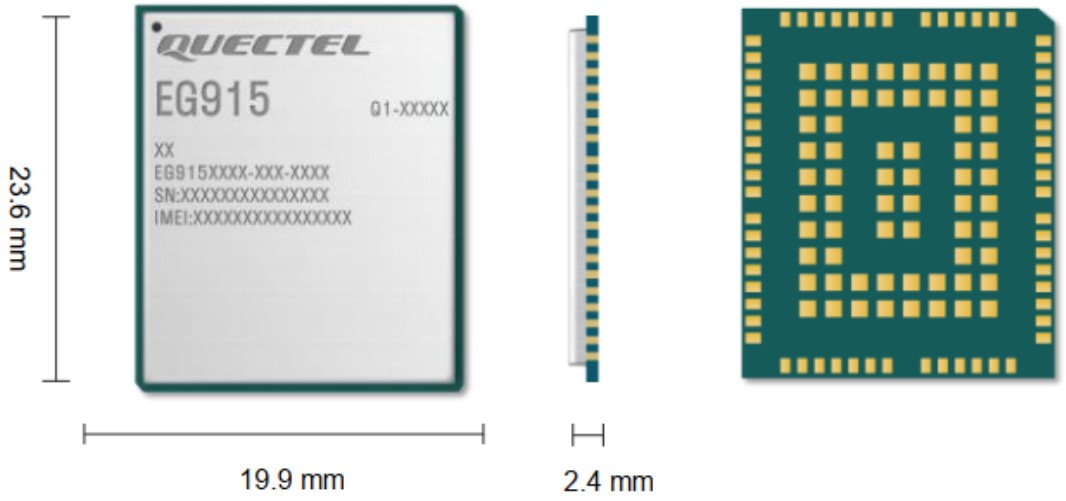


Figure 39: Top & Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1 Storage Conditions

Module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60%.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 [8] hours in a plant where the temperature is 23 ±5 °C and relative humidity is below 60%. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

[8] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.
3. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.

8.2

8.2 Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20 mm. For more details, see ***document [4]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

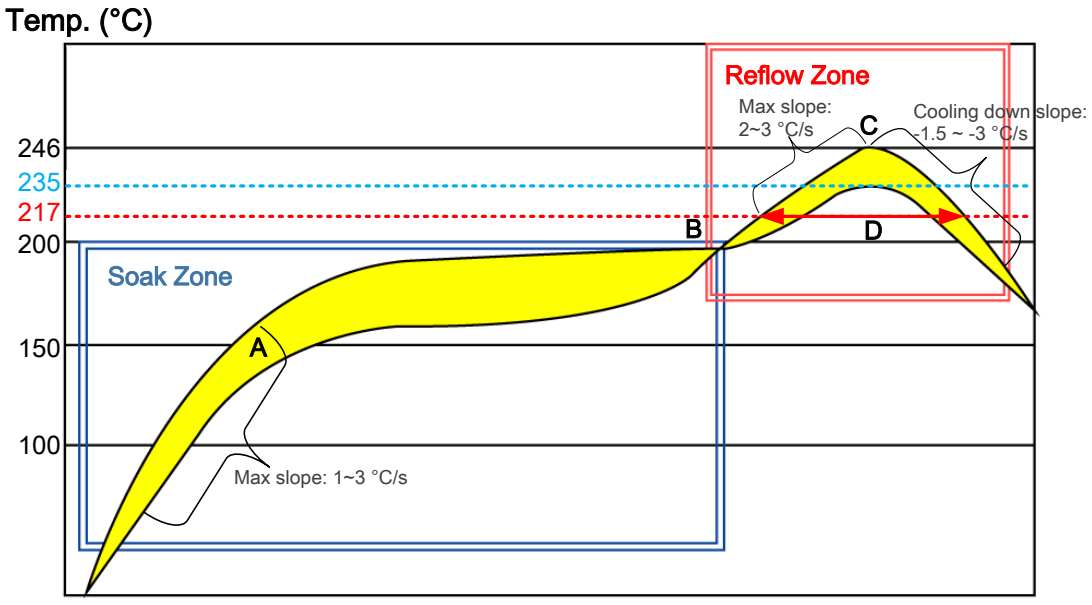


Figure 40: Recommended Reflow Soldering Thermal Profile

Table 41: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	2–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235–246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document [4]***.

8.3 Packaging Specifications

The module is packaged in tape and reel carriers. One reel is 300 mm long and contains 250 modules.

The figures below show the package details, measured in mm.

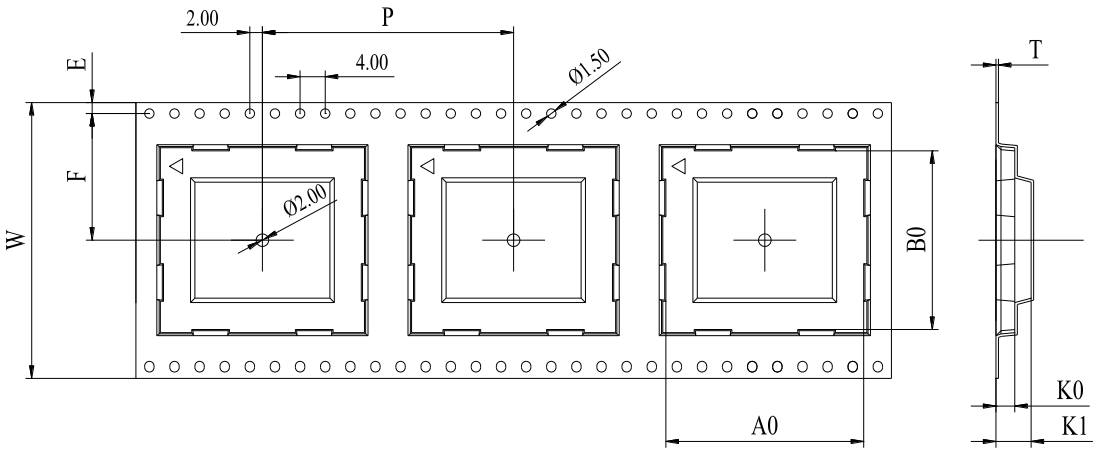


Figure 41: Tape Specifications

Table 39:Tape Size（mm）

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	20.2	24	3.15	6.65	20.2	1.75

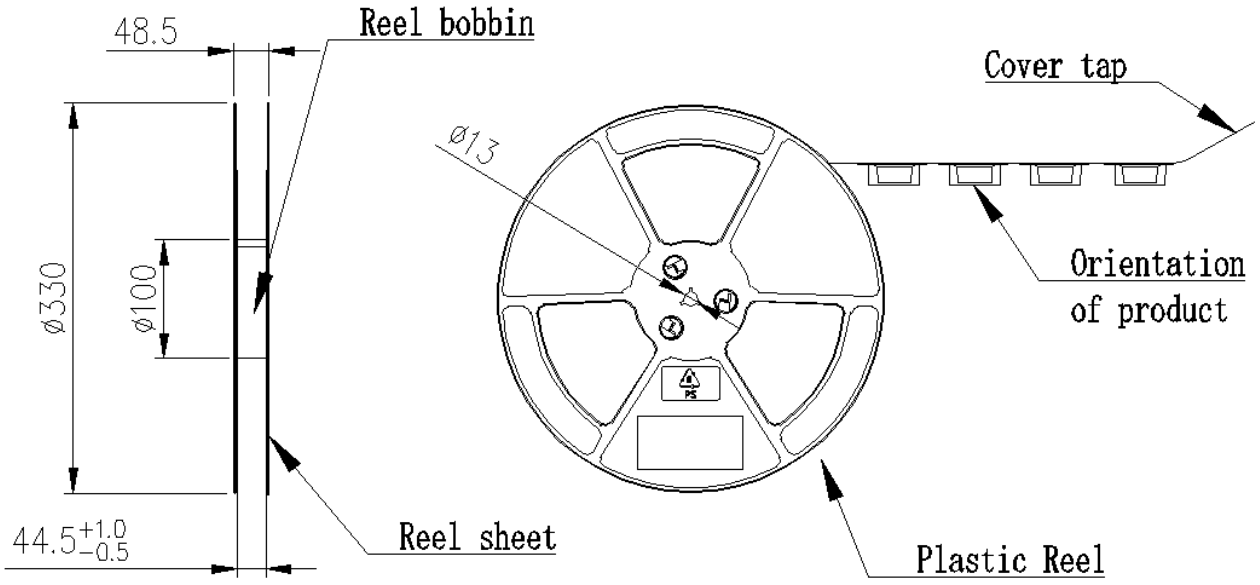


Figure 42: Reel Specifications

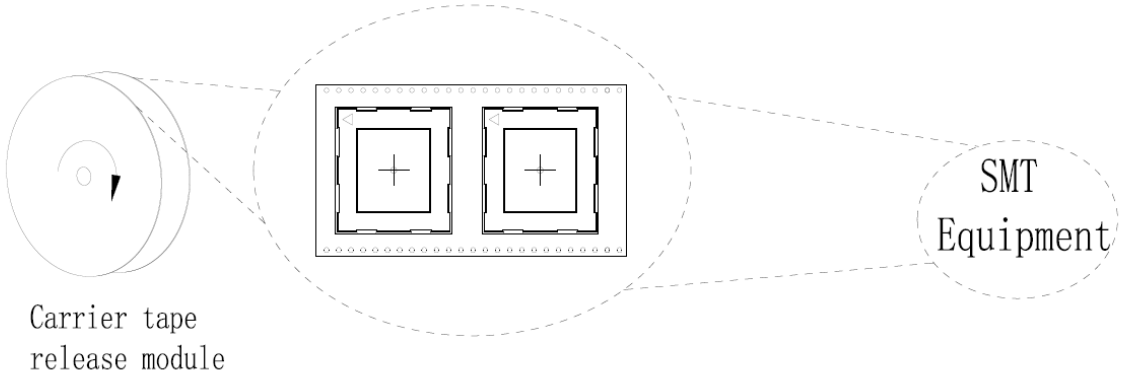
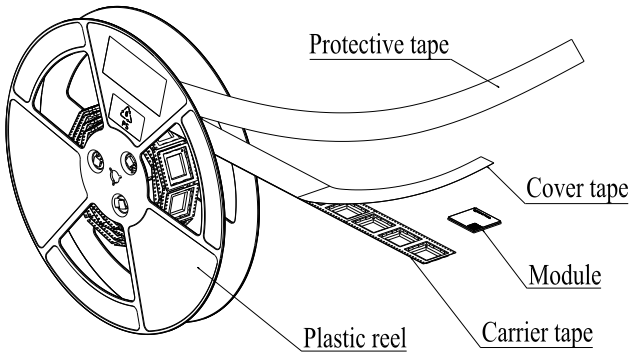


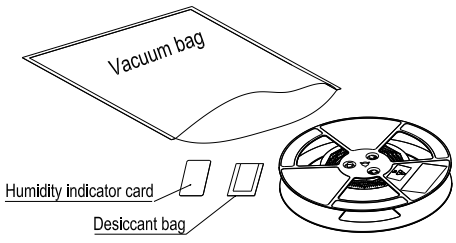
Figure 43: Tape and Reel Directions

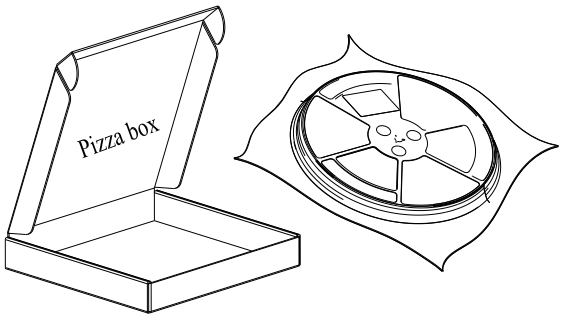
Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 cartoon box and seal it. 1 cartoon box can pack 1000 modules.

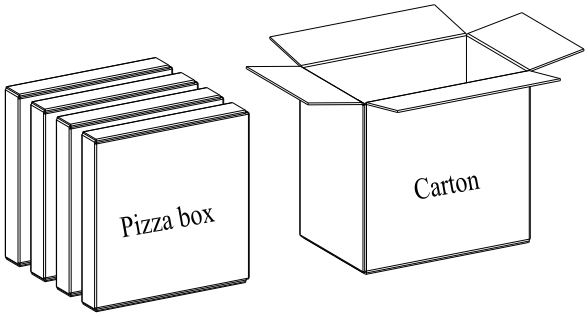


Figure 43: Packaging Process

9 Appendix References

Table 42: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EG915U-EU_Series_AT_Commands_Manual
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_SMT_User_Guide

Table 43: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR-WB	Adaptive Multi-Rate Wideband
AON	Active Optical Network
AP	Application Processor
bps	Bits Per Second
BPSK	Binary Phase Shift Keying
BW	Bandwidth
CA	Carrier Aggregation
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data
CS2	Commercial Sample II

CTS	Clear To Send
DAI	Digital Audio Interface
DCE	Data Communications Equipment
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DDR	Double Data Rate
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DRX	Discontinuous Reception
DRX	Diversity Receive
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FEM	Front-End Module
FR	Full Rate
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GRFC	General RF Control
HB	High Band
HPUE	High Power User Equipment
HR	Half Rate
HSDPA	High Speed Downlink Packet Access

HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
IC	Integrated Circuit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
I/O	Input/Output
Inorm	Normal Current
LAA	License Assisted Access
LB	Low Band
LED	Light Emitting Diode
LGA	Land Grid Array
LMHB	Low/Middle/High Band
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MAC	Media Access Control
MB	Middle Band
MCU	Microcontroller Unit
MDC	Management Data Clock
MDIO	Management Data Input/Output
MHB	Middle/High Band
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MS	Mobile Station
MT	Mobile Terminated
NR	New Radio

NSA	Non-Stand Alone
PA	Power Amplifier
PAP	Password Authentication Protocol
PC	Personal Computer
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PHY	Physical Layer
PMIC	Power Management Integrated Circuit
PRX	Primary Receive
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RI	Ring Indicator
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RHCP	Right Hand Circularly Polarized
Rx	Receive
SA	Stand Alone
SCS	Sub-Carrier Space
SD	Secure Digital
SIMO	Single Input Multiple Output
SMD	Surface Mount Device

SMS	Short Message Service
SoC	System on a Chip
SPI	Serial Peripheral Interface
STB	Set Top Box
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TRX	Transmit & Receive
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UHB	Ultra High Band
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage Value
Vnom	Nominal Voltage Value
Vmin	Minimum Voltage Value
$V_{IH}max$	Maximum Input High Level Voltage Value
$V_{IH}min$	Minimum Input High Level Voltage Value
$V_{IL}max$	Maximum Input Low Level Voltage Value
$V_{IL}min$	Minimum Input Low Level Voltage Value
$V_{I}max$	Absolute Maximum Input Voltage Value

$V_I$min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WWAN	Wireless Wide Area Network