EG95 Series

Hardware Design

LTE Standard Module Series

Version: 1.8

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Status: Preliminary

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About the Document

Revision History

Version	Date	Author	Description
1.0	2017-03-22	Felix YIN/ Yeoman CHEN/ Jackie WANG	Initial
1.1	2018-01-04	Yeoman CHEN/ Rex WANG	1. Added band B28A. 2. Updated the description of UMTS and GSM features in Table 2. 3. Updated the functional diagram in Figure 1. 4. Updated module operating frequencies in Table 21. 5. Updated current consumption in Table 26. 6. Updated the conducted RF receiving sensitivity in Table 28. 7. Updated the GPRS multi-slot classes in Table 33. 8. Added thermal consideration in Chapter 5.8 9. Added a GND pad in each of the four corners of the module's footprint in Chapter 6.2. 10. Added packaging information in Chapter 7.3.
1.2	2018-03-14	Felix YIN/ Rex WANG	1. Added the description of EG95-NA. 2. Updated the functional diagram in Figure 1. 3. Updated pin assignment in Figure 2. 4. Updated GNSS function in Table 1. 5. Updated GNSS Features in Table 2. 6. Updated reference circuit of USB interface in Figure 21. 7. Added description of GNSS receiver in Chapter 4. 8. Updated pin definition of RF antenna in Table 21.

			9. Updated module operating frequencies in Table 22. 10. Added description of GNSS antenna interface in Chapter 5.2. 11. Updated antenna requirements in Table 25. 12. Updated RF output power in Table 32.
1.3	2019-05-24	Ward WANG/ Nathan LIU/ Rex WANG	1. Added variant EG95-EX and related information. 2. Updated functional diagram in Figure 1. 3. Updated pin assignment (top view) in Figure 2. 4. Updated pin description in Table 4. 5. Updated star structure of power supply in Figure 8. 6. Updated the reference circuit of turning on the module using PWRKEY in Figure 10. 7. Updated the power-on scenario in Figure 12. 8. Updated reference circuit of SPI interface with peripherals in Figure 25. 9. Updated GNSS performance in Table 20. 10. Updated module operating frequencies in Table 22. 11. Updated GNSS frequency in Table 24. 12. Updated antenna requirements in Table 25. 13. Updated EG95-NA current consumption in Table 30. 14. Adeed EG95-EX current consumption in Table 31. 15. Updated EG95-E conducted RF receiving sensitivity in Table 34. 16. Updated EG95-NA conducted RF receiving sensitivity in Table 35. 17. Added EG95-EX conducted RF receiving sensitivity in Table 36.Updated GNSS current consumption of EG95 in Table 32.Updated related documents in Table 38.Updated reference circuit of PWRKEY interface in Figure 10. 18. Updated description of (U)SIM in Chapter 3.9. 19. Updated description of UART in Chapter 3.11. 20. Added description of ADC interface in Chapter 3.16.

			21. Added description of USB_BOOT interface in Chapter 3.18. 22. Updated description of manufacturing and soldering in Chapter 8.2.
1.4	2019-07-05	Ward WANG	1. Updated supported protocols (Table 2). 2. Updated timing of turning on module (Figure 12). 3. DFOTA is developed. 4. Updated description of USB_BOOT interface and timing sequence for entering emergency download mode (Chapter 3.18 and Figure 29).
1.5	2019-08-09	Fanny CHEN/ Rex WANG	1. Added ThreadX module EG95-NAX and updated related contents (Table 1 and 4, Chapter 2.2, 2.3, 3.2 and 5). 2. Updated module operating frequencies (Table 25). 3. Updated antenna requirements (Table 28). 4. Added current consumption of EG95-NAX (Table 35). 5. Updated RF output power (Table 37). 6. Updated EG95-NA conducted RF receiving sensitivity (Table 39). 7. Added EG95-NAX conducted RF receiving sensitivity (Table 41).
1.6	2019-11-07	Ward WANG	1. Removed related information of ThreadX OS. 2. Updated the supported USB serial drivers (Table 2) 3. Updated the notes for GNSS performance (Chapter 4.2). 4. Updated the AT command be used to disable the receive diversity (Chapter 5.1.3).
1.7	2020-04-15	Ward WANG	1. Updated description of airplane mode (Chapter 3.5.2). 2. Updated the functions of main UART interface (Chapter 3.11). 3. Added the note about the standard that the package warpage level of the module conforms to (Chapter 7.1). 4. Updated module storage information (Chapter 8.1). 5. Updated module manufacturing and soldering information (Chapter 8.2).

1.8	2020-08-24	Frank WANG	Added EG95-AUX and related information (Table 1, 36 and 43).

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1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text:
"Contains FCC ID: XMR202106EG95AUX "
The FCC ID can be used only when all FCC compliance requirements are met.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can

be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation,maximum antenna gain (including cable loss)must not exceed:

GSM850/WCDMA Band5/LTE Band 5:≤ 7.0dBi
GSM1900/WCDMA Band2/LTE Band 2:≤ 3.0dBi
LTE Band 4/ LTE Band 66≤ 5.0dBi
LTE Band 7:≤ 8.0dBi

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

1 Introduction

This document defines EG95 series module, and describes its air interface and hardware interfaces which are connected with customers' applications.

This document can help customers quickly understand module interface specifications, electrical and mechanical details as well as other related information of EG95 series module. To facilitate its application in different fields, relevant reference design is also provided for customers' reference. Associated with application note and user guide, customers can use EG95 series module to design and set up mobile applications easily.

Hereby, Quectel Wireless Solutions Co., Ltd. declares that the radio equipment type LTE Module EG95-AUX is in compliance with Directive 2014/53/EU.
The full text of the EU declaration of conformity is available at the following internet address: https://www.quectel.com/ProductDownload/

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating EG95 series module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.

Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.

The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.

In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

EG95 series module is an embedded 4G wireless communication module with receive diversity. It supports LTE-FDD/WCDMA/GSM wireless communication, and provides data connectivity on LTE-FDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, EDGE and GPRS networks. It can also provide voice functionality 1) to meet customers' specific application demands. EG95 series contains 5 variants: EG95-E, EG95-NA, EG95-EX, EG95-NAX and EG95-AUX. The following table shows the frequency bands of EG95 series module.

Table 1: Frequency Bands of EG95 Series Module

Module	LTE Bands (with Rx-diversity)	WCDMA (with Rx-diversity)	GSM	GNSS 2)
EG95-E	FDD: B1/B3/B7/B8/B20/B28A	B1/B8	900/1800 MHz	Not supported
EG95-NA	FDD: B2/B4/B5/B12/B13	B2/B4/B5	Not supported	GPS, GLONASS, BeiDou/Compass, Galileo, QZSS
EG95-EX	FDD: B1/B3/B7/B8/B20/B28	B1/B8	900/1800 MHz	GPS, GLONASS, BeiDou/Compass, Galileo, QZSS
EG95-NAX	FDD: B2/B4/B5/B12/B13/B25/B26	B2/B4/B5	Not supported	GPS, GLONASS, BeiDou/Compass, Galileo, QZSS
EG95-AUX	FDD: B1/B2/B3/B4/B5/B7/B8 B28/B66	B1/B2/B5/B8	850/900/1800/1900	GPS, GLONASS, BeiDou/Compass, Galileo, QZSS

NOTES

1. 1) EG95 contains **Telematics** version and **Data-only** version. **Telematics** version supports voice and data functions, while **Data-only** version only supports data function.
2. 2) GNSS function is optional.

With a compact profile of 29.0mm × 25.0mm × 2.3mm, EG95 can meet almost all requirements for M2M applications such as automotive, smart metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, tablet PC, etc.

EG95 is an SMD type module which can be embedded into applications through its 106 LGA pads.

EG95 is integrated with internet service protocols like TCP, UDP and PPP. Extended AT commands have been developed for customers to use these internet service protocols easily.

2.2. Key Features

The following table describes the detailed features of EG95 module.

Table 2: Key Features of EG95 Module

Features	Description
Power Supply	Supply voltage: 3.3–4.3 V Typical supply voltage: 3.8 V
Transmitting Power	Class 4 (33dBm±2dB) for GSM850 Class 4 (33dBm±2dB) for EGSM900 Class 1 (30dBm±2dB) for DCS1800 Class 1 (30dBm±2dB) for PCS1900 Class E2 (27dBm±3dB) for GSM850 8-PSK Class E2 (27dBm±3dB) for EGSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class E2 (26dBm±3dB) for PCS1900 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (23dBm±2dB) for LTE-FDD bands
LTE Features	Support up to non-CA Cat 4 FDD Support 1.4/3/5/10/15/20 MHz RF bandwidth Support MIMO in DL direction FDD: Max 150 Mbps (DL)/Max 50 Mbps (UL)
UMTS Features	Support 3GPP R8 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA Support QPSK, 16-QAM and 64-QAM modulation DC-HSDPA: Max 42 Mbps (DL) HSUPA: Max 5.76 Mbps (UL) WCDMA: Max 384 kbps (DL)/ Max 384 kbps (UL)
GSM Features	**R99:** CSD: 9.6 kbps **GPRS:**

	Support GPRS multi-slot class 33 (33 by default) Coding scheme: CS-1, CS-2, CS-3 and CS-4 Max 107 kbps (DL), Max 85.6 kbps (UL) **EDGE:** Support EDGE multi-slot class 33 (33 by default) Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: MCS 1-9 Uplink coding schemes: MCS 1-9 Max 296 kbps (DL)/Max 236.8 kbps (UL)
Internet Protocol Features	Support TCP/UDP/PPP/FTP/FTPS/HTTP/HTTPS/NTP/PING/QMI/NITZ/SMTP/SSL/MQTT/CMUX/SMTPS/MMS*/FILE* protocols Support PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) protocols which are usually used for PPP connections
SMS	Text and PDU modes Point-to-point MO and MT SMS cell broadcast SMS storage: ME by default
(U)SIM Interfaces	Support 1.8 V and 3.0 V (U)SIM cards
Audio Features	Support one digital audio interface: PCM interface GSM: HR/FR/EFR/AMR/AMR-WB WCDMA: AMR/AMR-WB LTE: AMR/AMR-WB Support echo cancellation and noise suppression
PCM Interface	Used for audio function with external codec Support 16-bit linear data format Support long frame synchronization and short frame synchronization Support master and slave modes, but must be the master in long frame synchronization
USB Interface	Compliant with USB 2.0 specification (slave only); the data transfer rate can reach up to 480 Mbps Used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB Support USB serial drivers for: Windows 7/8/8.1/10, Linux 2.6–5.4, Android 4.x/5.x/6.x/7.x/8.x/9.x, etc.
UART Interface	**Main UART:** Used for AT command communication and data transmission Baud rates reach up to 921600 bps, 115200 bps by default Support RTS and CTS hardware flow control **Debug UART:** Used for Linux console and log output

	115200 bps baud rate
SPI Interface	Provides a duplex, synchronous and serial communication link with the peripheral devices. Dedicated to one-to-one connection, without chip selection. 1.8 V operation voltage with clock rates up to 50 MHz.
Rx-diversity	Support LTE/WCDMA Rx-diversity
GNSS Features	Gen8C Lite of Qualcomm Protocol: NMEA 0183 Data update rate: 1Hz by default
AT Commands	Compliant with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands
Network Indication	NETLIGHT pin for network activity status indication
Antenna Interfaces	Including main antenna interface (ANT_MAIN), Rx-diversity antenna (ANT_DIV) interface and GNSS antenna interface (ANT_GNSS)1)
Physical Characteristics	Size: (29.0 ±0.15) mm × (25.0 ±0.15) mm × (2.3 ±0.2) mm Package: LGA Weight: approx. 3.8 g
Temperature Range	Operation temperature range: -35 °C to +75 °C 2) Extended temperature range: -40 °C to +85 °C 3) Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	USB interface or DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. 1) GNSS antenna interface is only supported on EG95-NA/-EX/-NAX/-AUX.
2. 2) Within operation temperature range, the module is 3GPP compliant.
3. 3) Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call*, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operation temperature levels, the module will meet 3GPP specifications again.
4. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of EG95 and illustrates the major functional parts.

- Power management
- Baseband
- DDR+NAND flash
- Radio frequency
- Peripheral interfaces

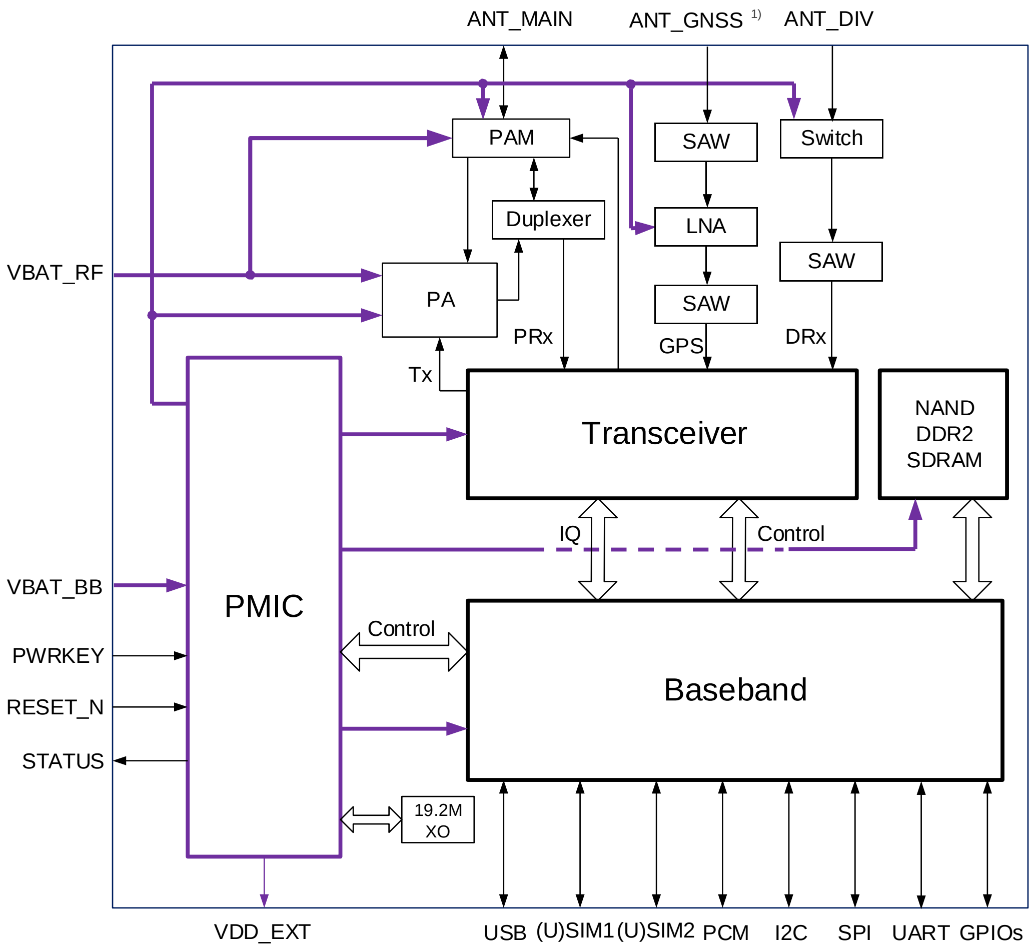


Figure 1: Functional Diagram

NOTE

[1] GNSS antenna interface is only supported on EG95-NA/-EX/-NAX/-AUX.

2.4. Evaluation Board

In order to help customers develop applications with EG95, Quectel supplies an evaluation board (UMTS&LTE EVB), USB data cable, earphone, antenna and other peripherals to control or test the module. For more details, please refer to ***document [7]***.

3 Application Interfaces

3.1. General Description

EG95 is equipped with 62 SMT pads and 44-pin ground/reserved pads that can be connected to cellular application platform. The subsequent chapters will provide detailed descriptions of the following functions/interfaces.

- Power supply
- (U)SIM interfaces
- USB interface
- UART interfaces
- PCM and I2C interfaces
- SPI interface
- Status indication
- USB_BOOT interface

3.2. Pin Assignment

The following figure shows the pin assignment of EG95 module.

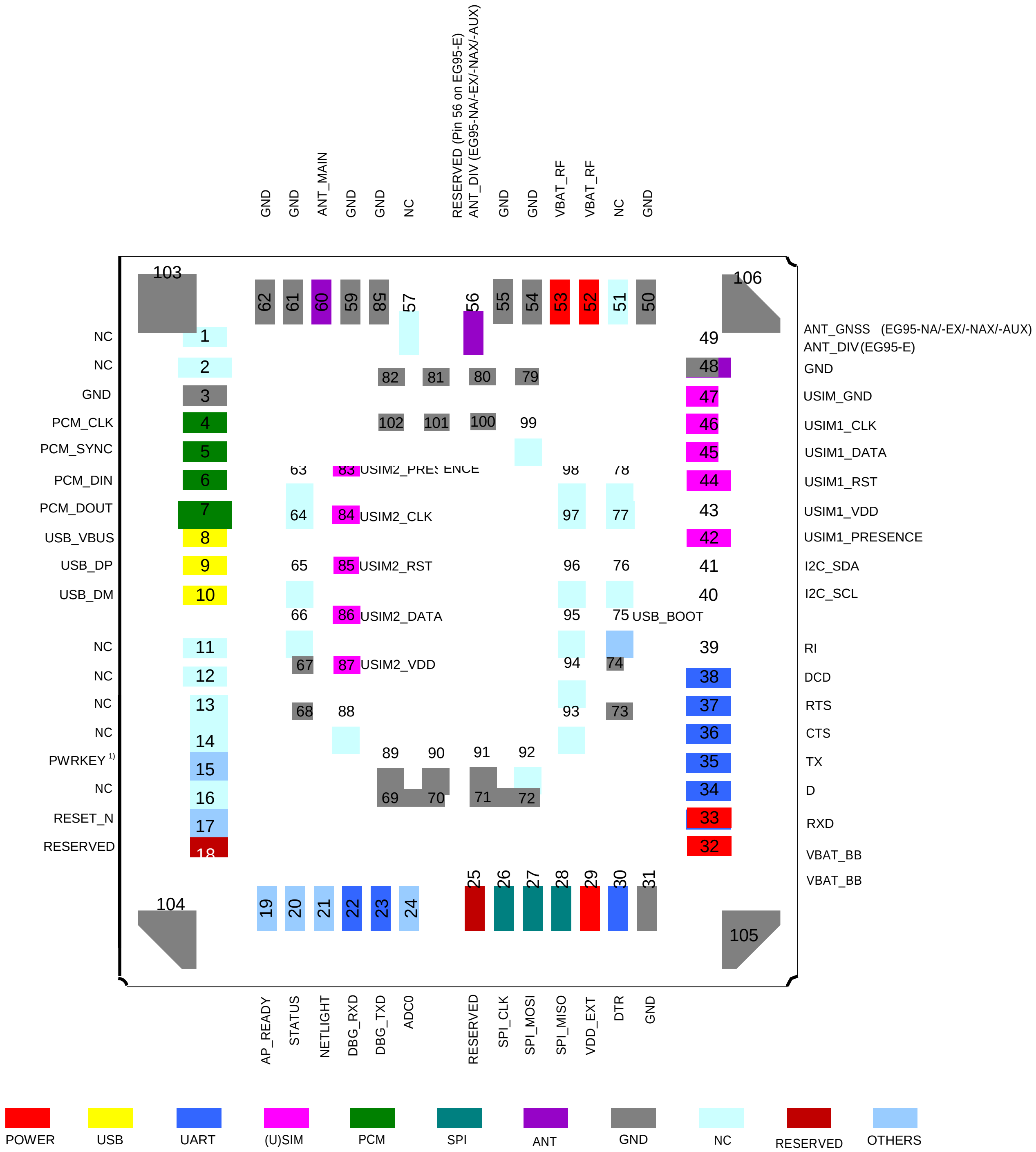


Figure 2: Pin Assignment (Top View)

NOTES

1. 1) PWRKEY output voltage is 0.8 V because of the diode drop in the Qualcomm chipset.
2. Keep all RESERVED pins and unused pins unconnected.
3. GND pads should be connected to ground in the design.
4. Please note that the definition of pin 49 and 56 are different among EG95-E and EG95-NA/-EX/-NAX/-AUX. For more details, please refer to ***Table 4***.

3.3. Pin Description

The following tables show the pin definition of EG95 module.

Table 3: IO Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
DI	Digital Input
DO	Digital Output
IO	Bidirectional
OD	Open Drain
PI	Power Input
PO	Power Output

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32, 33	PI	Power supply for module's baseband part	Vmax = 4.3 V Vmin = 3.3 V Vnorm = 3.8 V	It must be provided with sufficient current up to 0.8 A.
VBAT_RF	52, 53	PI	Power supply for	Vmax = 4.3 V	It must be provided

			module's RF part	Vmin = 3.3 V Vnorm = 3.8 V	with sufficient current up to 1.8 A in a burst transmission.
VDD_EXT	29	PO	Provide 1.8 V for external circuit	Vnorm = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull up circuits. If unused, keep it open.
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–106		Ground		
Power-on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turn on/off the module	V_H = 0.8 V	The output voltage is 0.8 V because of the diode drop in the Qualcomm chipset.
RESET_N	17	DI	Reset signal of the module	V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	Pull-up to 1.8 V internally. Active low. If unused, keep it open.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	20	DO	Indicate the module's operation status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
NETLIGHT	21	DO	Indicate the module's network activity status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	8	PI	USB connection detection	Vmax = 5.25 V Vmin = 3.0 V Vnorm = 5.0 V	Typical: 5.0 V If unused, keep it open.

USB_DP	9	IO	USB differential		USB 2.0 Compliant. Require differential
USB_DM	10	IO	USB differential data bus (-)		USB 2.0 Compliant. Require differential impedance of 90 Ω.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	47		Specified ground for (U)SIM card		
USIM1_VDD	43	PO	Power supply for (U)SIM card	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	45	IO	Data signal of (U)SIM card	**For 1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_CLK	46	DO	Clock signal of (U)SIM card	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	

USIM1_RST	44	DO	Reset signal of (U)SIM card	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_ PRESENCE	42	DI	(U)SIM card insertion detection	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
USIM2_VDD	87	PO	Power supply for (U)SIM card	**For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V $I_O$max = 50 mA	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM2_DATA	86	IO	Data signal of (U)SIM card	**For 1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_CLK	84	DO	Clock signal of (U)SIM card	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_RST	85	DO	Reset signal of (U)SIM card	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	

USIM2_ PRESENCE	83	DI	(U)SIM card insertion detection	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V	1.8 V power domain. If unused, keep it
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RI	39	DO	Ring indicator	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
DCD	38	DO	Data carrier detection	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
CTS	36	DO	Clear to send	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
RTS	37	DI	Request to send	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
DTR	30	DI	Data terminal ready. Sleep mode control.	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pull-up by default. Low level wakes up the module. If unused, keep it open.
TXD	35	DO	Transmit data	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
RXD	34	DI	Receive data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	23	DO	Transmit data	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
DBG_RXD	22	DI	Receive data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V	1.8 V power domain. If unused, keep it open.

PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_DIN	6	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
PCM_DOUT	7	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
PCM_SYNC	5	IO	PCM data frame synchronization signal	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_CLK	4	IO	PCM clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	40	OD	I2C serial clock. Used for external codec		An external pull-up to 1.8 V is required. If unused, keep it open.
I2C_SDA	41	OD	I2C serial data. Used for external codec		An external pull-up to 1.8 V is required. If unused, keep it open.
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	24	AI	General purpose analog to digital	Voltage range: 0.3 V to VBAT_BB	If unused, keep it open.

converter

SPI Interface [1]					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CLK	26	DO	Clock signal of SPI interface	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
SPI_MOSI	27	DO	Master output slave input of SPI interface	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
SPI_MISO	28	DI	Master input slave output of SPI interface	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
RF Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_GNSS	49 (EG95-NA/-EX/ -NAX/-AUX)	AI	GNSS antenna pad		50 Ω impedance. If unused, keep it open. The pin is defined as ANT_DIV on EG95-E.
ANT_DIV	49 (EG95-E) 56 (EG95-NA/-EX/ -NAX/-AUX)	AI	Receive diversity antenna pad		50 Ω impedance. If unused, keep it open. Pin 56 is reserved on EG95-E.
ANT_MAIN	60	IO	Main antenna pad		50 Ω impedance.
Other Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
AP_READY	19	DI	Application processor sleep state detection	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.

USB_BOOT	75	DI	Force the module to enter emergency	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V	1.8 V power domain. It is recommended to reserve the test
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NC	1,2, 11–14, 16, 51, 57, 63–66, 76–78, 88, 92–99		NC		Keep these pins unconnected.
RESERVED	18, 25, 56		Reserved		Keep these pins unconnected. Pin 56 is only reserved on EG95-E.

NOTE

Keep all RESERVED pins and unused pins unconnected.

3.4. Operating Modes

The following table briefly outlines the operating modes to be mentioned in the following chapters.

Table 5: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** command can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** command or W_DISABLE# pin can set the module to enter airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level.	

	During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.
Power Down Mode	In this mode, the power management unit shuts down the power supply. Softwar goes inactive. The serial interface is not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.

3.5. Power Saving

3.5.1. Sleep Mode

EG95 is able to reduce its current consumption to a minimum value during the sleep mode. The following sub-chapters describe the power saving procedures of EG95 module.

3.5.1.1. UART Application

If the host communicates with module via UART interface, the following preconditions can let the module enter sleep mode.

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Drive DTR to high level or keep it open.

The following figure shows the connection between the module and the host.

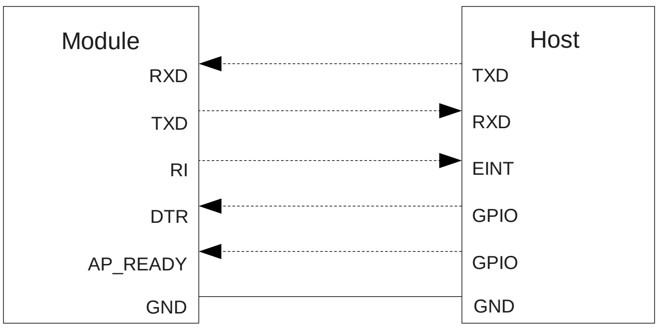


Figure 3: Sleep Mode Application via UART

Driving the host DTR to low level will wake up the module.

- When EG95 has a URC to report, RI signal will wake up the host. Please refer to ***Chapter 3.17*** for details about RI behaviors.
- AP_READY will detect the sleep state of host (can be configured to high level or low level detection). Please refer to **AT+QCFG="apready"** for details.

3.5.1.2. USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup functions, the following three preconditions must be met to let the module enter sleep mode.

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

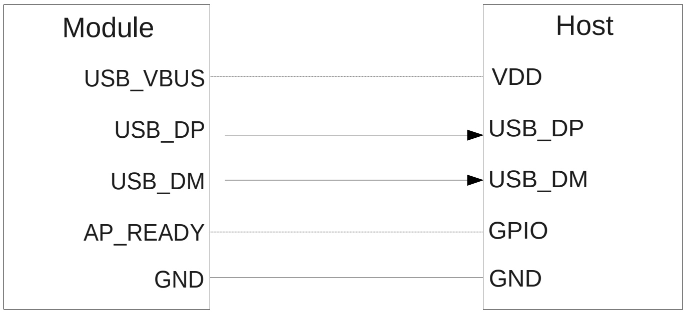


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to EG95 through USB will wake up the module.
- When EG95 has a URC to report, the module will send remote wakeup signals via USB bus so as to wake up the host.

3.5.1.3. USB Application with USB Suspend/Resume and RI Function

If the host supports USB suspend/resume, but does not support remote wake-up function, the RI signal is needed to wake up the host.

There are three preconditions to let the module enter sleep mode.

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters suspended state.

The following figure shows the connection between the module and the host.

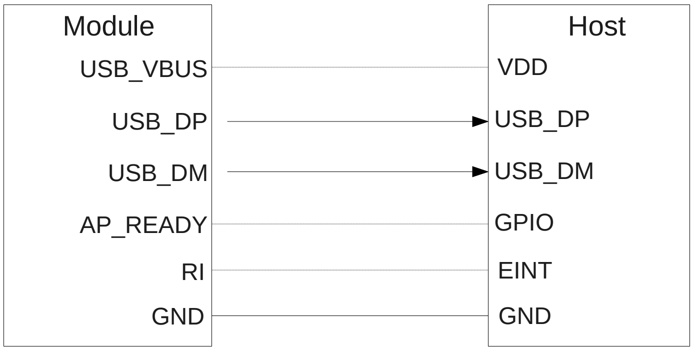


Figure 5: Sleep Mode Application with RI

- Sending data to EG95 via USB will wake up the module.
- When module has a URC to report, RI signal will wake up the host.

3.5.1.4. USB Application without USB Suspend Function

If the host does not support USB suspend function, USB_VBUS should be disconnected with an external control circuit to let the module enter sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

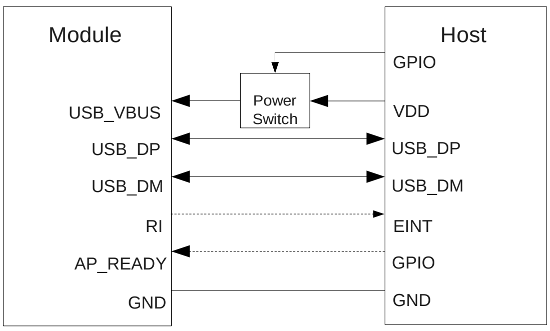


Figure 6: Sleep Mode Application without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

Please pay attention to the level match shown in dotted line between the module and the host. Please refer to ***document [1]*** for more details about EG95 power management application.

3.5.2. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

Software:

AT+CFUN command provides the choice of the functionality level through setting **<fun>** as 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

NOTES

1. Airplane mode control via W_DISABLE# is disabled in firmware by default. It can be enabled by **AT+QCFG="airplanecontrol"** command.
2. The execution of **AT+CFUN** command will not affect GNSS function.

3.6. Power Supply

3.6.1. Power Supply Pins

EG95 provides four VBAT pins for connection with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module’s RF part.
- Two VBAT_BB pins for module’s baseband part.

The following table shows the details of VBAT pins and ground pins.

Table 6: Pin Definition of VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	52, 53	Power supply for module’s RF part.	3.3	3.8	4.3	V

VBAT_BB	32, 33	Power supply for module's baseband part.	3.3	3.8	4.3	V
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–106	Ground	-	0	-	V

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.3V to 4.3V. Please make sure that the input voltage will never drop below 3.3V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G and 4G networks.

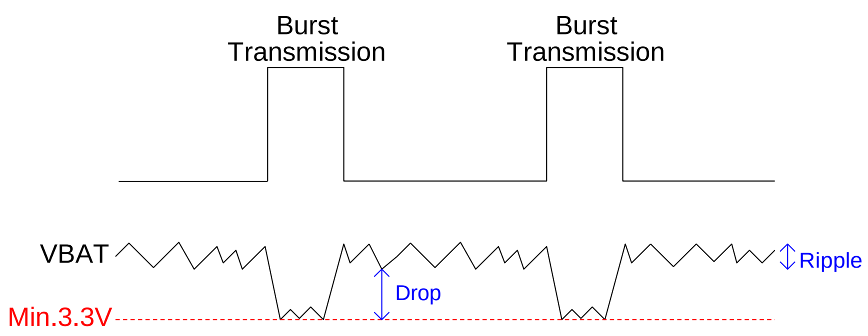


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100µF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT_BB/VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1 mm, and the width of VBAT_RF trace should be no less than 2 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to avoid the damage caused by electric surge and electrostatics discharge (ESD), it is suggested that a TVS diode with suggested low reverse stand-off voltage V_{RWM}, low clamping voltage V_C and high reverse peak pulse current I_{PP} should be used. The following figure shows the star structure of the power supply.

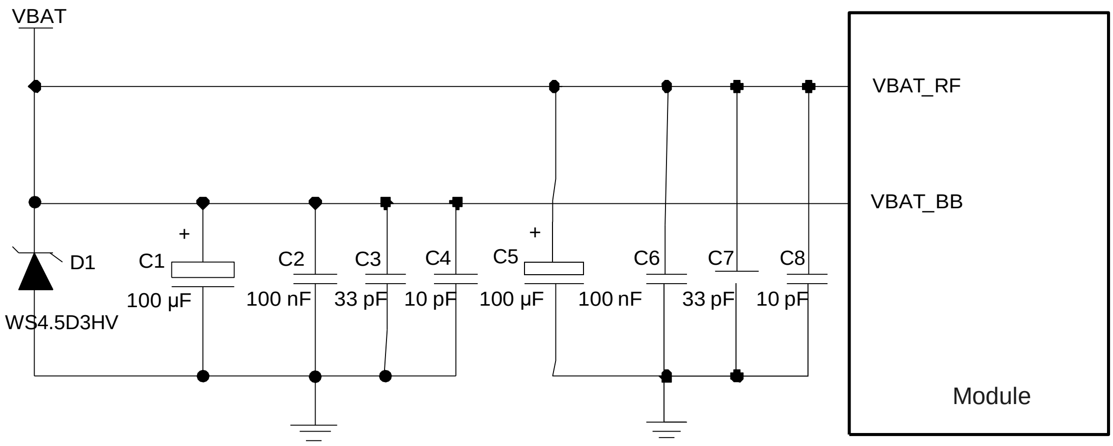


Figure 8: Star Structure of Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current up to 2A at least. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5V input power source. The typical output of the power supply is about 3.8V and the maximum load current is 3.0A.

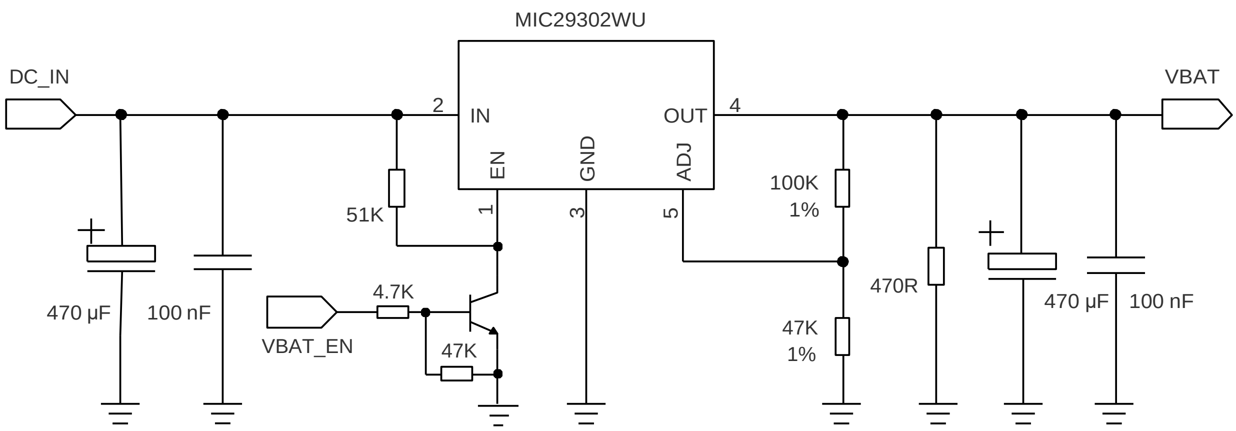


Figure 9: Reference Circuit of Power Supply

NOTE

In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.

3.6.4. Monitor the Power Supply

AT+CBC command can be used to monitor the VBAT_BB voltage value. For more details, please refer to ***document [2]***.

3.7. Power-on/off Scenarios

3.7.1. Turn on Module Using the PWRKEY

The following table shows the pin definition of PWRKEY.

Table 7: Pin Definition of PWRKEY

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRKEY	15	Turn on/off the module	V_{IH} = 0.8 V	The output voltage is 0.8 V because of the diode drop in the Qualcomm chipset.

When EG95 is in power down mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 500ms. It is recommended to use an open drain/collector driver to control the PWRKEY. After STATUS pin outputting a high level, PWRKEY pin can be released. A simple reference circuit is illustrated in the following figure.

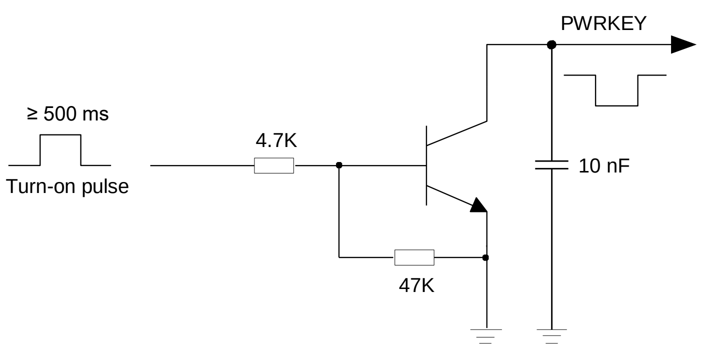


Figure 10: Turn on the Module by Using Driving Circuit

The other way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from the finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

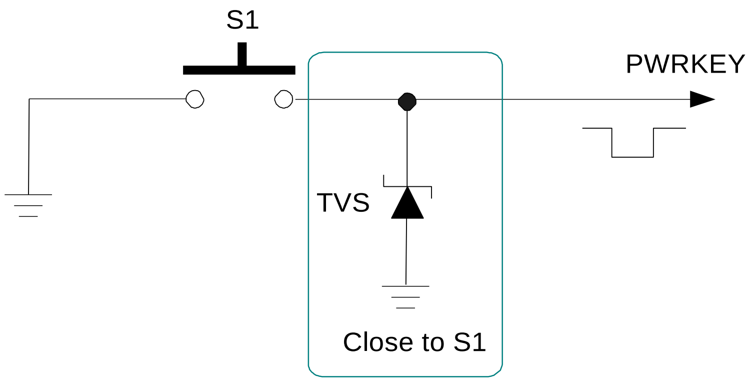


Figure 11: Turn on the Module by Using Keystroke

The power-on scenario is illustrated in the following figure.

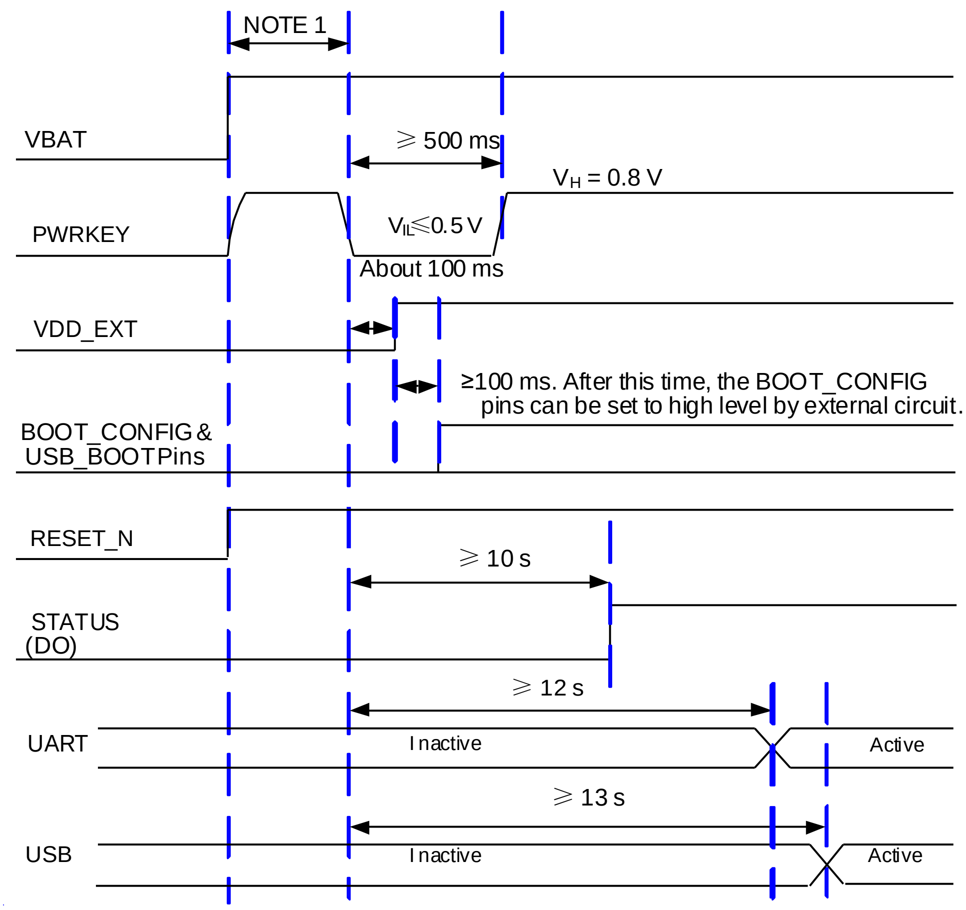


Figure 12: Timing of Turning on Module

NOTES

1. Please make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30ms.
2. PWRKEY can be pulled down directly to GND with a recommended 10 kΩ resistor if module needs to be powered on automatically and shutdown is not needed.

3.7.2. Turn off Module

The following procedures can be used to turn off the module normally:

- Use the PWRKEY pin.
- Use **AT+QPOWD** command.

3.7.2.1. Turn off Module Using the PWRKEY Pin

Driving the PWRKEY pin to a low level voltage for at least 650ms, the module will execute power-off procedure after the PWRKEY is released. The power-off scenario is illustrated in the following figure.

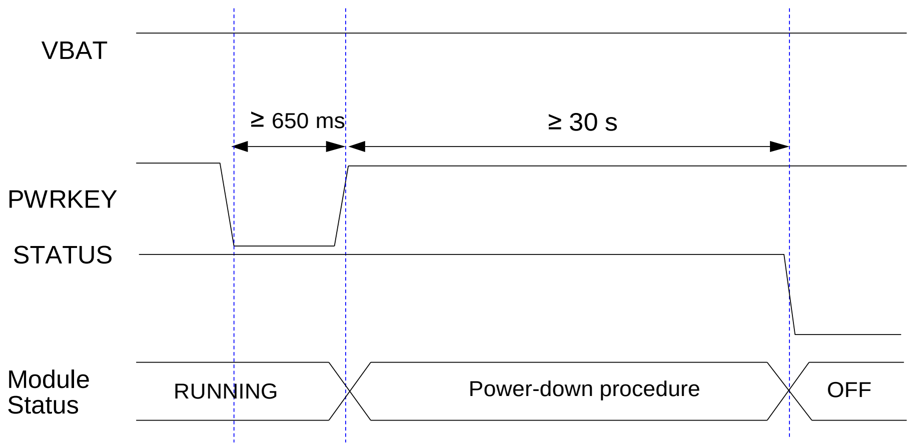


Figure 13: Timing of Turning off Module

3.7.2.2. Turn off Module Using AT Command

It is also a safe way to use **AT+QPOWD** command to turn off the module, which is similar to turning off the module via PWRKEY pin.

Please refer to ***document [2]*** for details about the **AT+QPOWD** command.

NOTES

1. In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.
2. When turning off module with the AT command, please keep PWRKEY at high level after the execution of the command. Otherwise the module will be turned on again after successfully turn-off.

3.8. Reset the Module

The RESET_N pin can be used to reset the module. The module can be reset by driving RESET_N to a low level voltage for 150–460 ms.

Table 8: Pin Definition of RESET_N

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET_N	17	Reset the module	V_{IH}max = 2.1V V_{IH}min = 1.3V V_{IL}max = 0.5V	

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

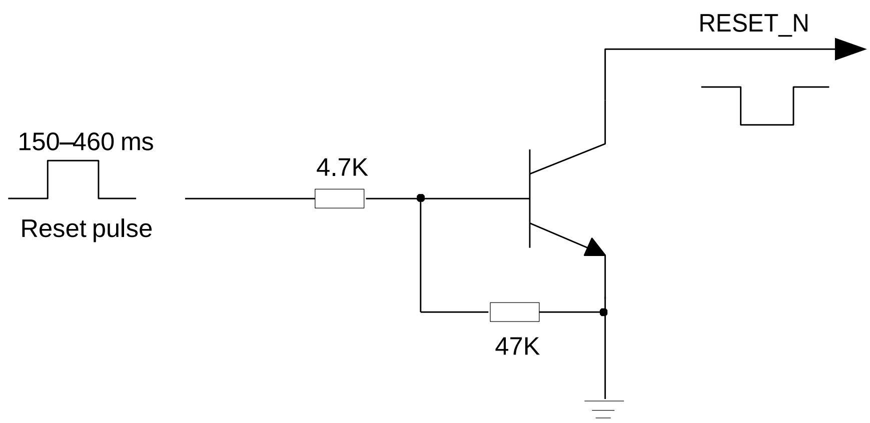


Figure 14: Reference Circuit of RESET_N by Using Driving Circuit

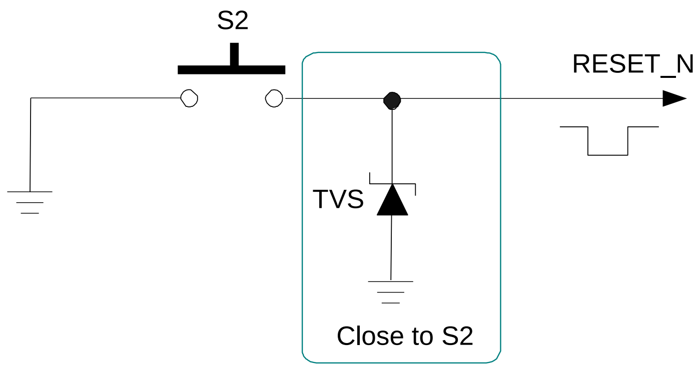


Figure 15: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the following figure.

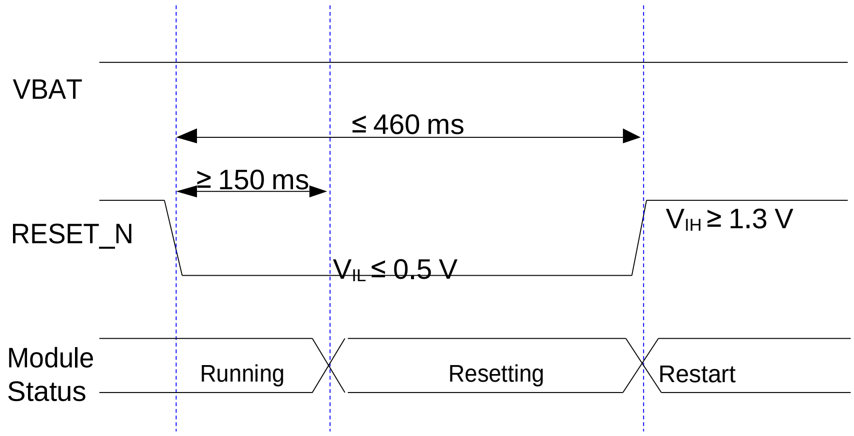


Figure 16: Timing of Resetting Module

NOTES

1. Use RESET_N only when failed to turn off the module by **AT+QPOWD** command and PWRKEY pin.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

3.9. (U)SIM Interfaces

EG95 provides two (U)SIM interfaces, and only one (U)SIM card can work at a time. The (U)SIM 1 and (U)SIM 2 cards can be switched by **AT+QDSIM** command. For more details, please refer to ***document [2]***.

The (U)SIM interfaces circuitry meet ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported.

Table 9: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	43	PO	Power supply for (U)SIM1 card	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	45	IO	Data signal of (U)SIM1 card	
USIM1_CLK	46	DO	Clock signal of (U)SIM1 card	
USIM1_RST	44	DO	Reset signal of (U)SIM1 card	
USIM1_ PRESENCE	42	DI	(U)SIM1 card insertion detection	
USIM_GND	47		Specified ground for (U)SIM card	
USIM2_VDD	87	PO	Power supply for (U)SIM2 card	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM2_DATA	86	IO	Data signal of (U)SIM2 card	
USIM2_CLK	84	DO	Clock signal of (U)SIM2 card	
USIM2_RST	85	DO	Reset signal of (U)SIM2 card	
USIM2_ PRESENCE	83	DI	(U)SIM2 card insertion detection	

EG95 supports (U)SIM card hot-plug via USIM_PRESENCE (USIM1_PRESENCE/USIM2_PRESENCE) pin. The function supports low level and high level detections. By default, it is disabled, and can be configured via **AT+QSIMDET** command. Please refer to ***document [2]*** for more details about the command.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

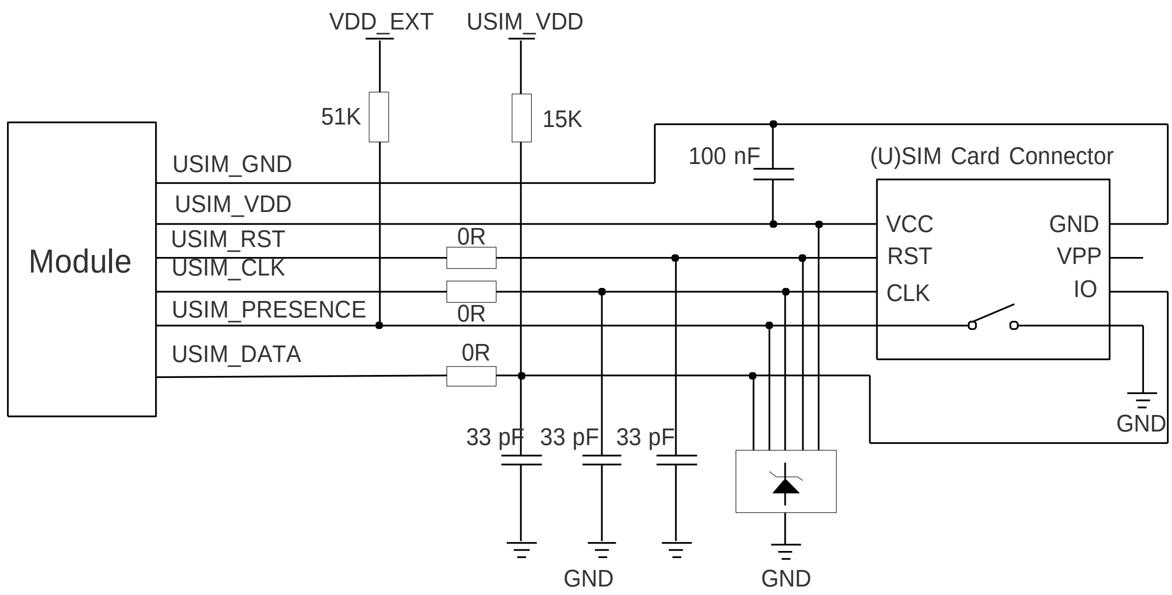


Figure 17: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_PRESENCE unconnected. A reference circuit of (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

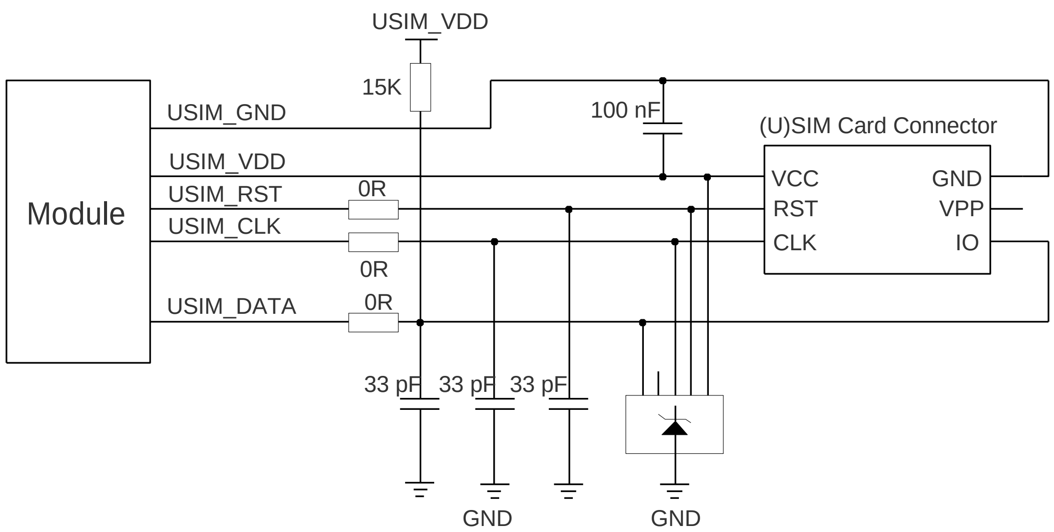


Figure 18: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM cards in customers' applications, please follow the criteria below in the (U)SIM circuit design:

- Keep placement of (U)SIM card connector to the module as close as possible. Keep the trace length as less than 200mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Make sure the bypass capacitor between USIM_VDD and USIM_GND less than 1 μF, and place it as

close to (U)SIM card connector as possible. If the ground is complete on customers' PCB, USIM_GND can be connected to PCB ground directly.

- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not be more than 15 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors are used for filtering interference of EGSM900. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

3.10. USB Interface

EG95 contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480 Mbps) and full-speed (12 Mbps) modes. The USB interface can only serves as a slave device and is used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB. The following table shows the pin definition of USB interface.

Table 10: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	9	IO	USB differential data bus (+)	Require differential impedance of 90 Ω.
USB_DM	10	IO	USB differential data bus (-)	Require differential impedance of 90 Ω.
USB_VBUS	8	PI	USB connection detection	Typical: 5.0 V
GND	3		Ground	

For more details about USB 2.0 specifications, please visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade in customers' design. The following figure shows a reference circuit of USB interface.

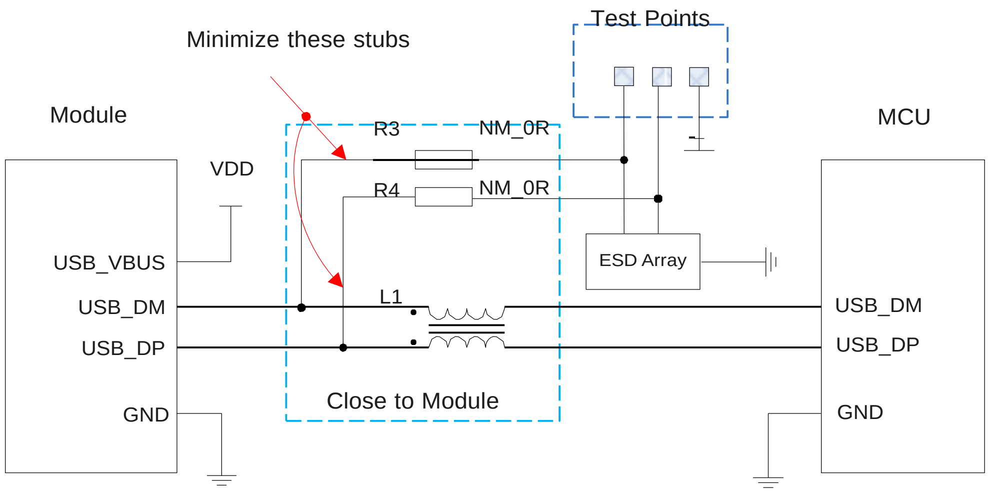


Figure 19: Reference Circuit of USB Interface

A common mode choke L1 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are

not mounted by default. In order to ensure the integrity of USB data line signal, L1/R3/R4 components must be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with when design the USB interface, so as to meet USB 2.0 specification.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Junction capacitance of the ESD protection component might cause influences on USB data lines, so please pay attention to the selection of the component. Typically, the stray capacitance should be less than 2 pF.
- Keep the ESD protection components to the USB connector as close as possible.

3.11. UART Interfaces

The module provides two UART interfaces: the main UART interface and the debug UART interface. The following shows their features.

- The main UART interface supports 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps and 3000000 bps baud rates, and the default is 115200 bps. It supports RTS and CTS hardware flow control, and is used for AT command communication and data transmission.
- The debug UART interface supports 115200 bps baud rate. It is used for Linux console and log output.

The following tables show the pin definition of the UART interfaces.

Table 11: Pin Definition of Main UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
RI	39	DO	Ring indicator	1.8 V power domain
DCD	38	DO	Data carrier detection	
CTS	36	DO	Clear to send	
RTS	37	DI	Request to send	
DTR	30	DI	Data terminal ready, sleep mode control	
TXD	35	DO	Transmit data	
RXD	34	DI	Receive data	

Table 12: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	23	DO	Transmit data	1.8 V power domain
DBG_RXD	22	DI	Receive data	1.8 V power domain

The logic levels are described in the following table.

Table 13: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V

V_{IH}	1.2	2.0	V

V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The module provides 1.8 V UART interfaces. A level translator should be used if customers' application is equipped with a 3.3V UART interface. A level translator TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure shows a reference design.

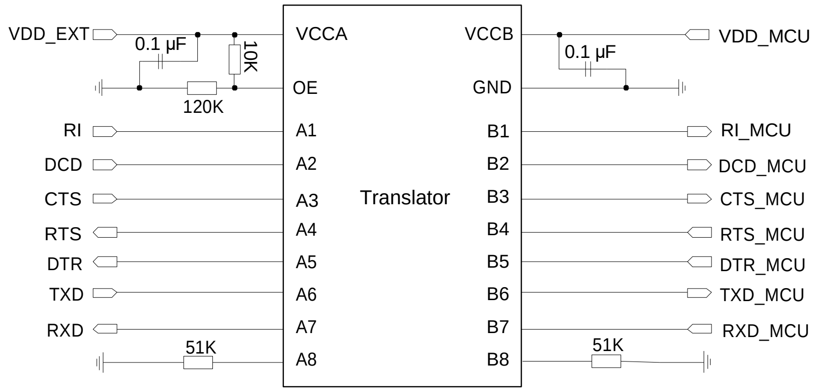


Figure 20: Reference Circuit with Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. For the design of circuits in dotted lines, please refer to that of circuits in solid lines, but please pay attention to the direction of connection.

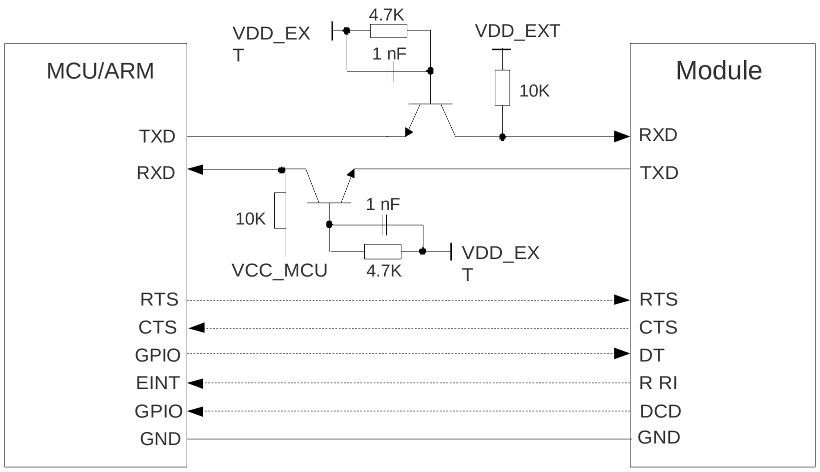


Figure 21: Reference Circuit with Transistor Circuit

NOTE

Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.

3.12. PCM and I2C Interfaces

EG95 provides one Pulse Code Modulation (PCM) digital interface for audio design, which supports the following modes and one I2C interface:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In auxiliary mode, the data is also sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with a 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK and an 8 kHz, 50% duty cycle PCM_SYNC.

EG95 supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

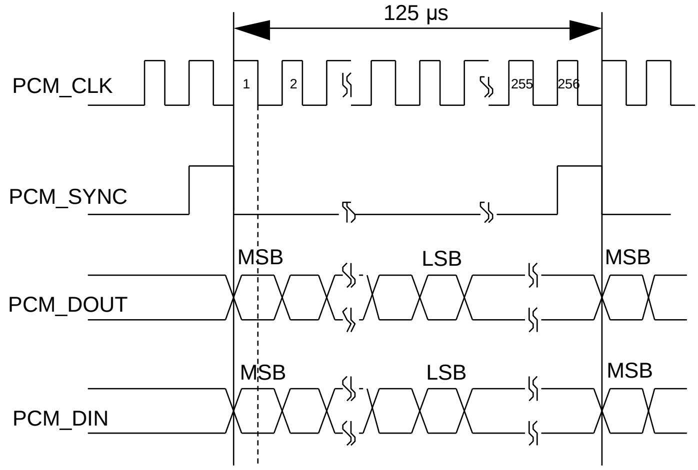


Figure 22: Primary Mode Timing

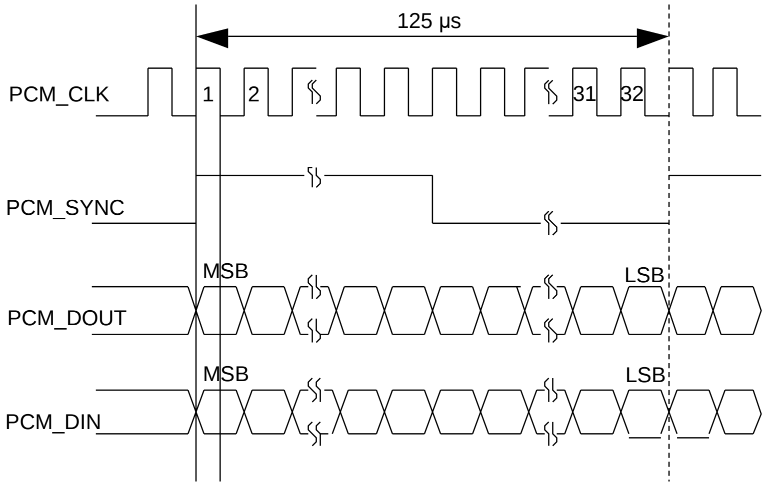


Figure 23: Auxiliary Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 14: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	6	DI	PCM data input	1.8 V power domain
PCM_DOUT	7	DO	PCM data output	1.8 V power domain
PCM_SYNC	5	IO	PCM data frame synchronization signal	1.8 V power domain
PCM_CLK	4	IO	PCM data bit clock	1.8 V power domain
I2C_SCL	40	OD	I2C serial clock	An external pull-up to 1.8 V is required.
I2C_SDA	41	OD	I2C serial data	An external pull-up to 1.8 V is required.

Clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. Please refer to ***document [2]*** about **AT+QDAI** command for details.

The following figure shows a reference design of PCM and I2C interfaces with external codec IC.

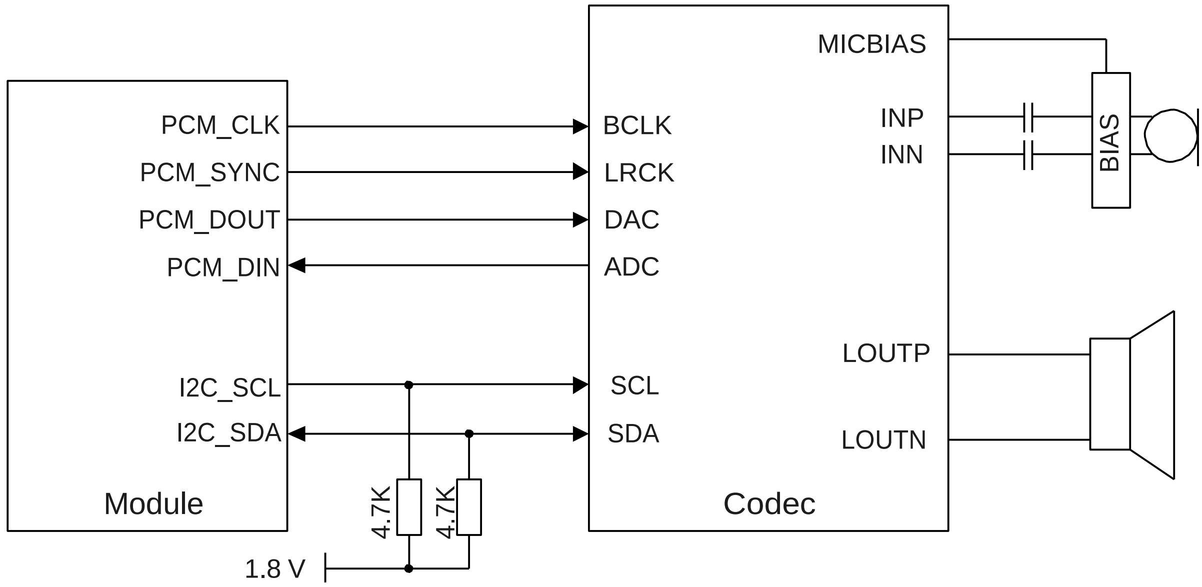


Figure 24: Reference Circuit of PCM and I2C Application with Audio Codec

NOTES

1. It is recommended to reserve an RC (R = 22 Ω, C = 22 pF) circuit on the PCM lines, especially for PCM_CLK.
2. EG95 works as a master device pertaining to I2C interface.

3.13. SPI Interface

SPI interface of EG95 acts as the master only. It provides a duplex, synchronous and serial communication link with the peripheral devices. It is dedicated to one-to-one connection, without chip select. Its operation voltage is 1.8 V with clock rates up to 50 MHz.

The following table shows the pin definition of SPI interface.

Table 15: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	26	DO	Clock signal of SPI interface	1.8 V power domain
SPI_MOSI	27	DO	Master output slave input of SPI interface	1.8 V power domain

SPI_MISO	28	DI	Master input slave output of SPI interface	1.8 V power domain

The following figure shows a reference design of SPI interface with peripherals.

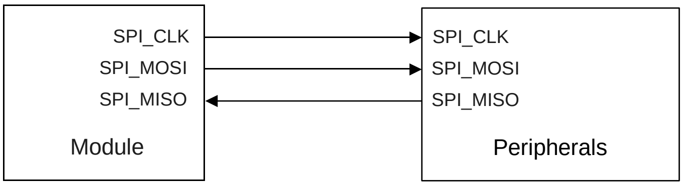


Figure 25: Reference Circuit of SPI Interface with Peripherals

NOTE

The module provides 1.8 V SPI interface. A level translator should be used between the module and the host if customer's application is equipped with a 3.3V processor or device interface.

3.14. Network Status Indication

The module provides one network indication pin: NETLIGHT. The pin is used to drive a network status indication LED.

The following tables describe the pin definition and logic level changes of NETLIGHT in different network status.

Table 16: Pin Definition of Network Status Indicator

Pin Name	Pin No.	I/O	Description	Comment
NETLIGHT	21	DO	Indicate the module's network activity status	1.8 V power domain

Table 17: Working State of Network Status Indicator

Pin Name	Logic Level Changes	Network Status
NETLIGHT	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle

	Flicker quickly (125 ms High/125 ms Low)	Data transfer is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

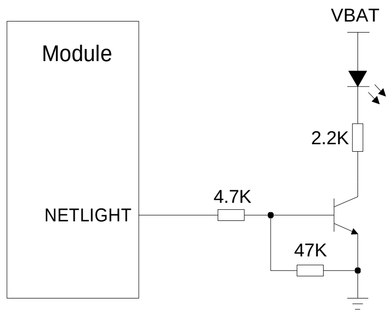


Figure 26: Reference Circuit of Network Status Indicator

3.15. STATUS

The STATUS pin is set as the module's operation status indicator. It will output high level when the module is powered on. The following table describes the pin definition of STATUS.

Table 18: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module's operation status	1.8 V power domain. If unused, keep it open.

The following figure shows the reference circuit of STATUS.

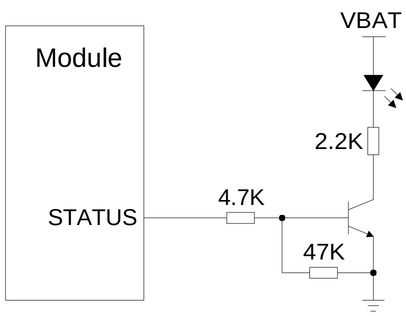


Figure 27: Reference Circuit of STATUS

3.16. ADC Interface

The module provides one analog-to-digital converter (ADC) interface. **AT+QADC=0** command can be used to read the voltage value on ADC0 pin. For more details about the command, please refer to ***document [2]***.

In order to improve the accuracy of ADC voltage values, the traces of ADC should be surrounded by ground.

Table 19: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	Force the module to enter emergency download mode	If unused, keep this pin open.

The following table describes the characteristics of ADC interface.

Table 20: Characteristics of ADC Interface

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0.3		VBAT_BB	V
ADC Resolution			15	bits

NOTES

1. It is prohibited to supply any voltage to ADC pins when ADC pins are not powered by VBAT.
2. It is recommended to use resistor divider circuit for ADC application.

3.17. Behaviors of RI

AT+QCFG="risignaltype","physical" command can be used to configure RI behaviors. Please refer to ***document [2]*** for details.

No matter on which port URC is presented, URC will trigger the behavior of RI pin.

NOTE

URC can be outputted from UART port, USB AT port and USB modem port through configuration via **AT+QURCCFG** command. The default port is USB AT port.

The default behaviors of the RI are shown as below, and can be changed by **AT+QCFG="urc/ri/ring"** command. Please refer to ***document [2]*** for details.

Table 21: Default Behaviors of RI

State	Response
Idle	RI keeps at high level
URC	RI outputs 120ms low pulse when a new URC returns

3.18. USB_BOOT Interface

EG95 provides a USB_BOOT pin. Customers can pull up USB_BOOT to 1.8 V before VDD_EXT is powered up, and the module will enter emergency download mode when it is powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 22: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module to enter emergency download mode	1.8 V power domain. Active high. It is recommended to reserve test points.

The following figures show the reference circuit of USB_BOOT interface and timing sequence of entering emergency download mode.

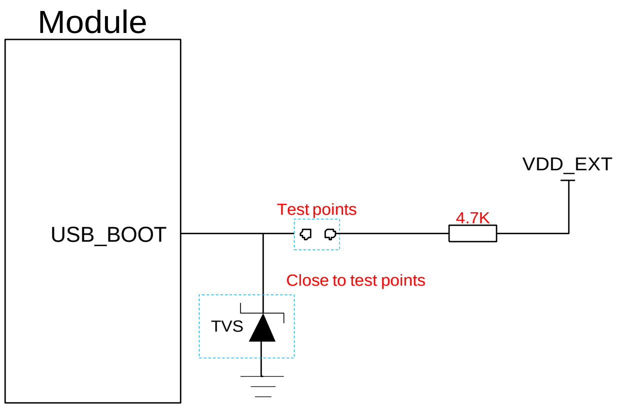


Figure 28: Reference Circuit of USB_BOOT Interface

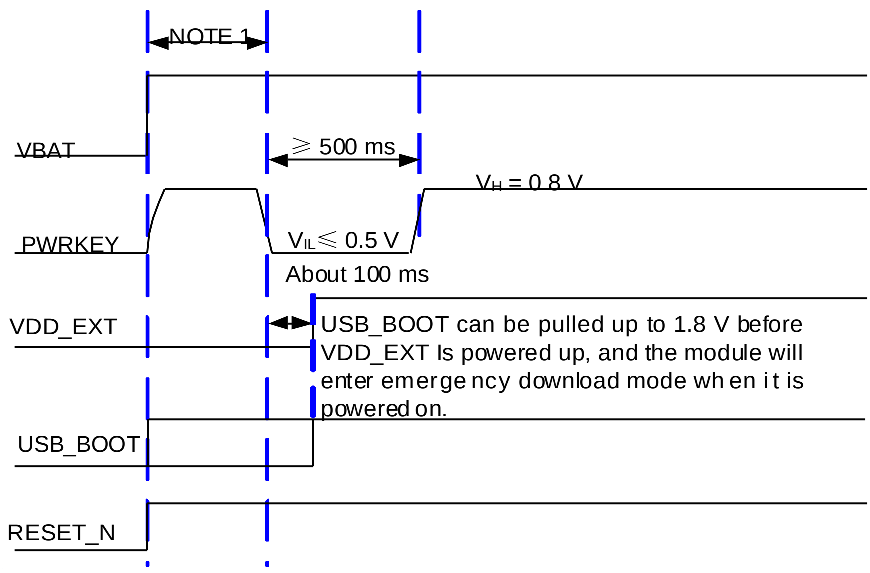


Figure 29: Timing Sequence for Entering Emergency Download Mode

NOTES

1. Please make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.
2. When using MCU to control module to enter the emergency download mode, please follow the above timing sequence. It is not recommended to pull up USB_BOOT to 1.8 V before powering up VBAT. Connect the test points as shown in ***Figure 28*** can manually force the module to enter download mode.

4 GNSS Receiver

4.1. General Description

EG95 includes a fully integrated global navigation satellite system solution that supports Gen8C-Lite of Qualcomm (GPS, GLONASS, BeiDou, Galileo and QZSS).

EG95 supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

By default, EG95 GNSS engine is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, please refer to ***document [3]***.

4.2. GNSS Performance

The following table shows GNSS performance of EG95.

Table 23: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-146	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-157	dBm
TTFF (GNSS)	Cold start @ open sky	Autonomous	34.6	s
		XTRA enabled	11.57	s
	Warm start @ open sky	Autonomous	26.09	s
		XTRA enabled	3.7	s
	Hot start	Autonomous	1.8	s

	@ open sky	XTRA enabled	3.4	s
Accuracy (GNSS)	CEP-50	Autonomous @ open sky	<2.5	m

NOTES

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Cold start sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in customers' design.

- Maximize the distance among GNSS antenna, main antenna and Rx-diversity antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module and display connector should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50 Ω characteristic impedance for the ANT_GNSS trace.

Please refer to ***Chapter 5*** for GNSS antenna reference design and antenna installation information.

5 Antenna Interfaces

EG95 antenna interfaces include a main antenna interface and an Rx-diversity antenna interface which is used to resist the fall of signals caused by high speed movement and multipath effect, and a GNSS antenna interface which is only supported on EG95-NA/-EX/-NAX/-AUX. The impedance of the antenna ports is 50 Ω.

5.1. Main/Rx-diversity Antenna Interfaces

5.1.1. Pin Definition

The pin definition of main antenna and Rx-diversity antenna interfaces is shown below.

Table 24: Pin Definition of RF Antennas

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	IO	Main antenna pad	50 Ω impedance
ANT_DIV (EG95-E)	49	AI	Receive diversity antenna pad	50 Ω impedance
ANT_DIV (EG95-NA/-EX/-NAX/-AUX)	56	AI	Receive diversity antenna pad	50 Ω impedance

5.1.2. Operating Frequency

Table 25: Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
GSM850	824~849	869~894	MHz
EGSM900	880~915	925~960	MHz
DCS1800	1710~1785	1805~1880	MHz
PCS1900	1850~1910	1930~1990	MHz

WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B2	1850–1910	1930–1990	MHz
WCDMA B4	1710–1755	2110–2155	MHz
WCDMA B5	824–849	869–894	MHz
WCDMA B8	880–915	925–960	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B2	1850–1910	1930–1990	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B4	1710–1755	2110–2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B12	699–716	729–746	MHz
LTE-FDD B13	777–787	746–756	MHz
LTE-FDD B20	832–862	791–821	MHz
LTE-FDD B25	1850–1915	1930–1995	MHz
LTE-FDD B26	814–849	859–894	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-FDD B66	1710~1780	2100~2200	MHz

5.1.3. Reference Design of RF Antenna Interface

A reference design of ANT_MAIN and ANT_DIV antenna pads is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

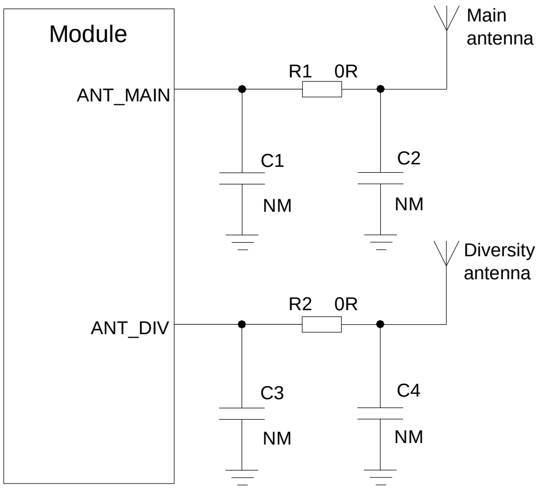


Figure 30: Reference Circuit of RF Antenna Interface

NOTES

1. Keep a proper distance between the main antenna and the Rx-diversity antenna to improve the receiving sensitivity.
2. ANT_DIV function is enabled by default. **AT+QCFG="divctl",0** command can be used to disable receive diversity. Please refer to ***document [2]*** for details.
3. Place the π-type matching components (R1&C1&C2, R2&C3&C4) as close to the antenna as possible.

5.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

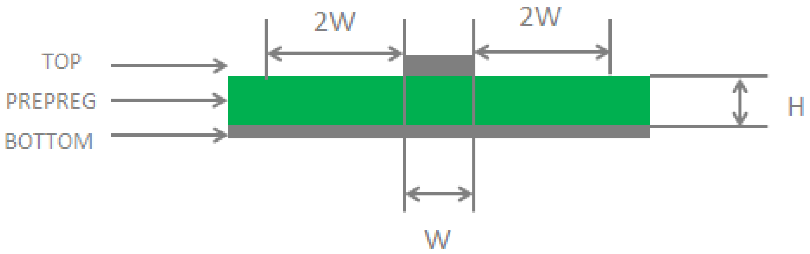


Figure 31: Microstrip Design on a 2-layer PCB

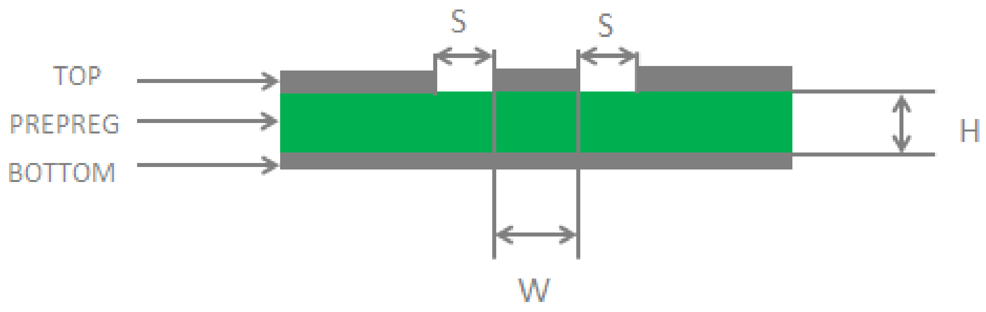


Figure 32: Coplanar Waveguide Design on a 2-layer PCB

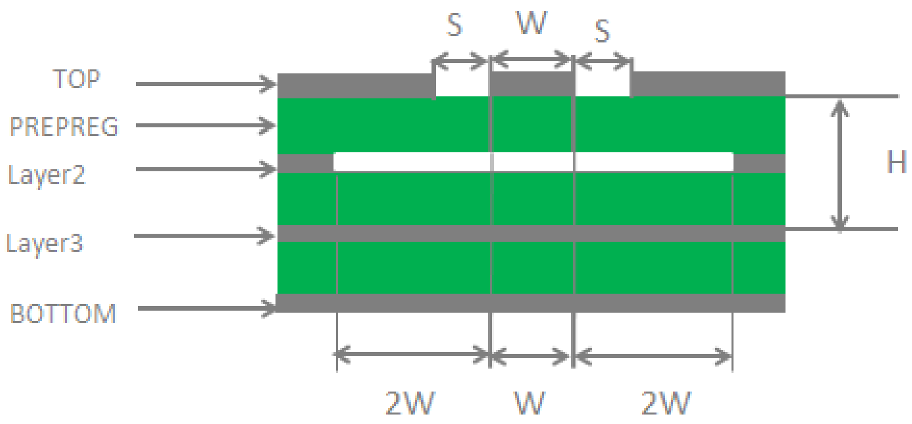


Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

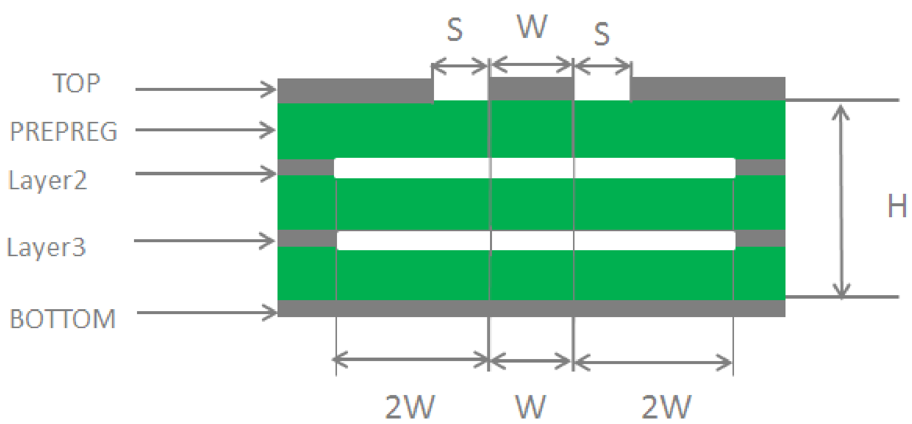


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 x W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, please refer to ***document [5]***.

5.2. GNSS Antenna Interface

The GNSS antenna interface is only supported on EG95-NA/-EX/-NAX/-AUX.The following tables show pin definition and frequency specification of GNSS antenna interface.

Table 26: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS (EG95-NA/-EX/-NAX/-AUX)	49	AI	GNSS antenna	50 Ω impedance

Table 27: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BeiDou (Compass)	1561.098 ±2.046	MHz

QZSS	1575.42	MHz

A reference design of GNSS antenna is shown as below.

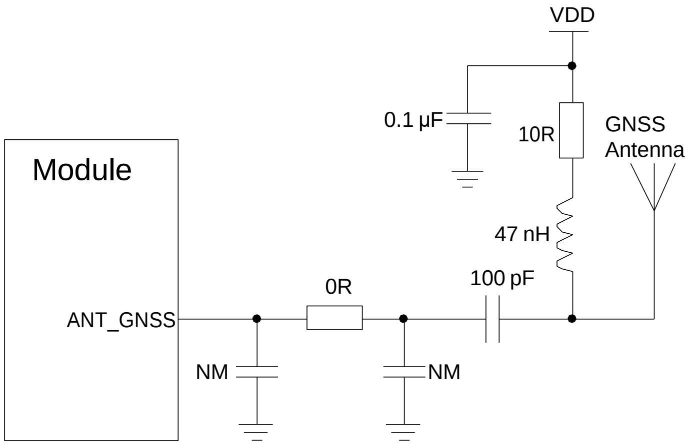


Figure 35: Reference Circuit of GNSS Antenna

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. Antenna Installation

5.3.1. Antenna Requirement

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 28: Antenna Requirements

Type	Requirements
GNSS 1)	Frequency range: 1559–1609 MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0 dBi Active antenna noise figure: < 1.5 dB Active antenna gain: > 0 dBi

	Active antenna embedded LNA gain: < 17 dB
GSM/WCDMA/LTE	VSWR: ≤ 2 Efficiency: > 30% Max input power: 50 W Input impedance: 50 Ω Cable insertion loss: < 1 dB (GSM850,EGSM900, WCDMA B5/B8, LTE-FDD B5/B8/B12/B13/B20/B26/B28) Cable insertion loss: < 1.5 dB (DCS1800, PCS1900,WCDMA B1/B2/B4, LTE-FDD B1/B2/B3/B4/B25/B66) Cable insertion loss: < 2 dB (LTE- FDD B7)

NOTE

[1)] It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.3.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by *Hirose*.

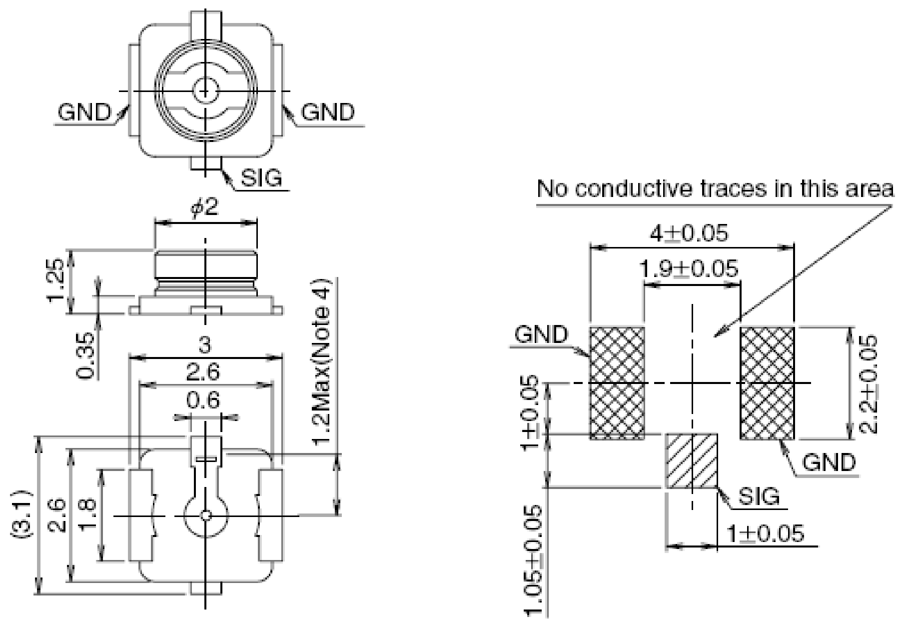


Figure 36: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

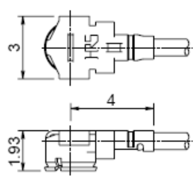
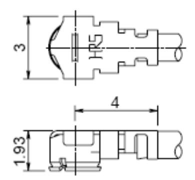
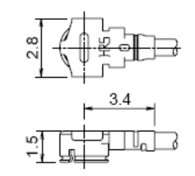
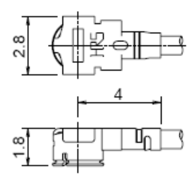
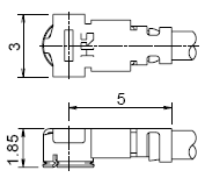
	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Part No.					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 37: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

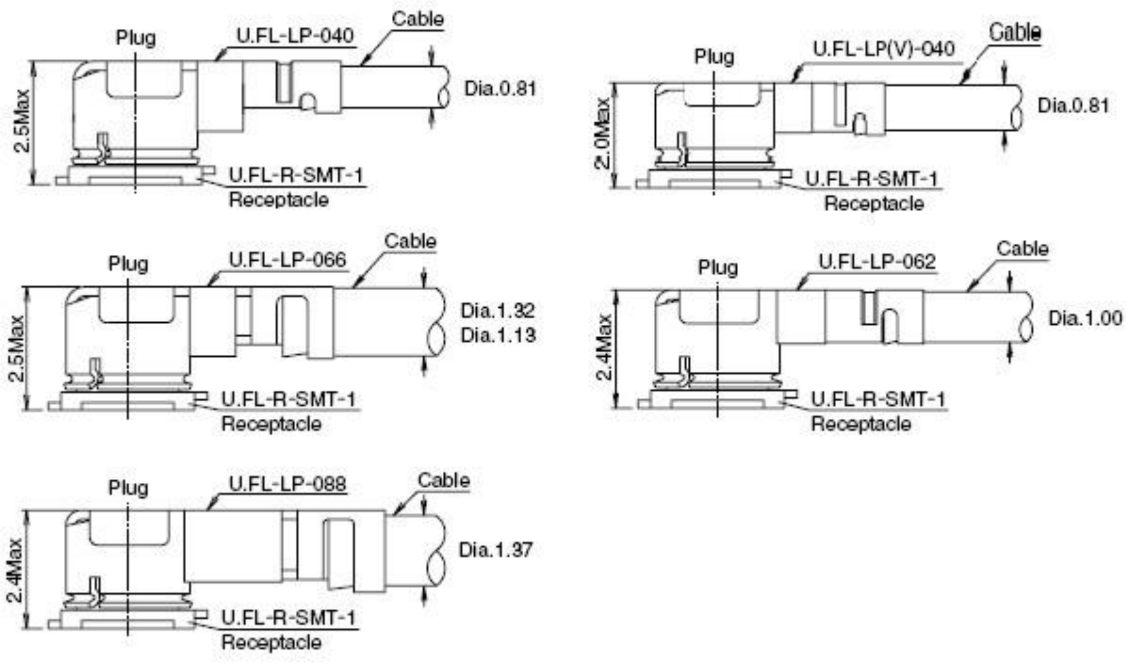


Figure 38: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://www.hirose.com.

6 Electrical, Reliability and Radio Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 29: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	0.8	A
Peak Current of VBAT_RF	0	1.8	A
Voltage at Digital Pins	-0.3	2.3	V

6.2. Power Supply Ratings

Table 30: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V

	Voltage drop during burst transmission	Maximum power control level on EGSM900			400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on EGSM900		1.8	2.0	A
USB_VBUS	USB connection detection		3.0	5.0	5.25	V

6.3. Operation and Storage Temperatures

The operation and storage temperatures are listed in the following table.

Table 31: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range 1)	-35	+25	+75	ºC
Extended Temperature Range 2)	-40		+85	ºC
Storage Temperature Range	-40		+90	ºC

1. 1) Within operation temperature range, the module is 3GPP compliant.
2. 2) Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call*, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like Pout might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operation temperature levels, the module will meet 3GPP specifications again.
3. "*" means under development.

6.4. Current Consumption

The values of current consumption are shown below.

Table 32: EG95-E Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	15	μA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.3	mA
		GSM DRX = 2 (USB disconnected)	2.3	mA
		GSM DRX = 5 (USB suspended)	2.0	mA
		GSM DRX = 9 (USB disconnected)	1.6	mA
		WCDMA PF = 64 (USB disconnected)	1.8	mA
		WCDMA PF = 64 (USB suspended)	2.1	mA
		WCDMA PF = 512 (USB disconnected)	1.3	mA
		LTE-FDD PF = 64 (USB disconnected)	2.3	mA
		LTE-FDD PF = 64 (USB suspended)	2.6	mA
		LTE-FDD PF = 256 (USB disconnected)	1.5	mA
	Idle state	GSM DRX = 5 (USB disconnected)	21.0	mA
		GSM DRX = 5 (USB connected)	31.0	mA
		WCDMA PF = 64 (USB disconnected)	21.0	mA
		WCDMA PF = 64 (USB connected)	31.0	mA
		LTE-FDD PF = 64 (USB disconnected)	21.0	mA
		LTE-FDD PF = 64 (USB connected)	31.0	mA
	GPRS data	EGSM900 4DL/1UL @ 32.35 dBm	268	mA
		EGSM900 3DL/2UL @ 32.16 dBm	[illegible]	mA

		EGSM900 1DL/4UL @ 29.45 dBm	631	mA
		DCS1800 4DL/1UL @ 29.14 dBm	177	mA
		DCS1800 3DL/2UL @ 29.07 dBm	290	mA
		DCS1800 2DL/3UL @ 28.97 dBm	406	mA
		DCS1800 1DL/4UL @ 28.88 dBm	517	mA
	EDGE data transfer	EGSM900 4DL/1UL PCL = 8 @ 26.88 dBm	167	mA
		EGSM900 3DL/2UL PCL = 8 @ 26.84 dBm	278	mA
		EGSM900 2DL/3UL PCL = 8 @ 26.76 dBm	385	mA
		EGSM900 1DL/4UL PCL = 8 @ 26.54 dBm	492	mA
		DCS1800 4DL/1UL PCL = 2 @ 25.66 dBm	169	mA
		DCS1800 3DL/2UL PCL = 2 @ 25.59 dBm	256	mA
		DCS1800 2DL/3UL PCL = 2 @ 25.51 dBm	341	mA
		DCS1800 1DL/4UL PCL = 2 @ 25.38 dBm	432	mA
	WCDMA data transfer	WCDMA B1 HSDPA @ 22.48 dBm	586	mA
		WCDMA B1 HSUPA @ 22.29 dBm	591	mA
		WCDMA B8 HSDPA @ 22.24 dBm	498	mA
		WCDMA B8 HSUPA @ 21.99 dBm	511	mA
	LTE data transfer	LTE-FDD B1 @ 23.37 dBm	736	mA
		LTE-FDD B3 @ 22.97 dBm	710	mA
		LTE-FDD B7 @ 23.17 dBm	775	mA
		LTE-FDD B8 @ 23.04 dBm	651	mA
		LTE-FDD B20 @ 23.21 dBm	699	mA
		LTE-FDD B28A @ 22.76 dBm	714	mA
	GSM voice call	EGSM900 PCL = 5 @ 32.36 dBm	271	mA
		DCS1800 PCL = 0 @ 29.19 dBm	181	mA

	WCDMA voice call	WCDMA B1 @ 22.91 dBm	632	mA
		WCDMA B8 @ 23.14 dBm	546	mA

Table 33: EG95-NA Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	13	μA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.0	mA
		WCDMA PF = 64 (USB disconnected)	2.2	mA
		WCDMA PF = 64 (USB suspended)	2.5	mA
		WCDMA PF = 512 (USB disconnected)	1.4	mA
		LTE-FDD PF = 64 (USB disconnected)	2.6	mA
		LTE-FDD PF = 64 (USB suspended)	2.9	mA
		LTE-FDD PF = 256 (USB disconnected)	1.7	mA
	Idle state	WCDMA PF = 64 (USB disconnected)	14.0	mA
		WCDMA PF = 64 (USB connected)	26.0	mA
		LTE-FDD PF = 64 (USB disconnected)	15.0	mA
		LTE-FDD PF = 64 (USB connected)	26.0	mA
	WCDMA data transfer	WCDMA B2 HSDPA CH9938 @ 22.45 dBm	569	mA
		WCDMA B2 HSUPA CH9938 @ 21.73 dBm	559	mA
		WCDMA B4 HSDPA CH1537 @ 23.05 dBm	572	mA
		WCDMA B4 HSUPA CH1537 @ 22.86 dBm	586	mA
		WCDMA B5 HSDPA CH4407 @ 23 dBm	518	mA
		WCDMA B5 HSUPA CH4407 @ 22.88 dBm	514	mA
	LTE data	LTE-FDD B2 CH1100 @ 23.29 dBm	705	mA

		LTE-FDD B5 CH2525 @ 23.39 dBm	601	mA
		LTE-FDD B12 CH5060 @ 23.16 dBm	650	mA
		LTE-FDD B13 CH5230 @ 23.36 dBm	602	mA
	WCDMA voice call	WCDMA B2 CH9938 @ 23.34 dBm	627	mA
		WCDMA B4 CH1537 @ 23.47 dBm	591	mA
		WCDMA B5 CH4357 @ 23.37 dBm	536	mA

Table 34: EG95-EX Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	15	μA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.3	mA
		GSM DRX = 2 (USB disconnected)	2.3	mA
		GSM DRX = 5 (USB suspend)	2.0	mA
		GSM DRX = 9 (USB disconnected)	1.6	mA
		WCDMA PF = 64 (USB disconnected)	1.8	mA
		WCDMA PF = 64 (USB suspend)	2.1	mA
		WCDMA PF = 512 (USB disconnected)	1.3	mA
		LTE-FDD PF = 64 (USB disconnected)	2.3	mA
		LTE-FDD PF = 64 (USB suspend)	2.6	mA
		LTE-FDD PF = 256 (USB disconnected)	1.5	mA
	Idle state	GSM DRX = 5 (USB disconnected)	21.0	mA
		GSM DRX = 5 (USB connected)	31.0	mA
		WCDMA PF = 64 (USB disconnected)	21.0	mA
		WCDMA PF = 64 (USB connected)	31.0	mA
		LTE-FDD PF = 64 (USB disconnected)	21.0	mA

	LTE-FDD PF = 64 (USB connected)	31.0	mA
GPRS data transfer	EGSM900 4DL/1UL @ 33.06 dBm	247.9	mA
	EGSM900 3DL/2UL @ 32.93 dBm	450.8	mA
	EGSM900 2DL/3UL @ 31.1 dBm	536.4	mA
	EGSM900 1DL/4UL @ 29.78 dBm	618	mA
	DCS1800 4DL/1UL @ 29.3 dBm	144	mA
	DCS1800 3DL/2UL @ 29.3 dBm	253.4	mA
	DCS1800 2DL/3UL @ 29.21 dBm	355.4	mA
	DCS1800 1DL/4UL @ 29.07 dBm	455.7	mA
EDGE data transfer	EGSM900 4DL/1UL PCL = 8 @ 27.29 dBm	169.5	mA
	EGSM900 3DL/2UL PCL = 8 @ 27.01 dBm	305.06	mA
	EGSM900 2DL/3UL PCL = 8 @ 26.86 dBm	434	mA
	EGSM900 1DL/4UL PCL = 8 @ 25.95 dBm	548	mA
	DCS1800 4DL/1UL PCL = 2 @ 26.11 dBm	135	mA
	DCS1800 3DL/2UL PCL = 2 @ 25.8 dBm	244	mA
	DCS1800 2DL/3UL PCL = 2 @ 25.7 dBm	349	mA
	DCS1800 1DL/4UL PCL = 2 @ 25.6 dBm	455	mA
WCDMA data transfer	WCDMA B1 HSDPA @ 22.48 dBm	485	mA
	WCDMA B1 HSUPA @ 21.9 dBm	458	mA
	WCDMA B8 HSDPA @ 22.6 dBm	556	mA
	WCDMA B8 HSUPA @ 22.02 dBm	520	mA
LTE data transfer	LTE-FDD B1 @ 23.37 dBm	605	mA
	LTE-FDD B3 @ 23.3 dBm	667	mA
	LTE-FDD B7 @ 23.2 dBm	783	mA
	LTE-FDD B8 @ 23.09 dBm	637	mA

		LTE-FDD B20 @ 23.21 dBm	646	mA
		LTE-FDD B28 @ 22.76 dBm	661	mA
	GSM voice call	EGSM900 PCL = 5 @ 32.36 dBm	259	mA
		DCS1800 PCL = 0 @ 29.5 dBm	149	mA
	WCDMA voice call	WCDMA B1 @ 23.4 dBm	494	mA
		WCDMA B8 @ 23.6 dBm	608	mA

Table 35: EG95-NAX Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	11	μA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.1	mA
		WCDMA PF = 64 (USB disconnected)	2.0	mA
		WCDMA PF = 64 (USB suspend)	2.4	mA
		WCDMA PF = 512 (USB disconnected)	1.5	mA
		LTE-FDD PF = 64 (USB disconnected)	2.6	mA
		LTE-FDD PF = 64 (USB suspend)	2.8	mA
		LTE-FDD PF = 256 (USB disconnected)	1.8	mA
	Idle state	WCDMA PF = 64 (USB disconnected)	17.4	mA
		WCDMA PF = 64 (USB connected)	34.3	mA
		LTE-FDD PF = 64 (USB disconnected)	17.8	mA
		LTE-FDD PF = 64 (USB connected)	34.7	mA
	WCDMA data transfer	WCDMA B2 HSDPA @ 21.64 dBm	547	mA
		WCDMA B2 HSUPA @ 21.13 dBm	543	mA
		WCDMA B4 HSDPA @ 22.15 dBm	554	mA
		WCDMA B4 HSUPA @ 22.21 dBm	541	mA

		WCDMA B5 HSDPA @ 22.39 dBm	502	mA
		WCDMA B5 HSUPA @ 22.12 dBm	509	mA
	LTE data transfer	LTE-FDD B2 @ 23.07 dBm	691	mA
		LTE-FDD B4 @ 23.09 dBm	713	mA
		LTE-FDD B5 @ 23.31 dBm	580	mA
		LTE-FDD B12 @ 23.30 dBm	627	mA
		LTE-FDD B13 @ 23.32 dBm	619	mA
		LTE-FDD B25 @ 23.03 dBm	693	mA
		LTE-FDD B26 @ 22.97 dBm	628	mA
	WCDMA voice call	WCDMA B2 @ 22.89 dBm	591	mA
		WCDMA B4 @ 22.76 dBm	577	mA
		WCDMA B5 @ 23.03 dBm	516	mA

Table 36: EG95-AUX Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	10	μA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.2	mA
		GSM DRX = 2 (USB disconnected)	2.3	mA
		GSM DRX = 5 (USB suspend)	2.0	mA
		GSM DRX = 9 (USB disconnected)	1.5	mA
		WCDMA PF = 64 (USB disconnected)	1.8	mA
		WCDMA PF = 64 (USB suspend)	2.1	mA
		WCDMA PF = 512 (USB disconnected)	1.3	mA
		LTE-FDD PF = 64 (USB disconnected)	2.3	mA

	LTE-FDD PF = 64 (USB suspend)	2.6	mA

	LTE-FDD PF = 256 (USB disconnected)	1.5	mA
Idle state	GSM DRX = 5 (USB disconnected)	18	mA
	GSM DRX = 5 (USB connected)	28	mA
	WCDMA PF = 64 (USB disconnected)	18	mA
	WCDMA PF = 64 (USB connected)	28	mA
	LTE-FDD PF = 64 (USB disconnected)	18	mA
	LTE-FDD PF = 64 (USB connected)	29	mA
GPRS data transfer	GSM850 4DL/1UL @ 32.48 dBm	217.9	mA
	GSM850 3DL/2UL @ 31.89dBm	372.3	mA
	GSM850 2DL/3UL @ 29.45 dBm	432.9	mA
	GSM850 1DL/4UL @ 28.31 dBm	513.9	mA
	EGSM900 4DL/1UL @ 33.17 dBm	235.1	mA
	EGSM900 3DL/2UL @ 32.16 dBm	387.7	mA
	EGSM900 2DL/3UL @ 29.77 dBm	446.5	mA
	EGSM900 1DL/4UL @ 28.59 dBm	540.0	mA
	DCS1800 4DL/1UL @ 30.19 dBm	154.4	mA
	DCS1800 3DL/2UL @ 29.23 dBm	258.0	mA
	DCS1800 2DL/3UL @ 27.19 dBm	332.4	mA
	DCS1800 1DL/4UL @ 26.14 dBm	419.1	mA
	PCS1900 4DL/1UL @ 30.22 dBm	155.0	mA
	PCS1900 3DL/2UL @ 29.48 dBm	259.5	mA
	PCS1900 2DL/3UL @ 27.50 dBm	333.1	mA
	PCS1900 1DL/4UL @ 26.44 dBm	416.8	mA
EDGE data transfer	GSM850 4DL/1UL PCL = 8 @ 25.75 dBm	161.8	mA
	GSM850 3DL/2UL PCL = 8 @ 25.49 dBm	291.8	mA

		GSM850 2DL/3UL PCL = 8 @ 23.26 dBm	410.2	mA
		GSM850 1DL/4UL PCL = 8 @ 22.01 dBm	520.5	mA
		EGSM900 4DL/1UL PCL = 8 @ 26.04 dBm	161.5	mA
		EGSM900 3DL/2UL PCL = 8 @ 25.86 dBm	294.6	mA
		EGSM900 2DL/3UL PCL = 8 @ 23.62 dBm	411.4	mA
		EGSM900 1DL/4UL PCL = 8 @ 22.27 dBm	520.8	mA
		DCS1800 4DL/1UL PCL = 2 @ 26.12 dBm	139.4	mA
		DCS1800 3DL/2UL PCL = 2 @ 25.02 dBm	250.7	mA
		DCS1800 2DL/3UL PCL = 2 @ 22.75 dBm	355.3	mA
		DCS1800 1DL/4UL PCL = 2 @ 21.47 dBm	452.1	mA
		PCS1900 4DL/1UL PCL = 2 @ 26.36 dBm	138.3	mA
		PCS1900 3DL/2UL PCL = 2 @ 25.2 dBm	248.2	mA
		PCS1900 2DL/3UL PCL = 2 @ 22.94 dBm	351.5	mA
		PCS1900 1DL/4UL PCL = 2 @ 21.67 dBm	448.8	mA
	WCDMA data transfer	WCDMA B1 HSDPA @ 22.30 dBm	609.6	mA
		WCDMA B1 HSUPA @ 21.50 dBm	640.5	mA
		WCDMA B2 HSDPA @ 22.14 dBm	557.4	mA
		WCDMA B2 HSUPA @ 21.18 dBm	539.4	mA
		WCDMA B5 HSDPA @ 22.6 dBm	588.2	mA
		WCDMA B5 HSUPA @ 21.45 dBm	545.2	mA
		WCDMA B8 HSDPA @ 21.92 dBm	578.1	mA
		WCDMA B8 HSUPA @ 21.93 dBm	592.5	mA
	LTE data transfer	LTE-FDD B1 @ 22.96 dBm	777.4	mA
		LTE-FDD B2 @ 22.79 dBm	634.4	mA
		LTE-FDD B3 @ 23.09 dBm	697.9	mA

		LTE-FDD B4 @ 22.83 dBm	704.6	mA
		LTE-FDD B5 @ 23.05 dBm	657.1	mA
		LTE-FDD B7 @ 22.71 dBm	765.3	mA
		LTE-FDD B8 @ 22.80 dBm	635.3	mA
		LTE-FDD B28 @ 22.84 dBm	670.0	mA
		LTE-FDD B66 @ 22.73 dBm	725.9	mA
	GSM voice call	GSM850 PCL5 @32.57dBm	227.8	mA
		EGSM900 PCL5 @33.21dBm	253.8	mA
		DCS1800 PCL0 @30.24dBm	168.0	mA
		PCS1900 PCL0 @30.33dBm	166.8	mA
	WCDMA voice call	WCDMA B1 @22.93dBm	656.2	mA
		WCDMA B2 @22.95dBm	579.8	mA
		WCDMA B5 @22.54dBm	589.8	mA
		WCDMA B8 @22.47dBm	627.8	mA

Table 37: GNSS Current Consumption of EG95

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT} (GNSS)	Searching (**AT+CFUN=0**)	Cold start @ Passive Antenna	54	mA
		Hot Start @ Passive Antenna	54	mA
		Lost state @ Passive Antenna	53	mA
	Tracking (**AT+CFUN=0**)	Open Sky @ Passive Antenna	32	mA

6.5. RF Output Power

The following table shows the RF output power of EG95 module.

Table 38: RF Output Power

Frequency	Max.	Min.
GSM850/EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
GSM850/EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800/PCS1900 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
WCDMA B1/B2/B4/B5/B8	24 dBm +1/ -3 dB	< -49 dBm
LTE-FDD B1/B2/B3/B4/B5/B7/ B8/B12/B13/B20/B25/B26/B28/B66	23 dBm ±2 dB	< -39 dBm

NOTE

In GPRS 4 slots TX mode, the maximum output power is reduced by 3.0dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

6.6. RF Receiving Sensitivity

The following tables show the conducted RF receiving sensitivity of EG95 module.

Table 39: EG95-E Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO	3GPP
EGSM900	-108.6 dBm	NA	NA	-102 dBm
DCS1800	-109.4 dBm	NA	NA	-102 dBm
WCDMA B1	-109.5 dBm	-110 dBm	-112.5 dBm	-106.7 dBm
WCDMA B8	-109.5 dBm	-110 dBm	-112.5 dBm	-103.7 dBm

LTE-FDD B1 (10 MHz)	-97.5 dBm	-98.3 dBm	-101.4 dBm	-96.3 dBm
LTE-FDD B3 (10 MHz)	-98.3 dBm	-98.5 dBm	-101.5 dBm	-93.3 dBm
LTE-FDD B7 (10 MHz)	-96.3 dBm	-98.4 dBm	-101.3 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-97.1 dBm	-99.1 dBm	-101.2 dBm	-93.3 dBm
LTE-FDD B20 (10 MHz)	-97 dBm	-99 dBm	-101.3 dBm	-93.3 dBm
LTE-FDD B28A (10 MHz)	-98.3 dBm	-99 dBm	-101.4 dBm	-94.8 dBm

Table 40: EG95-NA Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO	3GPP
WCDMA B2	-110 dBm	-110 dBm	-112.5 dBm	-104.7 dBm
WCDMA B4	-110 dBm	-110 dBm	-112.5 dBm	-106.7 dBm
WCDMA B5	-111 dBm	-111 dBm	-113 dBm	-104.7 dBm
LTE-FDD B2 (10 MHz)	-98 dBm	-99 dBm	-102.2 dBm	-94.3 dBm
LTE-FDD B4 (10 MHz)	-97.8 dBm	-99.5 dBm	-102.2 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-99.6 dBm	-100.3 dBm	-103 dBm	-94.3 dBm
LTE-FDD B12 (10 MHz)	-99.5 dBm	-100 dBm	-102.5 dBm	-93.3 dBm
LTE-FDD B13 (10 MHz)	-99.2 dBm	-100 dBm	-102.5 dBm	-93.3 dBm

Table 41: EG95-EX Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO	3GPP
EGSM900	-109.8 dBm	NA	NA	-102 dBm
DCS1800	-109.8 dBm	NA	NA	-102dbm
WCDMA B1	-110 dBm	-111 dBm	-112.5 dBm	-106.7 dBm
WCDMA B8	-110 dBm	-111 dBm	-112.5 dBm	-103.7 dBm
LTE-FDD B1 (10 MHz)	-98.7 dBm	-98.8 dBm	-102.4 dBm	-96.3 dBm

LTE-FDD B3 (10 MHz)	-98.3 dBm	-99.5 dBm	-102.5 dBm	-93.3 dBm
LTE-FDD B7 (10 MHz)	-97.5 dBm	-98.4 dBm	-100.3 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98.7 dBm	-99.6 dBm	-102.2 dBm	-93.3 dBm
LTE-FDD B20 (10 MHz)	-97 dBm	-97.5 dBm	-102.2 dBm	-93.3 dBm
LTE-FDD B28 (10 MHz)	-98.2 dBm	-99.5 dBm	-102 dBm	-94.8 dBm

Table 42: EG95-NAX Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO	3GPP
WCDMA B2	-110 dBm	-110 dBm	-112.5 dBm	-104.7 dBm
WCDMA B4	-110 dBm	-110 dBm	-112.5 dBm	-106.7 dBm
WCDMA B5	-111 dBm	-111 dBm	-113 dBm	-104.7 dBm
LTE-FDD B2 (10 MHz)	-98 dBm	-99 dBm	-102.2 dBm	-94.3 dBm
LTE-FDD B4 (10 MHz)	-97.8 dBm	-99.5 dBm	-102.2 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-99.4 dBm	-100 dBm	-102.7 dBm	-94.3 dBm
LTE-FDD B12 (10 MHz)	-99.5 dBm	-100 dBm	-102.5 dBm	-93.3 dBm
LTE-FDD B13 (10 MHz)	-99.2 dBm	-100 dBm	-102.5 dBm	-93.3 dBm
LTE-FDD B25 (10 MHz)	-97.6 dBm	-99 dBm	-102.2 dBm	-92.8 dBm
LTE-FDD B26 (10 MHz)	-99.1 dBm	-99.9 dBm	-102.7 dBm	-93.8 dBm

Table 43: EG95-AUX Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO	3GPP
GSM850	-109.1 dBm	NA	NA	-102 dBm
EGSM900	-109.7 dBm	NA	NA	-102 dBm
DCS1800	-110.0 dBm	NA	NA	-102 dBm
PCS1900	-109.4 dBm	NA	NA	-102 dBm

WCDMA B1	-109.2 dBm	-109.5 dBm	NA	-106.7 dBm
WCDMA B2	-109.8 dBm	-111 dBm	NA	-104.7 dBm
WCDMA B5	-110 dBm	-111 dBm	NA	-104.7 dBm
WCDMA B8	-110 dBm	-111 dBm	NA	-103.7 dBm
LTE-FDD B1 (10MHz)	-97.2dBm	-98.9dBm	-101.2dBm	-96.3dBm
LTE-FDD B2 (10MHz)	-97.7dBm	-98.9dBm	-101.7dBm	-94.3dBm
LTE-FDD B3 (10MHz)	-98.2dBm	-99.1dBm	-102.2dBm	-93.3dBm
LTE-FDD B4 (10MHz)	-97.7dBm	-98.7dBm	-101.2dBm	-96.3dBm
LTE-FDD B5 (10MHz)	-99.2dBm	-99.7dBm	-102.7dBm	-94.3dBm
LTE-FDD B7 (10MHz)	-96.7dBm	-97.1dBm	-99.7dBm	-94.3dBm
LTE-FDD B8 (10MHz)	-98.0dBm	-98.4dBm	-102.2dBm	-93.3dBm
LTE-FDD B28 (10MHz)	-98.7dBm	-98.5dBm	-101.7dBm	-94.8dBm
LTE-FDD B66 (10MHz)	-97.7dBm	-98.8dBm	-101.2dBm	-95.8dBm

6.7. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module's electrostatic discharge characteristics.

Table 44: Electrostatic Discharge Characteristics (25 ºC, 45% Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.8. Thermal Consideration

In order to achieve better performance of the module, it is recommended to comply with the following principles for thermal consideration:

- On customers' PCB design, please keep placement of the module away from heating sources, especially high power components such as ARM processor, audio power amplifier, power supply, etc.
- Do not place components on the opposite side of the PCB area where the module is mounted, in order to facilitate adding of heatsink when necessary.
- Do not apply solder mask on the opposite side of the PCB area where the module is mounted, so as to ensure better heat dissipation performance.
- The reference ground of the area where the module is mounted should be complete, and add ground vias as many as possible for better heat dissipation.
- Make sure the ground pads of the module and PCB are fully connected.
- According to customers' application demands, the heatsink can be mounted on the top of the module, or the opposite side of the PCB area where the module is mounted, or both of them.
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between the heatsink and module/PCB.

The following shows two kinds of heatsink designs for reference and customers can choose one or both of them according to their application structure.

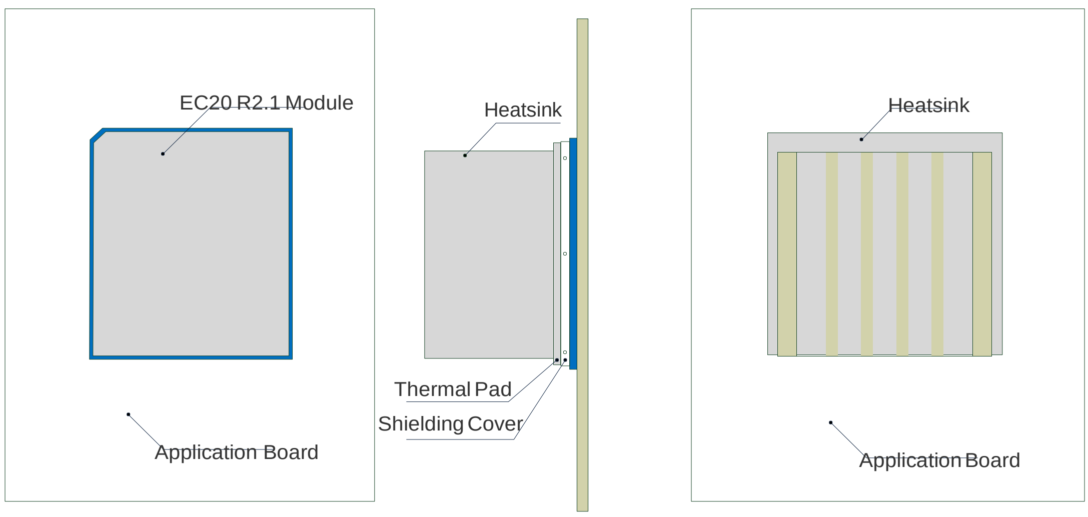


Figure 39: Referenced Heatsink Design (Heatsink at the Top of the Module)

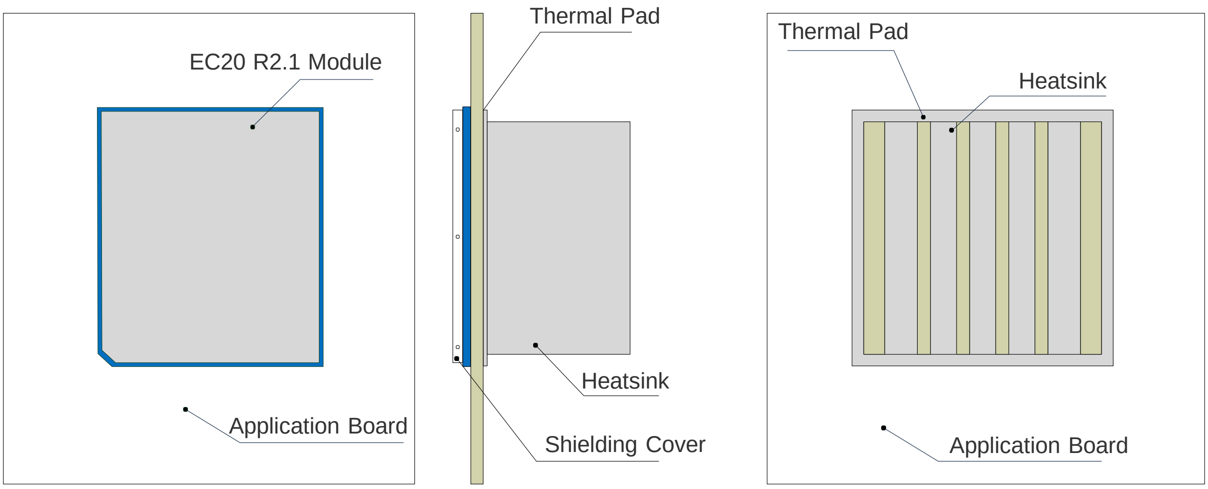


Figure 40: Referenced Heatsink Design (Heatsink at the Backside of Customers' PCB)

NOTE

The module offers the best performance when the internal BB chip stays below 105°C. When the maximum temperature of the BB chip reaches or exceeds 105°C, the module works normal but provides reduced performance (such as RF output power, data rate, etc.). When the maximum BB chip temperature reaches or exceeds 115°C, the module will disconnect from the network, and it will recover to network connected state after the maximum temperature falls below 115°C. Therefore, the thermal design should be maximally optimized to make sure the maximum BB chip temperature always maintains below 105°C. Customers can execute **AT+QTEMP** command and get the maximum BB chip temperature from the first returned value.

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm, and the dimensional tolerances are ±0.05 mm unless otherwise specified.

7.1. Mechanical Dimensions of the Module

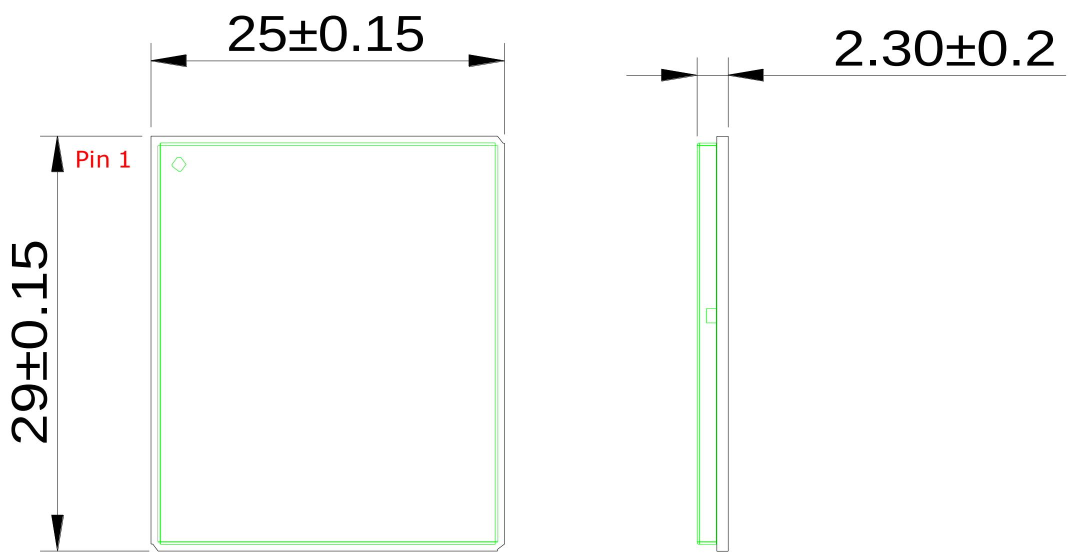


Figure 41: Module Top and Side Dimensions

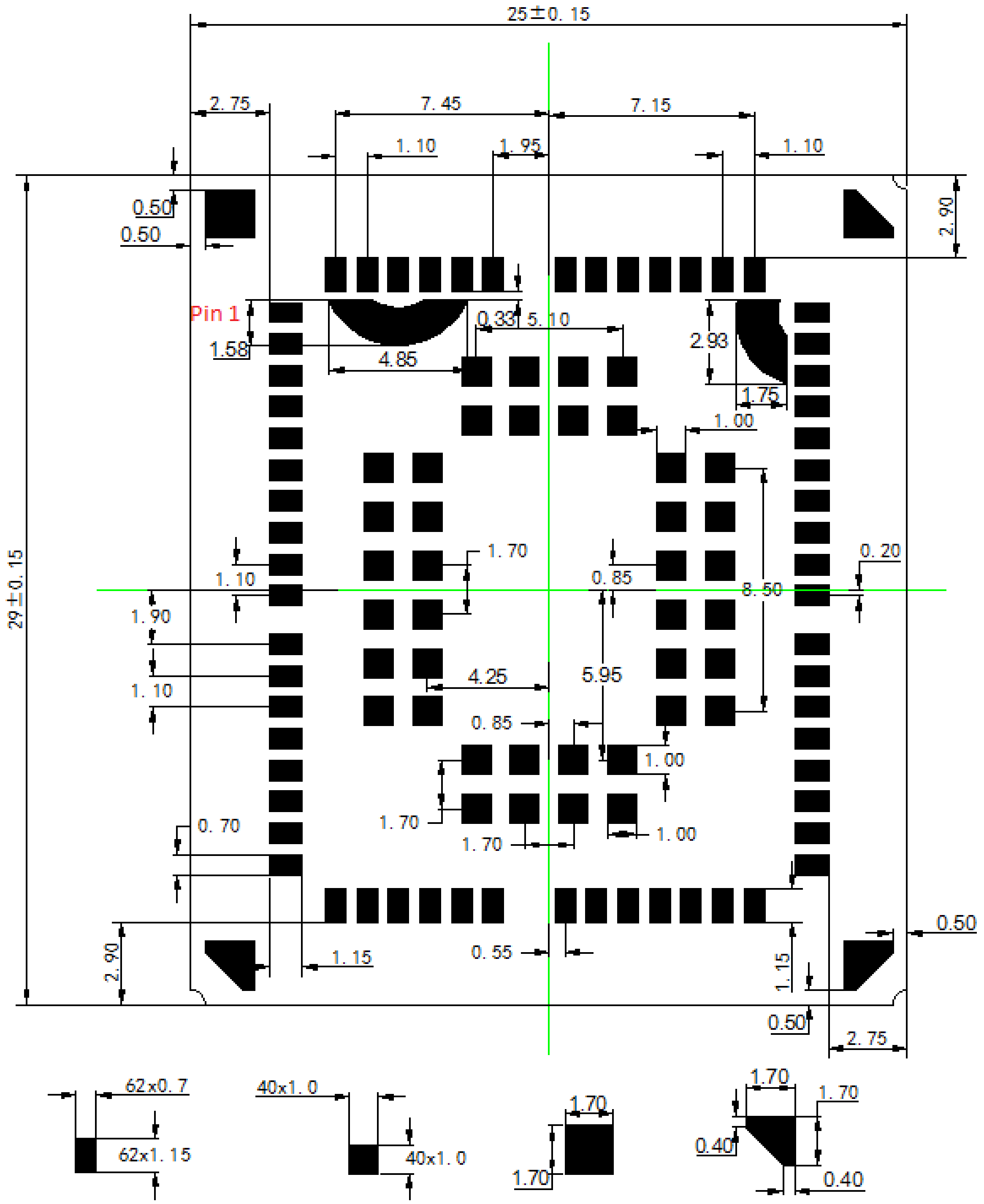


Figure 42: Module Bottom Dimensions (Top View)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

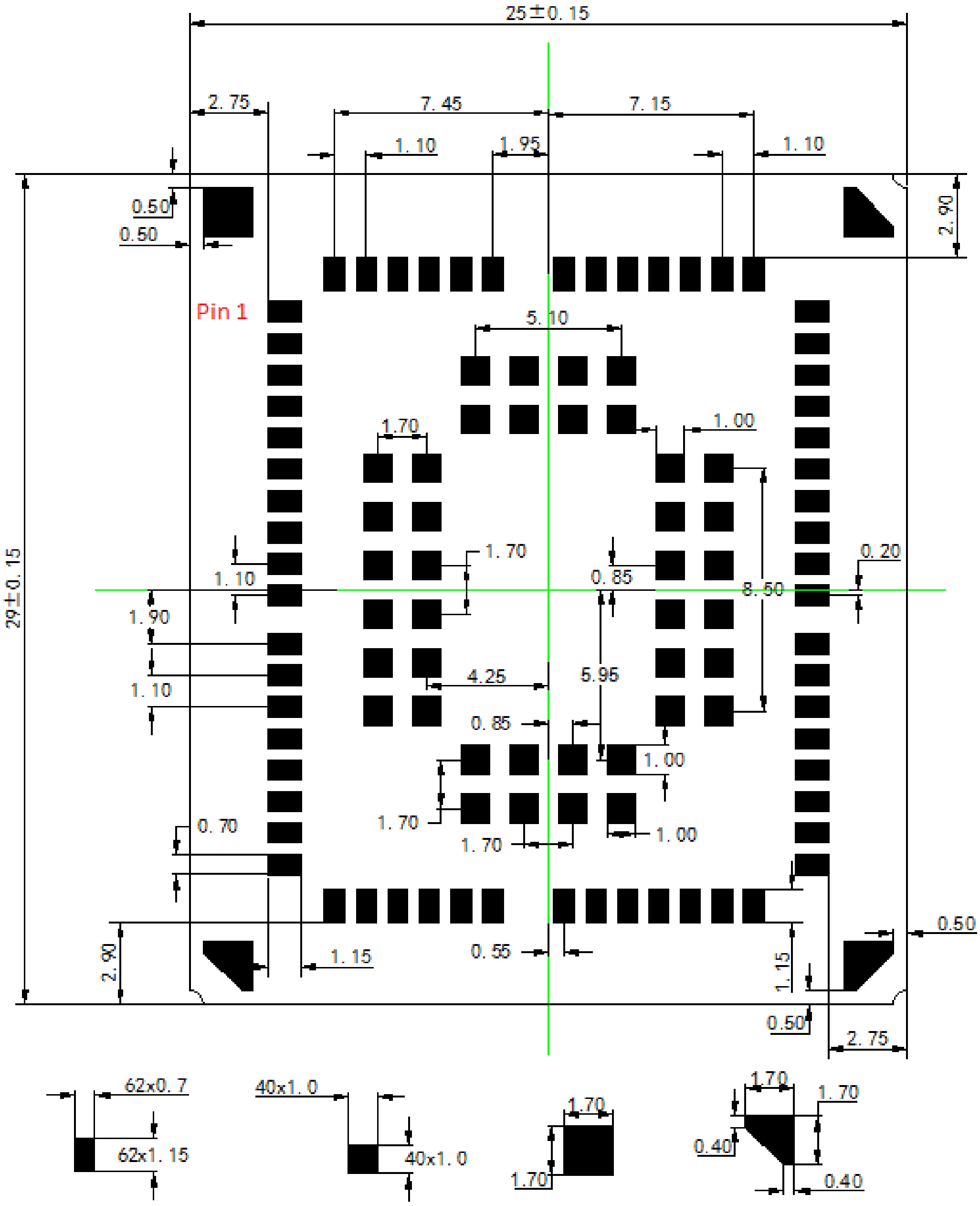


Figure 43: Recommended Footprint (Top View)

NOTE

For easy maintenance of the module, please keep about 3mm between the module and other components in the host PCB.

7.3. Top and Bottom Views of the Module

Figure 44: Top View of the Module

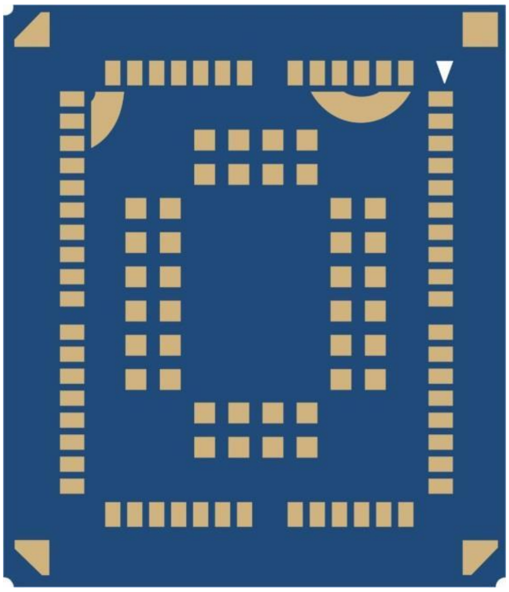


Figure 45: Bottom View of the Module

NOTE

These are renderings of the module. For authentic appearance, please refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35%–60%.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours 1) in a plant where the temperature is 23 ±5 °C and relative humidity is below 60%. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10% (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

NOTES

1. [1)] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*.
2. To avoid blistering, layer separation and other soldering issues, it is forbidden to expose the modules to the air for a long time. If the temperature and moisture do not conform to *IPC/JEDEC J-STD-033* or the relative moisture is over 60%, It is recommended to start the solder reflow process within 24 hours after the package is removed. And do not remove the packages of tremendous modules if they are not ready for soldering.
3. Please take the module out of the packaging and put it on high-temperature resistant fixtures before the baking. If shorter baking time is desired, please refer to *IPC/JEDEC J-STD-033* for baking procedure.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, please refer to ***document [4]***.

It is suggested that the peak reflow temperature is 238–246 ºC, and the absolute maximum reflow temperature is 246 ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

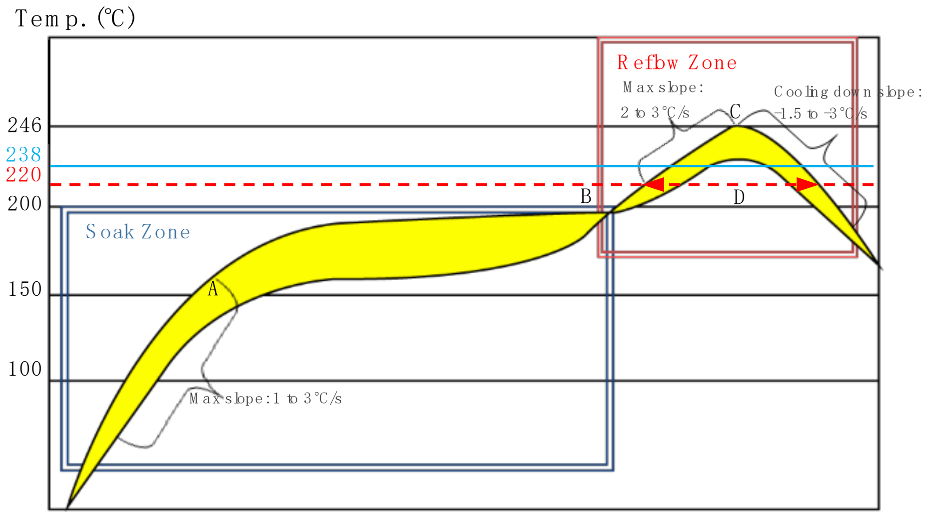


Figure 46: Recommended Reflow Soldering Thermal Profile

Table 45: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	2–3 °C/s
Reflow time (D: over 220°C)	45–70 s
Max temperature	238 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

8.3. Packaging

EG95 is packaged in a vacuum-sealed bag which is ESD protected. The bag should not be opened until the devices are ready to be soldered onto the application.

The reel is 330 mm in diameter and each reel contains 250pcs modules. The following figures show the packaging details, measured in mm.

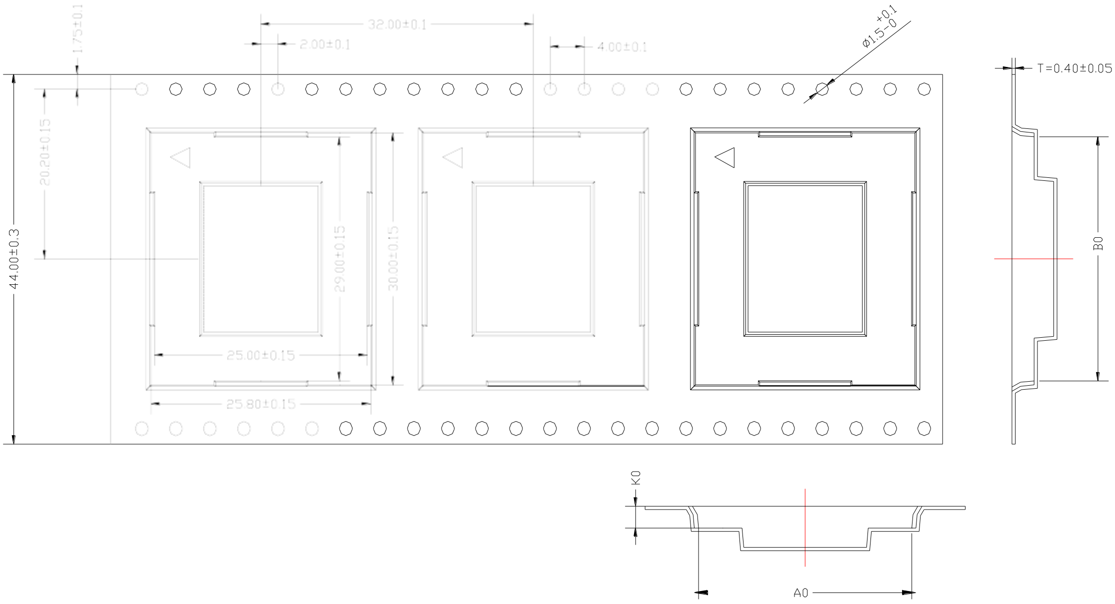


Figure 47: Tape Specifications

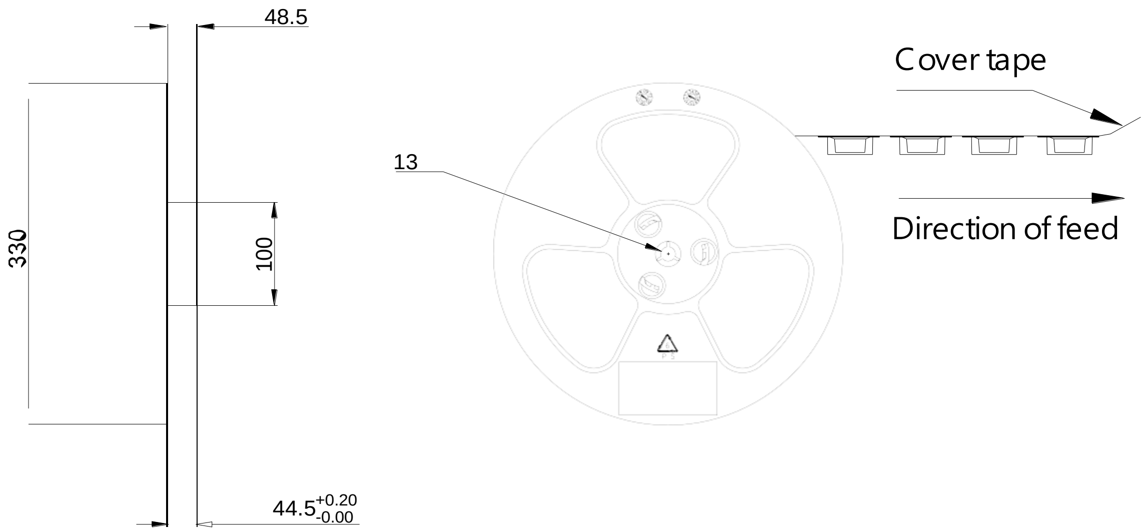


Figure 48: Reel Specifications

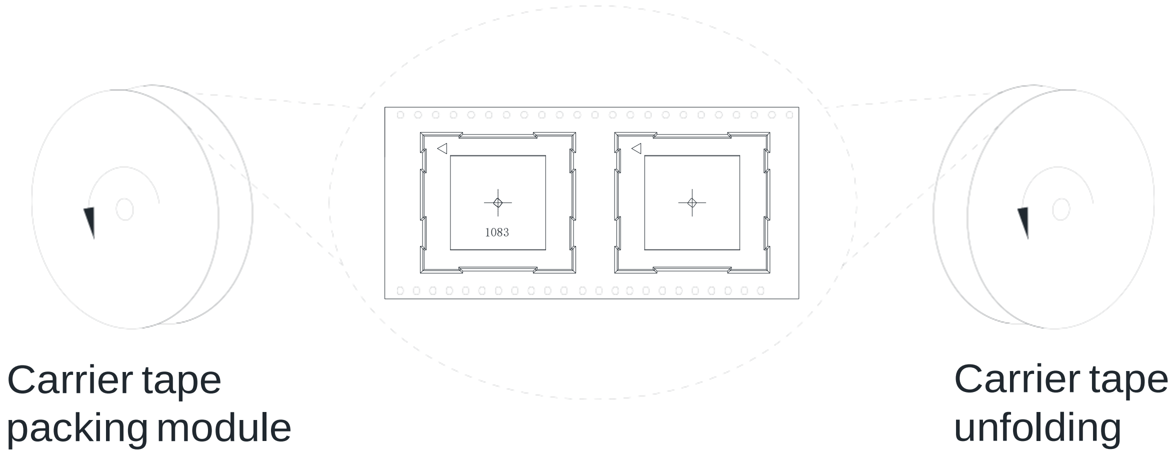


Figure 49: Tape and Reel Directions

9 Appendix A References

Table 46: Related Documents

SN	Document Name	Remark
[1]	Quectel_EC2x&EG9x_Power_Management_Application_Note	Power management application note for EC25 series, EC21 series, EC20 R2.1, EG95 series and EG91 series
[2]	Quectel_LTE_Standard_AT_Commands_Manual	AT commands manual for LTE Standard modules
[3]	Quectel_LTE_Standard_GNSS_Application_Note	GNSS application note for LTE Standard modules
[4]	Quectel_Module_Secondary_SMT_User_Guide	Module secondary SMT user guide
[5]	Quectel_RF_Layout_Application_Note	RF layout application note
[6]	Quectel_LTE_Module_Thermal_Design_Guide	Thermal design guide for LTE standard, LTE-A and Automotive modules
[7]	Quectel_UMTS&LTE_EVB_User_Guide	UMTS&LTE EVB user guide for UMTS&LTE modules

Table 47: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear To Send
DC-HSPA+	Dual-carrier High Speed Packet Access

DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
GLONASS	GLObalnaya NAvigatsionnaya Sputnikovaya Sistema, the Russian Global Navigation Satellite System
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
Inorm	Normal Current
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MS	Mobile Station (GSM engine)

MSL	Moisture Sensitivity Level
MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SMS	Short Message Service
TDD	Time Division Duplexing
TX	Transmitting Direction
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
$V_{IH}max$	Maximum Input High Level Voltage Value
$V_{IH}min$	Minimum Input High Level Voltage Value
$V_{IL}max$	Maximum Input Low Level Voltage Value
$V_{IL}min$	Minimum Input Low Level Voltage Value

$V_I$max	Absolute Maximum Input Voltage Value
$V_I$min	Absolute Minimum Input Voltage Value
V_{OH}in	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

10 Appendix B GPRS Coding Schemes

Table 48: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

11 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 49: GPRS Multi-slot Classes

Multi-slot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA

14	4	4	NA
15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

12 Appendix D EDGE Modulation and Coding Schemes

Table 50: EDGE Modulation and Coding Schemes

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
MCS-1	GMSK	C	8.80 kbps	17.60 kbps	35.20 kbps
MCS-2	GMSK	B	11.2 kbps	22.4 kbps	44.8 kbps
MCS-3	GMSK	A	14.8 kbps	29.6 kbps	59.2 kbps
MCS-4	GMSK	C	17.6 kbps	35.2 kbps	70.4 kbps
MCS-5	8-PSK	B	22.4 kbps	44.8 kbps	89.6 kbps
MCS-6	8-PSK	A	29.6 kbps	59.2 kbps	118.4 kbps
MCS-7	8-PSK	B	44.8 kbps	89.6 kbps	179.2 kbps
MCS-8	8-PSK	A	54.4 kbps	108.8 kbps	217.6 kbps
MCS-9	8-PSK	A	59.2 kbps	118.4 kbps	236.8 kbps