# FG50V Hardware Design

**Wi-Fi&BT Module Series**

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# About the Document

## Revision History

| Version | Date | Author | Description |
|---|---|---|---|
| - | 2019-11-25 | Jared WANG/ Felix FU | Creation of the document |
| 1.0 | 2020-12-08 | Hidy CHAI/ Lucas HUANG | First official release |

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# 1 Introduction

This document defines the FG50V module and describes its air interfaces and hardware interfaces which are connected with your application.

This document can help you quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, you can use FG50V module to design and set up applications easily.

Hereby, [Quectel Wireless Solutions Co., Ltd.] declares that the radio equipment type [FG50V] is in compliance with Directive 2014/53/EU.
The full text of the EU declaration of conformity is available at the following internet address: http://www.quectel.com.

The device could be used with a separation distance of 20cm to the human body.

FCC Certification Requirements.
According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.
And the following conditions must be met:
1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based timeaveraging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.
2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.
3. A label with the following statements must be attached to the host end product: This device contains FCC ID: XMR202103FG50V
4. To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:
WIFI 2.4G/5G : 5.38 dBi

5. This module must not transmit simultaneously with any other antenna or transmitter
6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.
For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093
If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.
For this device, OEM integrators must be provided with labeling instructions of finished products.
Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: XMR202103FG50V" or "Contains FCC ID: XMR202103FG50V" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier's Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.

**Manual Information To the End User**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Wireless Access Systems including Radio Local Area Networks (WAS/RLANs) frequency range 5150 – 5350 MHz is Restricted to indoor use in EU, this device contains 5150-5250 MHz.

## 1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating FG50V module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

| | |
|---|---|
|  | Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving. |
|  | Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft. |
|  | Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities. |
|  | Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances. |
|  | The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment. |

In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

# 2 Product Concept

## 2.1. General Description

FG50V is a Wi-Fi and Bluetooth (BT) module with low power consumption. It is a single-die WLAN (Wireless Local Area Network) and BT combo solution supporting IEEE 802.11a/b/g/n/ac/ax 2.4/5 GHz WLAN standards and BT 5.1* standard, which enables seamless integration of WLAN and BT low energy technologies.

With a low-power PCIe Gen 2 interface for WLAN, a UART and PCM* interface for BT, and an LTE/5G & WLAN/BT coexistence interface, FG50V can provide WLAN and BT functions.

## 2.2. Key Features

The following table describes the key features of FG50V module.

**Table 1: Key Features**

| Features | Details |
|---|---|
| Power Supply | ● Core supply voltage: 0.95 V, 1.35 V, 1.95 V<br>● I/O supply voltage: 1.8 V<br>● RF supply voltage: 3.85 V |
| Operating Frequency | ● 2.4 GHz WLAN: 2.400–2.4835 GHz<br>● 5 GHz WLAN: 5.150–5.850 GHz<br>● BT: 2.402–2.480 GHz |
| Transmission Data Rates | ● 802.11a: 6 Mbps, 9 Mbps, 12 Mbps, 18 Mbps, 24 Mbps, 36 Mbps, 48 Mbps, 54 Mbps<br>● 802.11b: 1 Mbps, 2 Mbps, 5.5 Mbps, 11 Mbps<br>● 802.11g: 6 Mbps, 9 Mbps, 12 Mbps, 18 Mbps, 24 Mbps, 36 Mbps, 48 Mbps, 54 Mbps<br>● 802.11n: HT20 (MCS0-7), HT40 (MCS8-15)<br>● 802.11ac: VHT20 (MCS0-8), VHT40 (MCS0-9), VHT80 (MCS0-9)<br>● 802.11ax: HE20 (MCS0-11), HE40 (MCS0-11), HE80 (MCS0-11) |

| | |
|---|---|
| Transmitting Power | **2.4 GHz**<br>802.11b @ 11 Mbps: 20 dBm<br>802.11g @ 54 Mbps: 17 dBm<br>802.11n, HT20 @ MCS7: 16 dBm<br>802.11n, HT40 @ MCS7: 16 dBm<br>802.11ax, HE20 @ MCS11: 13 dBm<br>802.11ax, HE40 @ MCS11: 13 dBm<br><br>**5 GHz**<br>802.11a @ 54 Mbps: 15.5 dBm<br>802.11n, HT20 @ MCS7: 15 dBm<br>802.11n, HT40 @ MCS7: 15 dBm<br>802.11ac, VHT20 @ MCS8: 14 dBm<br>802.11ac, VHT40 @ MCS9: 14 dBm<br>802.11ac, VHT80 @ MCS9: 14 dBm<br>802.11ax, HE20 @ MCS11: 13 dBm<br>802.11ax, HE40 @ MCS11: 13 dBm<br>802.11ax, HE80 @ MCS11: 13 dBm |
| Protocol Features | ● IEEE 802.11a/b/g/n/ac/ax<br>● BT 5.1* |
| Operation Mode | AP, STA |
| Modulation | BPSK, QPSK, CCK, 16QAM, 64QAM, 256QAM, 1024QAM |
| WLAN Interface | PCIe |
| BT Interface | UART and PCM* |
| RF Antenna Interfaces | ● ANT_WIFI0, ANT_WIFI1, ANT_BT*<br>● 50 Ω impedance |
| Physical Characteristics | ● Size: (19.5 ±0.2) mm × (21.5 ±0.2) mm × (2.1 ±0.2) mm<br>● Package: LGA<br>● Weight: TBD |
| Temperature Range | ● Operating temperature range: -40 °C to +85 °C [1)]<br>● Storage temperature range: -40 °C to +95 °C |
| RoHS | All hardware components are fully compliant with EU RoHS directive |

**NOTES**

1. [1)] Within operating temperature range, the module is IEEE compliant.
2. "*" means under development.

## 2.3. Functional Diagram

The following figure shows a block diagram of FG50V module.

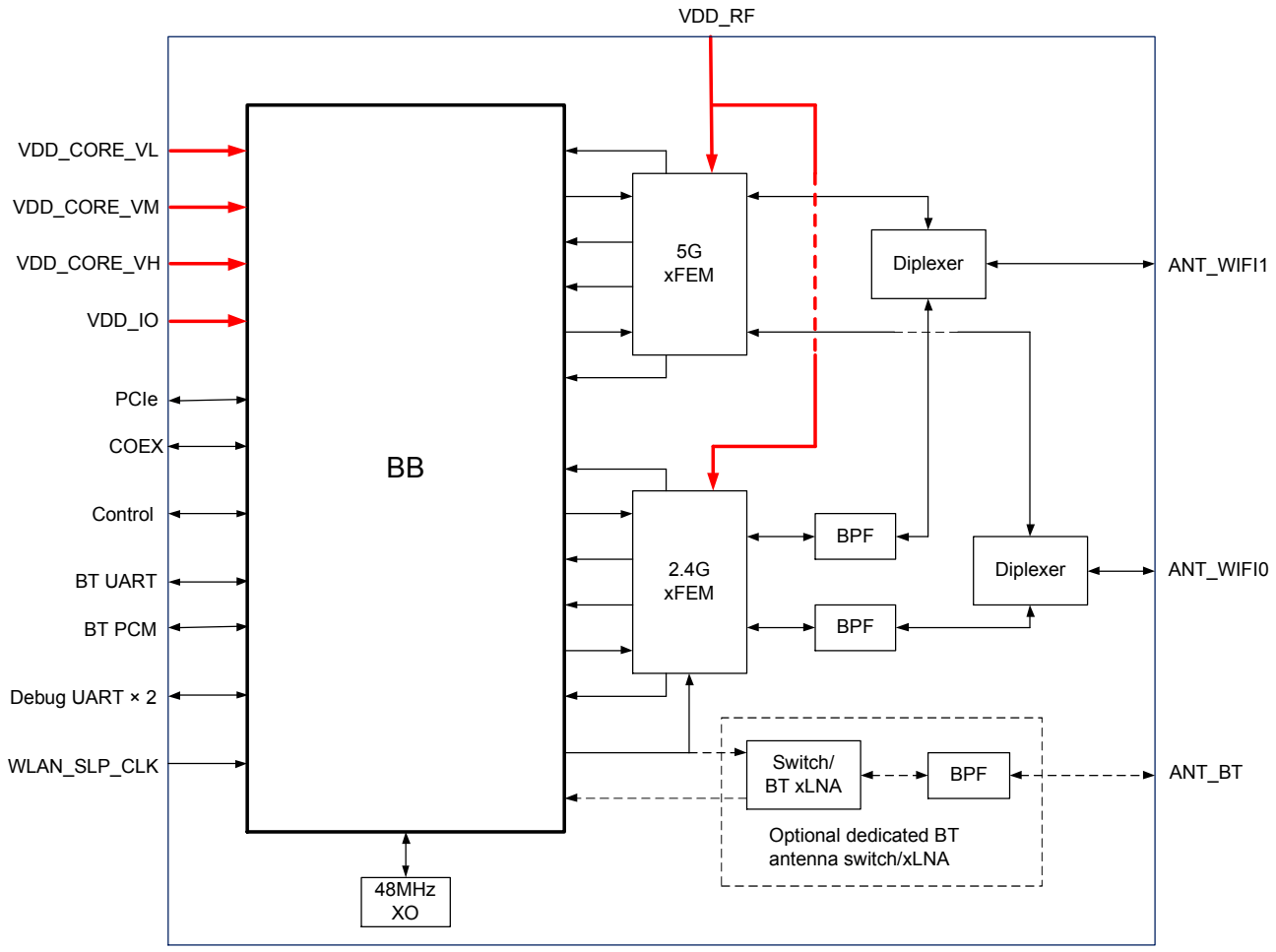



**Figure 1: Functional Diagram of FG50V Module**

## 2.4. Evaluation Board

In order to help you to develop applications with FG50V module conveniently, Quectel supplies the evaluation board (EVB), USB to RS-232 converter cable, USB data cable, power adapter, antenna and other peripherals to control or test the module. For more details, see ***document [1]***.

# 3 Application Interfaces

## 3.1. General Description

FG50V module is equipped with 108 LGA pins that can be connected to the cellular application platform. The subsequent chapters will provide a detailed introduction to the following interfaces and pins of the module:

- Power supply
- WLAN interface
- BT interface*
- Coexistence interface
- WLAN_SLP_CLK interface
- Other interfaces
- RF antenna interfaces

**NOTE**

"*" means under development.

## 3.2. Pin Assignment

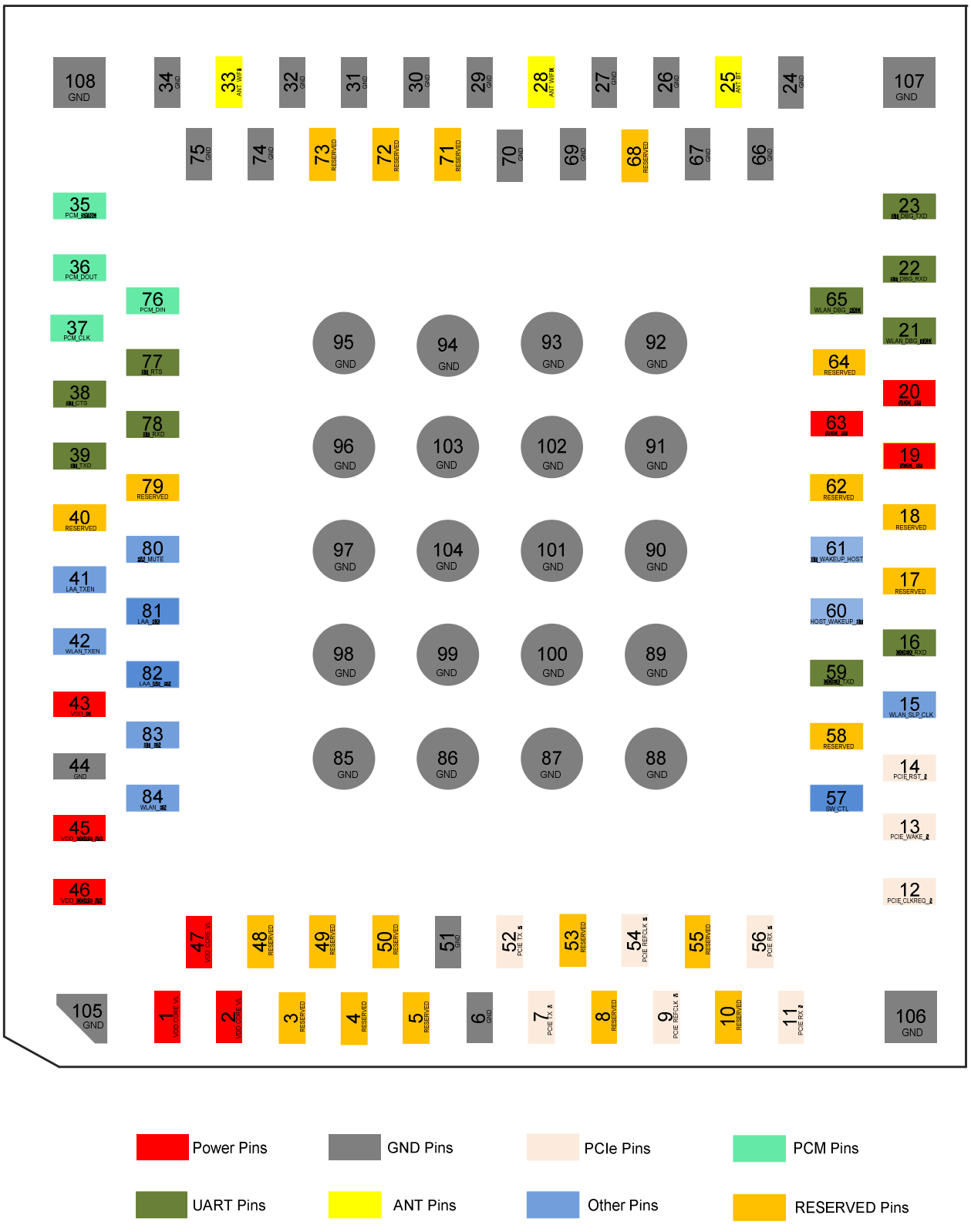



Figure 2: Pin Assignment (Top View)

**NOTE**

Please keep all RESERVED pins open.

## 3.3. Pin Description

The following tables show the pin description of FG50V module.

**Table 2: I/O Parameters Definition**

| Type | Description |
|---|---|
| AI | Analog Input |
| AO | Analog Input |
| DI | Digital Input |
| DO | Digital Output |
| IO | Bidirectional |
| PI | Power Input |

**Table 3: Pin Description**

| Power Supply | | | | | |
|---|---|---|---|---|---|
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| VDD_CORE_VL | 1, 2, 47 | PI | 0.95 V power supply for the module's main part | Vmin = 0.9 V<br>Vnorm = 0.95 V<br>Vmax = 1.0 V | It must be provided with sufficient current of up to 1.7 A. |
| VDD_CORE_VM | 45 | PI | 1.35 V power supply for the module's main part | Vmin = 1.28 V<br>Vnorm = 1.35 V<br>Vmax = 1.42 V | It must be provided with sufficient current of up to 0.4 A. |

| | | | | | |
|---|---|---|---|---|---|
| VDD_CORE_VH | 46 | PI | 1.95 V power supply for the module's main part | Vmin = 1.85 V<br>Vnorm = 1.95 V<br>Vmax = 2.05 V | It must be provided with sufficient current of up to 0.4 A. |
| VDD_IO | 43 | PI | 1.8 V power supply for the module's I/O pins | Vmin = 1.7 V<br>Vnorm = 1.8 V<br>Vmax = 1.9 V | It must be provided with sufficient current of up to 0.05 A. |
| VDD_RF | 19, 20, 63 | PI | 3.85 V power supply for the module's RF part | Vmin = 3.3 V<br>Vnorm = 3.85 V<br>Vmax = 4.25 V | It must be provided with sufficient current of up to 1.3 A. |
| GND | 6, 24, 26, 27, 29, 30, 31, 32, 34, 44, 51, 66, 67, 69, 70, 74, 75, 85–108 | | | | |
| **WLAN Interface** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| WLAN_EN | 84 | DI | WLAN enable | $V_{IL}$min = -0.3 V<br>$V_{IL}$max = 0.63 V<br>$V_{IH}$min = 1.17 V<br>$V_{IH}$max = 2.1 V | 1.8 V power domain.<br>Active high.<br>It is suggested to pull down this pin with a 100 kΩ resistor. |
| PCIE_REFCLK_P | 54 | AI | PCIe reference clock (+) | | Require differential impedance of 85 Ω. |
| PCIE_REFCLK_M | 9 | AI | PCIe reference clock (-) | | |
| PCIE_TX_P | 52 | AO | PCIe transmit (+) | | |
| PCIE_TX_M | 7 | AO | PCIe transmit (-) | | |
| PCIE_RX_P | 56 | AI | PCIe receive (+) | | |
| PCIE_RX_M | 11 | AI | PCIe receive (-) | | |
| PCIE_CLKREQ_N | 12 | DO | PCIe clock request | $V_{OL}$max = 0.45 V<br>$V_{OH}$min = 1.35 V | 1.8 V power domain.<br>Active low. |
| PCIE_RST_N | 14 | DI | PCIe reset | $V_{IL}$min = -0.3 V<br>$V_{IL}$max = 0.63 V<br>$V_{IH}$min = 1.17 V<br>$V_{IH}$max = 2.1 V | |
| PCIE_WAKE_N | 13 | DO | PCIe wake up | $V_{OL}$max = 0.45 V<br>$V_{OH}$min = 1.35 V | |
| **BT Interface** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |

| | | | | | |
|---|---|---|---|---|---|
| BT_EN | 83 | DI | BT enable | $V_{IL}$min = -0.3 V<br>$V_{IL}$max = 0.63 V<br>$V_{IH}$min = 1.17 V<br>$V_{IH}$max = 2.1 V | 1.8 V power domain.<br>Active high.<br>It is suggested to pull down this pin with a 100 kΩ resistor. |
| PCM_DIN* | 76 | DI | PCM data input | $V_{IL}$min = -0.3 V<br>$V_{IL}$max = 0.63 V<br>$V_{IH}$min = 1.17 V<br>$V_{IH}$max = 2.1 V | 1.8 V power domain. |
| PCM_SYNC* | 35 | DI | PCM data frame sync | $V_{IL}$min = -0.3 V<br>$V_{IL}$max = 0.63 V<br>$V_{IH}$min = 1.17 V<br>$V_{IH}$max = 2.1 V | 1.8 V power domain. |
| PCM_CLK* | 37 | DI | PCM clock | $V_{IL}$min = -0.3 V<br>$V_{IL}$max = 0.63 V<br>$V_{IH}$min = 1.17 V<br>$V_{IH}$max = 2.1 V | 1.8 V power domain. |
| PCM_DOUT* | 36 | DO | PCM data output | $V_{OL}$max = 0.45 V<br>$V_{OH}$min = 1.35 V | 1.8 V power domain.<br>Externally pull this pin up to VDD_IO. |
| BT_RTS | 77 | DO | BT UART request to send | $V_{OL}$max = 0.45 V<br>$V_{OH}$min = 1.35 V | 1.8 V power domain. |
| BT_CTS | 38 | DI | BT UART clear to send | $V_{IL}$min = -0.3 V<br>$V_{IL}$max = 0.63 V<br>$V_{IH}$min = 1.17 V<br>$V_{IH}$max = 2.1 V | 1.8 V power domain. |
| BT_TXD | 39 | DO | BT UART transmit | $V_{OL}$max = 0.45 V<br>$V_{OH}$min = 1.35 V | 1.8 V power domain. |
| BT_RXD | 78 | DI | BT UART receive | $V_{IL}$min = -0.3 V<br>$V_{IL}$max = 0.63 V<br>$V_{IH}$min = 1.17 V<br>$V_{IH}$max = 2.1 V | 1.8 V power domain. |
| BT_WAKEUP_HOST* | 61 | DO | BT wakes up host | $V_{OL}$max = 0.45 V<br>$V_{OH}$min = 1.35 V | 1.8 V power domain. |
| HOST_WAKEUP_BT* | 60 | DI | Host wakes up BT | $V_{IL}$min = -0.3 V<br>$V_{IL}$max = 0.63 V<br>$V_{IH}$min = 1.17 V<br>$V_{IH}$max = 2.1 V | 1.8 V power domain.<br>Externally pull this pin down. |
| **Coexistence Interface** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |

| | | | | | |
|---|---|---|---|---|---|
| COEX_TXD | 59 | DO | 2.4G WWAN & WLAN/BT coexistence transmit | $V_{OL}$max = 0.45 V<br>$V_{OH}$min = 1.35 V | |
| COEX_RXD | 16 | DI | 2.4G WWAN & WLAN/BT coexistence receive | $V_{IL}$min = -0.3 V<br>$V_{IL}$max = 0.63 V<br>$V_{IH}$min = 1.17 V<br>$V_{IH}$max = 2.1 V | |
| LAA_AS_EN | 82 | DI | Allows LAA/n79 to control WLAN xFEM during WLAN sleep mode | $V_{IL}$min = -0.3 V<br>$V_{IL}$max = 0.63 V<br>$V_{IH}$min = 1.17 V<br>$V_{IH}$max = 2.1 V | |
| LAA_TXEN | 41 | DI | WLAN xFEM control to enable LAA/n79 transmit | $V_{IL}$min = -0.3 V<br>$V_{IL}$max = 0.63 V<br>$V_{IH}$min = 1.17 V<br>$V_{IH}$max = 2.1 V | 1.8 V power domain.<br>If unused, keep these pins open. |
| LAA_RX | 81 | DI | WLAN xFEM control for LAA/n79 receiver | $V_{IL}$min = -0.3 V<br>$V_{IL}$max = 0.63 V<br>$V_{IH}$min = 1.17 V<br>$V_{IH}$max = 2.1 V | |
| WLAN_TXEN | 42 | DO | WLAN xFEM control to enable WLAN transmit | $V_{OL}$max = 0.45 V<br>$V_{OH}$min = 1.35 V | |
| PA_MUTE | 80 | DI | WLAN xFEM control to disable WLAN PA | $V_{IL}$min = -0.3 V<br>$V_{IL}$max = 0.63 V<br>$V_{IH}$min = 1.17 V<br>$V_{IH}$max = 2.1 V | |
| **Other Interfaces** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| SW_CTRL* | 57 | DO | Switch control | $V_{OL}$max = 0.45 V<br>$V_{OH}$min = 1.35 V | 1.8 V power domain.<br>Active high.<br>If unused, keep this pin open. |
| WLAN_DBG_TXD | 21 | DO | WLAN debug UART transmit | $V_{OL}$max = 0.45 V<br>$V_{OH}$min = 1.35 V | 1.8 V power domain.<br>If unused, keep these pins open. |
| WLAN_DBG_RXD | 65 | DI | WLAN debug UART receive | $V_{IL}$min = -0.3 V<br>$V_{IL}$max = 0.63 V<br>$V_{IH}$min = 1.17 V<br>$V_{IH}$max = 2.1 V | |
| BT_DBG_TXD | 23 | DO | BT debug UART transmit | $V_{OL}$max = 0.45 V<br>$V_{OH}$min = 1.35 V | |

| | | | | | |
|---|---|---|---|---|---|
| BT_DBG_RXD | 22 | DI | BT debug UART receive | $V_{IL}$min = -0.3 V<br>$V_{IL}$max = 0.63 V<br>$V_{IH}$min = 1.17 V<br>$V_{IH}$max = 2.1 V | |
| **RF Antenna Interfaces** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| ANT_WIFI0 | 28 | IO | BT and WLAN antenna interface | | 50 Ω impedance. |
| ANT_WIFI1 | 33 | IO | WLAN antenna interface | | 50 Ω impedance. |
| ANT_BT* | 25 | IO | Reserved dedicated BT antenna interface | | 50 Ω impedance. |
| **WLAN_SLP_CLK Interface** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| WLAN_SLP_CLK | 15 | DI | WLAN sleep clock | $V_{IL}$min = -0.3 V<br>$V_{IL}$max = 0.63 V<br>$V_{IH}$min = 1.17 V<br>$V_{IH}$max = 2.1 V | 1.8 V power domain.<br>If unused, keep this pin open. |
| **RESERVED Interfaces** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| RESERVED | 4, 5, 8, 10, 17, 18, 40, 49, 50, 53, 55, 58, 62, 64, 68, 71–73, 79 | | | | Keep these pins open. |

**NOTE**

"*" means under development.

## 3.4. Power Supply

The following table shows the power supply pins and ground pins of FG50V module.

**Table 4: Definition of Power Supply and GND Pins**

| Pin Name | Pin No. | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VDD_CORE_VL | 1, 2, 47 | 0.95 V power supply for the module's main part | 0.9 | 0.95 | 1.0 | V |
| VDD_CORE_VM | 45 | 1.35 V power supply for the module's main part | 1.28 | 1.35 | 1.42 | V |
| VDD_CORE_VH | 46 | 1.95 V power supply for the module's main part | 1.85 | 1.95 | 2.05 | V |
| VDD_IO | 43 | 1.8 V power supply for the module's I/O pins | 1.7 | 1.8 | 1.9 | V |
| VDD_RF | 19, 20, 63 | 3.85 V power supply for the module's RF part | 3.3 | 3.85 | 4.25 | V |
| GND | 6, 24, 26, 27, 29, 30, 31, 32, 34, 44, 51, 66, 67, 69, 70, 74, 75, 85–108 | | | | | |

Among them, VDD_CORE_VL, VDD_CORE_VM, VDD_CORE_VH, and VDD_IO can be powered by either Quectel RG50xQ series or discrete power supply chips while VDD_RF can be powered by a discrete power supply chip. The following figures show the two power designs. For more details, see ***document [2]***.

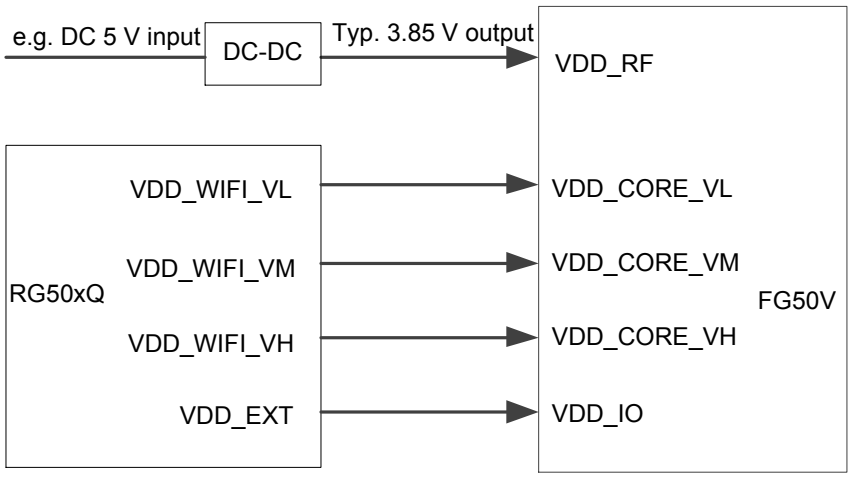



**Figure 3: Power Reference Design with RG50xQ Series**

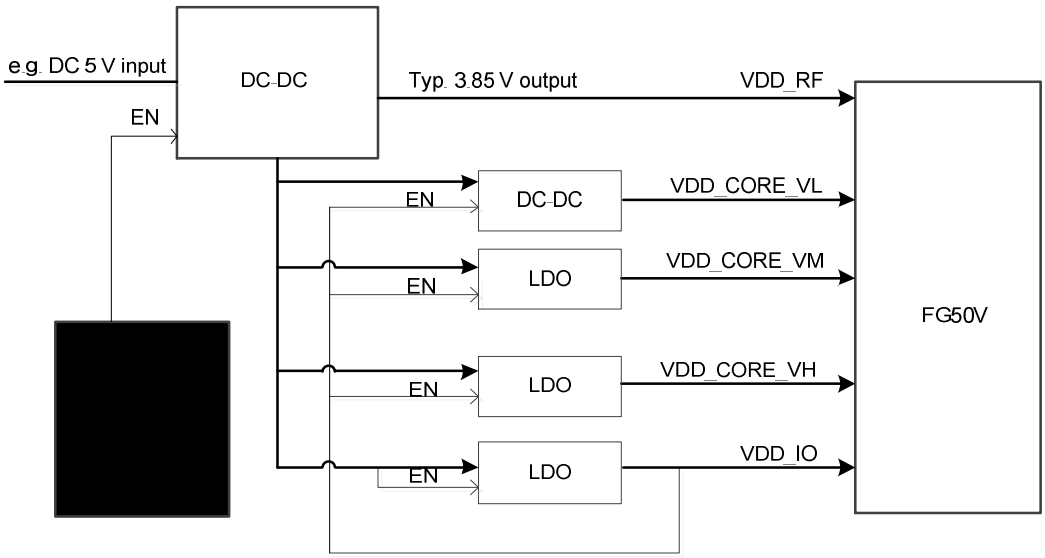



**Figure 4: Power Reference Design with Discrete Power Supply Chips**

## 3.5. WLAN Interface

The following figure shows the WLAN interface connection between FG50V and the host.

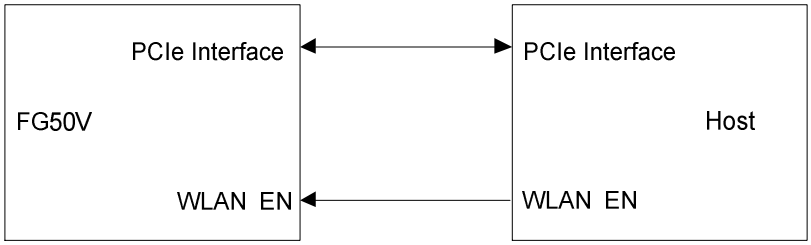



**Figure 4: WLAN Interface Connection**

### 3.5.1. WLAN_EN

WLAN_EN is used to control the WLAN function of FG50V module. WLAN function will be enabled when WLAN_EN is at high level.

**Table 5: Pin Definition of WLAN_EN**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| WLAN_EN | 84 | DI | WLAN enable | 1.8 V power domain.<br>Active high.<br>It is suggested to pull down this pin with a 100 kΩ resistor. |

### 3.5.2. PCIe Interface

The following table shows the pin definition of the PCIe interface of FG50V.

**Table 6: Pin Definition of PCIe Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| PCIE_REFCLK_P | 54 | AI | PCIe reference clock (+) | Require differential impedance of 85 Ω. |
| PCIE_REFCLK_M | 9 | AI | PCIe reference clock (-) | |
| PCIE_TX_P | 52 | AO | PCIe transmit (+) | |
| PCIE_TX_M | 7 | AO | PCIe transmit (-) | |
| PCIE_RX_P | 56 | AI | PCIe receive (+) | |
| PCIE_RX_M | 11 | AI | PCIe receive (-) | |
| PCIE_CLKREQ_N | 12 | DO | PCIe clock request | 1.8 V power domain.<br>Active low. |
| PCIE_RST_N | 14 | DI | PCIe reset | |
| PCIE_WAKE_N | 13 | DO | PCIe wakes up | |

The following figure shows the PCIe interface connection between FG50V and the host.

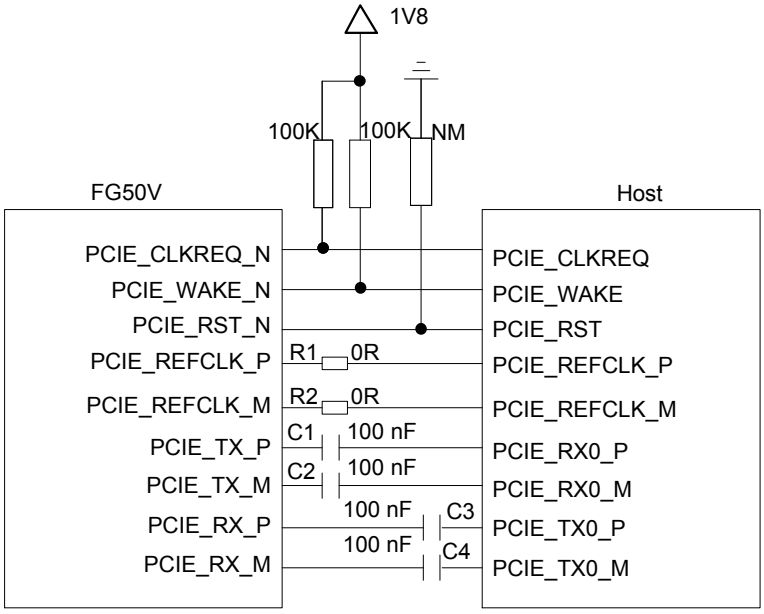



**Figure 5: PCIe Interface Connection**

To ensure the signal integrity of PCIe interface, C1 and C2 should be placed close to the FG50V module, and C3 and C4 should be placed close to the host The extra stubs of traces must be avoided.

The following principles of PCIe interface design should be complied with, so as to meet PCIe Gen2 specifications.

- It is important to route PCIE_TX_P/M, PCIE_RX_P/M, and PCIE_REFCLK_P/M as differential pairs with total grounding. And the differential impedance should be 85 Ω ±10 %.
- The maximum trace length of each differential pair (PCIE_TX_P/M, PCIE_RX_P/M, and PCIE_REFCLK_P/M) should be less than 300 mm, and trace length matching within each differential pair should be less than 0.7 mm.
- Space between PCIe signals and all other signals (inter-interface) should be four times the trace width.
- Do not route signal traces under crystals, oscillators, magnetic devices, or RF signal traces. It is important to route the PCIe differential traces in inner-layer of the PCB and surround the traces with ground on that layer and with ground planes above and below.

## 3.6. BT Interface

The following figure shows the block diagram of BT interface connection between FG50V and the host.

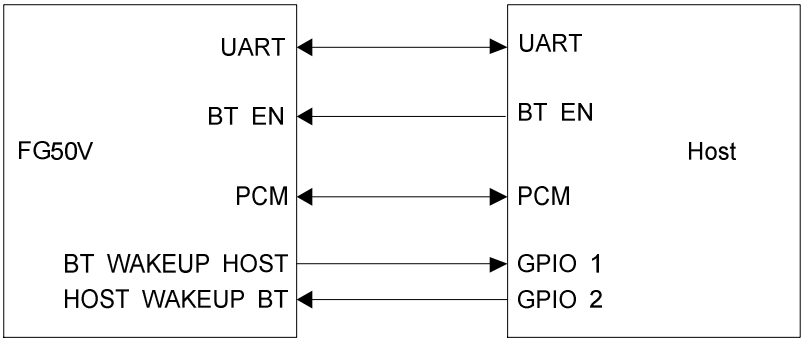



**Figure 6: Block Diagram of BT Interface Connection**

**NOTE**

The GPIO_1 connected to BT_WAKEUP_HOST must be interruptible.

### 3.6.1. BT_EN

BT_EN is used to control the BT function of FG50V module. BT function will be enabled when BT_EN is at high level.

**Table 7: Pin Definition of BT_EN**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| BT_EN | 83 | DI | BT enable | 1.8 V power domain.<br>Active high.<br>It is suggested to pull down this pin with a 100 kΩ resistor. |

### 3.6.2. BT_WAKEUP_HOST* and HOST_WAKEUP_BT*

BT_WAKEUP_HOST and HOST_WAKEUP_BT are used to wake up the host and FG50V. If you use Quectel RG50x series as the host, these two pins can be left unconnected because the wakeup function can be achieved through BT UART.

**Table 8: Pin Definition of BT_WAKEUP_HOST and HOST_WAKEUP_BT**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| BT_WAKEUP_HOST | 61 | DO | BT wakes up host | 1.8 V power domain. |
| HOST_WAKEUP_BT | 60 | DI | Host wakes up BT | 1.8 V power domain.<br>Externally pull this pin down. |

**NOTE**

"*" means under development.

### 3.6.3. PCM Interface*

The PCM interface is for audio over Bluetooth phone. The following table shows the pin definition of PCM interface.

**Table 10: Pin Definition of PCM Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| PCM_DIN | 76 | DI | PCM data input | 1.8 V power domain. |
| PCM_SYNC | 35 | DI | PCM data frame sync | 1.8 V power domain. |
| PCM_CLK | 37 | DI | PCM clock | 1.8 V power domain. |
| PCM_DOUT | 36 | DO | PCM data output | 1.8 V power domain.<br>Externally pull this pin up to VDD_IO. |

The following figure shows the PCM interface connection between FG50V and the host.

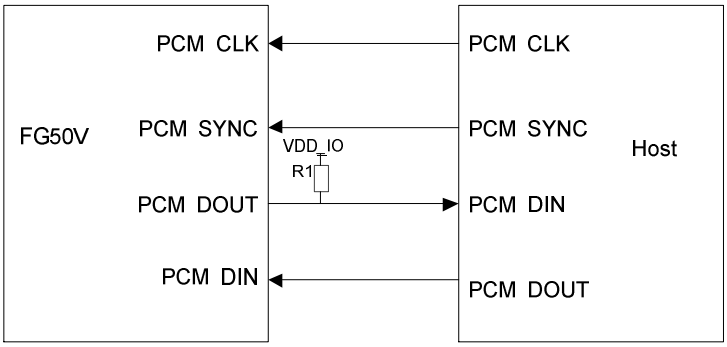



**Figure 7: PCM Interface Connection**

**NOTE**

"*" means under development.

### 3.6.4. UART Interface

FG50V supports an HCI UART as defined in *Bluetooth Core Specification Version 4.0*. In addition, the UART interface also supports software (in-band) sleep control of Bluetooth with Quectel RG50xQ series. You can also choose other 5G modules upon validation tests. If you have any questions, please contact Quectel Technical Support.

The following table shows the pin definition of UART interface.

**Table 11: Pin Definition of UART Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| BT_RTS | 77 | DO | BT UART request to send | 1.8 V power domain. |
| BT_CTS | 38 | DI | BT UART clear to send | 1.8 V power domain. |
| BT_TXD | 39 | DO | BT UART transmit | 1.8 V power domain. |
| BT_RXD | 78 | DI | BT UART receive | 1.8 V power domain. |

## 3.7. Conexistence Interface

FG50V supports 2.4G WWAN & WLAN/BT coexistence (with coexistence UART) and 5G WWAN & WLAN coexistence.

The following table shows the pin definition of coexistence interface.

**Table 9: Pin Definition of Coexistence Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| COEX_TXD | 59 | DO | 2.4G WWAN & WLAN/BT coexistence transmit | 1.8 V power domain.<br>If unused, keep these pins open. |
| COEX_RXD | 16 | DI | 2.4G WWAN & WLAN/BT coexistence receive | |
| LAA_AS_EN | 82 | DI | Allows LAA/n79 to control WLAN xFEM during WLAN sleep mode | |
| LAA_TXEN | 41 | DI | WLAN xFEM control to enable LAA/n79 transmit | |
| LAA_RX | 81 | DI | WLAN xFEM control for LAA/n79 receiver | |
| WLAN_TXEN | 42 | DO | WLAN xFEM control to enable WLAN transmit | |
| PA_MUTE | 80 | DI | WLAN xFEM control to disable WLAN PA | |

The following figure shows the coexistence interface connection between FG50V and Quectel RG50xQ series. You can also choose other 5G modules upon validation tests. If you have any questions, please contact Quectel Technical Support.

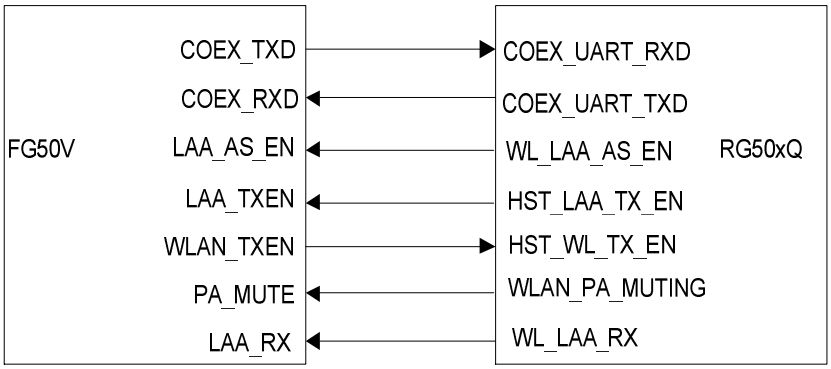



**Figure 8: Coexistence Interface Connection**

## 3.8. WLAN_SLP_CLK Interface

The 32.768 kHz clock is used in low power modes, such as IEEE power saving mode and sleep mode. It serves as a timer to determine when to wake up the FG50V module to receive signals in various power saving schemes, and to maintain basic logic operations when the module is in sleep mode.

**Table 10: Pin Definition of WLAN_SLP_CLK Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| WLAN_SLP_CLK | 15 | DI | WLAN sleep clock | If unused, keep this pin open. |

## 3.9. Others Interfaces

### 3.9.1. SW_CTRL*

The following table shows the pin definition of SW_CTRL.

**Table 11: Pin Definition of SW_CTRL**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| SW_CTRL | 57 | DO | Switch control | 1.8 V power domain.<br>Active high.<br>If unused, keep this pin open. |

The following figure shows the reference design for SW_CTRL connection between FG50V and the host.

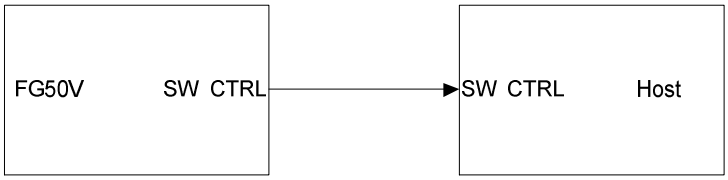



**Figure 9: SW_CTRL Connection**

**NOTE**

"*" means under development.

### 3.9.2. WLAN Debug Interface

The following table shows the pin definition of WLAN debug interface. Connect this interface to the test points in your application.

**Table 12: Pin Definition of WLAN Debug Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| WLAN_DBG_TXD | 21 | DO | WLAN debug UART transmit | 1.8 V power domain.<br>If unused, keep these pins open. |
| WLAN_DBG_RXD | 65 | DI | WLAN debug UART receive | |

### 3.9.3. BT Debug Interface

The following table shows the pin definition of BT debug interface. Connect this interface to the test points in your application.

**Table 13: Pin Definition of BT Debug interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| BT_DBG_TXD | 23 | DO | BT debug UART transmit | 1.8 V power domain.<br>If unused, keep these pins open. |
| BT_DBG_RXD | 22 | DI | BT debug UART receive | |

## 3.10. RF Antenna Interfaces

The following table shows the pin definition of RF antenna interfaces.

**Table 14: Pin Definition of RF Antenna Interfaces**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| ANT_WIFI0 | 28 | IO | BT and WLAN antenna interface | 50 Ω impedance |
| ANT_WIFI1 | 33 | IO | WLAN antenna interface | 50 Ω impedance |
| ANT_BT* | 25 | IO | Reserved dedicated BT antenna interface | 50 Ω impedance |

**NOTE**

"*" means under development.

### 3.10.1. Operating Frequency

**Table 15: Operating Frequency of the Module**

| Feature | Frequency | Unit |
|---|---|---|
| 2.4 GHz WLAN | 2.400–2.4835 | GHz |
| 5 GHz WLAN | 5.150–5.850 | GHz |
| BT | 2.402–2.480 | GHz |

### 3.10.2. Reference Design of RF Antenna Interfaces

FG50V provides three RF antenna interfaces for antenna connection. The following reference circuit design shows an example with ANT_WIFI0. For the other RF antenna interfaces, the reference design is the same.

It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (C1, C2, R1) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

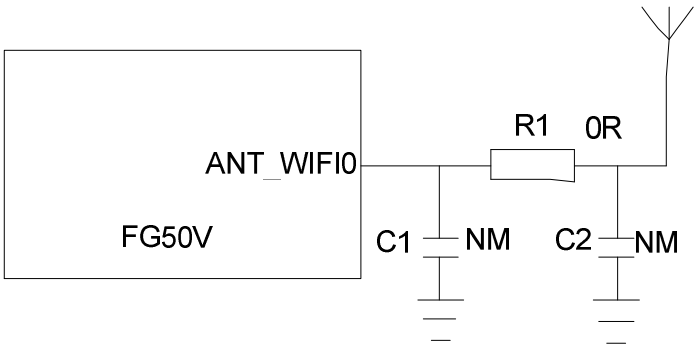



**Figure 10: Reference Circuit for RF Antenna Interfaces**

### 3.10.3. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

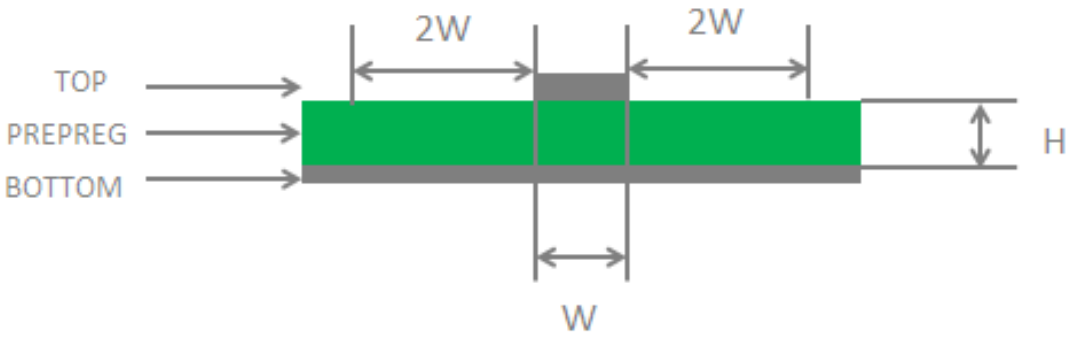



**Figure 11: Microstrip Design on a 2-layer PCB**

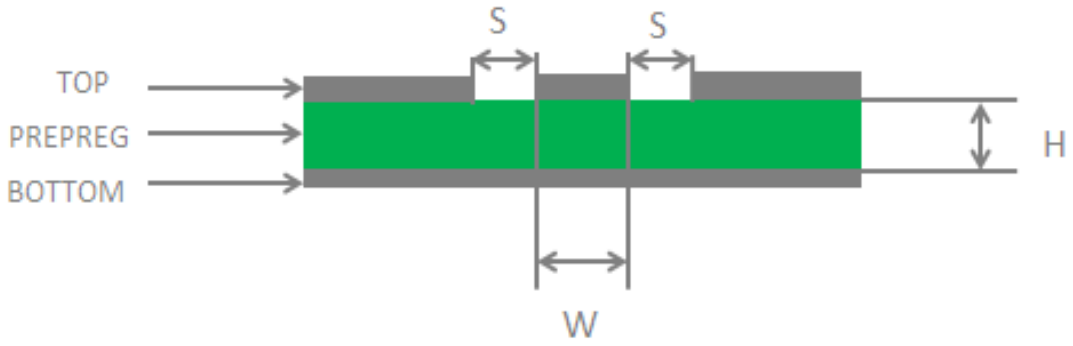


**Figure 12: Coplanar Waveguide Design on a 2-layer PCB**

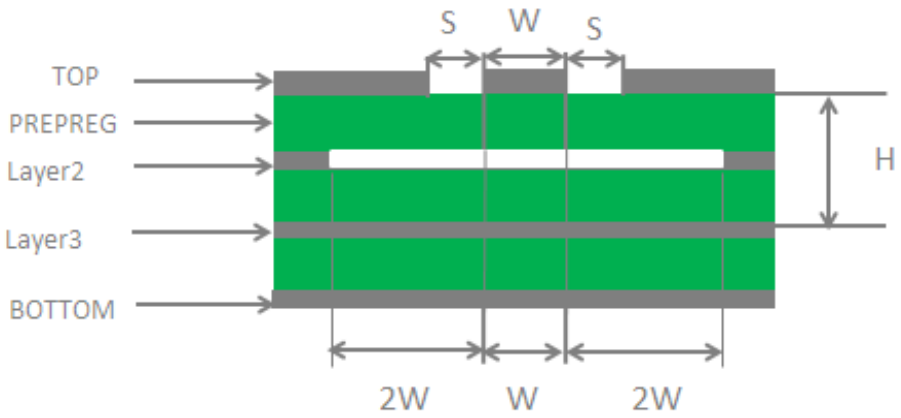



**Figure 13: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)**

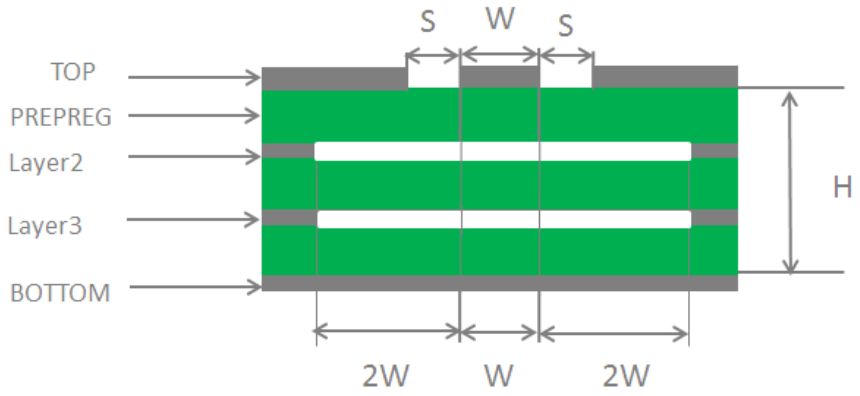



**Figure 14: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)**

To ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between

the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [3]***.

### 3.10.4. Antenna Requirements

The following table shows the requirements for antennas.

**Table 16: Antenna Requirements**

| Type | Requirements |
|---|---|
| Frequency Range | 2.400–2.4835 GHz<br>5.180–5.825 GHz |
| VSWR | < 2:1 (Recommended) |
| Gain | 5.38 dBi (Typ.) |
| Max Input Power | 50 W |
| Input Impedance | 50 Ω |
| Polarization Type | Vertical |
| Cable insertion loss | < 1 dB |

### 3.10.5. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

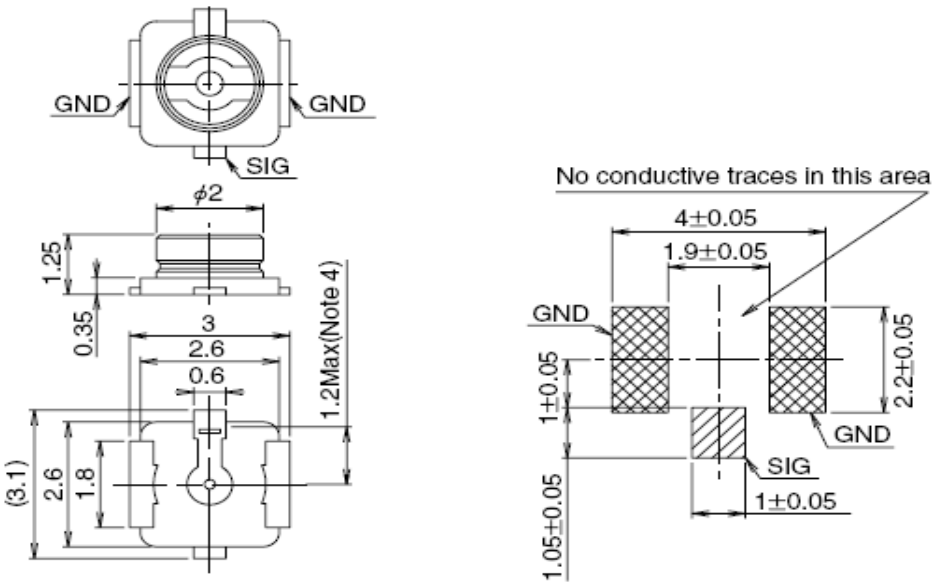



**Figure 15: Dimensions of the U.FL-R-SMT Connector (Unit: mm)**

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

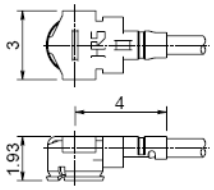
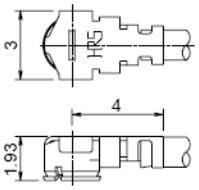
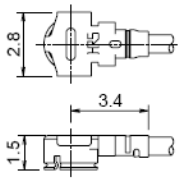
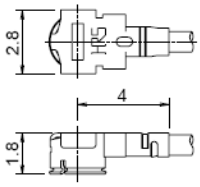
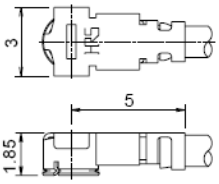
| Part No. | U.FL-LP-040 | U.FL-LP-066 | U.FL-LP(V)-040 | U.FL-LP-062 | U.FL-LP-088 |
|---|---|---|---|---|---|
| |  |  |  |  |  |
| Mated Height | 2.5mm Max.<br>(2.4mm Nom.) | 2.5mm Max.<br>(2.4mm Nom.) | 2.0mm Max.<br>(1.9mm Nom.) | 2.4mm Max.<br>(2.3mm Nom.) | 2.4mm Max.<br>(2.3mm Nom.) |
| Applicable cable | Dia. 0.81mm<br>Coaxial cable | Dia. 1.13mm and<br>Dia. 1.32mm<br>Coaxial cable | Dia. 0.81mm<br>Coaxial cable | Dia. 1mm<br>Coaxial cable | Dia. 1.37mm<br>Coaxial cable |
| Weight (mg) | 53.7 | 59.1 | 34.8 | 45.5 | 71.7 |
| RoHS | YES | | | | |

**Figure 16: Mechanicals of UF.L-LP Connectors (Unit: mm)**

The following figure describes the space factor of mated connector

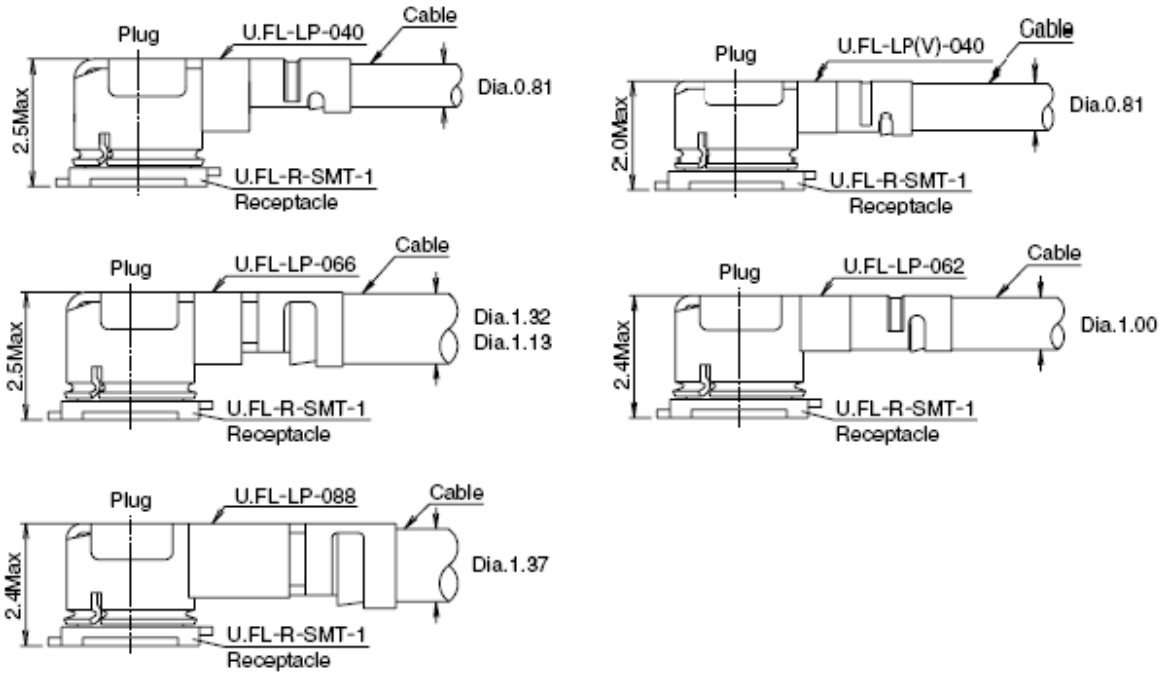



**Figure 17: Space Factor of Mated Connector (Unit: mm)**

For more details, visit http://www.hirose.com.

# 4 Reliability, Radio and Electrical Characteristics

## 4.1. General Description

This chapter mainly introduces electrical and radio characteristics of FG50V module. The details are listed in the subsequent chapters.

## 4.2. Electrical Characteristics

The following table shows the absolute maximum ratings.

**Table 17: Absolute Maximum Ratings**

| Parameter | Min. | Max. | Unit |
|---|---|---|---|
| VDD_CORE_VL | -0.3 | $V_{DDX}$ + 0.2 | V |
| VDD_CORE_VM | -0.3 | $V_{DDX}$ + 0.2 | V |
| VDD_CORE_VH | -0.3 | $V_{DDX}$ + 0.2 | V |
| VDD_IO | -0.3 | $V_{DDX}$ + 0.2 | V |
| VDD_RF | -0.3 | 4.8 | V |
| Digital I/O Input Voltage | -0.3 | VDD_IO + 0.2 | V |

**NOTE**

$V_{DDX}$ is the external supply voltage for the corresponding power input pins.

The following table shows the recommended operating conditions of the module.

**Table 18: Recommended Operating Conditions**

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| VDD_CORE_VL | 0.9 | 0.95 | 1.0 | V |
| VDD_CORE_VM | 1.28 | 1.35 | 1.42 | V |
| VDD_CORE_VH | 1.85 | 1.95 | 2.05 | V |
| VDD_IO | 1.7 | 1.8 | 1.9 | V |
| VDD_RF | 3.3 | 3.85 | 4.25 | V |

## 4.3. I/O Interface Characteristics

The following table shows the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

**Table 19: General DC Electrical Characteristics**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | 0.65 × VDD_IO | VDD_IO + 0.3 | V |
| $V_{IL}$ | Low Level Input Voltage | -0.3 | 0.35 × VDD_IO | V |
| $V_{OH}$ | High Level Output Voltage | VDD_IO - 0.45 | VDD_IO | V |
| $V_{OL}$ | Low Level Output Voltage | 0 | 0.45 | V |
| $I_{IL}$ | Input Leakage Current | TBD | TBD | μA |

## 4.4. Operating and Storage Temperatures

**Table 20: Operating and storage Temperatures**

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Operating Temperature Range [1)] | -40 | 25 | +85 | ºC |
| Storage Temperature Range | -40 | | +95 | ºC |

**NOTE**

[1)] Within operating temperature range, the module is IEEE compliant.

## 4.5. Current Consumption

The following tables show the current consumption of the module in different modes.

### 4.5.1. Current Consumption in Low Power Modes

**Table 21: Current Consumption of the Module (Low Power Modes, Unit: mm)**

| Module State | Wi-Fi State | VDD_CORE_VL (0.95 V) | VDD_CORE_ VM (1.35 V) | VDD_CORE_VH (1.95 V) | VDD_IO (1.8 V) | VDD_RF (3.85 V) |
|---|---|---|---|---|---|---|
| OFF [1)] | Wi-Fi disabled | 0.0479 | 0.210 | 0.001 | 0.001 | 0.018 |
| Idle [2)] | Wi-Fi enabled | 117.75 | 28.91 | 74.15 | 23.69 | 0.218 |

**NOTES**

1. [1)] OFF: A series of commands can be used to set the module to OFF state (Wi-Fi disabled). In this state, the sleep clock is disabled and no data is saved.
2. [2)] Idle: In this state, Wi-Fi is enabled but no device is connected.
3. For more detailed commands for Wi-Fi state, see ***document [4]***.
4. The current consumption above includes both ANT_WIFI0 and ANT_WIFI1.

### 4.5.2. Current Consumption in Normal Operation

**Table 22: Current Consumption of the Module (Normal Operation, Unit: mA)**

| Description | Conditions | VDD_CORE_VL (0.95 V) | VDD_CORE_VM (1.35 V) | VDD_CORE_VH (1.95 V) | VDD_IO (1.8 V) | VDD_RF (3.85 V) |
|---|---|---|---|---|---|---|
| 802.11b | TX (2.4 GHz) 1 Mbps | 460.7 | 185.5 | 127.0 | 2.3 | 565.1 |
| | TX (2.4 GHz) 11 Mbps | 501.9 | 179.7 | 118.3 | 2.5 | 445.1 |
| 802.11g | TX (2.4 GHz) 6 Mbps | 460.5 | 175.9 | 123.3 | 2.2 | 521.3 |
| | TX (2.4 GHz) 54 Mbps | 512.2 | 174.2 | 115.1 | 2.7 | 330.4 |
| 802.11n | TX (2.4 GHz) HT20 MCS0 | 442.6 | 170.6 | 120.7 | 2.4 | 521.2 |
| | TX (2.4 GHz) HT20 MCS7 | 443.9 | 170.2 | 120.3 | 2.4 | 472.9 |
| | TX (2.4 GHz) HT40 MCS0 | 475.8 | 171.2 | 120.2 | 2.4 | 517.2 |
| | TX (2.4 GHz) HT40 MCS7 | 476.1 | 170.7 | 120.0 | 2.4 | 495.2 |
| | TX (5 GHz) HT20 MCS0 | 418.7 | 206.8 | 118.0 | 2.7 | 497.2 |
| | TX (5 GHz) HT20 MCS7 | 421.3 | 206.6 | 117.4 | 2.8 | 427.1 |
| | TX (5 GHz) HT40 MCS0 | 452.7 | 207.6 | 117.5 | 2.8 | 504.3 |
| | TX (5 GHz) HT40 MCS7 | 451.9 | 207.2 | 116.9 | 2.8 | 429.6 |
| 802.11a | TX (5 GHz) 6 Mbps | 438.2 | 212.6 | 120.5 | 2.9 | 499.5 |
| | TX (5 GHz) 54 Mbps | 479.3 | 200.6 | 111.7 | 3.0 | 237.9 |
| 802.11ac | TX (5 GHz) VHT20 MCS0 | 432.1 | 201.5 | 117.9 | 2.8 | 481.0 |
| | TX (5 GHz) VHT20 MCS8 | 418.1 | 200.1 | 117.2 | 2.8 | 408.4 |
| | TX (5 GHz) VHT40 MCS0 | 453.6 | 201.8 | 118.0 | 2.8 | 486.7 |
| | TX (5 GHz) VHT40 MCS9 | 451.4 | 201.1 | 117.3 | 2.8 | 410.5 |

| | | | | | | |
|---|---|---|---|---|---|---|
| 802.11ax | TX (5 GHz) VHT80 MCS0 | 571.9 | 201.7 | 116.8 | 2.8 | 488.7 |
| | TX (5 GHz) VHT80 MCS9 | 570.0 | 203.1 | 117.1 | 2.8 | 409.6 |
| | TX (2.4 GHz) HE20 MCS0 | 452.0 | 174.6 | 120.9 | 2.4 | 512.1 |
| | TX (2.4 GHz) HE20 MCS11 | 449.1 | 174.2 | 119.7 | 2.5 | 441.9 |
| | TX (2.4 GHz) HE40 MCS0 | 481.8 | 175.4 | 120.4 | 2.5 | 515.3 |
| | TX (2.4 GHz) HE40 MCS11 | 483.4 | 174.5 | 119.6 | 2.4 | 443.2 |
| | TX (5 GHz) HE20 MCS0 | 430.1 | 202.0 | 135.9 | 2.8 | 483.8 |
| | TX (5 GHz) HE20 MCS11 | 428.6 | 201.1 | 135.1 | 2.8 | 393.9 |
| | TX (5 GHz) HE40 MCS0 | 461.9 | 202.2 | 135.9 | 2.8 | 482.9 |
| | TX (5 GHz) HE40 MCS11 | 461.6 | 201.5 | 135.2 | 2.9 | 395.6 |
| | TX (5 GHz) HE80 MCS0 | 585.7 | 214.7 | 135.8 | 2.8 | 488.0 |
| | TX (5 GHz) HE80 MCS11 | 584.4 | 214.1 | 134.9 | 2.8 | 392.4 |

## 4.6. RF Performances

The following tables summarize the transmitting and receiving performances of FG50V.

### 4.6.1. Conducted RF Output Power

**Table 23: Conducted RF Output Power at 2.4 GHz**

| Frequency | Min. | Typ. | Unit |
|---|---|---|---|
| 802.11b @ 1 Mbps | 17.5 | 20 | dBm |

| | | | |
|---|---|---|---|
| 802.11b @ 11 Mbps | 17.5 | 20 | dBm |
| 802.11g @ 6 Mbps | 15 | 18.5 | dBm |
| 802.11g @ 54 Mbps | 14.5 | 17 | dBm |
| 802.11n, HT20 @ MCS0 | 15 | 18.5 | dBm |
| 802.11n, HT20 @ MCS7 | 13.5 | 16 | dBm |
| 802.11n, HT40 @ MCS0 | 15.5 | 18 | dBm |
| 802.11n, HT40 @ MCS7 | 13.5 | 16 | dBm |
| 802.11ax, HE20 @ MCS0 | 15.5 | 18 | dBm |
| 802.11ax, HE20 @ MCS11 | 10.5 | 13 | dBm |
| 802.11ax, HE40 @ MCS0 | 15.5 | 18 | dBm |
| 802.11ax, HE40 @ MCS11 | 10.5 | 13 | dBm |

**Table 24: Conducted RF Output Power at 5 GHz**

| Frequency | Min. | Typ. | Unit |
|---|---|---|---|
| 802.11a @ 6 Mbps | 15.5 | 18 | dBm |
| 802.11a @ 54 Mbps | 13 | 15.5 | dBm |
| 802.11n, HT20 @ MCS0 | 15.5 | 18 | dBm |
| 802.11n, HT20 @ MCS7 | 12.5 | 15 | dBm |
| 802.11n, HT40 @ MCS0 | 15.5 | 18 | dBm |
| 802.11n, HT40 @ MCS7 | 12.5 | 15 | dBm |
| 802.11ac, VHT20 @ MCS0 | 15 | 17.5 | dBm |
| 802.11ac, VHT20 @ MCS8 | 11.5 | 14 | dBm |
| 802.11ac, VHT40 @ MCS0 | 15 | 17.5 | dBm |
| 802.11ac, VHT40 @ MCS9 | 11.5 | 14 | dBm |
| 802.11ac, VHT80 @ MCS0 | 15 | 17.5 | dBm |

| | | | |
|---|---|---|---|
| 802.11ac, VHT80 @ MCS9 | 11.5 | 14 | dBm |
| 802.11ax, HE20 @ MCS0 | 15 | 17.5 | dBm |
| 802.11ax, HE20 @ MCS11 | 10.5 | 13 | dBm |
| 802.11ax, HE40 @ MCS0 | 15 | 17.5 | dBm |
| 802.11ax, HE40 @ MCS11 | 10.5 | 13 | dBm |
| 802.11ax, HE80 @ MCS0 | 15 | 17.5 | dBm |
| 802.11ax, HE80 @ MCS11 | 10.5 | 13 | dBm |

### 4.6.2. Conducted RF Receiving Sensitivity

**Table 25: Conducted RF Receiving Sensitivity at 2.4 GHz**

| Frequency | Receiving Sensitivity (Typ.) |
|---|---|
| 802.11b @ 1 Mbps | -96 dBm |
| 802.11b @ 11 Mbps | -89 dBm |
| 802.11g @ 6 Mbps | -93 dBm |
| 802.11g @ 54 Mbps | -74 dBm |
| 802.11n, HT20 @ MCS0 | -93 dBm |
| 802.11n, HT20 @ MCS7 | -73 dBm |
| 802.11n, HT40 @ MCS0 | -91 dBm |
| 802.11n, HT40 @ MCS7 | -70 dBm |
| 802.11ax, HE20 @ MCS0 | -93 dBm |
| 802.11ax, HE20 @ MCS11 | -65 dBm |
| 802.11ax, HE40 @ MCS0 | -91 dBm |
| 802.11ax, HE40 @ MCS11 | -62 dBm |

**Table 26: Conducted RF Receiving Sensitivity at 5 GHz**

| Frequency | Receiving Sensitivity (Typ.) |
|---|---|
| 802.11a @ 6 Mbps | -94 dBm |
| 802.11a @ 54 Mbps | -75 dBm |
| 802.11n, HT20 @ MCS0 | -93 dBm |
| 802.11n, HT20 @ MCS7 | -75 dBm |
| 802.11n, HT40 @ MCS0 | -91 dBm |
| 802.11n, HT40 @ MCS7 | -72 dBm |
| 802.11ac, VHT20 @ MCS0 | -94 dBm |
| 802.11ac, VHT20 @ MCS8 | -72 dBm |
| 802.11ac, VHT40 @ MCS0 | -92 dBm |
| 802.11ac, VHT40 @ MCS9 | -67 dBm |
| 802.11ac, VHT80 @ MCS0 | -89 dBm |
| 802.11ac, VHT80 @ MCS9 | -62 dBm |
| 802.11ax, HE20 @ MCS0 | -94 dBm |
| 802.11ax, HE20 @ MCS11 | -65 dBm |
| 802.11ax, HE40 @ MCS0 | -92 dBm |
| 802.11ax, HE40 @ MCS11 | -63 dBm |
| 802.11ax, HE80 @ MCS0 | -89 dBm |
| 802.11ax, HE80 @ MCS11 | -59 dBm |

## 4.7. Electrostatic Discharge

The module is not protected against Electrostatic Discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module electrostatic discharge characteristics.

**Table 27: Electrostatic Discharge Characteristics**

| Tested Points | Contact Discharge | Air Discharge | Unit |
|---|---|---|---|
| VDD_RF, GND | ±6 | ±10 | kV |
| Antenna Interfaces | ±6 | ±10 | kV |
| Other Interfaces | ±0.5 | ±1 | kV |

# 5 Mechanical Dimensions

This chapter describes the mechanical dimensions of FG50V module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.05 mm unless otherwise specified.

## 5.1. Mechanical Dimensions of the Module

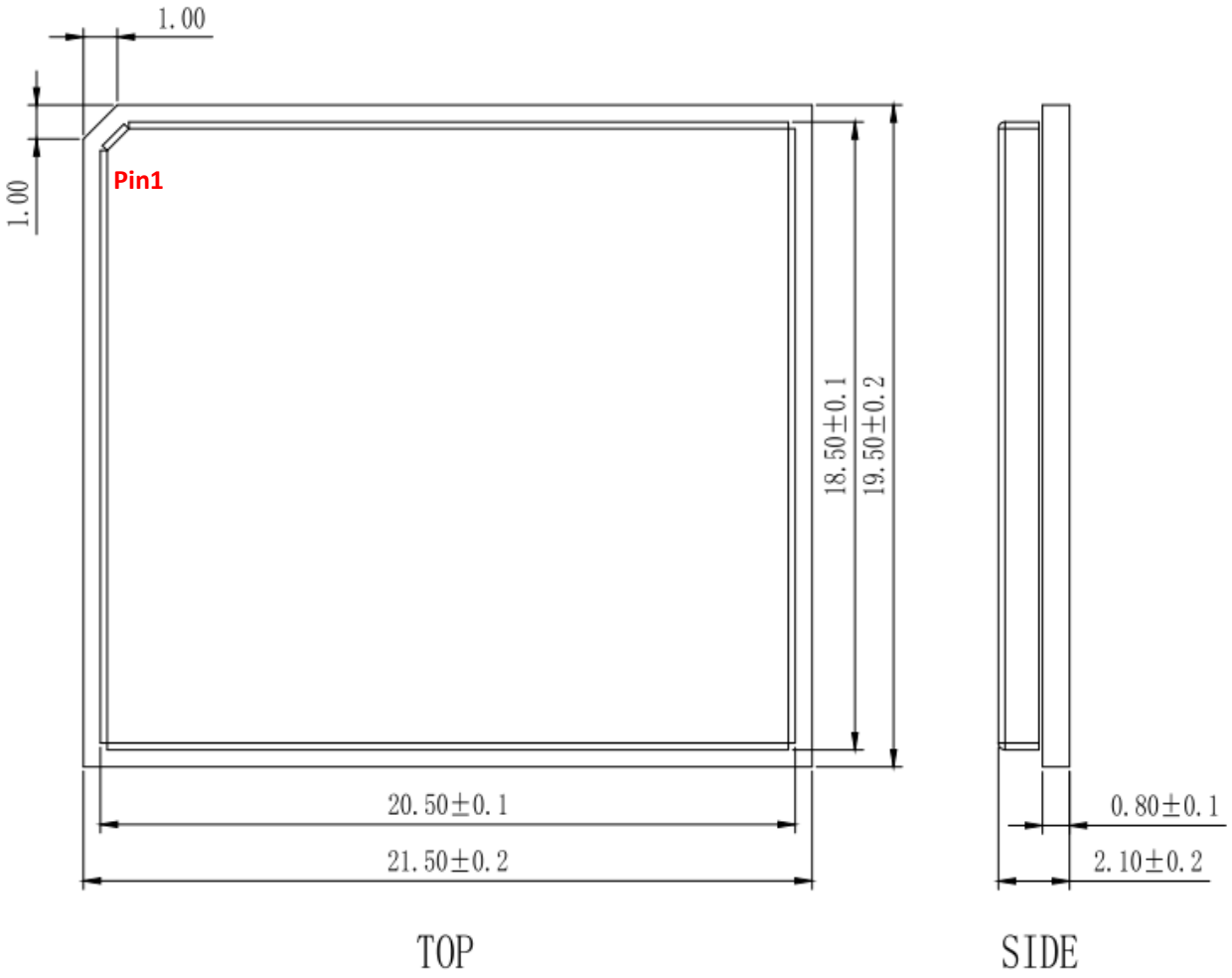



**Figure 18: FG50V Top and Side Dimensions (Top and Side View)**

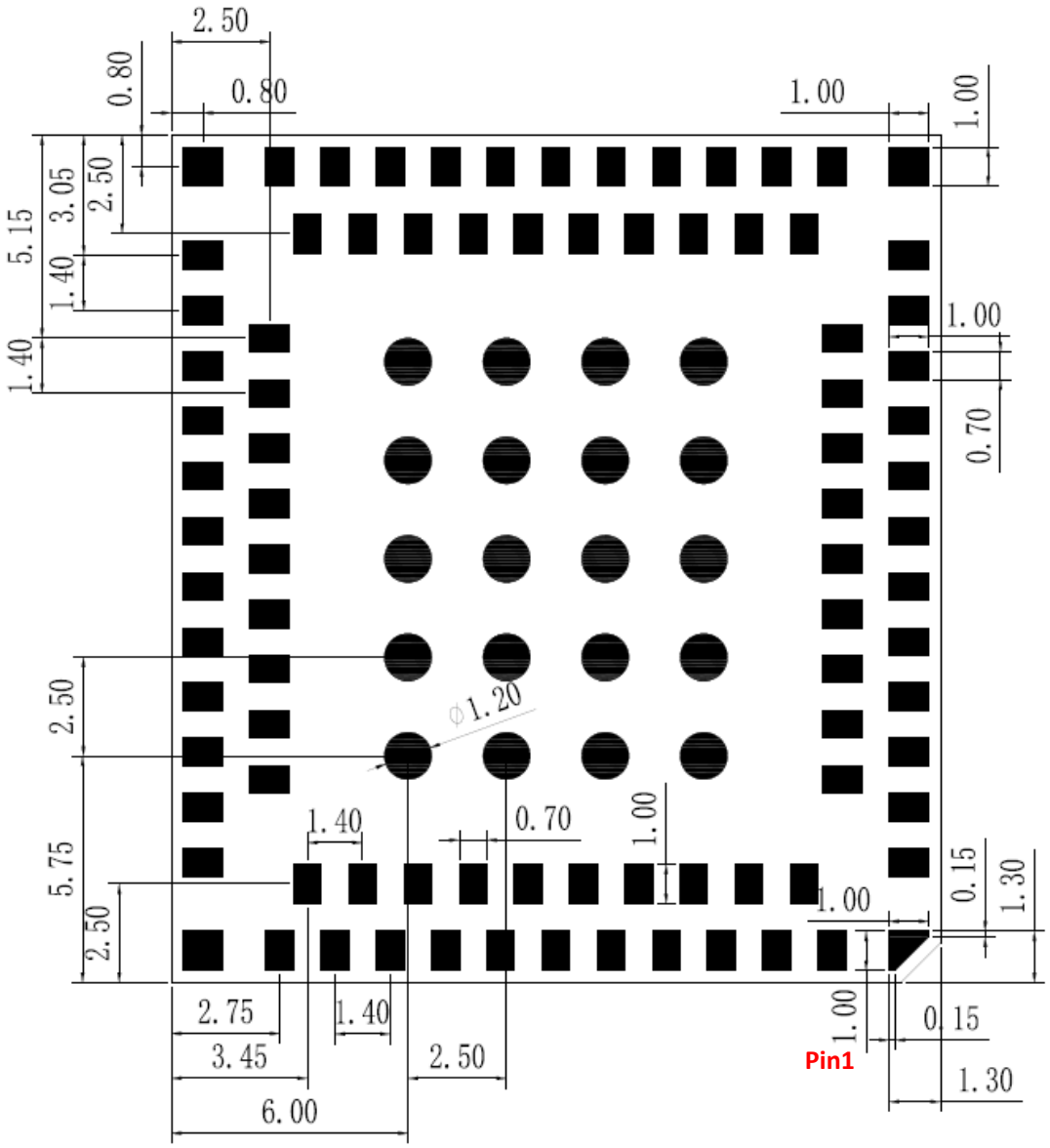



**Figure 19: FG50V Bottom Dimension (Bottom View)**

**NOTE**

The package warpage level of the module conforms to *JEITA ED-7306* standard.

## 5.2. Recommended Footprint

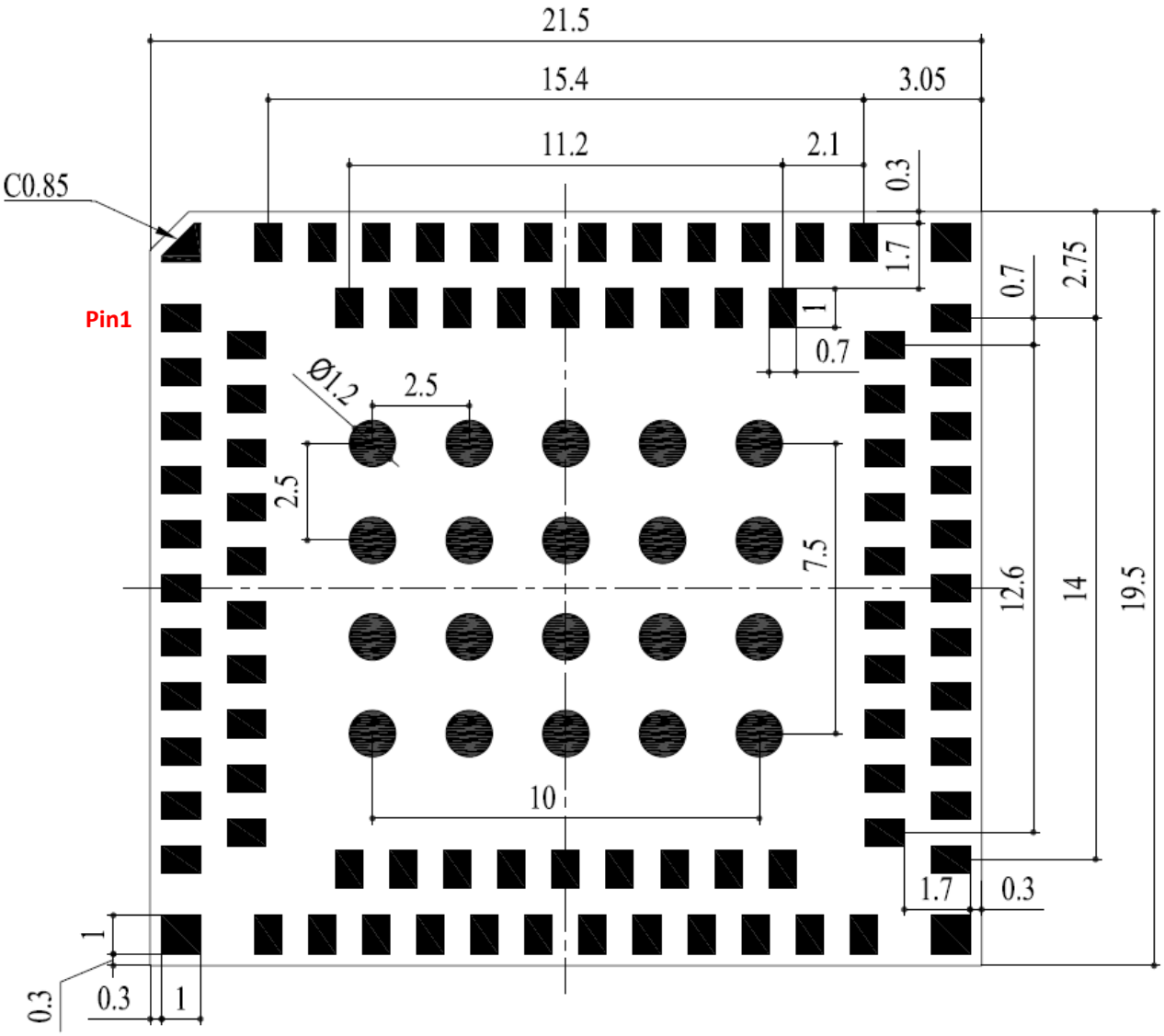



**Figure 20: Recommended Footprint (Top View)**

**NOTES**

1. For easy maintenance of this module, keep at least 3 mm between the module and other components on the motherboard.
2. Keep all RESERVED pins open.

## 5.3. Top and Bottom Views of the Module


**Figure 21: Top View of the Module**

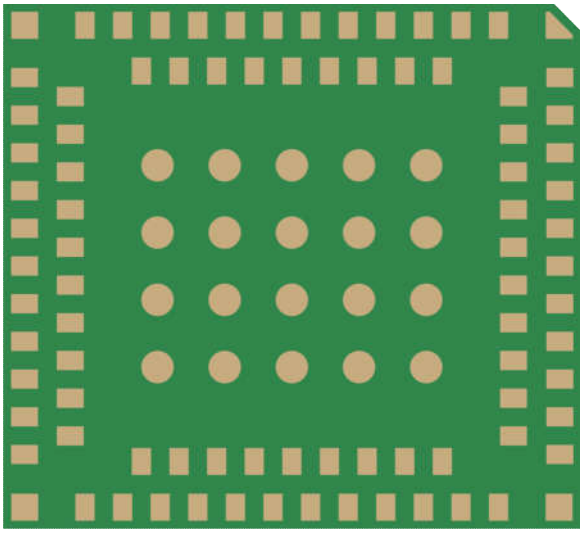


**Figure 22: Bottom View of the Module**

**NOTE**

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

# 6 Storage, Manufacturing and Packaging

## 6.1. Storage

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [1)] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 24 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

NOTES

1. [1)] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*.
2. To avoid blistering, layer separation and other soldering issues, it is forbidden to expose the modules to the air for a long time. If the temperature and moisture do not conform to *IPC/JEDEC J-STD-033* or the relative moisture is over 60%, it is recommended to start the solder reflow process within 24 hours after the package is removed. And do not remove the packages of tremendous modules if they are not ready for soldering.
3. Please take the module out of the packaging and put it on high-temperature resistant fixtures before the baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for baking procedure.

## 6.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [5]***.

It is suggested that the peak reflow temperature is 238–246 ºC, and the absolute maximum reflow temperature is 246 ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

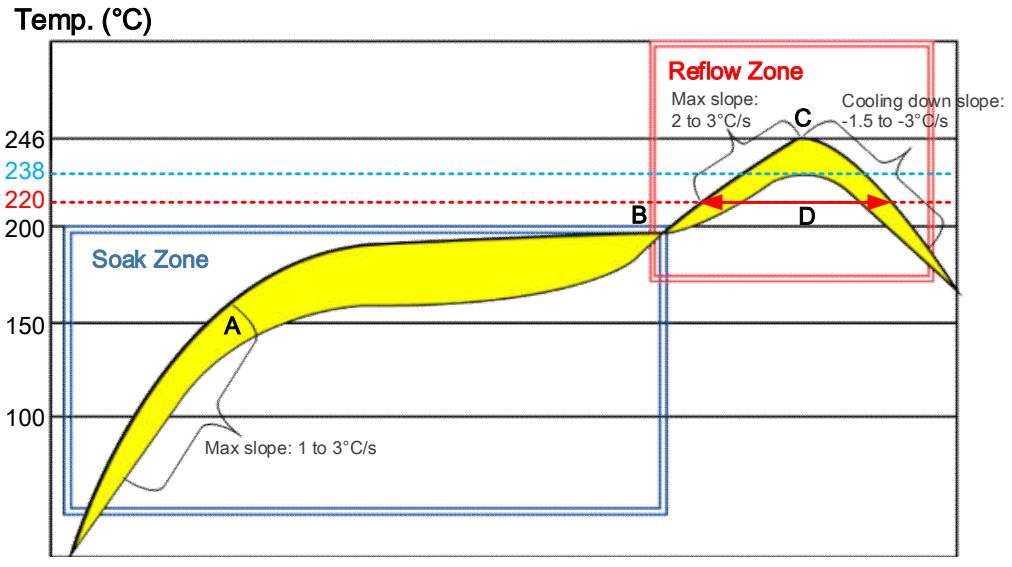



**Figure 23: Recommended Reflow Soldering Thermal Profile**

**Table 28: Recommended Thermal Profile Parameters**

| Factor | Recommendation |
|---|---|

| | |
|---|---|
| **Soak Zone** | |
| Max slope | 1–3 °C/s |
| Soak time (between A and B: 150 °C and 200 °C) | 70–120 s |
| **Reflow Zone** | |
| Max slope | 2–3 °C/s |
| Reflow time (D: over 220 °C) | 45–70 s |
| Max temperature | 238 °C to 246 °C |
| Cooling down slope | -1.5 to -3 °C/s |
| **Reflow Cycle** | |
| Max reflow cycle | 1 |

## 6.3. Packaging

FG50V is packaged in tape and reel carriers. Each reel is 330 mm in diameter and contains 200 modules. The dimensions of tape and reel will be added in the updated version of this document.

**Table 30: Reel Packaging**

| Model Name | MOQ for MP | Minimum Package: TBD | Minimum Package TBD |
|---|---|---|---|
| FG50V | TBD | Size: TBD<br>N.W: TBD<br>G.W: TBD | Size: TBD<br>N.W: TBD<br>G.W: TBD |

# 7 Appendix References

**Table 29: Related Documents**

| SN | Document Name | Description |
|---|---|---|
| [1] | Quectel_5G_EVB_User_Guide | EVB user guide for Quectel 5G modules |
| [2] | Quectel_FG50V_Reference_Design | FG50V reference design |
| [3] | Quectel_RF_Layout_Application_Note | RF layout application note |
| [4] | Quectel_RG500Q_Series_Wi-Fi_Application_Note | FG50V Wi-Fi_application note |
| [5] | Quectel_Module_Secondary_SMT_Application_Note | Module secondary SMT application note |

**Table 30: Terms and Abbreviations**

| Abbreviation | Description |
|---|---|
| AP | Access Point |
| BPF | Band-Pass Filter |
| BPSK | Binary Phase Shift Keying |
| BT | Bluetooth |
| CCK | Complementary Code Keying |
| CTS | Clear To Send |
| ESD | Electrostatic Discharge |
| EVB | Evaluation Board |
| FEM | Front-End Module |
| GND | Ground |
| HCI | Host Controller Interface |

| | |
|---|---|
| HE | High Efficiency |
| HT | High Throughput |
| IEEE | Institute of Electrical and Electronics Engineers |
| $I_{IL}$ | Input Leakage Current |
| I/O | Input/Output |
| LNA | Low-Noise Amplifier |
| LTE | Long Term Evolution |
| Mbps | Megabits per second |
| MCS | Modulation and Coding Scheme |
| MOQ | Minimum Order Quantity |
| PA | Power Amplifier |
| PCB | Printed Circuit Board |
| PCM | Pulse Code Modulation |
| QAM | Quadrature Amplitude Modulation |
| QPSK | Quadrature Phase Shift Keying |
| RF | Radio Frequency |
| RoHS | Restriction of Hazardous Substances |
| RTS | Request To Send |
| RX | Receive |
| TBD | To Be Determined |
| TX | Transmit |
| UART | Universal Asynchronous Receiver/Transmitter |
| USB | Universal Serial Bus |
| VHT | Very High Throughput |
| $V_{IH}$max | Maximum Input High Level Voltage Value |

| | |
|---|---|
| $V_{IH}$min | Minimum Input High Level Voltage Value |
| $V_{IL}$max | Maximum Input Low Level Voltage Value |
| $V_{IL}$min | Minimum Input Low Level Voltage Value |
| $V_{OL}$max | Maximum Output Low Level Voltage Value |
| $V_{OH}$min | Minimum Output High Level Voltage Value |
| VSWR | Voltage Standing Wave Ratio |
| Wi-Fi | Wireless-Fidelity |
| WLAN | Wireless Local Area Network |