EC200T-AU Series

Hardware Design

LTE Standard Module Series

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About the Document

Revision History

Version	Date	Author	Description
1.0	2019-09-12	Jaye SANG/ Niko WU	Initial
1.1	2020-08-10	Jaye SANG/ Owen WEI	1. Added related information of EC200T-AU. 2. Deleted B5 of EC200T-EU. 3. Updated the storage of SMS (Table 2) 4. Updated the pin assignment diagram (Figure 2). 5. Updated the pin description (Table 5). 6. Added the note of connecting between RTS and CTS pins between module and MCU for hardware flow control (Chapter 3.10). 7. Updated the comments of SD card interface pins (Chapter 3.12). 8. The AT command used for configuring MAIN_RI behavior (Chapter 3.17). 9. Updated the electrostatics discharge characteristics (25 ºC, 45% Relative Humidity) of VBAT, GND pins and all antenna interfaces (Table 41). 10. Updated the description of module storage (Chapter 7.1) 11. Update the description of manufacturing and soldering (Chapter 7.2).

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1 Introduction

This document defines the EC200T series module and describes its air interface and hardware interfaces which are connected with your applications.

This document can help you quickly understand module interface specifications, electrical and mechanical details, as well as other related information of EC200T series module. Associated with application note and user guide, you can use EC200T series module to design and set up wireless applications easily.

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.

And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based time-averaging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.

2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

3.A label with the following statements must be attached to the host end product: This device contains FCC ID: XMR202011EC200TAU.

4.To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

- GSM850 :≤8.571dBi
- GSM1900 :≤10.03dBi
- LTE Band2/25:≤11.000dBi

- ❒ WCDMA Band II/LTE Band2/ LTE Band 7 :≤8.000dBi
- ❒ WCDMA Band IV/ LTE Band 4 / LTE Band 66:≤5.000dBi
- ❒ WCDMA Band V / LTE Band 5:≤9.541dBi

5. This module must not transmit simultaneously with any other antenna or transmitter

6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

For this device, OEM integrators must be provided with labeling instructions of finished products. Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module:"Contains Transmitter Module FCC ID: XMR202011EC200TAU" or "Contains FCC ID: XMR202011EC200TAU" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating EC200T series module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergent help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.

In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as mobile phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders.

2 Product Concept

2.1. General Description

EC200T is a series of LTE-FDD, LTE-TDD, WCDMA and GSM wireless communication module with receive diversity, which provides data connectivity on LTE-FDD, LTE-TDD, HSDPA, HSUPA, HSPA+, WCDMA, EDGE and GPRS networks. It also provides voice functionality for your specific applications. EC200T series contains 3 variants: EC200T-CN, EC200T-EU and EC200T-AU*. You can choose a dedicated type based on the region or operator. The following table shows the frequency bands of EC200T series module.

Table 1: Frequency Bands of EC200T-CN Module

Network Type	Bands
LTE-FDD (with Rx-diversity)[1)]	B1/B3/B5/B8
LTE-TDD (with Rx-diversity)[1)]	B34/B38/B39/B40/B41
WCDMA	B1/B5/B8
GSM	900/1800MHz

Table 2: Frequency Bands of EC200T-EU Module

Network Type	Bands
LTE-FDD (with Rx-diversity)[1)]	B1/B3/B7/B8/B20/B28
LTE-TDD (with Rx-diversity)[1)]	B38/B40/B41
WCDMA	B1/B8
GSM	900/1800MHz

Table 3: Frequency Bands of EC200T-AU* Module

Network Type	Bands
LTE-FDD (with Rx-diversity)[1)]	B1/B2/B3/B4/B5/B7/B8/B28/B66
LTE-TDD (with Rx-diversity)[1)]	B40
WCDMA	B1/B2/B4/B5/B8
GSM	850/900/1800/1900 MHz

With a compact profile of 29.0 mm × 32.0 mm × 2.4 mm, EC200T series can meet almost all requirements for M2M applications such as automotive, metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, tablet PC, etc.

EC200T series is an SMD type module which can be embedded into applications through its 144-pin pads, including 80 LCC signal pads and 64 LGA pads.

NOTES

1. [1)] Rx-diversity is optional.
2. "*" means under development.

2.2. Key Features

The following table describes the detailed features of EC200T series module.

Table 4: Key Features of EC200T series Module

Feature	Details
Power Supply	Supply voltage: 3.4–4.5 V Typical supply voltage: 3.8 V
Transmitting Power	Class 4 (33 dBm ±2 dB) for EGSM900/GSM850 Class 1 (30 dBm ±2 dB) for DCS1800/PCS1900 Class E2 (27 dBm ±3 dB) for EGSM900/850 8-PSK Class E2 (26 dBm ±3 dB) for DCS1800/PCS1900 8-PSK Class 3 (24 dBm +1/-3 dB) for WCDMA bands Class 3 (23 dBm ±2 dB) for LTE-FDD bands Class 3 (23 dBm ±2 dB) for LTE-TDD bands

LTE Features	Supports up to non-CA Cat 4 FDD and TDD Supports 1.4/3/5/10/15/20 MHz RF bandwidth Supports MIMO in DL direction FDD: Max. 150 Mbps (DL), Max. 50 Mbps (UL) TDD: Max. 130 Mbps (DL), Max. 30 Mbps (UL)
UMTS Features	Supports 3GPP R7 HSDPA, HSUPA, HSPA+ and WCDMA Supports QPSK, 16-QAM modulation HSPA+: Max. 21 Mbps (DL) HSUPA: Max. 5.76 Mbps (UL) WCDMA: Max. 384 kbps (DL), Max. 384 kbps (UL)
GSM Features	**GPRS:** Supports GPRS multi-slot class 12 Coding scheme: CS-1/CS-2/CS-3/CS-4 Max. 85.6 kbps (DL), Max. 85.6 kbps (UL) **EDGE:** Supports EDGE multi-slot class 12 Supports GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: MCS 1-9 Uplink coding schemes: MCS 1-9 Max. 236.8 Kbps (DL), Max. 236.8 Kbps (UL)
Internet Protocol Features	Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS/FTPS/SSL/FILE/MQTT/MMS/SMTP*/SMTPS* protocols Supports PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) protocols which are usually used for PPP connection
SMS	Text and PDU mode Point-to-point MO and MT SMS cell broadcast SMS storage: ME&SM
(U)SIM Interface	Supports USIM/SIM card: 1.8 V, 3.0 V
Audio Features	Supports one digital audio interface: PCM interface GSM: HR/FR/EFR/AMR/AMR-WB WCDMA: AMR/AMR-WB Supports echo cancellation and noise suppression
PCM Interface	Used for audio function with external codec Supports 16-bit linear data format Supports short frame synchronization Supports master and slave modes
USB Interface	Compliant with USB 2.0 specification (slave only); the data transfer rate can reach up to 480 Mbps Used for AT command communication, data transmission, software debugging, firmware upgrade

	Supports USB serial drivers for: Windows 7/8/8.1/10, Linux 2.6/3.x/4.1–4.14, Android 4.x/5.x/6.x/7.x/8.x/9.x, etc.
UART Interfaces	**Main UART:** Used for AT command communication and data transmission Baud rates reach up to 1 Mbps, 115200 bps by default Supports RTS and CTS hardware flow control **Debug UART:** Used for the output of partial logs 115200 bps baud rate
SD Card Interface	Supports SD 3.0 protocol
WLAN Interface*	Supports SDIO 3.0 interface for WLAN
Rx-diversity	Supports LTE Rx-diversity
AT Commands	Compliant with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands
Network Indication	NET_MODE and NET_STATUS used to indicate the network connectivity status
Antenna Interfaces	Main antenna interface (ANT_MAIN) and Rx-diversity antenna interface (ANT_DIV) 50Ω impedance
Physical Characteristics	Size: (29.0 ±0.15) mm × (32.0 ±0.15) mm × (2.4 ±0.2) mm Weight: approx. 4.4 g
Temperature Range	Operation temperature range: -35 °C to +75 °C[1)] Extended temperature range: -40 °C to +85 °C[2)] Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	USB interface or FOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1)] Within operating temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.
3. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of EC200T series and illustrates the major functional parts.

- Power management
- Baseband
- Flash
- Radio frequency
- Peripheral interfaces

2.4. Evaluation Board

In order to help you develop applications with EC200T series, Quectel provides an evaluation board (UMTS & LTE EVB), USB to RS-232 converter cable, earphone, antenna and other peripherals to control or test the module. For more details, see ***document [4]***.

3 Application Interfaces

3.1. General Description

EC200T series is equipped with 80 LCC pins plus 64 LGA pins that can be connected to cellular application platform. The subsequent chapters will provide detailed descriptions of the following interfaces.

- Power supply
- (U)SIM interface
- USB interface
- UART interfaces
- PCM and I2C interfaces
- SD card interface
- WLAN interface*
- ADC interfaces
- Status indication
- FORCE_USB_BOOT interface

NOTE

"*" means under development.

3.2. Pin Assignment

The following figure shows the pin assignment of EC200T series module.

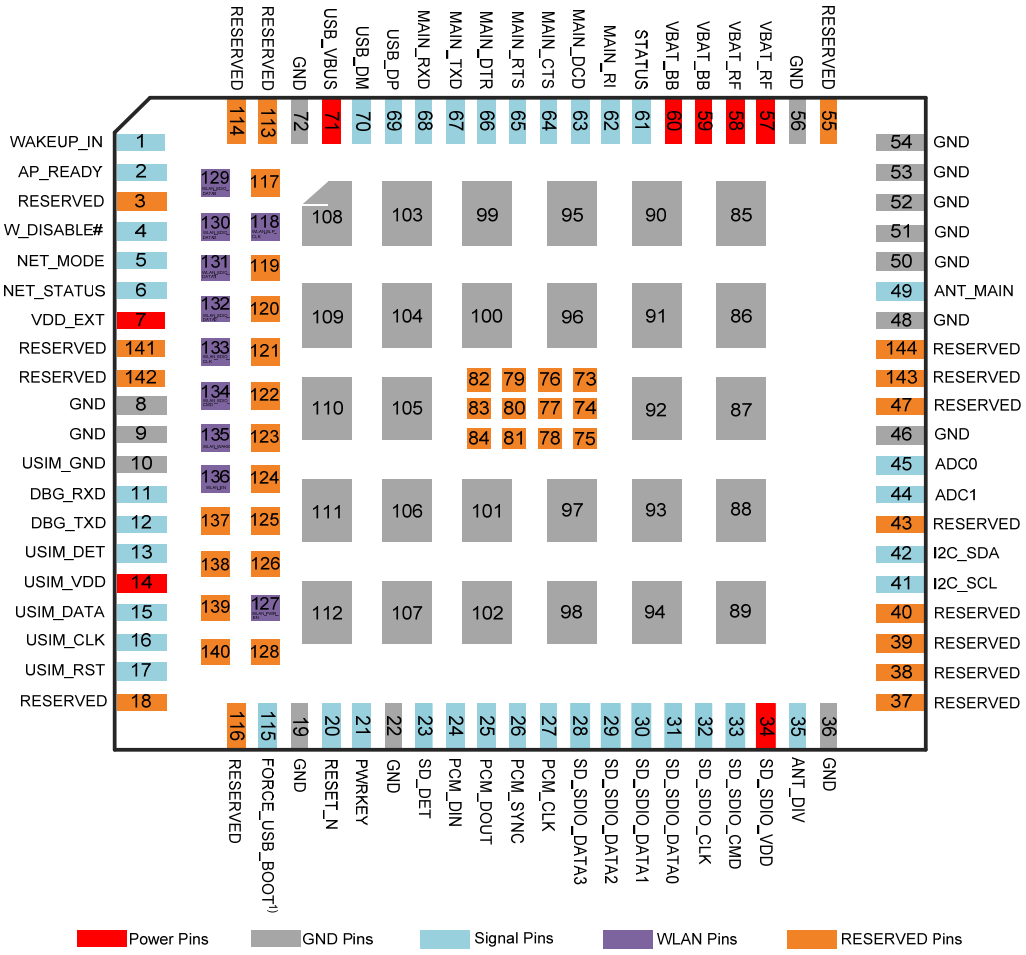


Figure 1: EC200T Series Module Pin Assignment (Top View)

NOTES

1. [1)] Pin FORCE_USB_BOOT cannot be pulled up before startup.
2. Other unused and RESERVED pins are kept open, and all GND pins are connected to the ground network.
3. GND pins 85–112 should be connected to ground in the design. RESERVED pins 73–84 should not be designed in schematic and PCB decal, and should be served as a keepout area.
4. The WLAN interface function is under development.

3.3. Pin Description

The following tables show the pin definition of EC200T series module.

Table 5: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
DI	Digital Input
DO	Digital Output
IO	Bidirectional
OD	Open Drain
PI	Power Input
PO	Power Output

Table 6: Pin Description

Power Supply Input					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	59, 60	PI	Power supply for module's baseband part	Vmax = 4.5 V Vmin = 3.4 V Vnorm = 3.8 V	It must be provided with sufficient current up to 0.8 A.
VBAT_RF	57, 58	PI	Power supply for module's RF part	Vmax = 4.5 V Vmin = 3.4 V Vnorm = 3.8 V	It must be provided with sufficient current up to 1.8 A.
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 85–112		Ground		
Power Supply Output					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VDD_EXT	7	PO	Provide 1.8 V for external circuit	Vnorm = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. If unused, keep it open.
Power on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESET_N	20	DI	Reset the module	V_{IL}max = 0.5 V	If unused, keep it open.
PWRKEY	21	DI	Turn on/off the module	V_{IL}max = 0.5 V	VBAT power domain.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NET_MODE	5	DO	Indicate the module's network registration mode	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
NET_ STATUS	6	DO	Indicate the module's network activity status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
STATUS	61	OD	Indicate the module's operation status		An external pull-up resistor is required. If unused, keep it open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_DP	69	IO	USB differential data (+)		Require differential impedance of 90 Ω. USB 2.0 compliant. If unused, keep it open.
USB_DM	70	IO	USB differential data (-)		Require differential impedance of 90 Ω. USB 2.0 compliant. If unused, keep it open.
USB_VBUS	71	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnorm = 5.0 V	Typical: 5.0 V If unused, keep it open.

(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	10		Specified ground for (U)SIM		Connect (U)SIM card connector GND.
USIM_DET	13	DI	(U)SIM card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
USIM_VDD	14	PO	(U)SIM card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax= 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM_DATA	15	IO	(U)SIM card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_CLK	16	DO	(U)SIM card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_RST	17	DO	(U)SIM card reset	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	

Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_RI	62	DO	Main UART ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_DCD	63	DO	Main UART data carrier detect	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_CTS	64	DO	Main UART clear to send	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_RTS	65	DI	Main UART request to send	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
MAIN_DTR	66	DI	Main UART data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
MAIN_TXD	67	DO	Main UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_RXD	68	DI	Main UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	11	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
DBG_TXD	12	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC1	44	AI	General-purpose ADC interface	Voltage range: 0 V to VBAT_BB	If unused, keep it open.

ADC0	45	AI	General-purpose ADC interface	Voltage range: 0 V to VBAT_BB	If unused, keep it open.
PCM & I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_DIN	24	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
PCM_DOUT	25	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
PCM_SYNC	26	IO	PCM data frame sync	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. In master mode, it serves as an output signal. In slave mode, it is used as an input signal. If unused, keep it open.
PCM_CLK	27	IO	PCM clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. In master mode, it serves as an output signal. In slave mode, it is used as an input signal. If unused, keep it open.
I2C_SCL	41	OD	I2C serial clock		Used for external codec. An external 1.8 V pull-up resistor is required. If unused, keep it open.
I2C_SDA	42	OD	I2C serial data		Used for external codec. An external 1.8 V pull-up resistor is required. If unused, keep it

					open.
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_DET*	23	DI	SD card detect		1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_DATA3	28	IO	SD card SDIO data bit 3		1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_DATA2	29	IO	SD card SDIO data bit 2		1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_DATA1	30	IO	SD card SDIO data bit 1		1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_DATA0	31	IO	SD card SDIO data bit 0		1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_CLK	32	DO	SD card SDIO clock		1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_CMD	33	IO	SD card SDIO command		1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_VDD	34	PO	SD card SDIO power supply		1.8/2.8 V power domain. If unused, keep it open.
WLAN Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_SLP_CLK	118	DO	WLAN sleep clock		If unused, keep it open.

WLAN_PWR_EN	127	DO	WLAN power supply enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
WLAN_SDIO_DATA3	129	IO	WLAN SDIO data bit 3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
WLAN_SDIO_DATA2	130	IO	WLAN SDIO data bit 2	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
WLAN_SDIO_DATA1	131	IO	WLAN SDIO data bit 1	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
WLAN_SDIO_DATA0	132	IO	WLAN SDIO data bit 0	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
WLAN_SDIO_CLK	133	DO	WLAN SDIO clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
WLAN_SDIO_CMD	134	DO	WLAN SDIO command	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
WLAN_WAKE	135	DI	Wake up the host (module)	V_{IL}min = -0.3 V V_{IL}max = 0.6V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	Wake up the host (module) by an external Wi-Fi module. 1.8 V power domain. If unused, keep it open.
WLAN_EN	136	DO	WLAN function enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.

RF Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_DIV	35	AI	Diversity antenna interface		50 Ω impedance. If unused, keep it open.
ANT_MAIN	49	IO	Main antenna interface		50 Ω impedance.
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WAKEUP_IN*	1	DI	Wake up the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
AP_READY	2	DI	Application processor ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
W_DISABLE#	4	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pull-up by default. In low voltage level, module can enter into airplane mode. If unused, keep it open.
FORCE_ USB_BOOT	115	DI	Force the module into emergency download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Active high. It is recommended to reserve test points.
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	3, 18, 37–40, 43, 47, 55, 73–84, 113, 114, 116, 117, 119–126, 128, 137–144		Reserved		Keep these pins unconnected.

NOTE

"*" means under development.

3.4. Operating Modes

The following table briefly outlines the operating modes to be mentioned in the following chapters.

Table 7: Overview of Operating Modes

Modes	Details	
Normal Operation	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level. In this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power Down Mode	In this mode, the power management unit (PMU) shuts down the power supply, software goes inactive and the serial interfaces are not accessible. However, the VBAT_RF and VBAT_BB pins are still powered.	

3.5. Power Saving

3.5.1. Sleep Mode

EC200T series is able to reduce its current consumption to an ultra-low value in the sleep mode. The following section describes power saving procedures of EC200T series module.

3.5.1.1. UART Application

If the host communicates with module via UART interface, the following preconditions should be met to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive MAIN_DTR to high level.

The following figure shows the connection between the module and the host.

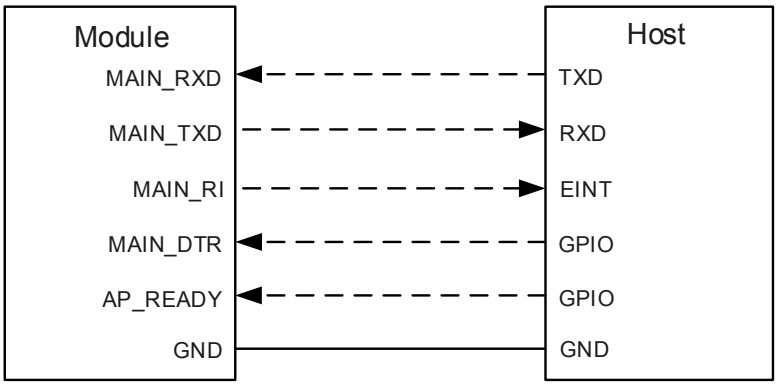


Figure 2: Sleep Mode Application via UART

- Driving MAIN_DTR to low level by host will wake up the module.
- When EC200T series has a URC to report, the URC will trigger the behavior of MAIN_RI pin. Please refer to ***Chapter 3.17*** for details about MAIN_RI behavior.

3.5.1.2. USB Application with USB Remote Wakeup Function

If the host supports USB Suspend/Resume and remote wakeup functions, the following three preconditions must be met to let the module enter sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the MAIN_DTR is kept at high level or kept open.
- The host's USB bus, which is connected with the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

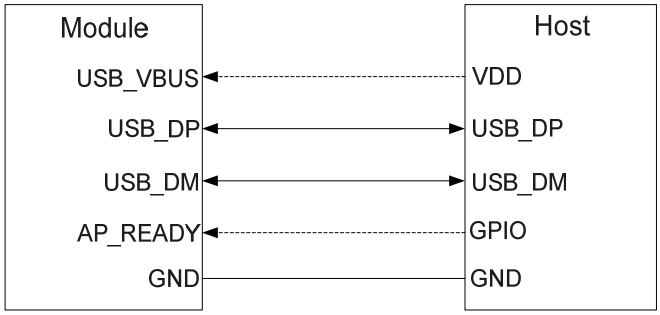


Figure 3: Sleep Mode Application with USB Remote Wakeup

- Sending data to EC200T series through USB will wake up the module.
- When EC200T series has a URC to report, the module will send remote wakeup signals via USB bus so as to wake up the host.

3.5.1.3. USB Application with USB Suspend/Resume and MAIN_RI Wakeup Function

If the host supports USB Suspend/Resume, but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host.

There are three preconditions to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

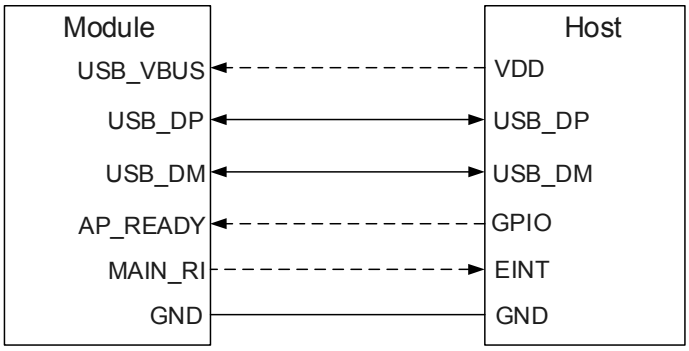


Figure 4: Sleep Mode Application with MAIN_RI

- Sending data to EC200T series through USB will wake up the module.
- When EC200T series has a URC to report, the URC will trigger the behavior of MAIN_RI pin.

3.5.1.4. USB Application without USB Suspend Function

If the host does not support USB Suspend function, please disconnect USB_VBUS with additional control circuit to let the module enter into sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

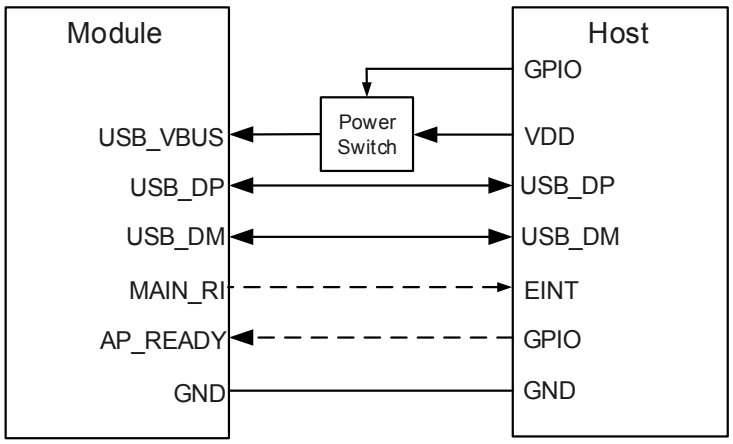


Figure 5: Sleep Mode Application without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

Please pay attention to the level match shown in dotted line between the module and the host.

3.5.2. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Its control function for airplane mode is disabled by default, and **AT+QCFG="airplanecontrol",1** can be used to enable the function. Driving it to low level can make the module enter airplane mode.

Software:

AT+CFUN=<fun> command provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode; both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

3.6. Power Supply

3.6.1. Power Supply Pins

EC200T series provides four VBAT pins dedicated to connecting with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's baseband part

The following table shows the details of power supply and GND pins.

Table 8: Power Supply and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	57, 58	Power supply for module's RF part	3.4	3.8	4.5	V
VBAT_BB	59, 60	Power supply for module's baseband part	3.4	3.8	4.5	V
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 85–112	Ground	-	0	-	V

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.4 V to 4.5 V. Please make sure that the input voltage will never drop below 3.4 V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G and 4G networks.

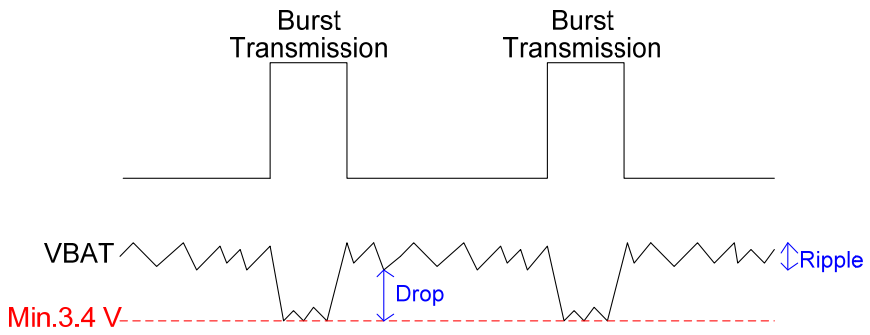


Figure 6: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100 μF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT_BB and VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1mm; and the width of VBAT_RF trace should be no less than 2 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to ensure the stability of power source, it is suggested that a TVS diode of which reverse stand-off voltage is 4.7 V and peak pulse power is up to 2550 W should be used. The following figure shows the star structure of the power supply.

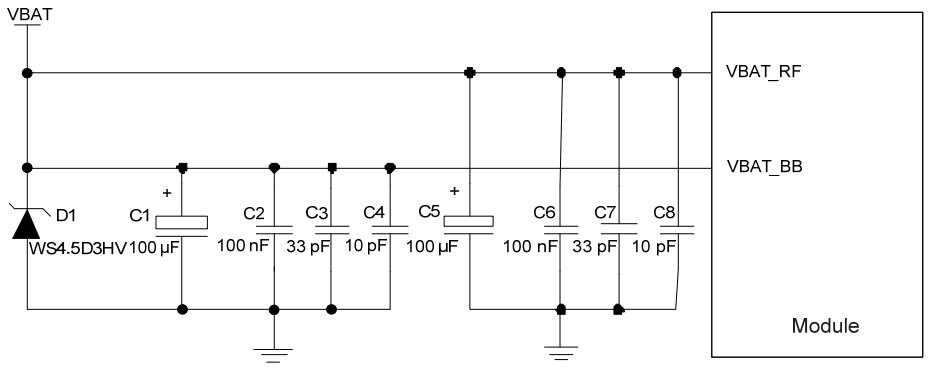


Figure 7: Star Structure of Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current up to 2.0 A at least to the module. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

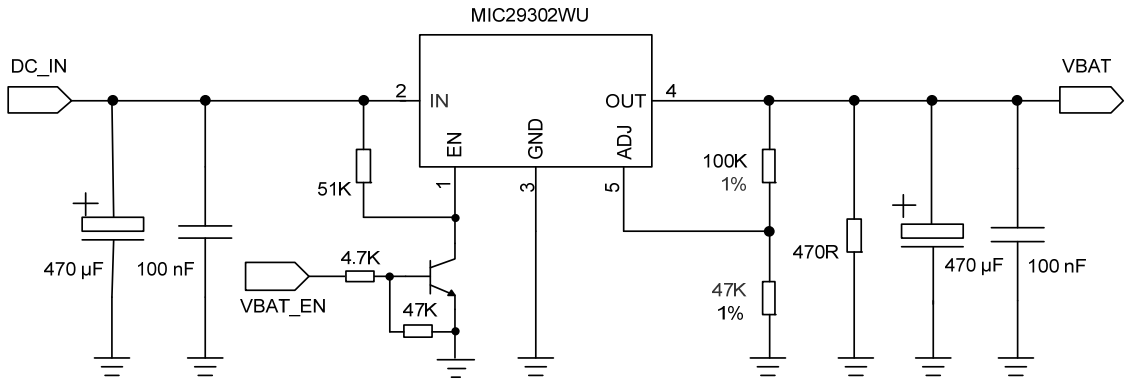


Figure 8: Reference Circuit of Power Supply

3.7. Power-on/off/Reset Scenarios

3.7.1. Turn on Module Using the PWRKEY

The following table shows the pin definition of PWRKEY.

Table 9: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	21	DI	Turn on/off the module	VBAT power domain

When EC200T series is in power down mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

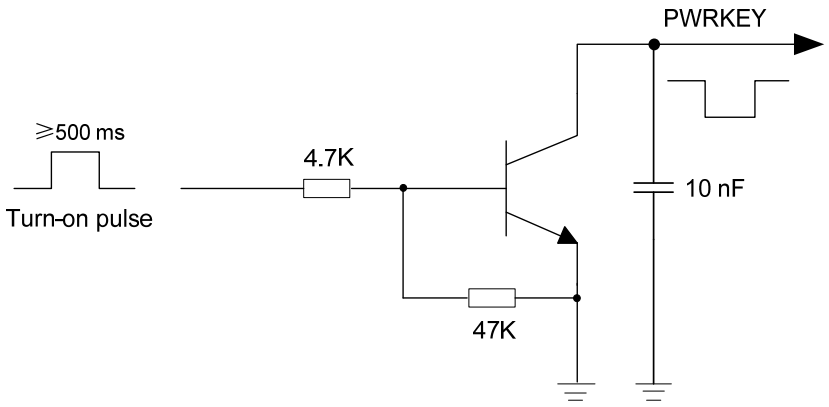


Figure 9: Reference Circuit of Turing on the Module Using Driving Circuit

The other way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

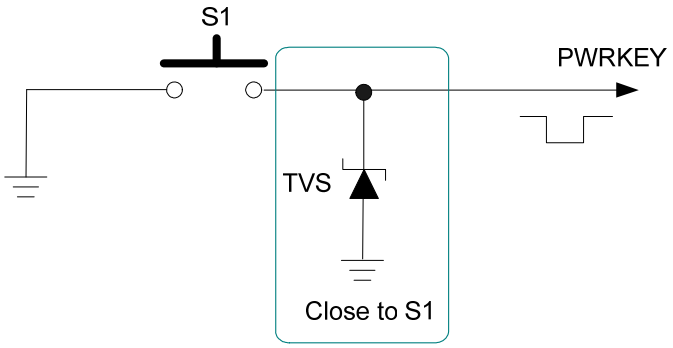


Figure 10: Reference Circuit of Turing on the Module Using Keystroke

The timing of turning on the module is illustrated in the following figure.

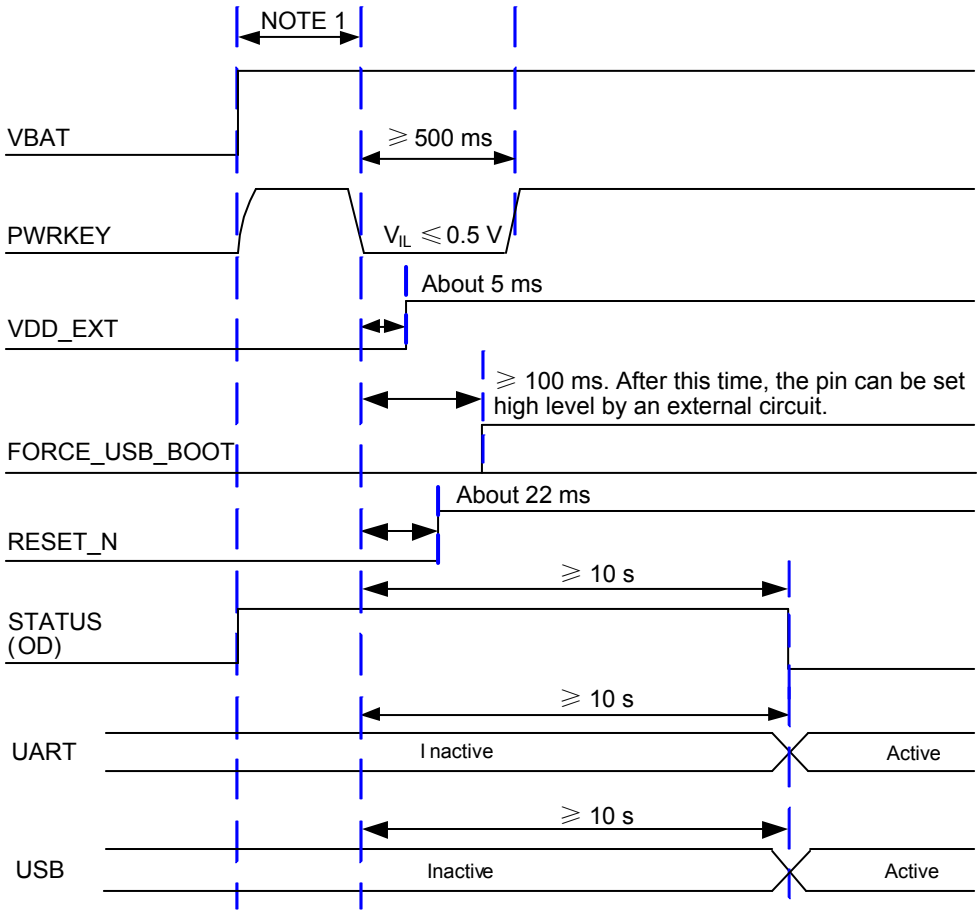


Figure 11: Timing of Turning on Module

NOTES

1. Please make sure that VBAT is stable before pulling down PWRKEY pin. The time between them is no less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 4.7 kΩ resistor if module needs to be powered on automatically and shutdown is not needed.

3.7.2. Turn off Module

The following procedures can be used to turn off the module:

- Using the PWRKEY pin.
- Using **AT+QPOWD** command.

3.7.2.1. Turn off Module Using the PWRKEY Pin

Driving the PWRKEY pin to a low level voltage for at least 650 ms, the module will execute power-down procedure after the PWRKEY is released. The timing of turning off the module is illustrated in the following figure.

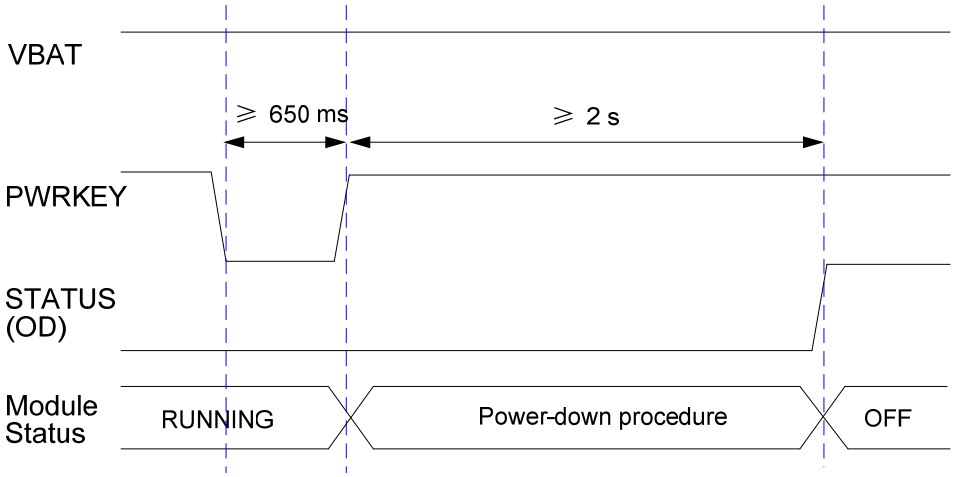


Figure 12: Timing of Turning off Module

3.7.2.2. Turn off Module Using AT Command

It is also a safe way to use **AT+QPOWD** command to turn off the module, which is similar to the procedure of turning off the module via PWRKEY pin.

Please refer to ***document [2]*** for details about **AT+QPOWD** command.

NOTES

1. In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.
2. When turning off module with the AT command, please keep PWRKEY at a high level after the execution of the command. Otherwise, the module will turn itself back on after being shut down.

3.7.3. Reset the Module

The RESET_N pin can be used to reset the module. The module can be reset by pulling the RESET_N pin low for at least 300 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 10: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	20	DI	Reset the module	1.8 V power domain

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

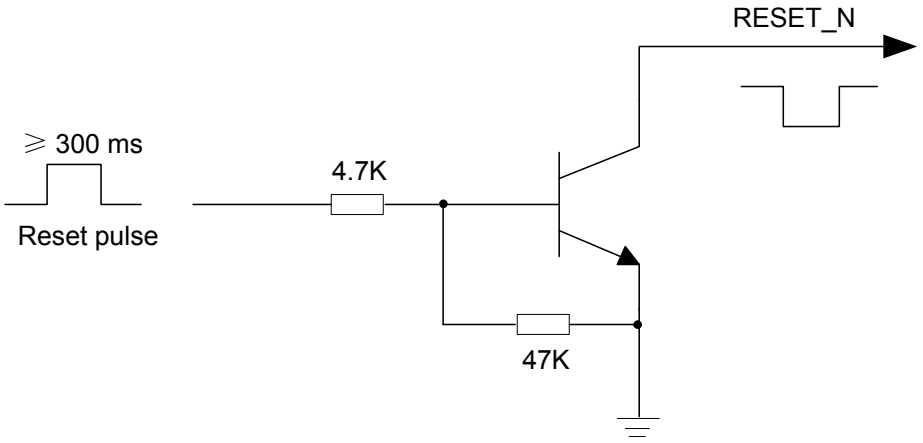


Figure 13: Reference Circuit of Resetting the Module by Using Driving Circuit

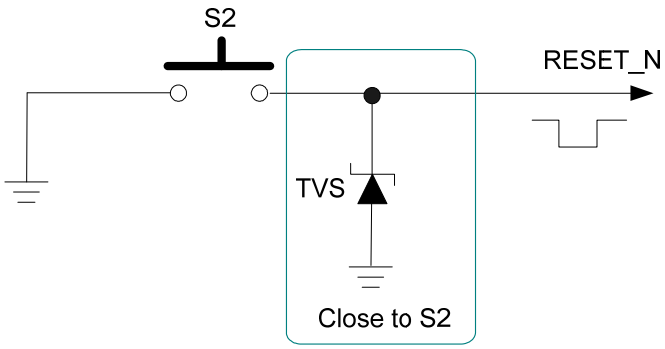


Figure 14: Reference Circuit of Resetting the Module by Using Keystroke

The timing of resetting module is illustrated in the following figure.

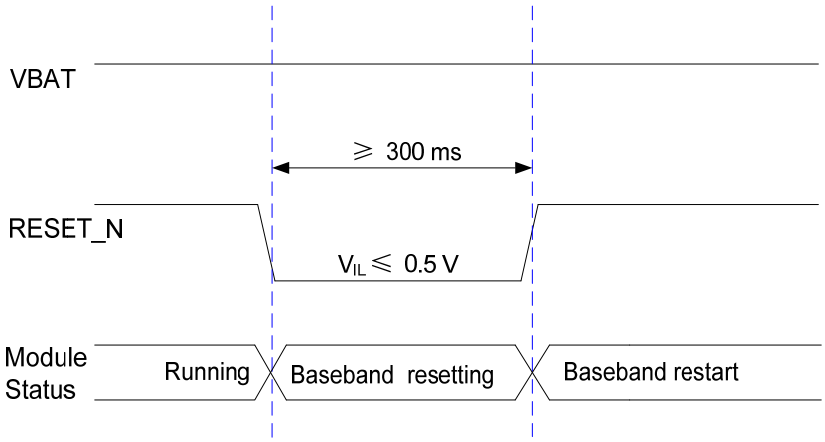


Figure 15: Timing of Resetting Module

NOTES

1. Please ensure that there is no large capacitance with the max value exceeding 10 nF on PWRKEY and RESET_N pins.
2. RESET_N only resets the internal baseband chip of the module and does not reset the power management chip.
3. It is recommended to use RESET_N only when failing to turn off the module by **AT+QPOWD** command or PWRKEY pin.

3.8. (U)SIM Interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported.

Table 11: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_GND	10		Specified ground for (U)SIM	
USIM_DET	13	DI	(U)SIM card detect	1.8 V power domain. If unused, keep it open.
USIM_VDD	14	PO	(U)SIM card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.

USIM_DATA	15	IO	(U)SIM card data
USIM_CLK	16	DO	(U)SIM card clock
USIM_RST	17	DO	(U)SIM card reset

EC200T series supports (U)SIM card hot-plug via the USIM_DET pin. The function supports low level and high level detections. By default, It is disabled, and can be configured via **AT+QSIMDET** command. Please refer to ***document [2]*** for details about the command.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

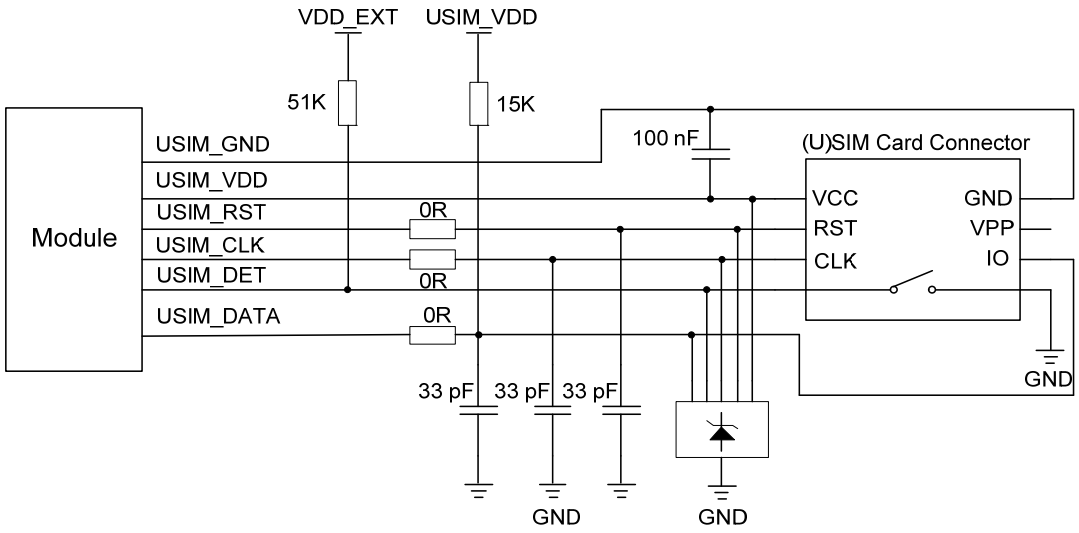


Figure 16: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

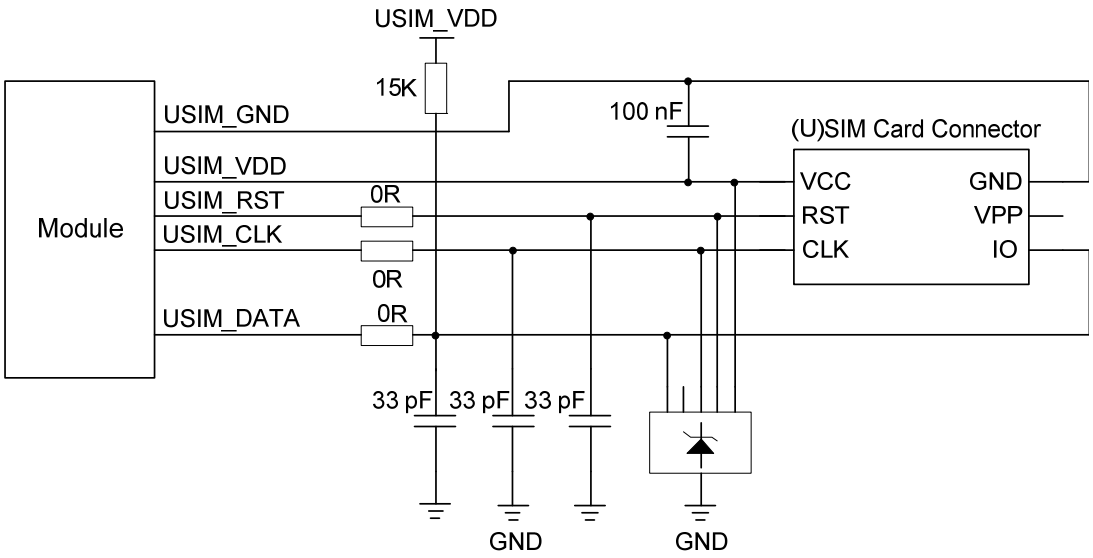


Figure 17: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in your applications, please follow the criteria below in (U)SIM circuit design:

- Keep placement of (U)SIM card connector as close to the module as possible. Keep the trace length less than 200 mm as far as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5 mm to maintain the same electric potential. If the ground is complete on your PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not be more than 15 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors are used for filtering interference of EGSM900. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

3.9. USB Interface

EC200T series provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports full-speed (12 Mbps) and high-speed (480 Mbps) modes. The USB interface can only serves as a slave device and is used for AT command communication, data transmission, software debugging and firmware upgrade. The following table shows the pin definition of USB interface.

Table 12: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	69	IO	USB differential data (+)	Require differential impedance of 90 Ω
USB_DM	70	IO	USB differential data (-)	Require differential impedance of 90 Ω
USB_VBUS	71	AI	USB connection detect	Typical 5.0 V
GND	72		Ground	

For more details about the USB 2.0 specifications, please visit http://www.usb.org/home.

It is recommended to reserve test points for debugging and firmware upgrade in your designs. The following figure shows a reference circuit of USB interface.

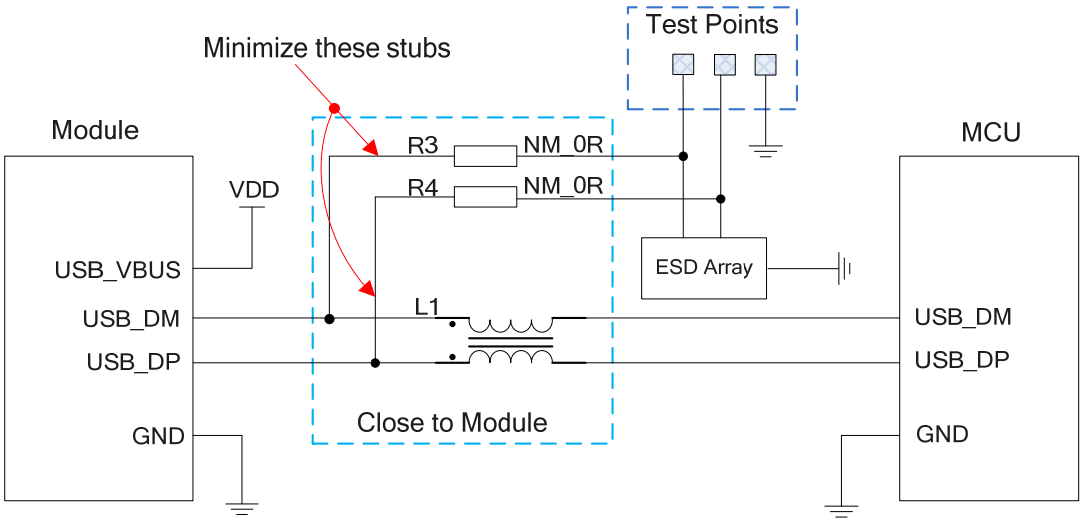


Figure 18: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data line signal, L1, R3 and R4 components must be placed close to the module, and also resistors R3 and R4 should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with when design the USB interface, so as to meet USB 2.0 specification.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below.
- Please pay attention to the selection of the ESD component on the USB data line. Its parasitic capacitance should not exceed 2 pF and should be placed as close as possible to the USB interface.

3.10. UART Interfaces

The module provides two UART interfaces: the main UART interface and the debug UART interface. The following shows their features.

- The main UART interface supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps and 1 Mbps baud rates, and the default is 115200 bps. This interface is used for data transmission and AT command communication. Also, it supports RTS and CTS hardware flow control.
- The debug UART interface supports 115200 bps baud rate. It is used for the output of partial logs.

The following tables show the pin definition of main UART interface.

Table 13: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_RI	62	DO	Main UART ring indication	1.8 V power domain. If unused, keep it open.
MAIN_DCD	63	DO	Main UART data carrier detect	
MAIN_CTS	64	DO	Main UART clear to send	

MAIN_RTS	65	DI	Main UART request to send
MAIN_DTR	66	DI	Main UART data terminal ready
MAIN_TXD	67	DO	Main UART transmit
MAIN_RXD	68	DI	Main UART receive

Table 14: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	11	DI	Debug UART receive	1.8 V power domain. If unused, keep it open.
DBG_TXD	12	DO	Debug UART transmit	

The logic levels are described in the following table.

Table 15: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The module provides a 1.8 V UART interface. A level translator should be used if the application is equipped with a 3.3 V UART interface. A level translator TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure shows a reference design.

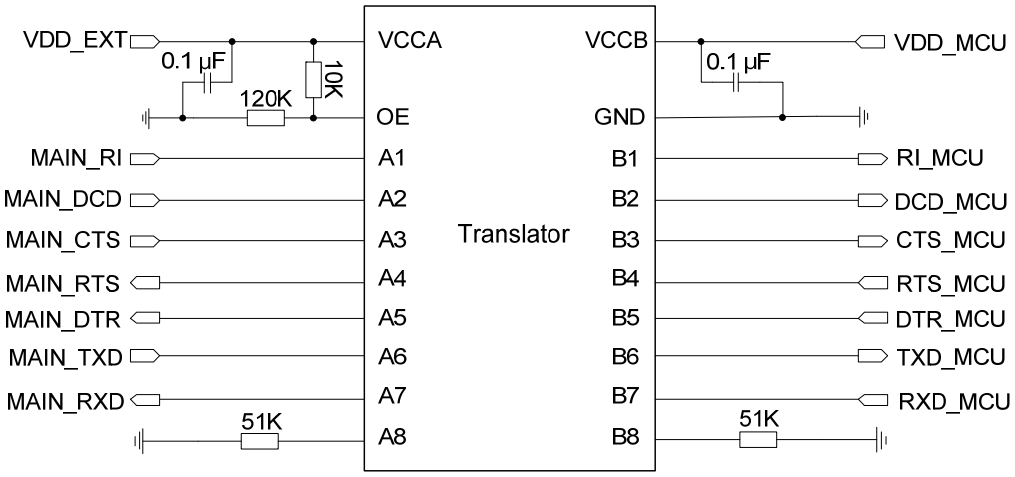


Figure 19: Reference Circuit with Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. For the design of circuits in dotted lines, see that of the circuits in solid lines, but please pay attention to the direction of connection.

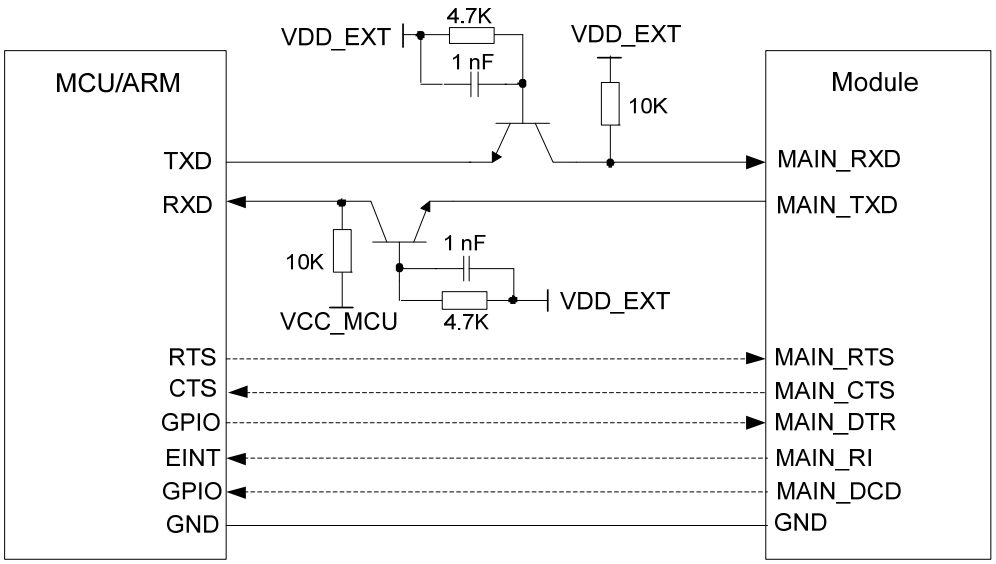


Figure 20: Reference Circuit with Transistor Circuit

NOTES

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS.

3.11. PCM and I2C Interfaces

EC200T series provides one Pulse Code Modulation (PCM) digital interface for audio design, which supports the primary mode (short frame synchronization) and EC200T series works as both master and slave.

EC200T series works as a master device pertaining to I2C interface.

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

EC200T series supports 16-bit linear data format. The following figure shows the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK.

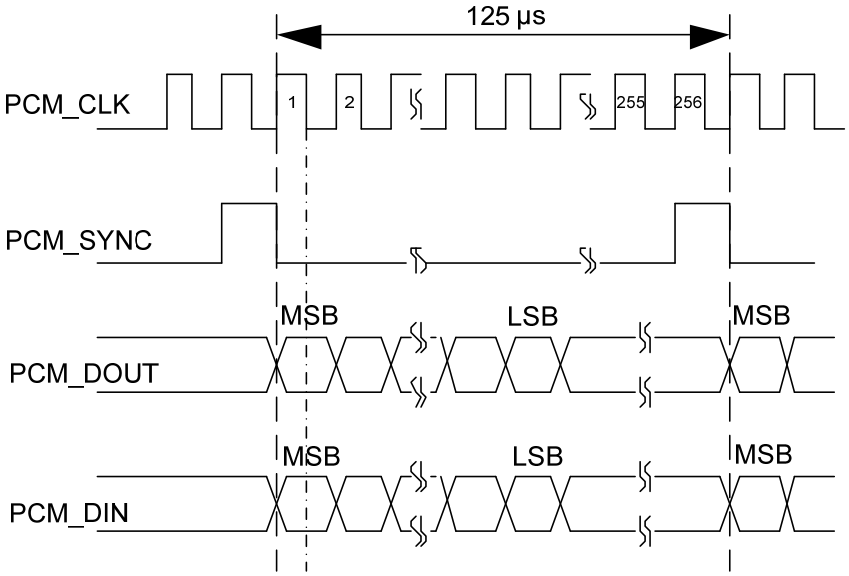


Figure 21: Primary Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 16: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	24	DI	PCM data input	1.8 V power domain. If unused, keep it open.
PCM_DOUT	25	DO	PCM data output	1.8 V power domain. If unused, keep it open.
PCM_SYNC	26	IO	PCM data frame sync	1.8 V power domain. In master mode, it serves as an output signal. In slave mode, it is used as an input signal. If unused, keep it open.
PCM_CLK	27	IO	PCM clock	1.8 V power domain. In master mode, it serves as an output signal. In slave mode, it is used as an input signal. If unused, keep it open.
I2C_SCL	41	OD	I2C serial clock	Used for external codec. An external 1.8 V pull-up resistor is required. If unused, keep it open.
I2C_SDA	42	OD	I2C serial data	Used for external codec. An external 1.8 V pull-up resistor is required. If unused, keep it open.

Clock and mode can be configured by AT command, and the default configuration is short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC.

The following figure shows a reference design of PCM interface with external codec IC.

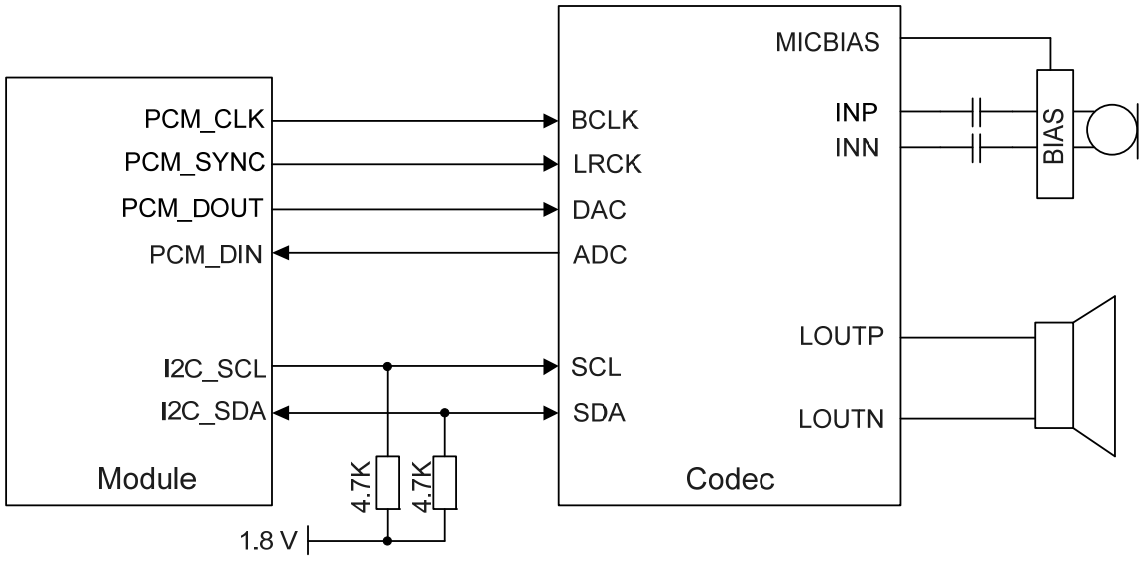


Figure 22: Reference Circuit of PCM Application with Audio Codec

NOTE

It is recommended to reserve an RC (R=22 Ω, C=22 pF) circuit on the PCM lines, especially for PCM_CLK.

3.12. SD Card Interface

EC200T series provides an SD card interface, which complies with SD 3.0 specification.

The following table shows the pin definition of SD card interface.

Table 17: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_DET*	23	DI	SD card detect	1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_DATA3	28	IO	SD card SDIO data bit 3	1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_DATA2	29	IO	SD card SDIO data bit 2	1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_DATA1	30	IO	SD card SDIO data bit 1	1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_DATA0	31	IO	SD card SDIO data bit 0	1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_CLK	32	DO	SD card SDIO clock	1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_CMD	33	IO	SD card SDIO command	1.8/2.8 V power domain. If unused, keep it open.
SD_SDIO_VDD	34	PO	SD card SDIO power supply	1.8/2.8 V power domain. If unused, keep it open.

The following figure shows a reference design of SD card interface.

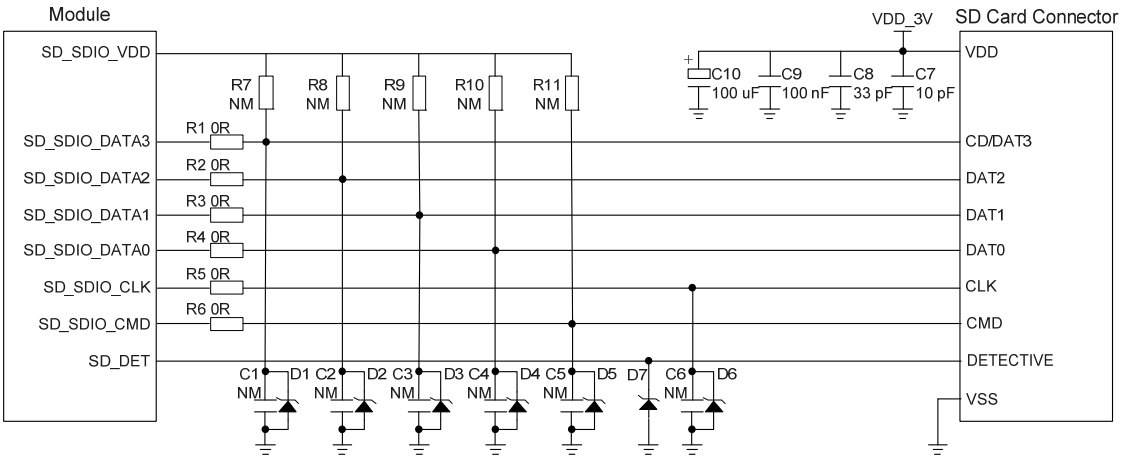


Figure 23: Reference Circuit of SD Card Interface

In SD card interface design, in order to ensure good communication performance with SD card, the following design principles should be complied with:

- The voltage range of SD card power supply VDD_3V is 2.7–3.6 V and a sufficient current up to 0.8 A should be provided. As the maximum output current of SD_SDIO_VDD is 50 mA which can only be used for SDIO pull-up resistors, an externally power supply is needed for SD card.
- To avoid jitter of bus, resistors R7–R11 are needed to pull up the SDIO to SD_SDIO_VDD. Value of these resistors is among 10 kΩ to 100 kΩ and the recommended value is 100 kΩ. SD_SDIO_VDD should be used as the pull-up power.
- In order to adjust signal quality, it is recommended to add 0 Ω resistors R1–R6 in series between the module and the SD card. The bypass capacitors C1–C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- In order to offer good ESD protection, it is recommended to add a TVS diode on SD card pins near the SD card connector with junction capacitance less than 15 pF.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
  It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50 Ω ±10%.
- Make sure the adjacent trace spacing is two times of the trace width and the load capacitance of SDIO bus should be less than 15 pF.
- It is recommended to keep the traces of SD_SDIO_CLK, SD_SDIO_DATA[0:3] and SD_SDIO_CMD with equal length (the difference among them is less than 1 mm) and the total routing length needs to be less than 50 mm.

3.13. WLAN Interface*①

EC200T series supports a SDIO 3.0 interface for WLAN.

The following table shows the pin definition of WLAN interface

Table 18: Pin Definition of WLAN Interface

Pin Name	Pin No.	I/O	Description	Comment
WLAN_SLP_CLK	118	DO	WLAN sleep clock	If unused, keep it open.
WLAN_PWR_EN	127	DO	WLAN power supply enable control	1.8 V power domain If unused, keep it open.
WLAN_SDIO_DATA3	129	IO	WLAN SDIO data bit 3	
WLAN_SDIO_DATA2	130	IO	WLAN SDIO data bit 2	
WLAN_SDIO_DATA1	131	IO	WLAN SDIO data bit 1	
WLAN_SDIO_DATA0	132	IO	WLAN SDIO data bit 0	
WLAN_SDIO_CLK	133	DO	WLAN SDIO clock	
WLAN_SDIO_CMD	134	DO	WLAN SDIO command	
WLAN_WAKE	135	DI	Wake up the host (module)	Wake up the host (module) by an external Wi-Fi module. 1.8 V power domain. If unused, keep it open.
WLAN_EN	136	DO	WLAN function enable control	1.8 V power domain If unused, keep it open.

As SDIO signals are very high-speed, in order to ensure the SDIO interface design meets SDIO 3.0 specification, please comply with the following principles:

- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO signal trace is 50 Ω ±10%.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is recommended to keep the traces of WLAN_SDIO_CLK, WLAN_SDIO_DATA[0:3] and WLAN_SDIO_CMD with equal length (the difference among them is less than 1 mm) and the total routing length needs to be less than 50 mm.

- Make sure the adjacent trace spacing is 2 times of the trace width and bus capacitance is less than 15 pF.

NOTE

"*" means under development.

"①"means only QuecOpen® scheme support

3.14. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces. **AT+QADC=0** can be used to read the voltage value on ADC0 pin. **AT+QADC=1** can be used to read the voltage value on ADC1 pin. For more details about these AT commands, see ***document [2]***.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 19: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description	Comment
ADC1	44	General-purpose ADC interface	If unused, keep it open.
ADC0	45	General-purpose ADC interface	If unused, keep it open.

The following table describes the characteristic of the ADC function.

Table 20: Characteristic of the ADC

Parameter	Min.	Typ.	Max.	Unit
ADC1 Voltage Range	0		VBAT_BB	V
ADC0 Voltage Range	0		VBAT_BB	V
ADC Resolution		12		bits

3.15. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides two pins which are NET_MODE and NET_STATUS for network status indication. The following tables describe pin definition and logic level changes in different network status.

Table 21: Pin Definition of Network Connection Status/Activity Indication

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	5	DO	Indicate the module's network registration mode	1.8 V power domain If unused, keep it open.
NET_STATUS	6	DO	Indicate the module's network activity status	1.8 V power domain If unused, keep it open.

Table 22: Working State of Network Connection Status/Activity Indication

Pin Name	Logic Level Changes	Network Status
NET_MODE	Always high	Registered on LTE network
	Always low	Others
NET_STATUS	Flicker slowly (200 ms high/1800 ms low)	Network searching
	Flicker slowly (1800 ms high/200 ms low)	Idle
	Flicker quickly (125 ms high/125 ms low)	Data transfer is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

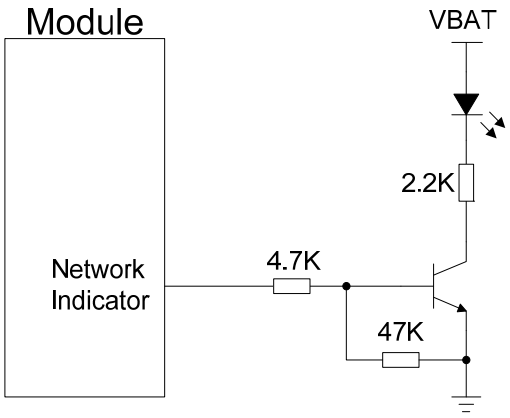


Figure 24: Reference Circuit of Network Status Indication

3.16. STATUS

The STATUS pin is an open drain output for module's operation status indication. It can be connected to a GPIO of DTE with a pulled-up resistor, or as an LED indication circuit as below. When the module is turned on normally, the STATUS will present the low state. Otherwise, the STATUS will present high-impedance state.

Table 23: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	61	OD	Indicate the module's operation status	An external pull-up resistor is required. If unused, keep it open.

The following figure shows different circuit designs of STATUS, and you can choose either one according to the application demands.

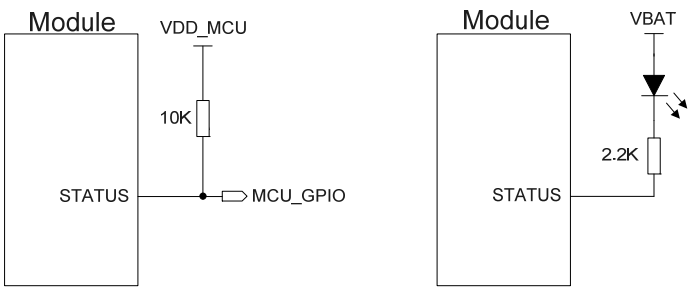


Figure 25: Reference Circuits of STATUS

NOTE

The status pin cannot be used as indication of module shutdown status when VBAT is removed.

3.17. Behaviors of the MAIN_RI

AT+QCFG="risignaltype","physical" can be used to configure MAIN_RI behaviors.

No matter on which port a URC is presented, the URC will trigger the behaviors of MAIN_RI pin.

NOTE

The URC can be outputted via UART port, USB AT port and USB modem port, which can be set by **AT+QURCCFG** command. The default port is USB AT port.

In addition, MAIN_RI behavior can be configured flexibly. The default behavior of the MAIN_RI is shown as below.

Table 24: Behaviors of the MAIN_RI

State	Response
Idle	MAIN_RI keeps at high level
URC	MAIN_RI outputs 120ms low pulse when a new URC returns

The MAIN_RI behavior can be changed via **AT+QCFG="urc/ri/ring"**. Please refer to ***document [2]*** for details.

3.18. FORCE_USB_BOOT Interface

EC200T series provides a FORCE_USB_BOOT pin. You can pull up FORCE_USB_BOOT to 1.8 V before VDD_EXT is powered up, and the module will enter emergency download mode when it is powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 25: Pin Definition of FORCE_USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
FORCE_ USB_BOOT	115	DI	Force the module into emergency download mode	1.8 V power domain. Active high. It is recommended to reserve test points.

The following figure shows a reference circuit of FORCE_USB_BOOT interface.

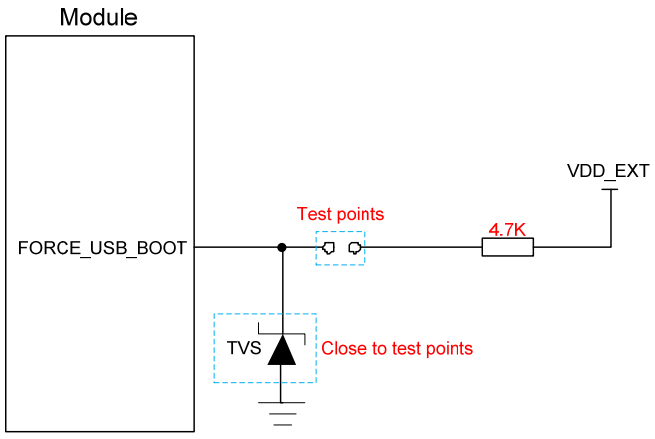


Figure 26: Reference Circuit of FORCE_USB_BOOT Interface

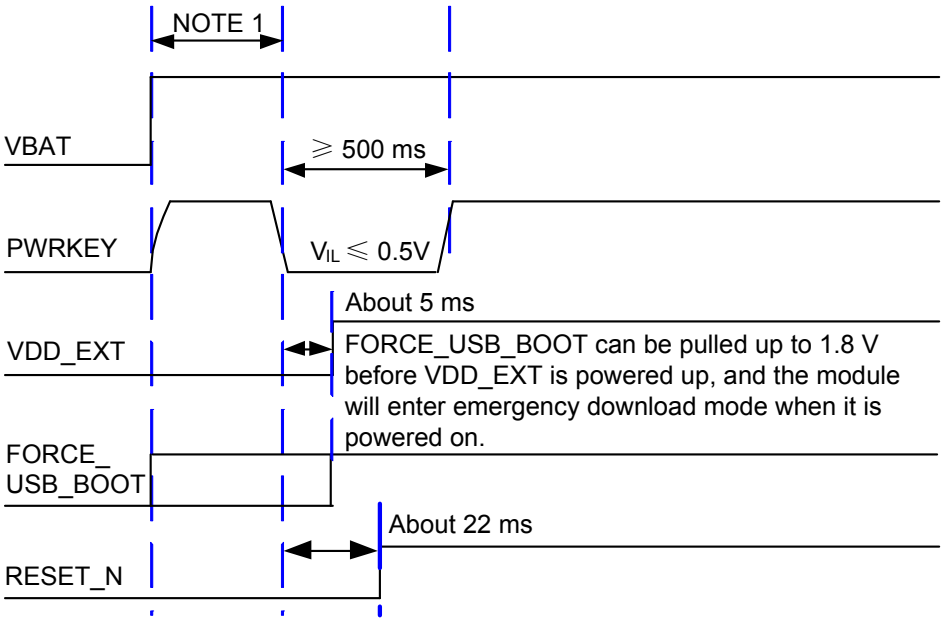


Figure 27: Timing Sequence for Entering Emergency Download Mode

NOTES

1. Please make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.
2. When using MCU to control module to enter the emergency download mode, please follow the above timing sequence. It is not recommended to pull up FORCE_USB_BOOT to 1.8 V before powering up VBAT. Directly connect the test points as shown in ***Figure 27*** can manually force the module to enter download mode.

4 Antenna Interfaces

EC200T series antenna interfaces include a main antenna interface, an Rx-diversity antenna interface which is used to resist the fall of signals caused by high speed movement and multipath effect. The antenna ports have an impedance of 50 Ω.

4.1. Main/Rx-diversity Antenna Interfaces

4.1.1. Pin Definition

The pin definition of main antenna and Rx-diversity antenna interfaces is shown below.

Table 26: Pin Definition of RF Antennas

Pin Name	Pin No.	I/O	Description	Comment
ANT_DIV	35	AI	Diversity antenna interface	50 Ω impedance If unused, keep it open.
ANT_MAIN	49	IO	Main antenna interface	50 Ω impedance

4.1.2. Operating Frequency

Table 27: EC200T-CN Operating Frequencies

3GPP Band	Transmit	Receive	Unit
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B5	824–849	869–894	MHz
WCDMA B8	880–915	925–960	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz

LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-TDD B34	2010–2025	2010–2025	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B39	1880–1920	1880–1920	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2555–2655	2555–2655	MHz

Table 28: EC200T-EU Operating Frequencies

3GPP Band	Transmit	Receive	Unit
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B8	880–915	925–960	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B20	832–862	791–821	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2555–2655	2555–2655	MHz

Table 29: EC200T-AU* Operating Frequencies

3GPP Band	Transmit	Receive	Unit
EGSM900	880–915	925–960	MHz
GSM850	824–849	869–894	MHz
DCS1800	1710–1785	1805–1880	MHz
PCS1900	1850–1910	1930–1990	MHz
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B2	1850–1910	1930–1990	MHz
WCDMA B4	1710–1755	2110–2155	MHz
WCDMA B5	824–849	869–894	MHz
WCDMA B8	880–915	925–960	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B2	1850–1910	1930–1990	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B4	1710–1755	2110–2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz

NOTE

"*" means under development.

4.1.3. Reference Design of RF Antenna Interface

A reference design of ANT_MAIN and ANT_DIV antenna pads is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

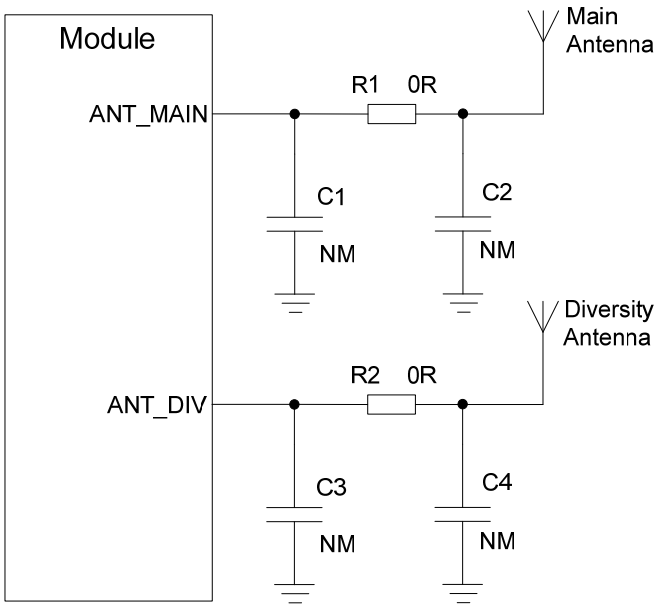


Figure 28: Reference Circuit of RF Antenna Interface

NOTES

1. Keep a proper distance between the main antenna and the Rx-diversity antenna to improve the receiving sensitivity.
2. Place the π-type matching components (R1 & C1 & C2 and R2 & C3 & C4) as close to the antenna as possible.

4.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the space between the RF trace and the ground (S). Microstrip and coplanar waveguide are typically used in RF layout to control characteristic impedance. The following figures are reference designs of microstrip or coplanar waveguide with different PCB structures.

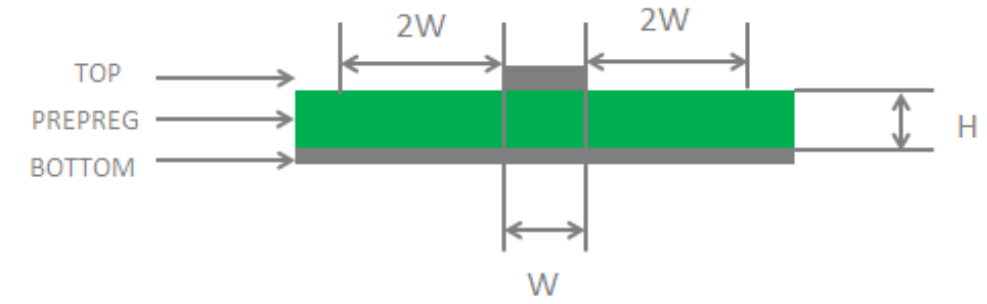


Figure 29: Microstrip Design on a 2-layer PCB

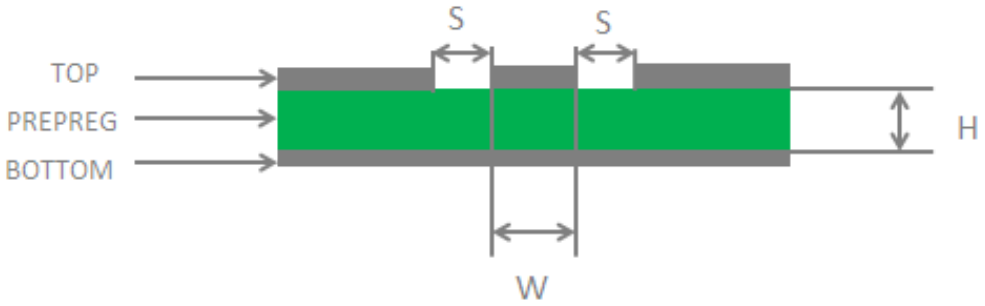


Figure 30: Coplanar Waveguide Design on a 2-layer PCB

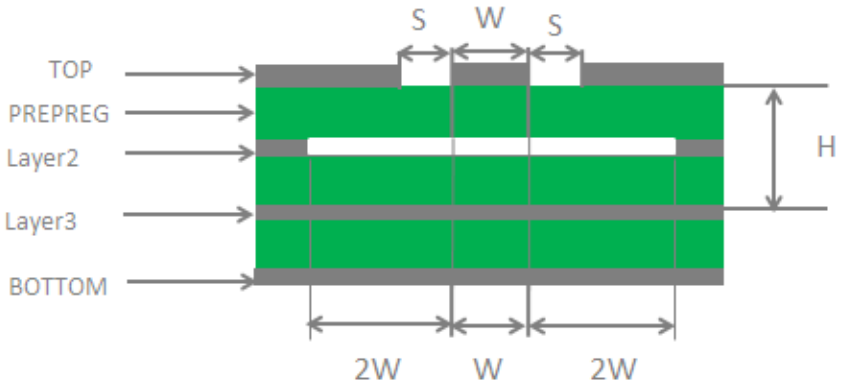


Figure 31: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

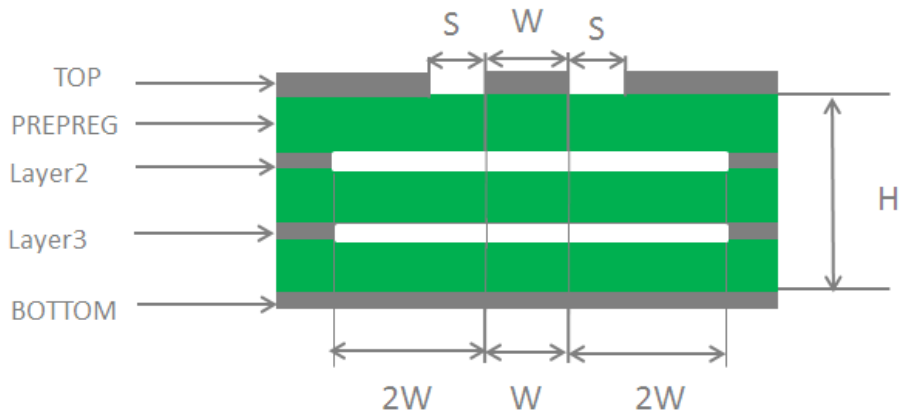


Figure 32: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use impedance simulation tool to control the characteristic impedance of RF traces as 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).

For more details about RF layout, see ***Document [3]***.

4.2. Antenna Installation

4.2.1. Antenna Requirement

The following table shows the requirements on main antenna and RX-diversity antenna.

Table 30: Antenna Requirements

Type	Requirements
GSM/UMTS/LTE	VSWR: ≤ 2 Efficiency: > 30% Max. input power: 50 W

	Input impedance: 50 Ω Cable insertion loss: < 1 dB (EGSM900, WCDMA B5, WCDMA B8, LTE-FDD B5/B8/B20/B28) Cable insertion loss: < 1.5 dB (DCS1800, WCDMA B1, LTE B1/B3/B34/B39) Cable insertion loss: < 2 dB (LTE-TDD B7/B38/B40/B41)

4.2.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

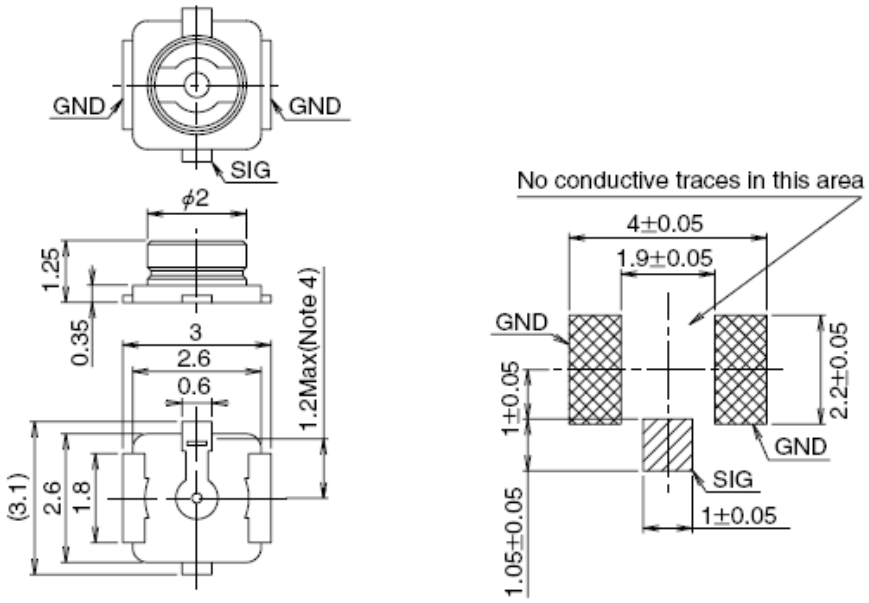


Figure 33: Dimensions of U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

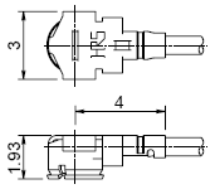
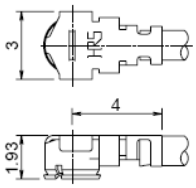
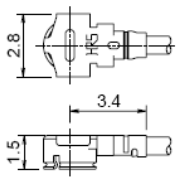
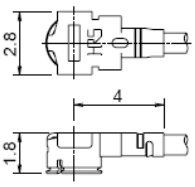
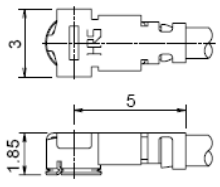
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 34: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

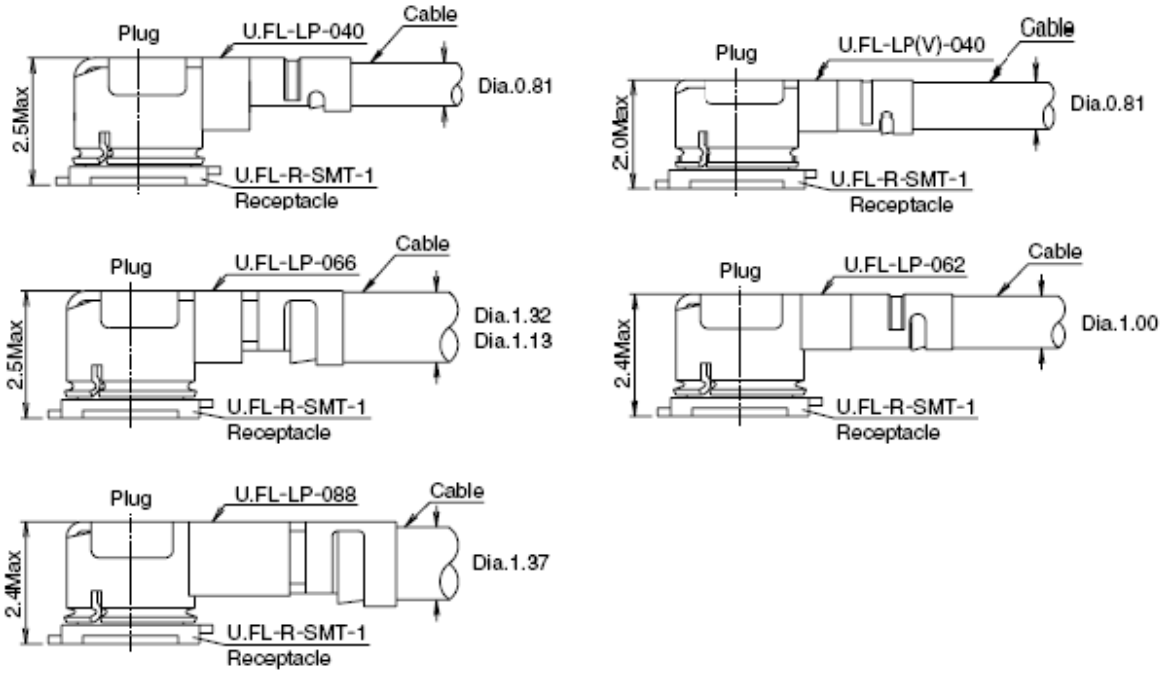


Figure 35: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://hirose.com.

5 Electrical, Reliability and Radio Characteristics

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 31: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	0.8	A
Peak Current of VBAT_RF	0	1.8	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V
Voltage at ADC1	0	VBAT_BB	V

5.2. Power Supply Ratings

Table 32: The Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.4	3.8	4.5	V
	Voltage drop during burst transmission	Maximum power control level on EGSM900.			400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on EGSM900.		1.8	2.0	A
USB_VBUS	USB connection detection		3.0	5.0	5.25	V

5.3. Operating and Storage Temperatures

The operating and storage temperatures are listed in the following table.

Table 33: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range[1)]	-35	+25	+75	ºC
Extended Operation Range[2)]	-40		+85	ºC
Storage Temperature Range	-40		+90	ºC

NOTES

1. [1] Within operating temperature range, the module is 3GPP compliant.
2. [2] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

5.4. Current Consumption

The following table shows the current consumption of EC200T-CN.

Table 34: EC200T-CN Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	11	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.67	mA
		EGSM900 @ DRX = 2 (USB disconnected)	3.04	mA
		EGSM900 @ DRX = 5 (USB disconnected)	1.94	mA
		EGSM900 @ DRX = 5 (USB suspend)	2.11	mA
		EGSM900 @ DRX = 9 (USB disconnected)	1.64	mA
		DCS1800 @ DRX = 2 (USB disconnected)	3.01	mA
		DCS1800 @ DRX = 5 (USB disconnected)	1.93	mA
		DCS1800 @ DRX = 5 (USB suspend)	2.08	mA
		DCS1800 @ DRX = 9 (USB disconnected)	1.61	mA
		WCDMA @ PF = 64 (USB disconnected)	3.93	mA
		WCDMA @ PF = 64 (USB suspend)	4.08	mA
		WCDMA @ PF = 128 (USB disconnected)	2.70	mA
		WCDMA @ PF = 256 (USB disconnected)	2.12	mA

		WCDMA @ PF = 512 (USB disconnected)	1.75	mA
		LTE-FDD @ PF = 32 (USB disconnected)	4.21	mA
		LTE-FDD @ PF = 64 (USB disconnected)	2.59	mA
		LTE-FDD @ PF = 64 (USB suspend)	2.79	mA
		LTE-FDD @ PF = 128 (USB disconnected)	1.78	mA
		LTE-FDD @ PF = 256 (USB disconnected)	1.49	mA
		LTE-TDD @ PF = 32 (USB disconnected)	4.99	mA
		LTE-TDD @ PF = 64 (USB disconnected)	3.26	mA
		LTE-TDD @ PF = 64 (USB suspend)	3.52	mA
		LTE-TDD @ PF = 128 (USB disconnected)	2.43	mA
		LTE-TDD @ PF = 256 (USB disconnected)	2.01	mA
	Idle state	EGSM900 @ DRX = 5 (USB disconnected)	30.55	mA
		EGSM00 @ DRX = 5 (USB connected)	30.64	mA
		WCDMA @ PF = 64 (USB disconnected)	30.85	mA
		WCDMA @ PF = 64 (USB connected)	31.44	mA
		LTE-FDD @ PF = 64 (USB disconnected)	31.58	mA
		LTE-FDD @ PF = 64 (USB connected)	31.68	mA
		LTE-TDD @ PF = 64 (USB disconnected)	31.78	mA
		LTE-TDD @ PF = 64 (USB connected)	31.99	mA
	GPRS data transfer	EGSM900 4DL/1UL @ 32.25 dBm	249.1	mA
		EGSM900 3DL/2UL @ 32.17 dBm	407.3	mA
		EGSM900 2DL/3UL @ 31.18 dBm	511.1	mA
		EGSM900 1DL/4UL @ 29.18 dBm	534.8	mA
		DCS1800 4DL/1UL @ 29.95 dBm	233.6	mA
		DCS1800 3DL/2UL @ 29.94 dBm	372.1	mA

		DCS1800 2DL/3UL @ 28.45 dBm	445.9	mA
		DCS1800 1DL/4UL @ 26.53 dBm	470.3	mA
	EDGE data transfer	EGSM900 4DL/1UL @ 28.21 dBm	221.8	mA
		EGSM900 3DL/2UL @ 27.51 dBm	351.8	mA
		EGSM900 2DL/3UL @ 25.46 dBm	470.2	mA
		EGSM900 1DL/4UL @ 23.28 dBm	582.1	mA
		DCS1800 4DL/1UL @ 27.31 dBm	195.8	mA
		DCS1800 3DL/2UL @ 26.84 dBm	301.1	mA
		DCS1800 2DL/3UL @ 25.56 dBm	393.9	mA
		DCS1800 1DL/4UL @ 22.87 dBm	476.3	mA
	WCDMA data transfer	WCDMA B1 HSDPA @ 23.57 dBm	675.2	mA
		WCDMA B1 HSUPA @ 22.91 dBm	657.9	mA
		WCDMA B5 HSDPA @ 23.06 dBm	574.5	mA
		WCDMA B5 HSUPA @ 22.73 dBm	575.9	mA
		WCDMA B8 HSDPA @ 23.36 dBm	673.2	mA
		WCDMA B8 HSUPA @ 22.97 dBm	669.2	mA
	LTE data transfer	LTE-FDD B1 @ 22.54 dBm	684.1	mA
		LTE-FDD B3 @ 22.22 dBm	690.1	mA
		LTE-FDD B5 @ 22.39 dBm	613.2	mA
		LTE-FDD B8 @ 22.42 dBm	676.8	mA
		LTE-TDD B34 @ 23.01 dBm	336.5	mA
		LTE-TDD B38 @ 22.81 dBm	405.2	mA
		LTE-TDD B39 @ 22.87 dBm	334.1	mA
		LTE-TDD B40 @ 23.12 dBm	469.3	mA
		LTE-TDD B41 @ 23.37 dBm	428.5	mA

	GSM voice call	EGSM900 PCL = 5 @ 32.27 dBm	242.2	mA
		EGSM900 PCL = 12 @ 19.64 dBm	120.1	mA
		EGSM900 PCL = 19 @ 5.75 dBm	94.2	mA
		DCS1800 PCL = 0 @ 29.95 dBm	223.6	mA
		DCS1800 PCL = 7 @ 16.27 dBm	116.2	mA
		DCS1800 PCL = 15 @ 1.11 dBm	92.2	mA
	WCDMA voice call	WCDMA B1 @ 23.57 dBm	646.9	mA
		WCDMA B5 @ 23.07 dBm	556.1	mA
		WCDMA B8 @ 23.21 dBm	653.1	mA

NOTE

"*" means under development.

Table 35：EC200T-EU Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	11	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.02	mA
		EGSM900 @ DRX = 2 (USB disconnected)	3.67	mA
		EGSM900 @ DRX = 5 (USB disconnected)	3.00	mA
		EGSM900 @ DRX = 5 (USB suspend)	3.15	mA
		EGSM900 @ DRX = 9 (USB disconnected)	3.47	mA
		DCS1800 @ DRX = 2 (USB disconnected)	3.55	mA
		DCS1800 @ DRX = 5 (USB disconnected)	3.24	mA

	DCS1800 @ DRX = 5 (USB suspend)	3.12	mA
	DCS1800 @ DRX = 9 (USB disconnected)	3.38	mA
	WCDMA @ PF = 64 (USB disconnected)	4.18	mA
	WCDMA @ PF = 64 (USB suspend)	3.89	mA
	WCDMA @ PF = 128 (USB disconnected)	2.64	mA
	WCDMA @ PF = 256 (USB disconnected)	2.61	mA
	WCDMA @ PF = 512 (USB disconnected)	4.63	mA
	LTE-FDD @ PF = 32 (USB disconnected)	4.38	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.99	mA
	LTE-FDD @ PF = 64 (USB suspend)	3.48	mA
	LTE-FDD @ PF = 128 (USB disconnected)	2.58	mA
	LTE-FDD @ PF = 256 (USB disconnected)	3.41	mA
	LTE-TDD @ PF = 32 (USB disconnected)	5.11	mA
	LTE-TDD @ PF = 64 (USB disconnected)	3.53	mA
	LTE-TDD @ PF = 64 (USB suspend)	3.72	mA
	LTE-TDD @ PF = 128 (USB disconnected)	2.93	mA
	LTE-TDD @ PF = 256 (USB disconnected)	3.60	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	29.18	mA
	EGSM900 @ DRX = 5 (USB connected)	37.19	mA
	WCDMA @ PF = 64 (USB disconnected)	30.26	mA
	WCDMA @ PF = 64 (USB connected)	38.28	mA

	LTE-FDD @ PF = 64 (USB disconnected)	30.20	mA
	LTE-FDD @ PF = 64 (USB connected)	40	mA
	LTE-TDD @ PF = 64 (USB disconnected)	30.6	mA
	LTE-TDD @ PF = 64 (USB connected)	49.83	mA
GPRS data transfer	EGSM900 4DL/1UL @ 33.07 dBm	274	mA
	EGSM900 3DL/2UL @ 33.04 dBm	459	mA
	EGSM900 2DL/3UL @ 31.29 dBm	529	mA
	EGSM900 1DL/4UL @ 29.16 dBm	545	mA
	DCS1800 4DL/1UL @ 31.52 dBm	230	mA
	DCS1800 3DL/2UL @ 31.55 dBm	371	mA
	DCS1800 2DL/3UL @ 30.21 dBm	449	mA
	DCS1800 1DL/4UL @ 28.25 dBm	473	mA
EDGE data transfer	EGSM900 4DL/1UL @ 26.88 dBm	216	mA
	EGSM900 3DL/2UL @ 26.61 dBm	346	mA
	EGSM900 2DL/3UL @ 24.91 dBm	471	mA
	EGSM900 1DL/4UL @ 23.15 dBm	586	mA
	DCS1800 4DL/1UL @ 26.73 dBm	188	mA
	DCS1800 3DL/2UL @ 26.59 dBm	293	mA
	DCS1800 2DL/3UL @ 25.10 dBm	389	mA
	DCS1800 1DL/4UL @ 22.70 dBm	479	mA
WCDMA data transfer	WCDMA B1 HSDPA @ 23.07 dBm	659	mA
	WCDMA B1 HSUPA @ 22.24 dBm	640	mA
	WCDMA B8 HSDPA @ 23.22 dBm	612	mA
	WCDMA B8 HSUPA @ 22.50 dBm	600	mA

	LTE data transfer	LTE-FDD B1 @ 23.10 dBm	704	mA
		LTE-FDD B3 @ 23.17 dBm	670	mA
		LTE-FDD B7 @ 24.41 dBm	890	mA
		LTE-FDD B8 @ 22.76 dBm	630	mA
		LTE-FDD B20 @ 24.09 dBm	703	mA
		LTE-FDD B28 @ 23.9 dBm	738	mA
		LTE-TDD B38 @ 23.13 dBm	360	mA
		LTE-TDD B40 @ 23.23 dBm	393	mA
		LTE-TDD B41 @ 23.81 dBm	391	mA
	GSM voice call	EGSM900 PCL = 5 @ 33.00 dBm	270	mA
		EGSM900 PCL = 12 @ 19.53 dBm	123	mA
		EGSM900 PCL = 19 @ 5.71 dBm	97	mA
		DCS1800 PCL = 0 @ 31.47 dBm	226	mA
		DCS1800 PCL = 7 @ 18.37 dBm	116	mA
		DCS1800 PCL = 15 @ 2.74 dBm	94	mA
	WCDMA voice cal	WCDMA B1 @ 23.06 dBm	636	mA
		WCDMA B8 @ 23.34 dBm	597	mA

备注

“*” means under development.

Table 36：EC200T-AU Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	9	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.07	mA
		EGSM900 @ DRX = 2 (USB disconnected)	3.55	mA
		EGSM900 @ DRX = 5 (USB disconnected)	2.45	mA
		EGSM900 @ DRX = 5 (USB suspend)	2.80	mA
		EGSM900 @ DRX = 9 (USB disconnected)	2.87	mA
		DCS1800 @ DRX = 2 (USB disconnected)	3.60	mA
		DCS1800 @ DRX = 5 (USB disconnected)	2.77	mA
		DCS1800 @ DRX = 5 (USB suspend)	2.85	mA
		DCS1800 @ DRX = 9 (USB disconnected)	3.03	mA
		WCDMA @ PF = 64 (USB disconnected)	3.89	mA
		WCDMA @ PF = 64 (USB suspend)	3.90	mA
		WCDMA @ PF = 128 (USB disconnected)	3.31	mA
		WCDMA @ PF = 256 (USB disconnected)	2.74	mA
		WCDMA @ PF = 512 (USB disconnected)	4.42	mA
		LTE-FDD @ PF = 32 (USB disconnected)	5.48	mA
		LTE-FDD @ PF = 64 (USB disconnected)	3.62	mA
		LTE-FDD @ PF = 64 (USB suspend)	3.58	mA
		LTE-FDD @ PF = 128 (USB disconnected)	2.92	mA

	LTE-FDD @ PF = 256 (USB disconnected)	2.34	mA
	LTE-TDD @ PF = 32 (USB disconnected)	5.76	mA
	LTE-TDD @ PF = 64 (USB disconnected)	3.72	mA
	LTE-TDD @ PF = 64 (USB suspend)	3.92	mA
	LTE-TDD @ PF = 128 (USB disconnected)	2.76	mA
	LTE-TDD @ PF = 256 (USB disconnected)	2.72	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	30.12	mA
	EGSM900 @ DRX = 5 (USB connected)	49.22	mA
	WCDMA @ PF = 64 (USB disconnected)	31.07	mA
	WCDMA @ PF = 64 (USB connected)	50.13	mA
	LTE-FDD @ PF = 64 (USB disconnected)	30.82	mA
	LTE-FDD @ PF = 64 (USB connected)	49.90	mA
	LTE-TDD @ PF = 64 (USB disconnected)	31.34	mA
	LTE-TDD @ PF = 64 (USB connected)	50.31	mA
GPRS data transfer	EGSM900 4DL/1UL @ 33.44 dBm	268.3	mA
	EGSM900 3DL/2UL @ 33.39 dBm	467.8	mA
	EGSM900 2DL/3UL @ 31.44 dBm	543.9	mA
	EGSM900 1DL/4UL @ 29.45 dBm	567.6	mA
	DCS1800 4DL/1UL @ 30.29 dBm	217.0	mA
	DCS1800 3DL/2UL @ 30.31 dBm	364.4	mA
	DCS1800 2DL/3UL @ 28.85 dBm	437.5	mA
	DCS1800 1DL/4UL @ 26.88 dBm	464	mA

		PCS1900 4DL/1UL @ 30.10 dBm	212.5	mA
		PCS1900 3DL/2UL @ 30.10 dBm	355.6	mA
		PCS1900 2DL/3UL @ 28.65 dBm	425.4	mA
		PCS1900 1DL/4UL @ 26.72 dBm	450.9	mA
		EGSM850 4DL/1UL @ 33.01 dBm	265.2	mA
		EGSM850 3DL/2UL @ 32.97 dBm	459.4	mA
		EGSM850 2DL/3UL @ 31.48 dBm	554.3	mA
		EGSM850 1DL/4UL @ 29.37 dBm	580.2	mA
	EDGE data transfer	EGSM900 4DL/1UL @ 28.69 dBm	215.2	mA
		EGSM900 3DL/2UL @ 28.49 dBm	366.1	mA
		EGSM900 2DL/3UL @ 25.67 dBm	489.6	mA
		EGSM900 1DL/4UL @ 23.43 dBm	610.4	mA
		DCS1800 4DL/1UL @ 26.93 dBm	179.7	mA
		DCS1800 3DL/2UL @ 26.80 dBm	296.2	mA
		DCS1800 2DL/3UL @ 25.29 dBm	394.7	mA
		DCS1800 1DL/4UL @ 22.88 dBm	495.4	mA
		PCS1800 4DL/1UL @ 26.38 dBm	176.2	mA
		PCS1800 3DL/2UL @ 26.29 dBm	288.6	mA
		PCS1800 2DL/3UL @ 24.88 dBm	389.7	mA
		PCS1800 1DL/4UL @ 22.62 dBm	490.7	mA
		EGSM850 4DL/1UL @ 27.18 dBm	214.0	mA
		EGSM850 3DL/2UL @ 26.68 dBm	359.6	mA
		EGSM850 2DL/3UL @ 24.94 dBm	487.2	mA
		EGSM850 1DL/4UL @ 22.60 dBm	606.3	mA
	WCDMA data	WCDMA B1 HSDPA @ 23.77 dBm	740.0	mA

	transfer	WCDMA B1 HSUPA @ 23.10 dBm	729.1	mA
		WCDMA B2 HSDPA @ 23.73 dBm	835.1	mA
		WCDMA B2 HSUPA @ 22.24 dBm	761.2	mA
		WCDMA B4 HSDPA @ 24.29 dBm	767.6	mA
		WCDMA B4 HSUPA @ 22.59 dBm	689.6	mA
		WCDMA B5 HSDPA @23.65dBm	643.5	mA
		WCDMA B5 HSUPA @ 22.79 dBm	631.4	mA
		WCDMA B8 HSDPA @ 23.94 dBm	677.2	mA
		WCDMA B8 HSUPA @ 23.22 dBm	653.1	mA
	LTE data transfer	LTE-FDD B1 @ 22.89 dBm	737.4	mA
		LTE-FDD B2 @ 22.29 dBm	780.8	mA
		LTE-FDD B3 @ 23.21 dBm	729.4	mA
		LTE-FDD B4 @ 22.49 dBm	717.3	mA
		LTE-FDD B5 @ 23.41 dBm	677.3	mA
		LTE-FDD B7 @ 23.18 dBm	895.5	mA
		LTE-FDD B8 @ 22.12 dBm	676.4	mA
		LTE-FDD B28 @ 23.67 dBm	744.8	mA
		LTE-FDD B66 @ 22.71 dBm	722.7	mA
		LTE-TDD B40 @ 23.25 dBm	423.9	mA
	GSM voice call	EGSM900 PCL = 5 @ 33.49 dBm	280.2	mA
		EGSM900 PCL = 12 @ 19.79 dBm	126.4	mA
		EGSM900 PCL = 19 @ 7.03 dBm	98.9	mA
		DCS1800 PCL = 0 @ 30.33 dBm	226.2	mA
		DCS1800 PCL = 7 @ 16.97 dBm	117.6	mA
		DCS1800 PCL = 15 @ 1.45 dBm	96.6	mA

	PCS1900 PCL = 0 @ 30.16 dBm	220.2	mA
	PCS1900 PCL = 7 @ 16.78 dBm	117.3	mA
	PCS1900 PCL = 15 @ 1.63 dBm	97.5	mA
	EGSM850 PCL = 5 @ 32.97 dBm	276.1	mA
	EGSM850 PCL = 12 @ 19.79 dBm	128.5	mA
	EGSM850 PCL = 19 @ 6.73 dBm	100.0	mA
WCDMA voice call	WCDMA B1 @ 23.42 dBm	718.3	mA
	WCDMA B2 @ 23.44 dBm	818.6	mA
	WCDMA B4 @ 24.02 dBm	752.1	mA
	WCDMA B5 @ 23.38 dBm	625.6	mA
	WCDMA B8 @ 23.57 dBm	658.3	mA

备注

“*” means under development.

5.5. RF Output Power

The following table shows the RF output power of EC200T series module.

Table 37: EC200T-CN RF Output Power

Frequency	Max.	Min.
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB

WCDMA B1/B5/B8	24 dBm +1/-3 dB	< -49 dBm
LTE-FDD B1/B3/B5/B8	23 dBm ±2 dB	< -39 dBm
LTE-TDD B34/B38/B39/B40/B41	23 dBm ±2 dB	< -39 dBm

Table 38: EC200T-EU RF Output Power

Frequency	Max.	Min.
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
WCDMA B1/B8	24 dBm +1/-3 dB	< -49 dBm
LTE-FDD B1/B3/B7/B8/B20/B28	23 dBm ±2 dB	< -39 dBm
LTE-TDD B38/B40/B41	23 dBm ±2 dB	< -39 dBm

Table 39: EC200T-AU* RF Output Power

Frequency	Max.	Min.
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
GSM850	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
EGSM850 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
PCS1900 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
WCDMA B1/B2/B4/B5/B8	24 dBm +1/-3 dB	< -49 dBm

LTE-FDD B1/B2/B3/B4/B5/B7/B8/B28	23 dBm ±2 dB	< -39 dBm
LTE-TDD B40	23 dBm ±2 dB	< -39 dBm

NOTES

1. In GPRS 4 slots Tx mode, the maximum output power is reduced by 2.5 dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.
2. "*" means under development.

5.6. RF Receiving Sensitivity

The following table shows conducted RF receiving sensitivity of EC200T-CN module. And the data for EC200T-EU and EC200T-AU* will be supplemented in subsequent versions of this document.

Table 40: EC200T-CN Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
EGSM900	-108 dBm	NA	NA	-102 dBm
DCS1800	-108 dBm	NA	NA	-102 dBm
WCDMA B1	-108 dBm	NA	NA	-106.7 dBm
WCDMA B5	-109 dBm	NA	NA	-104.7 dBm
WCDMA B8	-110 dBm	NA	NA	-103.7 dBm
LTE-FDD B1 (10 MHz)	-97 dBm	-98.5 dBm	-100 dBm	-96.3 dBm
LTE-FDD B3 (10 MHz)	-97.5 dBm	-97.5 dBm	-100.5 dBm	-93.3 dBm
LTE-FDD B5 (10 MHz)	-98 dBm	-99 dBm	-101 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98 dBm	-98 dBm	-101 dBm	-93.3 dBm
LTE-TDD B34 (10 MHz)	-96.5 dBm	-97 dBm	-100 dBm	-96.3 dBm
LTE-TDD B38 (10 MHz)	-97 dBm	-97.5 dBm	-100 dBm	-96.3 dBm

LTE-TDD B39 (10 MHz)	-97 dBm	-97.5 dBm	-100 dBm	-96.3 dBm
LTE-TDD B40 (10 MHz)	-97 dBm	-97 dBm	-100 dBm	-96.3 dBm
LTE-TDD B41 (10 MHz)	-96 dBm	-97 dBm	-99 dBm	-94.3 dBm

Table 41: EC200T-EU Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
EGSM900	TBD	NA	NA	-102 dBm
DCS1800	TBD	NA	NA	-102 dBm
WCDMA B1	TBD	NA	NA	-106.7 dBm
WCDMA B8	TBD	NA	NA	-103.7 dBm
LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	-93.3 dBm
LTE-FDD B7 (10 MHz)	TBD	TBD	TBD	-94.3 dBm
LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	-93.3 dBm
LTE-TDD B20 (10 MHz)	TBD	TBD	TBD	-93.3 dBm
LTE-TDD B28 (10 MHz)	TBD	TBD	TBD	-94.8 dBm
LTE-TDD B38 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-TDD B40 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	-94.3 dBm

Table 42: EC200T-AU* Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
GSM850	TBD	NA	NA	-102 dBm
EGSM900	TBD	NA	NA	-102 dBm

DCS1800	TBD	NA	NA	-102 dBm
DCS1900	TBD	NA	NA	-102 dBm
WCDMA B1	TBD	NA	NA	-106.7 dBm
WCDMA B2	TBD	NA	NA	-104.7 dBm
WCDMA B4	TBD	NA	NA	-106.7 dBm
WCDMA B5	TBD	NA	NA	-104.7 dBm
WCDMA B8	TBD	NA	NA	-103.7 dBm
LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-FDD B2 (10 MHz)	TBD	TBD	TBD	-94.3 dBm
LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	-93.3 dBm
LTE-FDD B4 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	-94.3 dBm
LTE-FDD B7 (10 MHz)	TBD	TBD	TBD	-94.3 dBm
LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	-93.3 dBm
LTE-TDD B28 (10 MHz)	TBD	TBD	TBD	-94.8 dBm
LTE-TDD B40 (10 MHz)	TBD	TBD	TBD	-96.3 dBm
LTE-TDD B66 (10 MHz)	TBD	TBD	TBD	-96.3 dBm

NOTE

"*" means under development.

5.7. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module electrostatics discharge characteristics.

Table 43: Electrostatics Discharge Characteristics (25 ºC, 45% Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±8	±10	kV
All Antenna Interfaces	±8	±10	kV
Other Interfaces	±0.5	±1	kV

6 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.05 mm unless otherwise specified.

6.1. Mechanical Dimensions of the Module

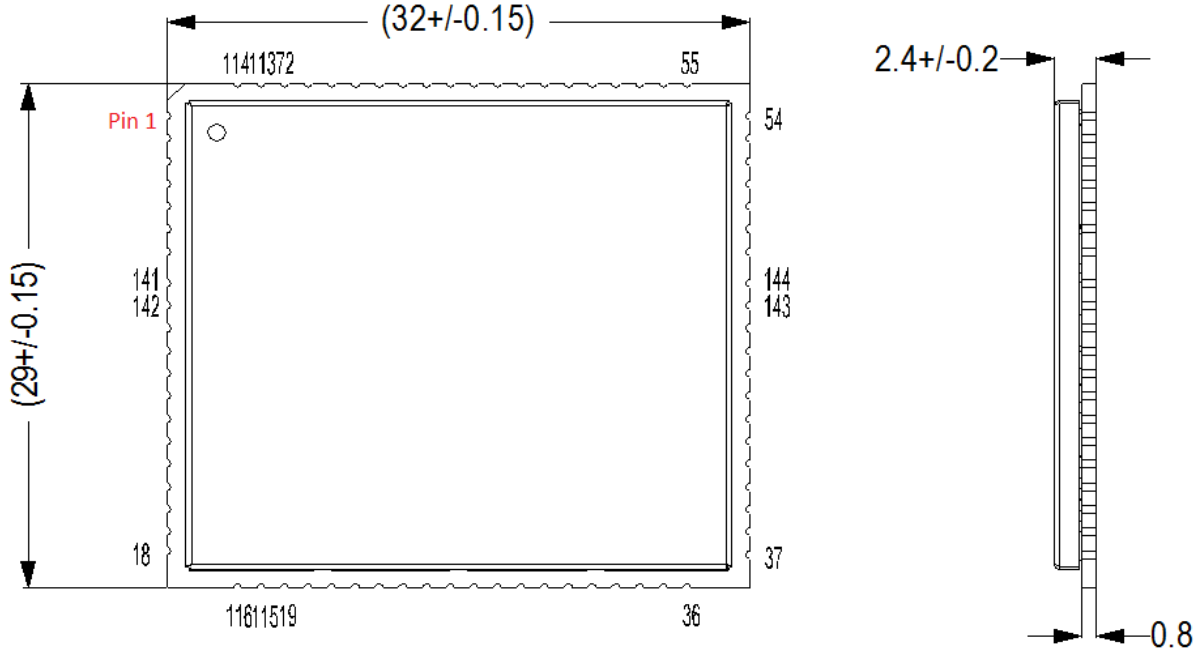


Figure 36: Module Top and Side Dimensions

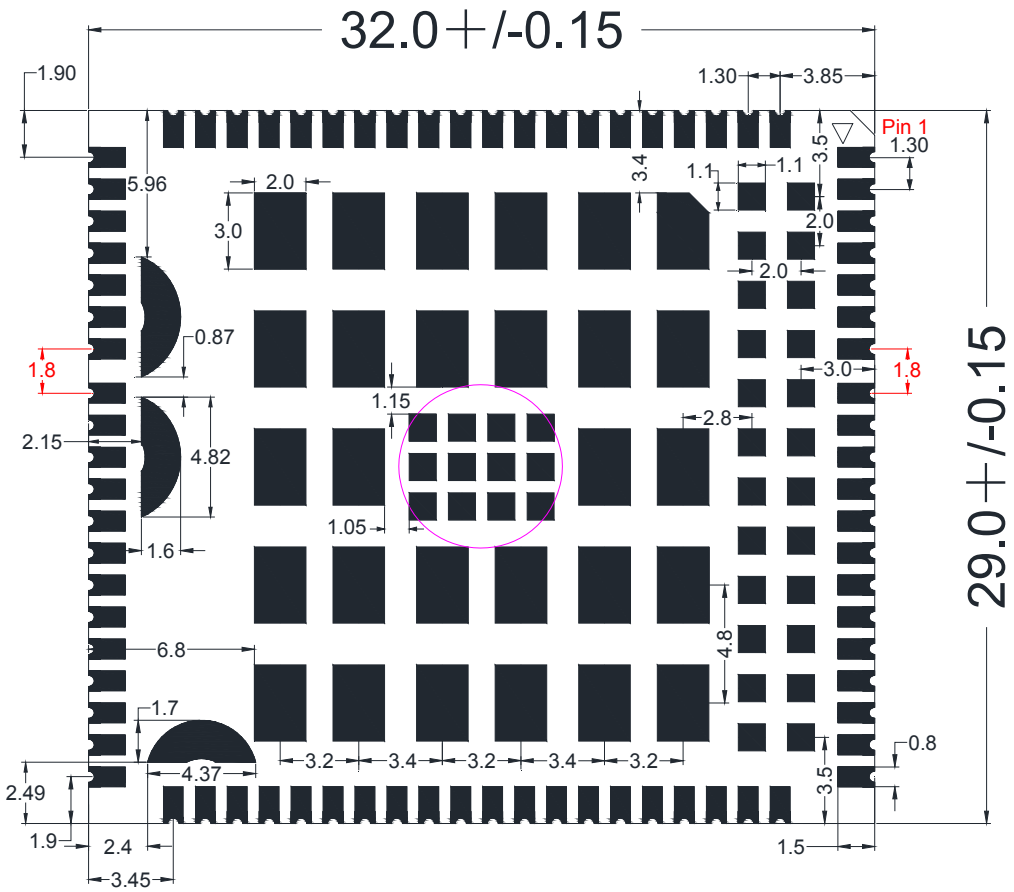


Figure 37: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to *JEITA ED-7306* standard.

6.2. Recommended Footprint

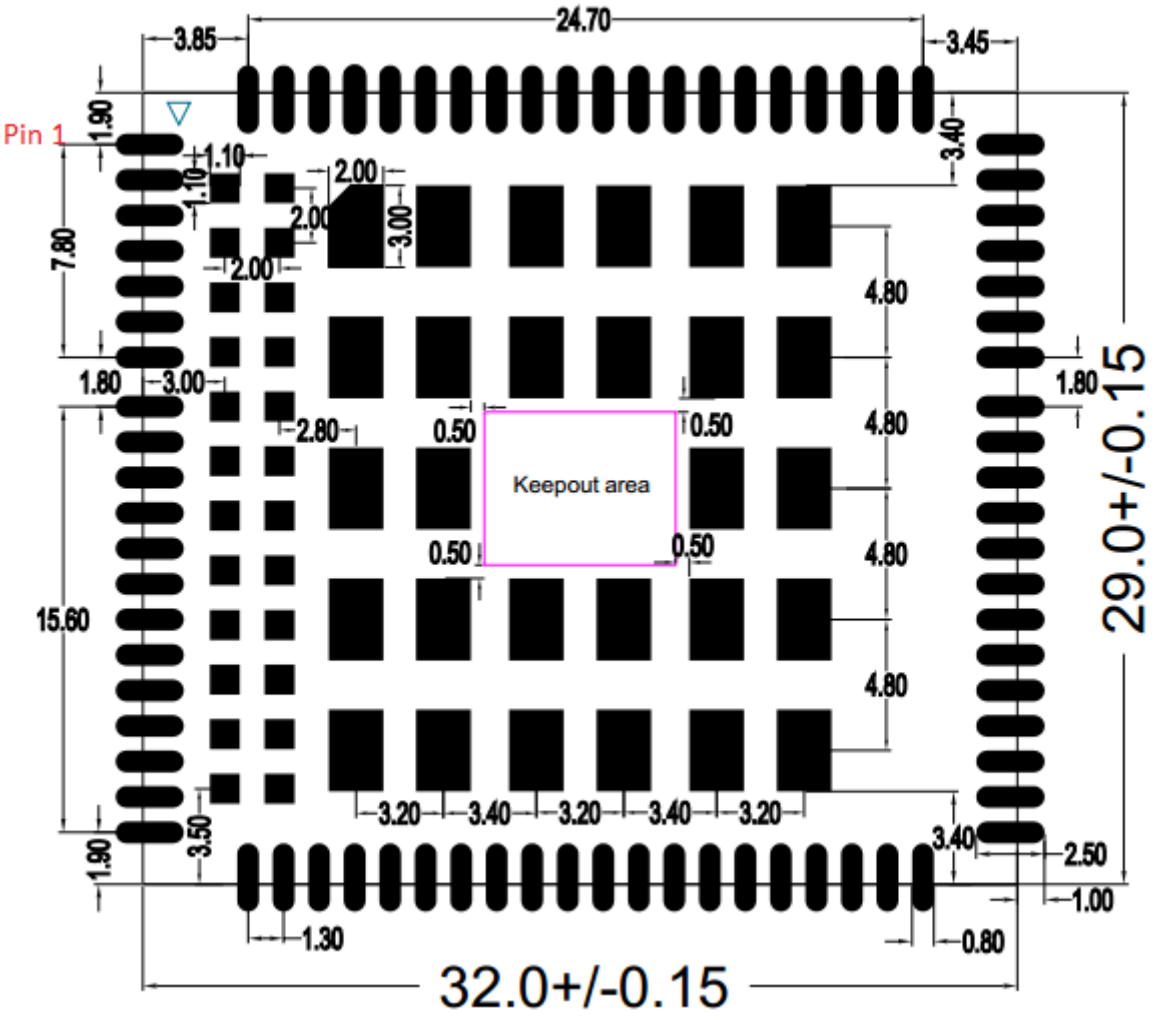


Figure 38: Recommended Footprint (Top View)

NOTES

1. The keepout area should not be designed.
2. For easy maintenance of the module, please keep about 3 mm between the module and other components in the host PCB.

6.3. Design Effect Drawings of the Module

Figure 39: Top View of the Module

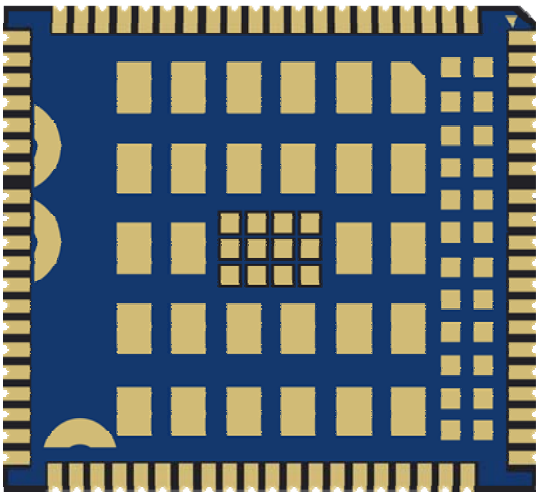


Figure 40: Bottom View of the Module

NOTE

These are renderings of EC200T series module. For authentic appearance, please refer to the module that you receive from Quectel.

7 Storage, Manufacturing and Packaging

7.1. Storage

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35%–60%.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [1)] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60%. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10% (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

NOTES

1. [1)] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*.
2. To avoid blistering, layer separation and other soldering issues, it is forbidden to expose the modules to the air for a long time. If the temperature and moisture do not conform to *IPC/JEDEC J-STD-033* or the relative moisture is over 60%, It is recommended to start the solder reflow process within 24 hours after the package is removed. And do not remove the packages of tremendous modules if they are not ready for soldering.
3. Please take the module out of the packaging and put it on high-temperature resistant fixtures before the baking. If shorter baking time is desired, please refer to *IPC/JEDEC J-STD-033* for baking procedure.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20 mm. For more details, see ***document [1]***.

It is suggested that the peak reflow temperature is 238–246 ºC, and the absolute maximum reflow temperature is 246 ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

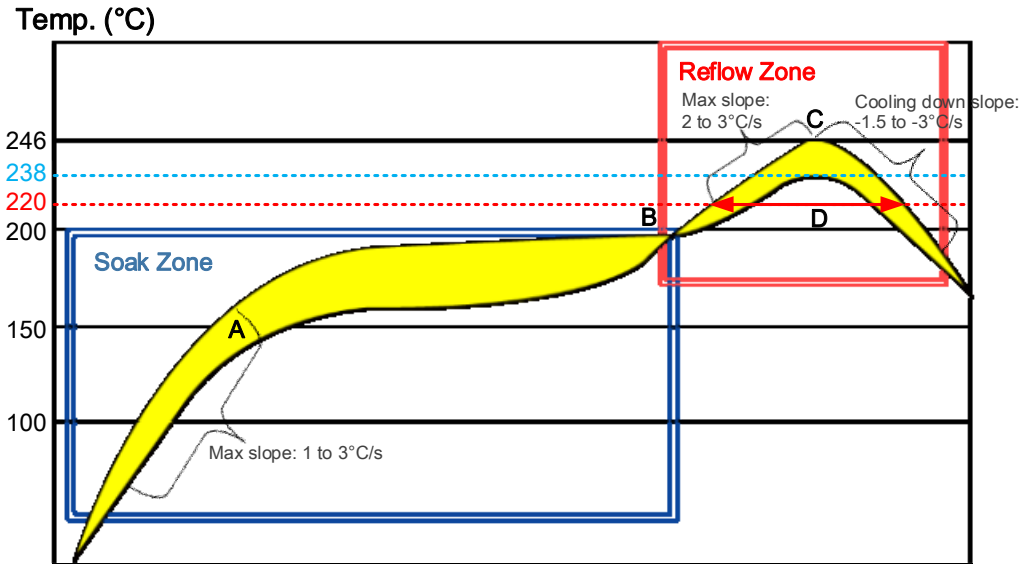


Figure 41: Recommended Reflow Soldering Thermal Profile

Table 44: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	2–3 °C/s
Reflow time (D: over 220°C)	45–70 s
Max temperature	238 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTES

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.

7.3. Packaging

EC200T series is packaged in tape and reel carriers. One reel is 11.88 m long and contains 250 modules. The figure below shows the package details, measured in mm.

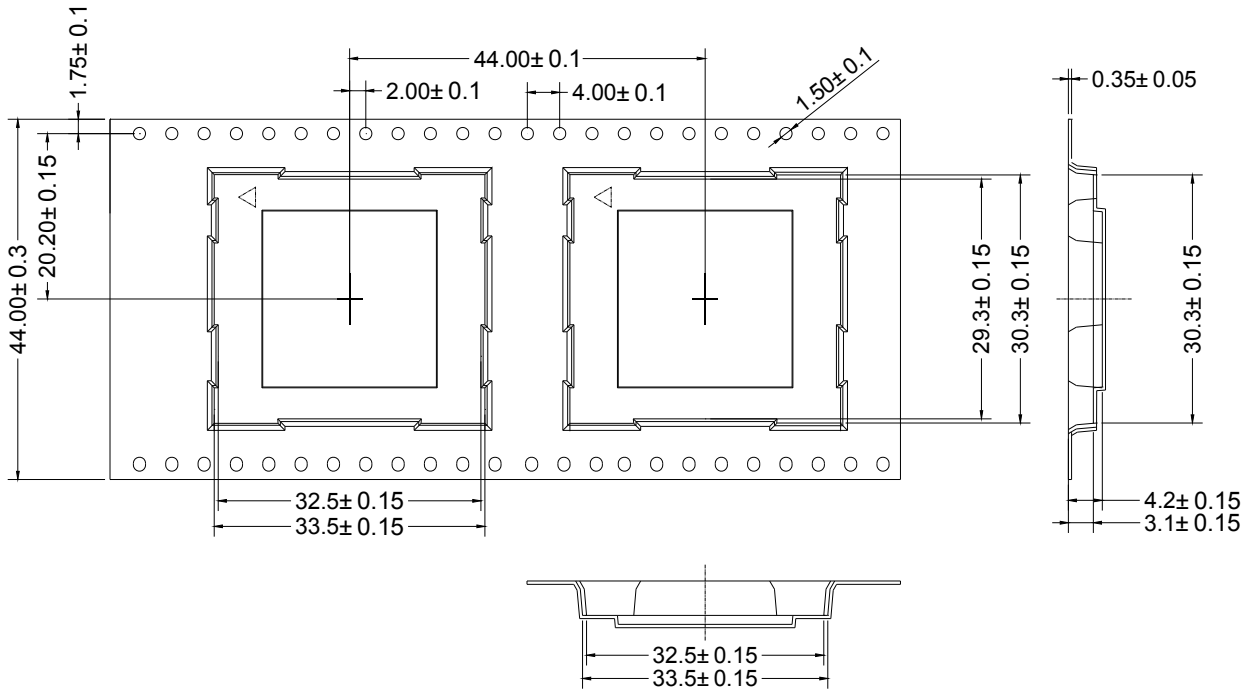


Figure 42: Tape Specifications

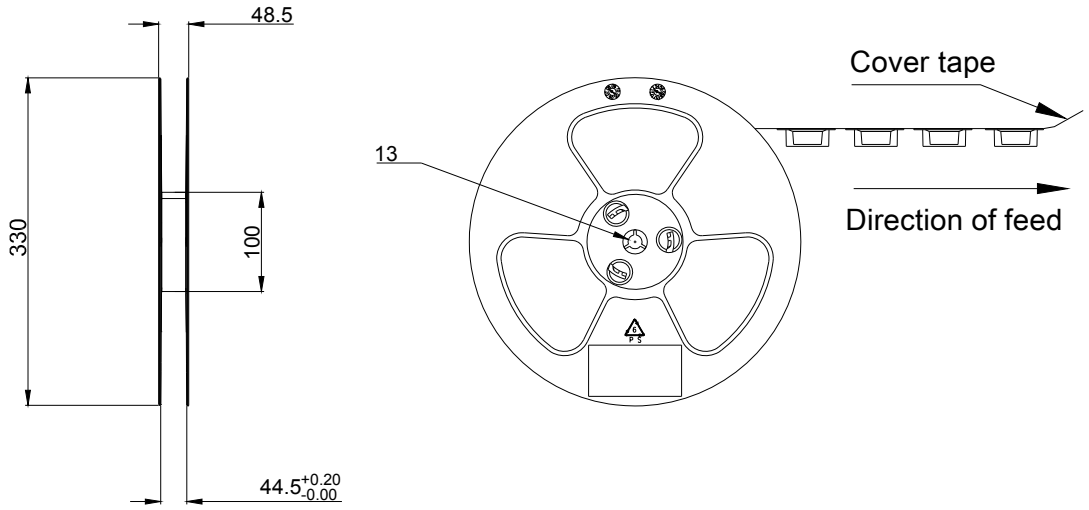


Figure 43: Reel Specifications

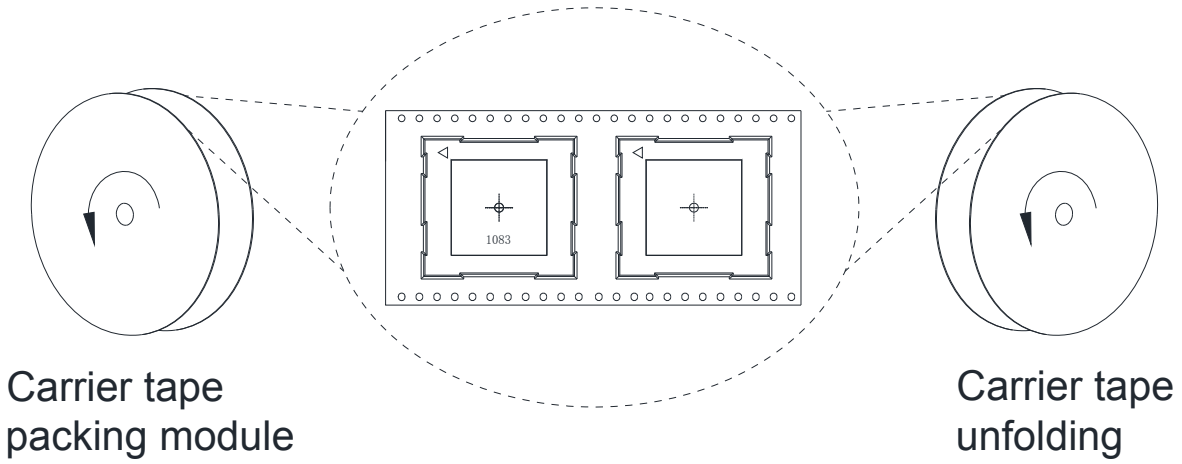


Figure 44: Tape and Reel Directions

8 Appendix A References

Table 45: Related Documents

SN	Document Name	Remark
[1]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide
[2]	Quectel_EC200T-CN_AT_Commands_Manual	EC200T-CN AT Commands Manual
[3]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[4]	Quectel_UMTS&LTE_EVB_User_Guide	UMTS&LTE EVB user guide for UMTS&LTE modules

Table 46: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear To Send
DL	Downlink
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
EGSM	Extended GSM900 Band (including standard GSM900 band)

ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP over SSL
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	Hyper Text Transfer Protocol
HTTPS	Hyper Text Transfer Protocol over Secure Socket Layer
LED	Light Emitting Diode
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport
MSL	Moisture Sensitivity Level
NITZ	Network Identity and Time Zone
NTP	Network Time Protocol
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PF	Paging Frame

PPP	Point-to-Point Protocol
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SIMO	Single Input Multiple Output
SM	Smart Media
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver &Transmitter
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal)Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value

V_{IL}min	Minimum Input Low Level Voltage Value
$V_I$max	Absolute Maximum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

9 Appendix B GPRS Coding Schemes

Table 47: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

10 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3 + 1 or 2 + 2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 48: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA

14	4	4	NA
15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

11 Appendix D EDGE Modulation and Coding Schemes

Table 49: EDGE Modulation and Coding Schemes

Coding Scheme	Modulation	Coding Family	Timeslot 1	Timeslot 2	Timeslot 4
MCS-1	GMSK	C	8.80 kbps	17.60 kbps	35.20 kbps
MCS-2	GMSK	B	11.2 kbps	22.4 kbps	44.8 kbps
MCS-3	GMSK	A	14.8 kbps	29.6 kbps	59.2 kbps
MCS-4	GMSK	C	17.6 kbps	35.2 kbps	70.4 kbps
MCS-5	8-PSK	B	22.4 kbps	44.8 kbps	89.6 kbps
MCS-6	8-PSK	A	29.6 kbps	59.2 kbps	118.4 kbps
MCS-7	8-PSK	B	44.8 kbps	89.6 kbps	179.2 kbps
MCS-8	8-PSK	A	54.4 kbps	108.8 kbps	217.6 kbps
MCS-9	8-PSK	A	59.2 kbps	118.4 kbps	236.8 kbps