SC600Y&SC600T

Hardware Design

Smart Module Series

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GENERAL NOTES

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About the Document

History

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1 Introduction

This document defines the SC600Y/SC600T module and describes its air interfaces and hardware interfaces which are connected with customers' applications.

This document helps customers quickly understand module interface specifications, electrical and mechanical details as well as other related information of SC600Y/SC600T module. Associated with application note and user guide, customers can use SC600Y/SC600T module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating SC600Y/SC600T module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.

Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.

The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.

In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

SC600Y/SC600T is a series of Smart module based on Qualcomm platform and Android operating system, and provides industrial grade performance. Their general features are listed below:

- Support short-range wireless communication via Wi-Fi 802.11a/b/g/n/ac and BT4.2 LE standards
- Integrate GPS/GLONASS/BeiDou satellite positioning systems
- Support multiple audio and video codecs
- Built-in high performance Adreno^{TM}506 graphics processing unit
- Provide multiple audio and video input/output interfaces as well as abundant GPIO interfaces

删除的内容: <#>Support worldwide LTE-FDD, LTE-TDD, DC-HSDPA, DC-HSUPA, HSPA+, HSDPA, HSUPA, WCDMA, EDGE, GPRS and GSM coverage .

SC600Y (standard version) and SC600T (high-performance version) are available in SC600Y-EM/ SC600T-EM, SC600Y-NA/SC600T-NA, SC600Y-JP/SC600T-JP and SC600Y-WF/SC600T-WF.

The following table shows the supported frequency bands of SC600Y/SC600T.

Table 1: SC600Y-EM/SC600T-EM Frequency Bands

Type	Frequency Bands
Wi-Fi 802.11a/b/g/n/ac	2402MHz~2482MHz; 5180MHz~5825MHz*
BT4.2 LE	2402MHz~2480MHz
GNSS	GPS: 1575.42MHz±1.023MHz GLONASS: 1597.5MHz~1605.8MHz BeiDou: 1561.098MHz±2.046MHz

删除的内容: LTE-FDD ... [3]

Table 2: SC600Y-NA/SC600T-NA Frequency Bands

Type	Frequency Bands
Wi-Fi 802.11a/b/g/n/ac	2402MHz~2482MHz; 5180MHz~5825MHz*
BT4.2 LE	2402MHz~2480MHz

删除的内容: LTE-FDD ... [4]

GNSS	GPS: 1575.42MHz±1.023MHz GLONASS: 1597.5MHz~1605.8MHz BeiDou: 1561.098MHz±2.046MHz

Table 3: SC600Y-JP/SC600T-JP Frequency Bands

Type	Frequency Bands
Wi-Fi 802.11a/b/g/n/ac	2402MHz~2482MHz; 5180MHz~5825MHz*
BT4.2 LE	2402MHz~2480MHz
GNSS	GPS: 1575.42MHz±1.023MHz GLONASS: 1597.5MHz~1605.8MHz BeiDou: 1561.098MHz±2.046MHz

删除的内容: LTE-FDD ... [5]

Table 4: SC600Y-WF/SC600T-WF Frequency Bands

Type	Frequency Bands
Wi-Fi 802.11a/b/g/n/ac	2402MHz~2482MHz; 5180MHz~5825MHz *
BT4.2 LE	2402MHz~2480MHz
GNSS	/

删除的内容: LTE-FDD ... [6]

SC600Y/SC600T is an SMD-type module, which can be embedded into applications through its 323 pins (including 152 LCC pins and 171 LGA pins). With a compact profile of 43.0mm × 44.0mm × 2.85mm, SC600Y/SC600T can meet almost all requirements for M2M applications such as smart metering, smart home, security, routers, wireless POS, mobile computing devices, PDA phone, tablet PC, etc. Additionally, SC600Y/SC600T supports AI applications such as face and vehicle recognition.

* The device is restricted to indoor use only when operation in the 5150 to 5350 MHz frequency range.

2.2. Key Features

The following table describes the detailed features of SC600Y/SC600T module.

Table 5: SC600Y/SC600T Key Features

Features	Details
Application Processor	**SC600Y** Octa-core ARM Cortex-A53 64-bit CPU @1.8GHz (standard) ● Two quad-core processors with 512KB L2 cache **SC600T** Octa-core ARM Cortex-A53 64-bit CPU @2.0GHz (high performance) ● One quad-core with 1MB L2 cache ● One quad-core with 512KB L2 cache
Modem system	Hexagon DSP v56 core up to 850MHz 768KB L2 caches
GPU	**SC600Y** Adreno™ 506 with 64-bit addressing, designed for 600MHz **SC600T** Adreno™ 506 with 64-bit addressing, designed for 650MHz
Operating System	Android OS 9.0
Power Supply	VBAT Supply Voltage: 3.55V~4.4V Typical: 3.8V
WLAN Features	2.4GHz/5GHz, 802.11a/b/g/n/ac, maximally up to 433Mbps Support AP and STA modes
Bluetooth Features	BT4.2 LE
GNSS Features	GPS/GLONASS/BeiDou
SMS	Text and PDU mode Point-to-point MO and MT SMS cell broadcast
LCM Interfaces	Support two groups of 4-lane MIPI_DSI Support dual LCDs Support WUXGA up to (1920×1200) at 60fps Provide one high voltage output for powering a string of WLEDs Provide four drivers for sinking the current from WLED strings, and each sink current can reach up to 25mA
Camera Interfaces	Support three groups of 4-lane MIPI_CSI, up to 2.1Gbps per lane Support 3 cameras (4-lane + 4-lane + 4-lane) or 4 cameras (4-lane + 4-lane +

删除的内容: Memory ... [7]

删除的内容: Transmitting Power ... [8]

	2-lane + 1-lane) **SC600Y** Up to 21MP with dual ISP **SC600T** Up to 24MP with dual ISP
Video Codec	**SC600Y** Video encoding and decoding: up to 1080P @60fps Wi-Fi Video: encoding up to 1080P @30fps; decoding up to 1080P @60fps **SC600T** Video encoding and decoding: up to 4K @30fps, up to 1080P @60fps Wi-Fi Video: encoding up to 1080P @30fps; decoding up to 1080P @60fps
Audio Interfaces	**Audio Input** Three analog microphone inputs, integrating internal bias voltage **Audio Output** Class AB stereo headphone output Class AB earpiece differential output Class D speaker differential amplifier output
Audio Codec	G711, QCELP, EVRC, EVRC-B, EVRC-WB, AMR-NB, AMR-WB, GSM-EFR, GSM-FR, GSM-HR
USB Interface	Support with USB 3.0 or 2.0 specifications, with transmission rates up to 5Gbps on USB 3.0 and 480Mbps on USB 2.0 Support USB OTG Used for AT command communication, data transmission, software debugging and firmware upgrade
UART Interfaces	4 UART Interfaces: UART5, UART6, UART4 and UART2 ● UART5 & UART6: 4-wire UART interface with RTS/CTS hardware flow control, baud rate up to 4Mbps ● UART4: 2-wire UART interface ● UART2: 2-wire UART interface used for debugging
Vibrator drive interface	Drive ERM vibrator
SD Card Interface	Support SD 3.0 Support SD card hot-plug
(U)SIM Interfaces	2 (U)SIM interfaces Support USIM/SIM card: 1.8V/2.95V Support Dual SIM Dual Standby (supported by default)
I2C Interfaces	5 I2C interfaces, used for peripherals such as TP, camera, sensor, etc.
I2S Interface	Support for I2S peripherals
Flashlight Interfaces	2 high current Flash and torch LED driver ● Up to 0.75A each for two LEDs and 1.5A for one LED in Flash mode ● Up to 300mA each for two LEDs and 300mA for one LED in torch mode

ADC Interfaces	2 general purpose ADC interfaces Support up to 15-bit sampling accuracy
SPI Interfaces	2 SPI interfaces, only support master mode ● One SPI interface used for peripheral device ● One SPI interface used for sensor application, such as fingerprint sensor
Charging Interface	Used for battery voltage detection, fuel gauge, battery temperature detection
Real Time Clock	Supported
Antenna Interfaces	Main antenna, Rx-diversity antenna, GNSS antenna, Wi-Fi/BT antenna and FM antenna
Physical Characteristics	Size: (43.0±0.15)mm × (44.0±0.15)mm × (2.85±0.2)mm Package: LCC + LGA Weight: approx. 13.0g
Temperature Range	Operating temperature range: -35°C ~ +65°C [1)] Extended temperature range: -40°C ~ +75°C [2)] Storage temperature range: -40°C ~ +90°C
Firmware Upgrade	Over USB interface
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1)] Within operating temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

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2.3. Functional Diagram

The following figure shows a block diagram of SC600Y/SC600T and illustrates the major functional parts.

- Power management
- Radio frequency
- Baseband
- LPDDR3+eMMC flash
- Peripheral interfaces

  -- USB interface
  -- UART interfaces
  -- (U)SIM interfaces
  -- SD card interface
  -- GPIO interfaces
  -- I2C interfaces
  -- I2S interface
  -- SPI interfaces
  -- ADC interfaces
  -- Vibrator Drive interface
  -- LCM (MIPI) interfaces
  -- TP (touch panel) interfaces
  -- Camera (MIPI) interfaces
  -- Flashlight interfaces
  -- Sensor interfaces
  -- Audio interfaces
  -- Emergency Download interface

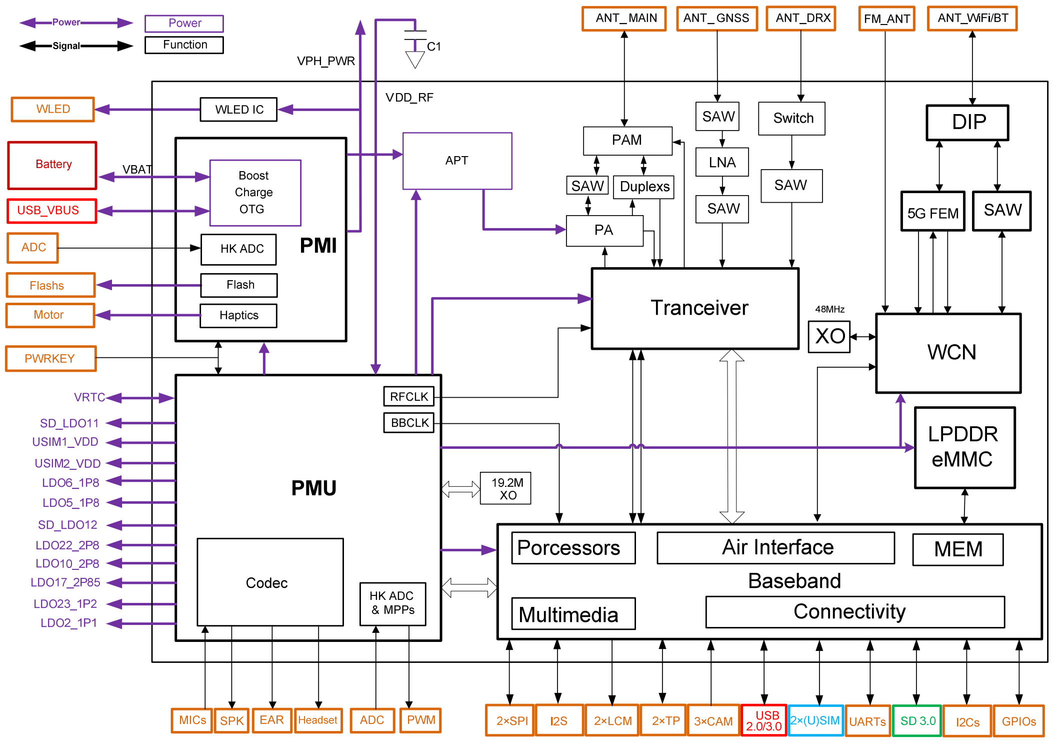

Figure 1: Functional Diagram

2.4. Evaluation Board

In order to help customers develop applications with SC600Y/SC600T conveniently, Quectel supplies the evaluation board, USB to RS232 converter cable, USB Type-C data cable, power adapter, earphone, antenna and other peripherals to control or test the module. For more details, please refer to ***document [1]***.

3 Application Interfaces

3.1. General Description

SC600Y/SC600T is equipped with 323 pins that can be embedded into cellular application platform. The following chapters provide the detailed description of pins/interfaces listed below.

- Power supply
- VRTC interface
- Charging interface
- USB interface
- UART interfaces
- (U)SIM interfaces
- SD card interface
- GPIO interfaces
- I2C interfaces
- I2S interface
- SPI interfaces
- ADC interfaces
- Vibrator drive interface
- LCM interfaces
- TP (touch panel) interfaces
- Camera interfaces
- Flashlight interfaces
- Sensor interfaces
- Audio interfaces
- Emergency download interface

3.2. Pin Assignment

The following figure shows the pin assignment of SC600Y/SC600T module.

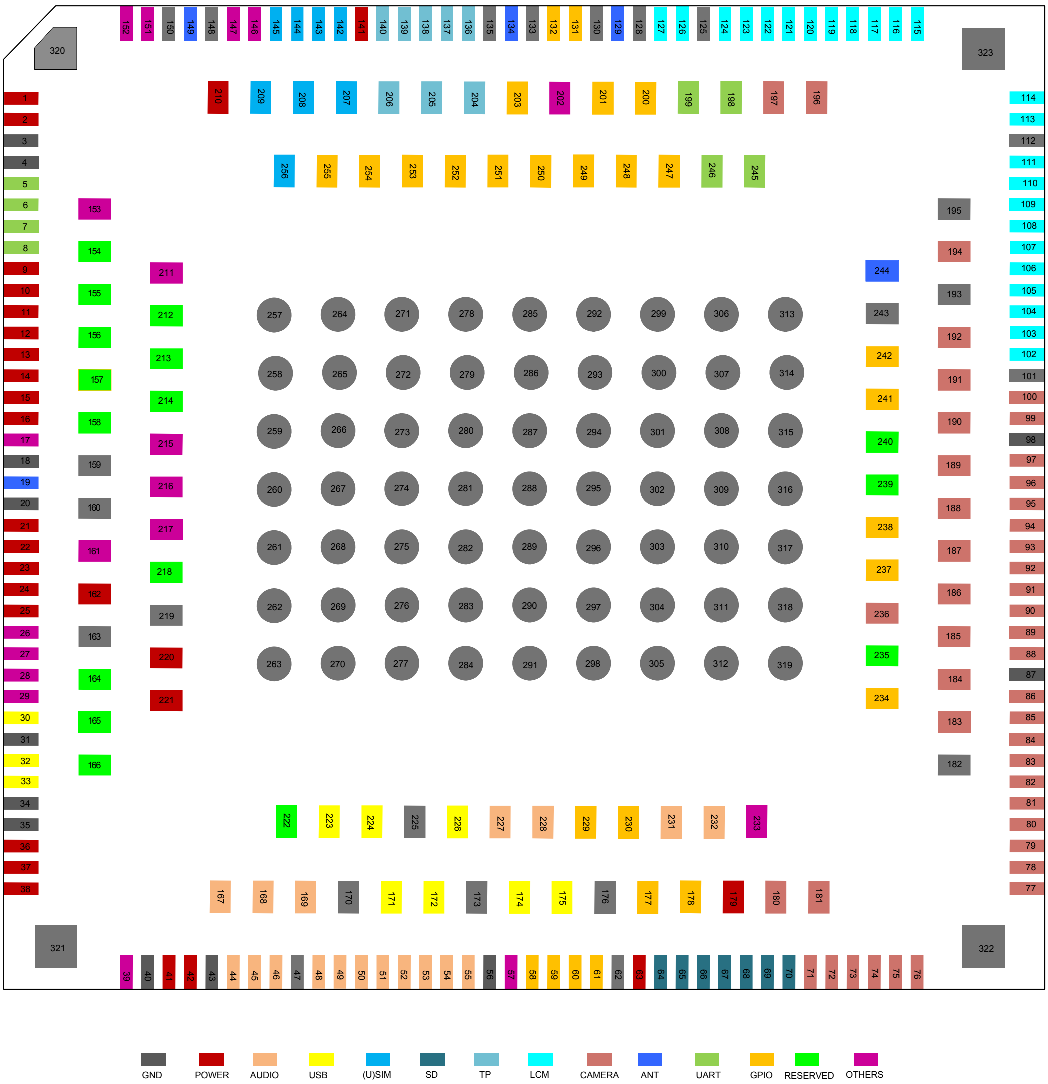

Figure 2: Pin Assignment (Top View)

3.3. Pin Description

Table 6: I/O Parameters Definition

Type	Description
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output
IO	Bidirectional
OD	Open drain
PI	Power input
PO	Power output

The following tables show the SC600Y/SC600T's pin definitions and electrical characteristics.

Table 7: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	36, 37, 38	PI/ PO	Power supply for the module	Vmax=4.4V Vmin=3.55V Vnorm=3.8V	It must be provided with sufficient current up to 3.0A. It is suggested to use a TVS to increase voltage surge withstand capability.
VDD_RF	1, 2		Connect to external bypass capacitors to eliminate voltage fluctuation of RF part.		Do not load externally.
VPH_PWR	220, 221	PO	Power supply for peripherals	Vmax=4.4V Vmin=3.55V	It can provide a maximum continuous

				Vnorm=3.8V	current of 1A approximately. The value of capacitors placed on this pin should not exceed 120uF.
VRTC	16	PI/PO	Power supply for internal RTC circuit	$V_O$max=3.2V V_I=2.0V~3.25V	
LDO5_1P8	9	PO	1.8V output power supply	Vnorm=1.8V $I_O$max=20mA	Power supply for external GPIO's pull up circuits and level shift circuit.
LDO10_2P8	11	PO	2.8V output power supply	Vnorm=2.8V $I_O$max=150mA	Power supply for VDD of sensors and TPs. Add a 1.0uF~4.7uF bypass capacitor if used. If unused, keep this pin open.
LDO6_1P8	10	PO	1.8V output power supply	Vnorm=1.8V $I_O$max=300mA	Power supply for I/O VDD of cameras, LCDs and sensors. Add a 1.0uF~2.2uF bypass capacitor if used. If unused, keep this pin open.
LDO17_2P85	12	PO	2.85V output power supply	Vnorm=2.85V $I_O$max=300mA	Power supply for cameras and LCDs. Add a 1.0uF~4.7uF bypass capacitor if used. If unused, keep this pin open.
LDO23_1P2	15	PO	1.2V output power supply	Vnorm=1.2V $I_O$max=600mA	Power supply for DVDD of front camera. Add a 1.0uF~2.2uF bypass capacitor if used. If unused, keep this pin open.

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
LDO2_1P1	13	PO	1.1V output power supply	Vnorm=1.1V $I_O$max=1200mA	Power supply for DVDD of rear camera. Add a 1.0uF~2.2uF bypass capacitor if used. If unused, keep this pin open.
LDO22_2P8	14	PO	2.8V output power supply	Vnorm=2.8V $I_O$max=150mA	Power supply for AVDD of camera. Add a 1.0uF~4.7uF bypass capacitor if used. If unused, keep this pin open.
GND	3, 4, 18, 20, 31, 34, 35, 40, 43, 47, 56, 62, 87, 98, 101, 112, 125, 128, 130, 133, 135, 148, 150, 159, 163, 170, 173, 176, 182, 193, 195, 219, 225, 243, 257~323		Ground		
Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC_BIAS	167	AO	Microphone bias voltage	V_O=1.6V~2.85V	
MIC1_P	44	AI	Microphone input for channel 1 (+)		
MIC1_N	45	AI	Microphone input for channel 1 (-)		
MIC_GND	168		Microphone reference ground		If unused, connect this pin to the ground.

MIC2_P	46	AI	Microphone input for headset (+)		
MIC3_P	169	AI	Microphone input for channel 2 (+)		
EAR_P	53	AO	Earpiece output (+)		
EAR_N	52	AO	Earpiece output (-)		
SPK_P	55	AO	Speaker output (+)		
SPK_N	54	AO	Speaker output (-)		
HPH_R	51	AO	Headphone right channel output		
HPH_REF	50	AI	Headphone reference ground		It should be connected to main GND.
HPH_L	49	AO	Headphone left channel output		
HS_DET	48	AI	Headset insertion detection		Pulled up internally.
LINE_OUT_P	227	AO	Audio line differential (+)		
LINE_OUT_N	228	AO	Audio line differential (-)		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	41, 42	PI/ PO	Charging power input. Power supply output for OTG device USB/charger insertion detection	Vmax=10V Vmin=4.0V Vnorm=5.0V	
USB_DM	33	AI/ AO	USB 2.0 differential data bus (-)		90Ω differential impedance. USB 2.0 standard compliant.
USB_DP	32	AI/ AO	USB 2.0 differential data bus (+)		
USB_ID	30	AI	USB ID detection		High level by default.
USB_SS_RX_P	171	AI	USB 3.0 differential receive data (+)		90Ω differential impedance. USB 3.0 standard compliant.
USB_SS_RX_M	172	AI	USB 3.0 differential receive data (-)		

USB_SS_TX_P	174	AO	USB 3.0 differential transmit data (+)		
USB_SS_TX_M	175	AO	USB 3.0 differential transmit data (-)		
USBC_CC2	223	AI	USB Type-C control configuration channel 2		
USBC_CC1	224	AI	USB Type-C control configuration channel 1		
USB_SS_SEL	226	DO	USB Type-C switch control		
USB_OPT	217		Type-C/Micro USB select control		If Micro USB is intended to be used, this pin should be connected to ground via a 1KΩ resistor; If Type-C is intended to be used, this pin should be left open.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_DET	145	DI	(U)SIM1 card hot-plug detection	V_{IL}max=0.63V V_{IH}min=1.17V	Active low. Require external pull-up to 1.8V. If unused, keep this pin open. Disabled by default and can be enabled through software configuration.
USIM1_RST	144	DO	(U)SIM1 card reset	V_{OL}max=0.4V V_{OH}min= 0.8 × USIM1_VDD	
USIM1_CLK	143	DO	(U)SIM1 card clock	V_{OL}max=0.4V V_{OH}min= 0.8 × USIM1_VDD	
USIM1_DATA	142	IO	(U)SIM1 card data	V_{IL}max= 0.2 × USIM1_VDD V_{IH}min= 0.7 × USIM1_VDD V_{OL}max=0.4V	

				V_{OH}min= 0.8 × USIM1_VDD	
USIM1_VDD	141	PO	(U)SIM1 card power supply	**1.8V (U)SIM:** Vmax=1.90V Vmin=1.70V **2.95V (U)SIM:** Vmax=3.04V Vmin=2.7V	Either 1.8V or 2.95V (U)SIM card is supported.
USIM2_DET	256	DI	(U)SIM2 card hot-plug detection	V_{IL}max=0.63V V_{IH}min=1.17V	Active low. Require external pull-up to 1.8V. If unused, keep this pin open. Disabled by default and can be enabled through software configuration.
USIM2_RST	207	DO	(U)SIM2 card reset	V_{OL}max=0.4V V_{OH}min= 0.8 × USIM2_VDD	
USIM2_CLK	208	DO	(U)SIM2 card clock	V_{OL}max=0.4V V_{OH}min= 0.8 × USIM2_VDD	
USIM2_DATA	209	IO	(U)SIM2 card data	V_{IL}max= 0.2 × USIM2_VDD V_{IH}min= 0.7 × USIM2_VDD V_{OL}max=0.4V V_{OH}min= 0.8 × USIM2_VDD	
USIM2_VDD	210	PO	(U)SIM2 card power supply	**1.8V (U)SIM:** Vmax=1.90V Vmin=1.70V **2.95V (U)SIM:** Vmax=3.04V Vmin=2.7V	Either 1.8V or 2.95V (U)SIM card is supported.
UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART2_TXD	5	DO	UART2 transmit data. Used for debugging	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep these

			by default		pins open.
UART2_RXD	6	DI	UART2 receive data. Used for debugging by default	V_{IL}max=0.63V V_{IH}min=1.17V	
UART4_TXD	7	DO	UART4 transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	
UART4_RXD	8	DI	UART4 receive data	V_{IL}max=0.63V V_{IH}min=1.17V	
UART5_RXD	198	DI	UART5 receive data	V_{IL}max=0.63V V_{IH}min=1.17V	
UART5_TXD	199	DO	UART5 transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	
UART5_RTS	245	DO	UART5 request to send	V_{OL}max=0.45V V_{OH}min=1.35V	
UART5_CTS	246	DI	UART5 clear to send	V_{IL}max=0.63V V_{IH}min=1.17V	
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_CLK	70	DO	SD card clock	**1.8V SD card:** V_{OL}max=0.45V V_{OH}min=1.4V **2.95V SD card:** V_{OL}max=0.37V V_{OH}min=2.2V	
SD_CMD	69	IO	SD card command	**1.8V SD card:** V_{IL}max=0.58V V_{IH}min=1.27V V_{OL}max=0.45V V_{OH}min=1.4V **2.95V SD card:** V_{IL}max=0.73V V_{IH}min=1.84V V_{OL}max=0.37V V_{OH}min=2.2V	
SD_DATA0	68	IO	SD card data	**1.8V SD card:** V_{IL}max=0.58V V_{IH}min=1.27V	

SD_DATA1	67	IO		V_{OL}max=0.45V V_{OH}min=1.4V	
SD_DATA2	66	IO		**2.95V SD card:** V_{IL}max=0.73V V_{IH}min=1.84V V_{OL}max=0.37V V_{OH}min=2.2V	
SD_DATA3	65	IO			
SD_DET	64	DI	SD card insertion detection	V_{IL}max=0.63V V_{IH}min=1.17V	Active low.
SD_LDO11	63	PO	Power supply for SD card	Vnorm=2.95V $I_O$max=800mA	
SD_LDO12	179	PO	1.8V/2.95V output	Vnorm=1.8V/2.95V $I_O$max=50mA	Power supply for SD card's pull-up circuit.
TP (Touch Panel) Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TP0_RST	138	DO	TP0 reset	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. Active low.
TP0_INT	139	DI	TP0 interrupt	V_{IL}max=0.63V V_{IH}min=1.17V	1.8V power domain.
TP0_I2C_SCL	140	OD	TP0 I2C clock		1.8V power domain.
TP0_I2C_SDA	206	OD	TP0 I2C data		1.8V power domain.
TP1_RST	136	DO	TP1 reset	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. Active low.
TP1_INT	137	DI	TP1 interrupt	V_{IL}max=0.63V V_{IH}min=1.17V	1.8V power domain.
TP1_I2C_SDA	204	OD	TP1 I2C data		1.8V power domain.
TP1_I2C_SCL	205	OD	TP1 I2C clock		1.8V power domain.
LCM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

LCD_BL_A	21	PO	Current output for LCD backlight		
LCD_BL_K1	22	AI	Current sink for LCD backlight		
LCD_BL_K2	23	AI	Current sink for LCD backlight		
LCD_BL_K3	24	AI	Current sink for LCD backlight		
LCD_BL_K4	25	AI	Current sink for LCD backlight		
PMU_MPP4	152	DO	PWM output	V_{OL}max=0.45V V_{OH}min=1.35V	
LCD0_RST	127	DO	LCD0 reset	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. Active low.
LCD0_TE	126	DI	LCD0 tearing effect	V_{IL}max=0.63V V_{IH}min=1.17V	1.8V power domain.
LCD1_RST	113	DO	LCD1 reset	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. Active low.
LCD1_TE	114	DI	LCD1 tearing effect	V_{IL}max=0.63V V_{IH}min=1.17V	1.8V power domain.
DSI0_CLK_N	116	AO	LCD0 MIPI clock signal (-)		
DSI0_CLK_P	115	AO	LCD0 MIPI clock signal (+)		
DSI0_LN0_N	118	AO	LCD0 MIPI lane 0 data signal (-)		
DSI0_LN0_P	117	AO	LCD0 MIPI lane 0 data signal (+)		
DSI0_LN1_N	120	AO	LCD0 MIPI lane 1 data signal (-)		
DSI0_LN1_P	119	AO	LCD0 MIPI lane 1 data signal (+)		
DSI0_LN2_N	122	AO	LCD0 MIPI lane 2 data signal (-)		
DSI0_LN2_P	121	AO	LCD0 MIPI lane 2 data signal (+)		
DSI0_LN3_N	124	AO	LCD0 MIPI lane 3 data signal (-)		

DSI0_LN3_P	123	AO	LCD0 MIPI lane 3 data signal (+)		
DSI1_CLK_N	103	AO	LCD1 MIPI clock signal (-)		
DSI1_CLK_P	102	AO	LCD1 MIPI clock signal (+)		
DSI1_LN0_N	105	AO	LCD1 MIPI lane 0 data signal (-)		
DSI1_LN0_P	104	AO	LCD1 MIPI lane 0 data signal (+)		
DSI1_LN1_N	107	AO	LCD1 MIPI lane 1 data signal (-)		
DSI1_LN1_P	106	AO	LCD1 MIPI lane 1 data signal (+)		
DSI1_LN2_N	109	AO	LCD1 MIPI lane 2 data signal (-)		
DSI1_LN2_P	108	AO	LCD1 MIPI lane 2 data signal (+)		
DSI1_LN3_N	111	AO	LCD1 MIPI lane 3 data signal (-)		
DSI1_LN3_P	110	AO	LCD1 MIPI lane 3 data signal (+)		
Camera Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CSI0_CLK_N	89	AO	MIPI clock signal of rear camera (-)		
CSI0_CLK_P	88	AO	MIPI clock signal of rear camera (+)		
CSI0_LN0_N	91	AI	MIPI lane 0 data signal of rear camera (-)		
CSI0_LN0_P	90	AI	MIPI lane 0 data signal of rear camera (+)		
CSI0_LN1_N	93	AI	MIPI lane 1 data signal of rear camera (-)		
CSI0_LN1_P	92	AI	MIPI lane 1 data signal of rear camera (+)		
CSI0_LN2_N	95	AI	MIPI lane 2 data signal of rear camera (-)		
CSI0_LN2_P	94	AI	MIPI lane 2 data signal of rear camera (+)		

CSI0_LN3_N	97	AI	MIPI lane 3 data signal of rear camera (-)	
CSI0_LN3_P	96	AI	MIPI lane 3 data signal of rear camera (+)	
CSI1_CLK_N	184	AO	MIPI clock signal of depth camera (-)	
CSI1_CLK_P	183	AO	MIPI clock signal of depth camera (+)	
CSI1_LN0_N	186	AI	MIPI lane 0 data signal of depth camera (-)	
CSI1_LN0_P	185	AI	MIPI lane 0 data signal of depth camera (+)	
CSI1_LN1_N	188	AI	MIPI lane 1 data signal of depth camera (-)	
CSI1_LN1_P	187	AI	MIPI lane 1 data signal of depth camera (+)	
CSI1_LN2_N	190	AI	MIPI lane 2 data signal of depth camera (-)	Can be multiplexed into differential data of the fourth camera (-).
CSI1_LN2_P	189	AI	MIPI lane 2 data signal of depth camera (+)	Can be multiplexed into differential data of the fourth camera (+).
CSI1_LN3_N	192	AI	MIPI lane 3 data signal of depth camera (-)	Can be multiplexed into differential clock of the fourth camera (-).
CSI1_LN3_P	191	AI	MIPI lane 3 data signal of depth camera (+)	Can be multiplexed into differential clock of the fourth camera (+).
CSI2_CLK_N	78	AO	MIPI clock signal of front camera (-)	
CSI2_CLK_P	77	AO	MIPI clock signal of front camera (+)	
CSI2_LN0_N	80	AI	MIPI lane 0 data signal of front camera (-)	
CSI2_LN0_P	79	AI	MIPI lane 0 data signal of front camera (+)	
CSI2_LN1_N	82	AI	MIPI lane 1 data signal of front camera (-)	
CSI2_LN1_P	81	AI	MIPI lane 1 data signal of front camera (+)	
CSI2_LN2_N	84	AI	MIPI lane 2 data signal of front camera (-)	

CSI2_LN2_P	83	AI	MIPI lane 2 data signal of front camera (+)		
CSI2_LN3_N	86	AI	MIPI lane 3 data signal of front camera (-)		
CSI2_LN3_P	85	AI	MIPI lane 3 data signal of front camera (+)		
MCAM_MCLK	99	DO	Master clock of rear camera	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
SCAM_MCLK	100	DO	Master clock of front camera	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
MCAM_RST	74	DO	Reset of rear camera	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
MCAM_PWDN	73	DO	Power down of rear camera	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
SCAM_RST	72	DO	Reset of front camera	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
SCAM_PWDN	71	DO	Power down of front camera	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
CAM_I2C_SCL	75	OD	I2C clock for camera		1.8V power domain.
CAM_I2C_SDA	76	OD	I2C data for camera		1.8V power domain.
DCAM_MCLK	194	DO	Master clock of depth camera	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
CAM4_MCLK	236	DO	Master clock of fourth camera	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
DCAM_RST	180	DO	Reset of depth camera	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
DCAM_PWDN	181	DO	Power down of depth camera	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain.
DCAM_I2C_SDA	197	OD	I2C data for depth camera		1.8V power domain.
DCAM_I2C_SCL	196	OD	I2C clock for depth camera		1.8V power domain.
Keypad Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

PWRKEY	39	DI	Turn on/off the module	V_{IL}max=0.63V V_{IH}min=1.17V	Pull-up to 1.8V internally. Active low.
VOL_UP	146	DI	Volume up	V_{IL}max=0.63V V_{IH}min=1.17V	If unused, keep this pin open.
VOL_ DOWN	147	DI	Volume down	V_{IL}max=0.63V V_{IH}min=1.17V	If unused, keep this pin open.
SENSOR_I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SENSOR_I2C_ SCL	131	OD	I2C clock for external sensors		1.8V power domain.
SENSOR_I2C_ SDA	132	OD	I2C data for external sensors		1.8V power domain.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PMI_ADC	153	AI	General purpose ADC interface		Maximum input voltage: 1.5V.
PMU_MPP2	151	AI	General purpose ADC interface		Maximum input voltage: 1.7V.
Charging Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BAT_PLUS	27	AI	Differential input of battery voltage detection (+)		Must be connected.
BAT_MINUS	28	AI	Differential input of battery voltage detection (-)		Must be connected.
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	19	AI/ AO	Main antenna interface		50Ω impedance.
ANT_DRX	149	AI	Diversity antenna interface		

ANT_GNSS	134	AI	GNSS antenna interface		
ANT_WIFI/BT	129	AI/ AO	Wi-Fi/BT antenna interface		
ANT_FM	244	AI	FM antenna interface		
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_0	248	IO	General-purpose input/output	$V_{IL}max=0.63V$ $V_{IH}min=1.17V$ $V_{OL}max=0.45V$ $V_{OH}min=1.4V$	
GPIO_1	247	IO	General-purpose input/output		
GPIO_2	201	IO	General-purpose input/output		
GPIO_3	200	IO	General-purpose input/output		
GPIO_33	238	IO	General-purpose input/output		
GPIO_36	237	IO	General-purpose input/output		
GPIO_42	252	IO	General-purpose input/output		
GPIO_43	253	IO	General-purpose input/output		
GPIO_44	254	IO	General-purpose input/output		
GPIO_45	255	IO	General-purpose input/output		
GPIO_66	234	IO	General-purpose input/output		
GPIO_89	232	IO	General-purpose input/output		
GPIO_90	231	IO	General-purpose input/output		
GPIO_96	230	IO	General-purpose input/output		
GPIO_97	229	IO	General-purpose input/output		
GPIO_98	177	IO	General-purpose input/output		

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
GPIO_99	178	IO	General-purpose input/output		
SPI Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CS	58	DO	SPI chip select		Can be multiplexed into UART6_CTS.
SPI_CLK	59	DO	SPI clock		Can be multiplexed into UART6_RTS.
SPI_MOSI	60	DO	SPI master-out slave-in		Can be multiplexed into UART6_TXD.
SPI_MISO	61	DI	SPI master-in salve-out		Can be multiplexed into UART6_RXD.
FP_SPI_CS	203	DO	SPI chip select		Can be multiplexed into I2S_WS.
FP_SPI_CLK	250	DO	SPI clock		Can be multiplexed into I2S_SCK.
FP_SPI_MOSI	249	DO	SPI master-out slave-in		Can be multiplexed into I2S_D0.
FP_SPI_MISO	251	DI	SPI master-in salve-out		Can be multiplexed into I2S_D1.
Vibrator Drive Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VIB_GND	160		Vibrator ground (-)		Connected to the negative terminal of vibrator.
VIB_DRV	161	PO	Vibrator drive (+)		Connected to the positive terminal of vibrator.
Flashlight Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
FLASH_LED1	26	AO	Flash/torch current driver output		Support flash and torch modes.
FLASH_LED2	162	AO	Flash/torch current driver output		
Emergency Download Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

USB_BOOT	57	DI	Force the module enter emergency download mode		Pulled up to LDO5_1P8 during power-up will force the module to enter emergency download mode.
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BAT_ID	17	AI	Battery type detection		If unused, keep this pin open.
BAT_THERM	29	AI	Battery temperature measurement		Internally pulled up. Externally connected to GND via a 47K NTC resistor.
GNSS_LNA_EN	202	DO	LNA enable control		For test purpose only. If unused, keep this pin open.
GRFC_5	242	IO	Generic RF control 1		Only used for RF tuner control.
GRFC_7	241	IO	Generic RF control 2		
S1A	215		S1A and S1B are connected in the module		
S1B	216				
S2A	211		S2A and S2B are connected in the module		
S2B	233				
Reserved Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	154, 155, 156, 157, 158, 164, 165, 166, 212, 213, 214, 218, 222, 235, 239, 240,		Reserved		Keep these pins open.

3.4. Power Supply

3.4.1. Power Supply Pins

SC600Y/SC600T provides 3 VBAT pins and 2 VPH_PWR pins. VBAT pins are dedicated for connection with an external power supply. VPH_PWR pins can supply power for peripherals, and it can provide a maximum continuous current of 1A approximately. The value of capacitors placed on this pin should not exceed 120uF.

3.4.2. Decrease Voltage Drop

The power supply range of the module is from 3.55V to 4.4V, and the recommended value is 3.8V. The power supply performance, such as load capacity, voltage ripple, etc. directly influences the module's performance and stability. Under ultimate conditions, the module may have a transient peak current up to 3A. If the power supply capability is not sufficient, there will be voltage drops, and if the voltage drops below 3.1V, the module will be powered off automatically. Therefore, please make sure the input voltage will never drop below 3.1V.

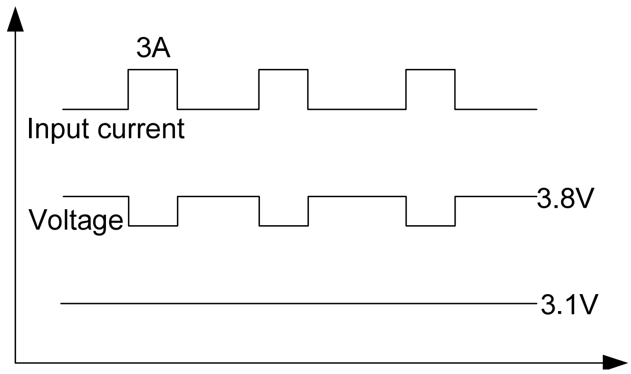

Figure 3: Voltage Drop Sample

To decrease voltage drop, a bypass capacitor of about 100µF with low ESR (ESR=0.7Ω) should be used in VBAT pins, and a multi-layer ceramic chip capacitor (MLCC) array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100nF, 33pF, 10pF) for composing the MLCC array, and place these capacitors close to VBAT/VDD_RF/VPH_PWR pins. The width of VBAT trace should be no less than 3mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to get a stable power source, it is suggested to use a 0.5W TVS and place it as close to the VBAT pins as possible to increase voltage surge withstand capability. The following figure shows the structure of the power supply.

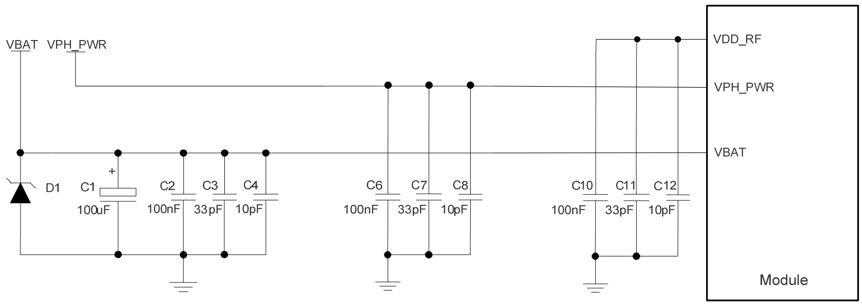

Figure 4: Star Structure of Power Supply

3.4.3. Reference Design for Power Supply

The power design for the module is very important, as the performance of module largely depends on the power source. The power supply of SC600Y/SC600T should be able to provide sufficient current up to 3A at least. By default, it is recommended to use a battery to supply power for SC600Y/SC600T. But if battery is not intended to be used, it is recommended to use a regulator for SC600Y/SC600T. If the voltage difference between the input and output is not too high, it is suggested to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5V input power source which adopts an LDO (MIC29502WU) from MICROCHIP. The typical output voltage is 3.8V and the maximum rated current is 5.0A.

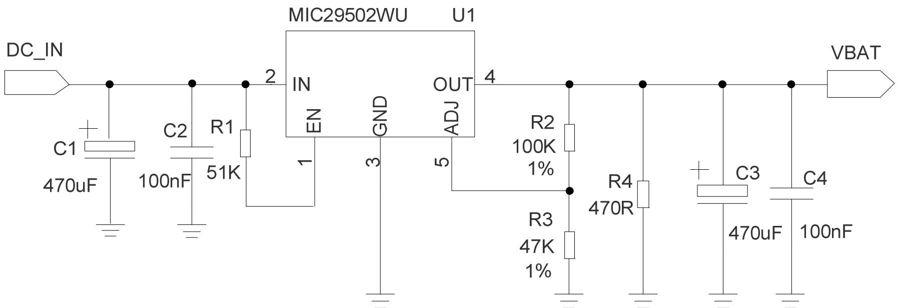

Figure 5: Reference Circuit of Power Supply

NOTES

1. It is recommended to switch off the power supply for module in abnormal state, and then switch on the power to restart the module.
2. The module supports battery charging function by default. If the above power supply design is adopted, please make sure the charging function is disabled by software, or connect VBAT to Schottky diode in series to avoid the reverse current to the power supply chip.
3. When the battery power is reduced to 0%, the system will trigger automatic shutdown, so the design of power supply should be consistent with the configuration of fuel gauge driver.

3.5. Turn on and off Timing

3.5.1. Turn on Module Using the PWRKEY

The module can be turned on by driving PWRKEY pin to a low level for at least 1.6s. PWRKEY pin is pulled to 1.8V internally. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

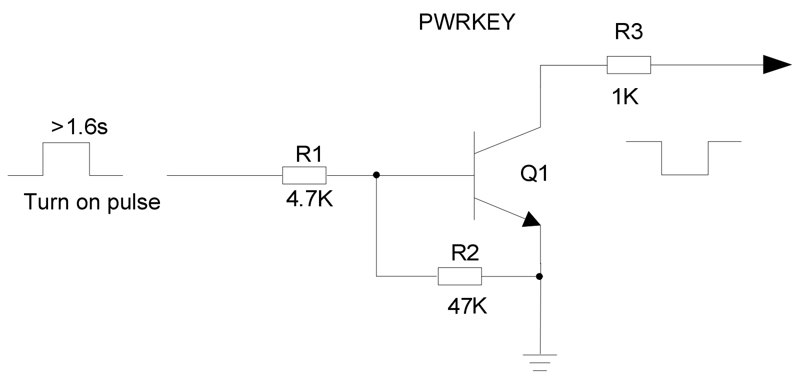

Figure 6: Turn on the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. A TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

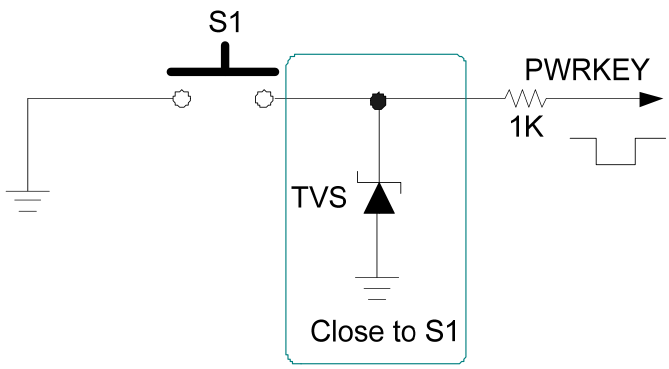

Figure 7: Turn on the Module Using Keystroke

The timing of turning on is illustrated in the following figure.

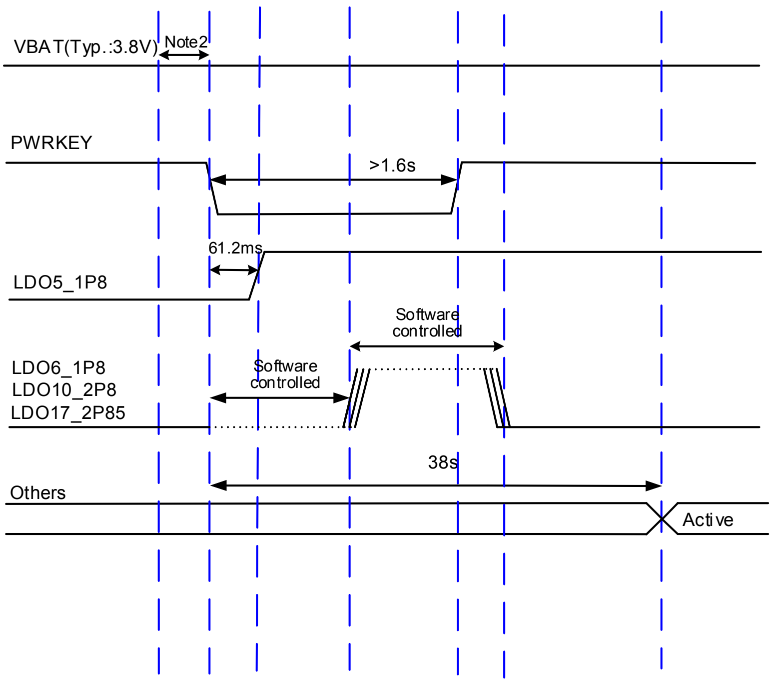

Figure 8: Timing of Turning on Module

NOTES

1. The turn-on timing might be different from the above figure when the module powers on for the first time.
2. Make sure that VBAT is stable before pulling down PWRKEY pin. The recommended time between them is no less than 30ms. PWRKEY cannot be pulled down all the time.

3.5.2. Turn off Module

Pull down PWRKEY for at least 1s, and then choose to turn off the module when a prompt window comes up.

Another way to turn off the module is to drive PWRKEY to a low level for at least 8s. The module will execute forced shutdown. The forced power-down timing is illustrated in the following figure.

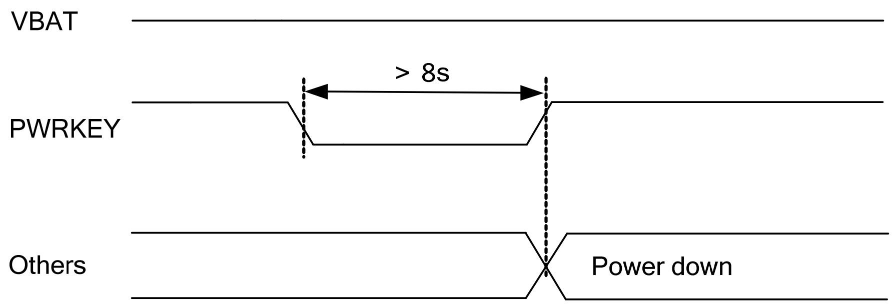

Figure 9: Timing of Turning off Module

3.6. VRTC Interface

The RTC (Real Time Clock) can be powered by an external power source through VRTC when the module is powered down and there is no power supply for the VBAT. The external power source can be rechargeable battery (such as coil cells) according to application demands. The following reference circuit design when an external battery is utilized for powering RTC.

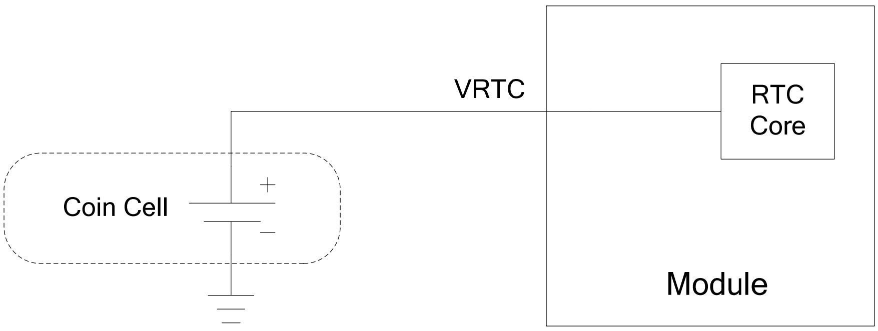

Figure 10: RTC Powered by Coin Cell

If RTC is ineffective, it can be synchronized through network after the module is powered on.

- 2.0V~3.25V input voltage range and 3.0V typical value for VRTC, when VBAT is disconnected.
- When powered by VBAT, the RTC error is 50ppm. When powered by VRTC, the RTC error is about 200ppm.
- If the rechargeable battery is used, the ESR of battery should be less than 2KΩ, and it is recommended to use the MS621FE FL11E of SEIKO.

3.7. Power Output

SC600Y/SC600T supports output of regulated voltages for peripheral circuits. During application, it is recommended to use parallel capacitors (33pF and 10pF) in the circuit to suppress high frequency noise.

Table 8: Power Description

Pin Name	Default Voltage (V)	Drive Current (mA)	Idle
LDO5_1P8	1.8	20	Keep
LDO6_1P8	1.8	300	/
LDO10_2P8	2.8	150	/
LDO17_2P85	2.85	300	/
LDO2_1P1	1.1	1200	/
LDO22_2P8	2.8	150	/
LDO23_1P2	1.2	600	/
SD_LDO12	1.8/2.95	50	/
SD_LDO11	2.95	800	/
USIM1_VDD	1.8/2.95	50	/
USIM2_VDD	1.8/2.95	50	/
VPH_PWR	Equal to VBAT voltage	1000	Keep

3.8. Battery Charge and Management

SC600Y/SC600T supports a fully programmable switch-mode Li-ion battery charge function. It can charge single-cell Li-ion and Li-polymer batteries. The battery charger of SC600Y/SC600T supports trickle charging, pre-charge, constant current charging and constant voltage charging modes, which optimize the charging procedure for Li-ion and Li-polymer batteries.

- **Trickle charging:** When the battery voltage is below 2.1V, a 75mA trickle charging current is applied to the battery.
- **Pre-charge:** When the battery voltage is charged up and exceeds 2.1V (the maximum pre-charge voltage is 2.3V~3.0V programmable, 3.0V by default), the system will enter into pre-charge mode. The charging current is 250mA (100mA~450mA programmable, 250mA by default).
- **Constant current mode (CC mode):** When the battery voltage is increased to between the maximum pre-charge voltage and 4.35V (3.6V~4.35V programmable, 4.35V by default), the system will switch to CC mode. The charging current is programmable from 300mA~3000mA. The default charging current is 500mA for USB charging and 2A for adapter.
- **Constant voltage mode (CV mode):** When the battery voltage reaches the final value 4.35V, the system will switch to CV mode and the charging current will decrease gradually. When the charging current reduces to about 100mA, the charging is completed.

Table 9: Pin Definition of Charging Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	41, 42	PI/PO	Charging power input Power supply output for OTG device USB/charger insertion detection	Vmax=10V Vmin=4.0V Vnorm=5.0V
VBAT	36, 37, 38	PI/PO	Power supply for the module	Vmax=4.4V Vmin=3.55V Vnorm=3.8V
BAT_ID	17	AI	Battery type detection	If unused, keep this pin open.
BAT_PLUS	27	AI	Differential input of battery voltage detection (+)	Must be connected.
BAT_MINUS	28	AI	Differential input of battery voltage detection (-)	Must be connected.
BAT_THERM	29	AI	Battery temperature measurement	Internally pulled up. Externally connected to GND via a 47KΩ NTC resistor.

SC600Y/SC600T supports battery temperature detection in the condition that the battery integrates a thermistor (47KΩ 1% NTC thermistor with B-constant of 4050KΩ by default; SDNT1608X473F4050FTF of SUNLORD is recommended) and the thermistor is connected to BAT_THERM pin. If BAT_THERM pin is not connected, there will be malfunctions such as boot error, battery charging failure, battery level display error, etc.

A reference design for battery charging circuit is shown below.

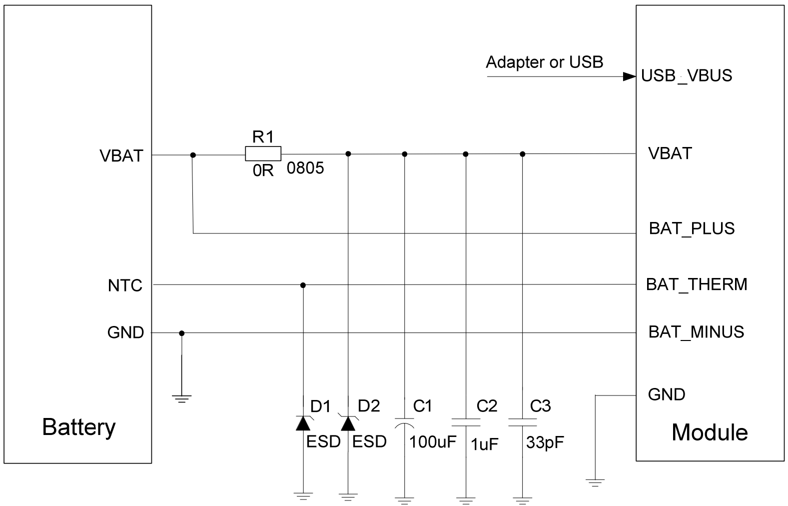

Figure 11: Reference Design for Battery Charging Circuit

SC600Y/SC600T offers a fuel gauge algorithm which is able to accurately estimate the battery's state by current and voltage monitor techniques. Using precise measurements of battery voltage, current, and temperature, the fuel gauge provides a dependable state of charge estimate throughout the entire life of the battery and across a broad range of operating conditions. It effectively protects the battery from over-discharging, and also allows users to estimate the battery life based on the battery level so as to timely save important data before completely power-down.

Mobile devices such as mobile phone and handheld POS systems are powered by batteries. When different batteries are utilized, the charging and discharging curve has to be modified correspondingly so as to achieve the best effect.

If thermistor is not available in the battery, or adapter is utilized for powering the module, then there is only a need for VBAT and GND connection. In this case, the system may be unable to detect the battery, which will cause power-on failure. In order to avoid this, BAT_THERM should be connected to GND with a 47KΩ resistor. BAT_PLUS and BAT_MINUS must be connected, otherwise there may be abnormalities in use of the module. Among them, BAT_PLUS and BAT_MINUS are used for battery level detection, and they should be routed as differential pair to ensure accuracy.

3.9. USB Interface

SC600Y/SC600T provides one USB 3.0/2.0 compliant integrated Universal Serial Bus (USB) interface, which supports super speed (5Gbps) on USB 3.0, high speed (480Mbps) on USB 2.0, full speed (12Mbps) modes as well as USB OTG function. This USB interface is used for AT command communication, data transmission, software debugging and firmware upgrade.

The following table shows the pin definition of USB interface.

Table 10: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	41, 42	PI/PO	Charging power input Power supply output for OTG device USB/charger insertion detection	Vmax=10V Vmin=4.0V Vnorm=5.0V
USB_DM	33	AI/AO	USB 2.0 USB differential data (-)	90Ω differential impedance.
USB_DP	32	AI/AO	USB 2.0 USB differential data (+)	
USB_ID	30	AI	USB ID detection	High level by default.
USB_SS_RX_P	171	AI	USB 3.0 differential receive data (+)	90Ω differential impedance.
USB_SS_RX_M	172	AI	USB 3.0 differential receive data (-)	
USB_SS_TX_P	174	AO	USB 3.0 differential transmit data (+)	
USB_SS_TX_M	175	AO	USB 3.0 differential transmit data (-)	
USBC_CC2	223	AI	USB Type-C control configuration channel 2	
USBC_CC1	224	AI	USB Type-C control configuration channel 1	
USB_SS_SEL	226	DO	USB Type-C switch control	
USB_OPT	217		Type-C/ Micro USB select control	If Micro USB is intended to be used, this pin should be connected to ground via a 1KΩ resistor; If Type-C is intended to be used, this pin should be left open.

USB_VBUS can be powered by a USB power or an adapter. It is used for USB connection detection and power supply input for battery charging. Its input voltage ranges from 4.0V to 10.0V, and the typical value is 5.0V. SC600Y/SC600T supports charging management for a single cell Li-ion battery, but varied charging parameters should be set for batteries with varied models or capacities. The maximum charging current is up to 3.0A.

SC600Y/SC600T supports USB On-The-Go (OTG) function. USB_ID pin is used to detect whether the OTG device is attached. If USB_ID is kept open (high level by default), the module will be in USB device mode; if USB_ID is connected to ground, the module will be in host mode and the USB_VBUS is used to supply power for peripherals with maximum output of 5V/1A.
The use of Type-C and Micro USB is up to the design of USB_OPT. If Micro USB is intended to be used, USB_OPT should be connected to ground via a 1KΩ resistor, and if Type-C is intended to be used, USB_OPT should be left open.

The following is a reference design for Micro USB interface:

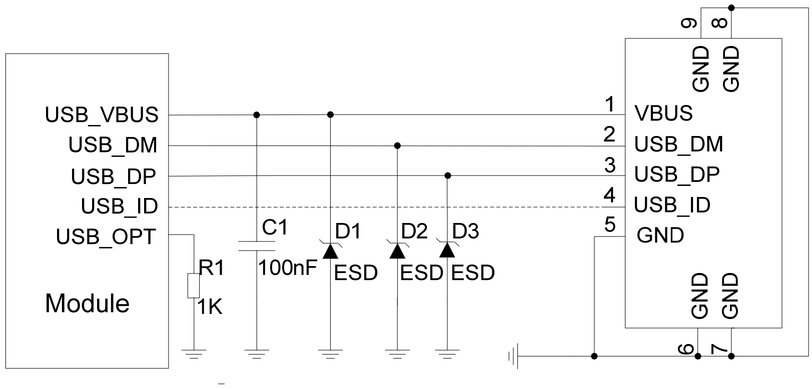

Figure 12: Micro USB Interface Reference Design

The following is a reference design for USB Type-C interface:

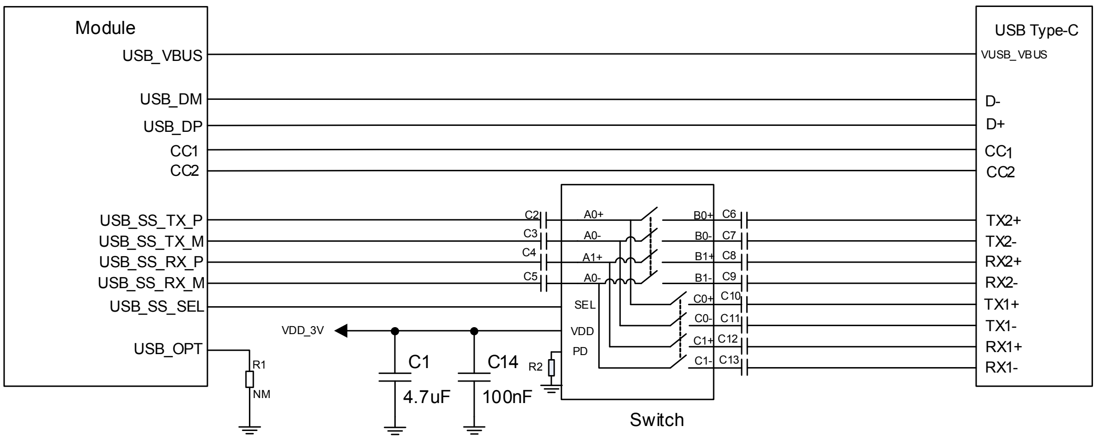

Figure 13: USB Type-C Interface Reference Design

In order to ensure USB performance, please follow the following principles while designing USB interface.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90Ω.
- Pay attention to the influence of junction capacitance of ESD protection devices on USB data lines. Typically, the capacitance value should be less than 2pF for USB 2.0 and less than 0.5pF for USB 3.0.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Keep the ESD protection devices as close as possible to the USB connector.
- Make sure the trace length difference between USB 2.0 DM/DP differential pair and that between USB 3.0 RX/TX differential pairs both do not exceed 0.7mm.

Table 11: USB Trace Length Inside the Module

<table>
<tr><th>Pin No.</th><th>Signal</th><th>Length (mm)</th><th>Length Difference (DP-DM)</th></tr>
<tr><td>33</td><td>USB_DM</td><td>39.52</td><td rowspan="2">-0.45</td></tr>
<tr><td>32</td><td>USB_DP</td><td>39.07</td></tr>
<tr><td>171</td><td>USB_SS_RX_P</td><td>28.55</td><td>0.32</td></tr>
</table>

172	USB_SS_RX_M	28.23	
174	USB_SS_TX_P	19.58	0.23
175	USB_SS_TX_M	19.35	

3.10. UART Interfaces

The module provides the following four UART interfaces:

- **UART5:** 4-wire UART interface, hardware flow control supported.
- **UART6:** 4-wire UART interface, hardware flow control supported, multiplexed from SPI interface.
- **UART2:** 2-wire UART interface, used for debugging.
- **UART4:** 2-wire UART interface.

The following table shows the pin definition of UART interfaces.

Table 12: Pin Definition of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
UART2_TXD	5	DO	UART2 transmit data. Used for debugging by default	1.8V power domain. If unused, keep these pins open.
UART2_RXD	6	DI	UART2 receive data. Used for debugging by default	
UART4_TXD	7	DO	UART4 transmit data	
UART4_RXD	8	DI	UART4 receive data	
UART5_RXD	198	DI	UART5 receive data	
UART5_TXD	199	DO	UART5 transmit data	
UART5_CTS	246	DI	UART5 clear to send	
UART5_RTS	245	DO	UART5 request to send	
SPI_MISO	61	DI	UART6 receive data	SPI interface pin by default. Can be multiplexed into UART6_RXD.
SPI_MOSI	60	DO	UART6 transmit data	SPI interface pin by default.

				Can be multiplexed into UART6_TXD.
SPI_CS	58	DI	UART6 clear to send	SPI interface pin by default. Can be multiplexed into UART6_CTS.
SPI_CLK	59	DO	UART6 request to send	SPI interface pin by default. Can be multiplexed into UART6_RTS.

UART5 is a 4-wire UART interface with 1.8V power domain. A level translator chip should be used if customers' application is equipped with a 3.3V UART interface. A level translator chip TXS0104EPWR provided by Texas Instruments is recommended.

The following figure shows a reference design.

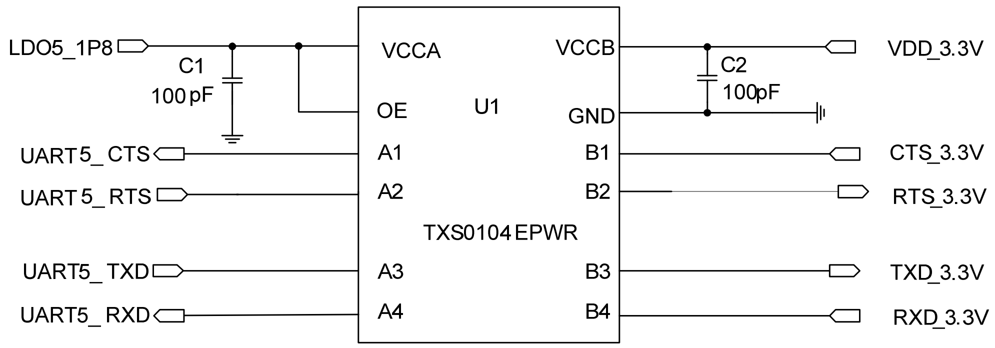

Figure 14: Reference Circuit with Level Translator Chip (for UART5)

The following figure is an example of connection between SC600Y/SC600T and PC. A voltage level translator and a RS-232 level translator chip are recommended to be added between the module and PC, as shown below:

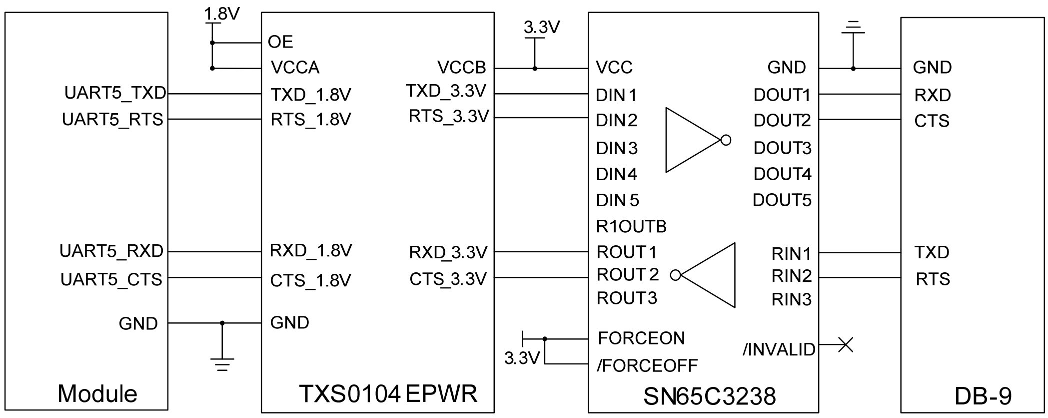

Figure 15: RS232 Level Match Circuit (for UART5)

NOTE

UART2, UART4 and UART6 are similar to UART5. Please refer to UART5 reference circuit design for that of the UART2, UART4 and UART6.

3.11. (U)SIM Interfaces

SC600Y/SC600T provides two (U)SIM interfaces which both meet ETSI and IMT-2000 requirements. Dual SIM Dual Standby is supported by default. Both 1.8V and 2.95V (U)SIM cards are supported, and the (U)SIM interfaces are powered by the dedicated low dropout regulators in SC600Y/SC600T module.

Table 13: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_DET	145	DI	(U)SIM1 card hot-plug detection	Active Low. Require external pull-up to 1.8V. If unused, keep this pin open. Disabled by default, and can be enabled through software configuration.

USIM1_RST	144	DO	(U)SIM1 card reset	
USIM1_CLK	143	DO	(U)SIM1 card clock	
USIM1_DATA	142	IO	(U)SIM1 card data	Pull up to USIM1_VDD with a 10KΩ resistor.
USIM1_VDD	141	PO	(U)SIM1 card power supply	Either 1.8V or 2.95V (U)SIM card is supported.
USIM2_DET	256	DI	(U)SIM2 card hot-plug detection	Active low. Require external pull-up to 1.8V. If unused, keep this pin open. Disabled by default and can be enabled through software configuration.
USIM2_RST	207	DO	(U)SIM2 card reset signal	
USIM2_CLK	208	DO	(U)SIM2 card clock signal	
USIM2_DATA	209	IO	(U)SIM2 card data signal	Pull up to USIM2_VDD with a 10KΩ resistor.
USIM2_VDD	210	PO	(U)SIM2 card power supply	Either 1.8V or 2.95V (U)SIM card is supported.

SC600Y/SC600T supports (U)SIM card hot-plug via the USIM_DET pin, which is disabled by default and can be enabled through software configuration. A reference circuit for (U)SIM interface with an 8-pin (U)SIM card connector is shown as below.

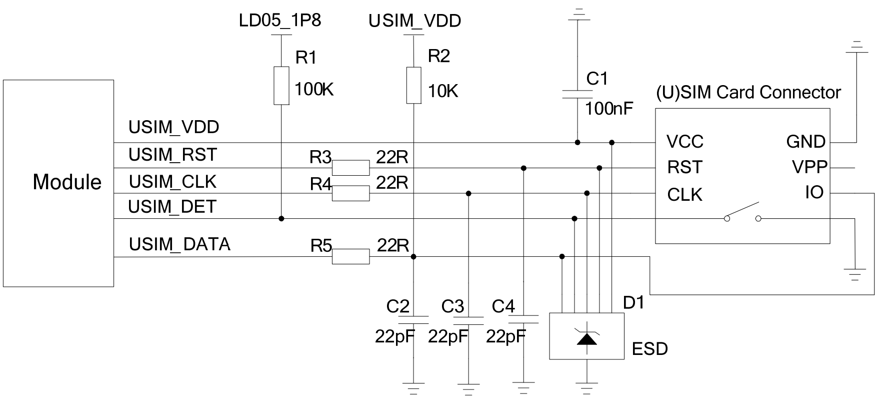

Figure 16: Reference Circuit for (U)SIM Interface with an 8-pin (U)SIM Card Connector

If there is no need to use USIM_DET, please keep it open. The following is a reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector.

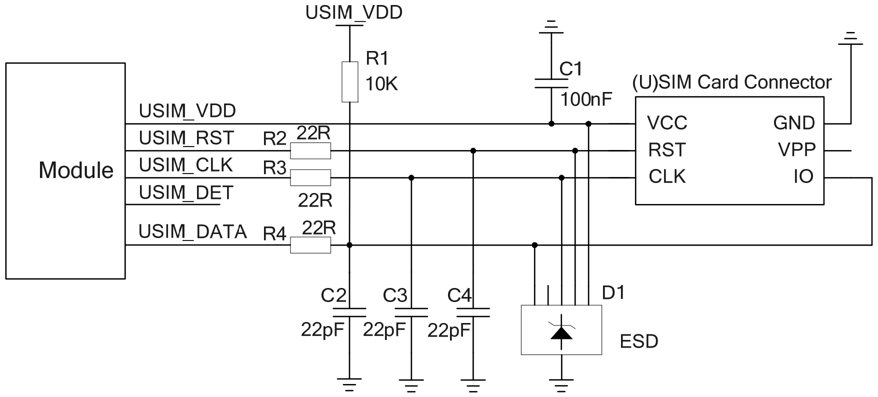

Figure 17: Reference Circuit for (U)SIM Interface with a 6-pin (U)SIM Card Connector

In order to ensure good performance and avoid damage of (U)SIM cards, please follow the criteria below in (U)SIM circuit design:

- Keep placement of (U)SIM card connector as close to the module as possible. Keep the trace length of (U)SIM card signals as less than 200mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- A filter capacitor shall be reserved for USIM_VDD, and its maximum capacitance should not exceed 1uF. The capacitor should be placed near to (U)SIM card.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with ground. USIM_RST also needs ground protection.
- In order to offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 50pF. The 22Ω resistors should be added in series between the module and (U)SIM card so as to suppress EMI spurious transmission and enhance ESD protection. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The 22pF capacitors should be added in parallel on USIM_DATA, USIM_CLK and USIM_RST signal lines so as to filter RF interference, and they should be placed as close to the (U)SIM card connector as possible.

3.12. SD Card Interface

SC600Y/SC600T supports SD 3.0 specifications. The pin definition of the SD card interface is shown below.

Table 14: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_LDO11	63	PO	Power supply for SD card	Vnorm=2.95V $I_O$max=800mA
SD_LDO12	179	PO	Power supply for SD card's pull-up circuit	1.8V/2.95V output.
SD_CLK	70	DO	SD card clock	Control characteristic impedance as 50Ω.
SD_CMD	69	IO	SD card command	
SD_DATA0	68	IO	SD card data	
SD_DATA1	67	IO		
SD_DATA2	66	IO		
SD_DATA3	65	IO		
SD_DET	64	DI	SD card insertion detection	Active low.

A reference circuit for SD card interface is shown as below.

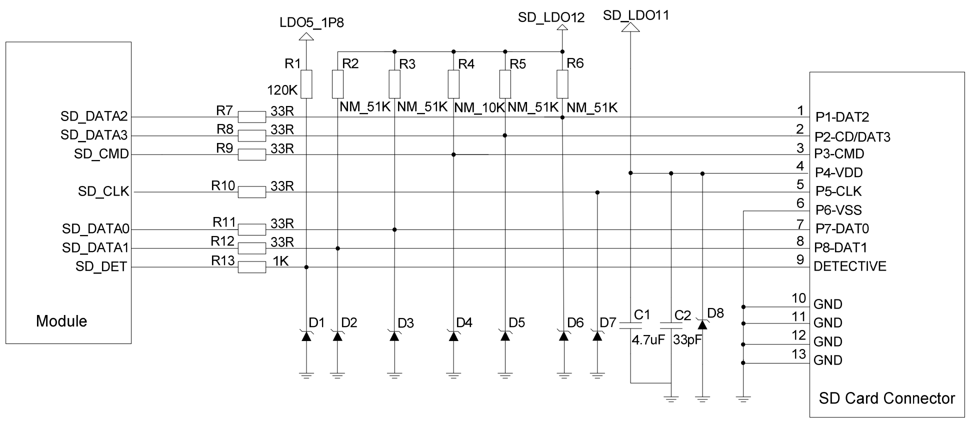

Figure 18: Reference Circuit for SD Card Interface

SD_LDO11 is a peripheral driver power supply for SD card. The maximum drive current is approximate 800mA. Because of the high drive current, it is recommended that the trace width is 0.5mm or above. In order to ensure the stability of drive power, a 4.7uF and a 33pF capacitor should be added in parallel near the SD card connector.
CMD, CLK, DATA0, DATA1, DATA2 and DATA3 are all high speed signal lines. In PCB design, please control the characteristic impedance of them to 50Ω, and do not cross them with other traces. It is recommended to route the trace on the inner layer of PCB, and keep the same trace length for CLK, CMD, DATA0, DATA1, DATA2 and DATA3. CLK should be encircled by ground traces separately.

Layout guidelines:

- Control impedance to 50Ω±10%, and DATA0, DATA1, DATA2 and DATA3 should be encircled by ground traces.
- The total trace length difference between CLK and other signal line traces should not exceed 1mm.

Table 15: SD Card Signal Trace Length Inside the Module

Pin No.	Signal	Length (mm)	Comment
70	SD_CLK	32.11	
69	SD_CMD	32.11	
68	SD_DATA0	32.11	
67	SD_DATA1	32.11	
66	SD_DATA2	32.11	
65	SD_DATA3	32.11	

3.13. GPIO Interfaces

SC600Y/SC600T has abundant GPIO interfaces with power domain of 1.8V. The pin definition is listed below.

Table 16: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	GPIO	Default Status	Comment
GPIO_0	248	GPIO_0	B-PD:nppukp [1)]	
GPIO_1	247	GPIO_1	B-PD:nppukp	Wake up [2)]
GPIO_2	201	GPIO_2	B-PD:nppukp	
GPIO_3	200	GPIO_3	B-PD:nppukp	
UART2_TXD	5	GPIO_4	B-PD:nppukp	
UART2_RXD	6	GPIO_5	B-PD:nppukp	Wake up
TP1_I2C_SDA	204	GPIO_6	B-PD:nppukp	
TP1_I2C_SCL	205	GPIO_7	B-PD:nppukp	
TP1_RST	136	GPIO_8	B-PD:nppukp	
TP1_INT	137	GPIO_9	B-PD:nppukp	Wake up
TP0_I2C_SDA	206	GPIO_10	B-PD:nppukp	
TP0_I2C_SCL	140	GPIO_11	B-PD:nppukp	
UART4_TXD	7	GPIO_12	B-PD:nppukp	Wake up
UART4_RXD	8	GPIO_13	B-PD:nppukp	Wake up
SENSOR_I2C_SDA	132	GPIO_14	B-PD:nppukp	
SENSOR_I2C_SCL	131	GPIO_15	B-PD:nppukp	
UART5_TXD	199	GPIO_16	B-PD:nppukp	
UART5_RXD	198	GPIO_17	B-PD:nppukp	Wake up
UART5_CTS	246	GPIO_18	B-PD:nppukp	
UART5_RTS	245	GPIO_19	B-PD:nppukp	

SPI_MOSI	60	GPIO_20	B-PD:nppukp	
SPI_MISO	61	GPIO_21	B-PD:nppukp	Wake up
SPI_CS	58	GPIO_22	B-PD:nppukp	
SPI_CLK	59	GPIO_23	B-PD:nppukp	
LCD0_TE	126	GPIO_24	B-PD:nppukp	
LCD1_TE	114	GPIO_25	B-PD:nppukp	Wake up
MCAM_MCLK	99	GPIO_26	B-PD:nppukp	
SCAM_MCLK	100	GPIO_27	B-PD:nppukp	
DCAM_MCLK	194	GPIO_28	B-PD:nppukp	Wake up
CAM_I2C_SDA	76	GPIO_29	B-PD:nppukp	
CAM_I2C_SCL	75	GPIO_30	B-PD:nppukp	
DCAM_I2C_SDA	197	GPIO_31	B-PD:nppukp	Wake up
DCAM_I2C_SCL	196	GPIO_32	B-PD:nppukp	
GPIO_33	238	GPIO_33	B-PD:nppukp	
GPIO_36	237	GPIO_36	B-PD:nppukp	Wake up
MCAM_PWDN	73	GPIO_39	B-PD:nppukp	
MCAM_RST	74	GPIO_40	B-PD:nppukp	
GPIO_42	252	GPIO_42	B-PD:nppukp	Wake up
GPIO_43	253	GPIO_43	B-PD:nppukp	Wake up
GPIO_44	254	GPIO_44	B-PD:nppukp	Wake up
GPIO_45	255	GPIO_45	B-PD:nppukp	Wake up
LCD0_RST	127	GPIO_61	B-PD:nppukp	Wake up
TP0_RST	138	GPIO_64	B-PD:nppukp	
TP0_INT	139	GPIO_65	B-PD:nppukp	Wake up
GPIO_66	234	GPIO_66	B-PD:nppukp	
VOL_UP	146	GPIO_85	B-PD:nppukp	Wake up
LCD1_RST	113	GPIO_87	B-PD:nppukp	Wake up

GPIO_89	232	GPIO_89	B-PD:nppukp	
GPIO_90	231	GPIO_90	B-PD:nppukp	Wake up
GPIO_96	230	GPIO_96	B-PD:nppukp	
GPIO_97	229	GPIO_97	B-PD:nppukp	Wake up
GPIO_98	177	GPIO_98	B-PD:nppukp	
GPIO_99	178	GPIO_99	B-PD:nppukp	
CAM4_MCLK	236	GPIO_128	B-PD:nppukp	
SCAM_RST	72	GPIO_129	B-PD:nppukp	Wake up
SCAM_PWDN [3)]	71	GPIO_130	B-PD:nppukp	Wake up
DCAM_RST	180	GPIO_131	B-PD:nppukp	Wake up
DCAM_PWDN [3)]	181	GPIO_132	B-PD:nppukp	Wake up
SD_DET	64	GPIO_133	B-PD:nppukp	Wake up
FP_SPI_CLK	250	GPIO_135	B-PD:nppukp	
FP_SPI_CS	203	GPIO_136	B-PD:nppukp	
FP_SPI_MOSI	249	GPIO_137	B-PD:nppukp	Wake up
FP_SPI_MISO	251	GPIO_138	B-PD:nppukp	Wake up
USB_SS_SEL	226	GPIO_139	B-PD:nppukp	Wake up

NOTES

1. [1)] B: Bidirectional digital with CMOS input; PD: nppukp = default pulldown with programmable options following the colon (:).
2. [2)] Wakeup: interrupt pins that can wake up the system.
3. [3)] SCAM_PWDN and DCAM_PWDN cannot be pulled up when the module starts up.
4. More details about GPIO configuration, please refer to ***document [2]***.

3.14. I2C Interfaces

SC600Y/SC600T provides five groups of I2C interfaces. As an open drain output, each I2C interface should be pulled up to 1.8V. The SENSOR_I2C interface supports only sensors of the aDSP architecture. CAM/DCAM_I2C bus is controlled by Linux Kernel code and supports connection to video output related devices.

Table 17: Pin Definition of I2C Interfaces

Pin Name	Pin No	I/O	Description	Comment
TP0_I2C_SCL	140	OD	TP0 I2C clock	Used for TP0
TP0_I2C_SDA	206	OD	TP0 I2C data	
TP1_I2C_SCL	205	OD	TP1 I2C clock	Used for TP1
TP1_I2C_SDA	204	OD	TP1 I2C data	
CAM_I2C_SCL	75	OD	I2C clock for camera	Used for cameras
CAM_I2C_SDA	76	OD	I2C data for camera	
DCAM_I2C_SCL	196	OD	I2C clock for depth camera	Used for depth camera
DCAM_I2C_SDA	197	OD	I2C data for depth camera	
SENSOR_I2C_SCL	131	OD	I2C clock for external sensors	Used for external sensors
SENSOR_I2C_SDA	132	OD	I2C data for external sensors	

3.15. I2S Interface

SC600Y/SC600T provides one I2S interface. The I2S interface is multiplexed from FP_SPI, with power domain of 1.8V .

Table 18: Pin Definition of I2S Interface

Pin Name	Pin No	I/O	Description	Comment
FP_SPI_CS	203	DO	SPI chip select	SPI interface pin by default. Can be multiplexed into I2S_WS (I2S word select (L/R)).
FP_SPI_CLK	250	DO	SPI clock	SPI interface pin by default. Can be multiplexed into I2S_SCK (I2S bit clock).
FP_SPI_MOSI	249	DO	SPI master-out slave-in	SPI interface pin by default. Can be multiplexed into I2S_D0 (I2S serial data channel 0).
FP_SPI_MISO	251	DI	SPI master-in salve-out	SPI interface pin by default. Can be multiplexed into I2S_D1 (I2S serial data channel 1).
LCD1_TE	114	DI	LCD1 tearing effect	LCM interface pin by default. Can be multiplexed into I2S_MCLK_A (I2S master clock A).
GPIO_66	234	DI/DO	General-purpose input/output	GPIO by default. Can be multiplexed into I2S_MCLK_B (I2S master clock B).

3.16. SPI Interfaces

SC600Y/SC600T provides two SPI interfaces which only support master mode. The two interfaces are typically applied for fingerprint identification.

Table 19: Pin Definition of SPI Interfaces

Pin Name	Pin No	I/O	Description	Comment
SPI_CS	58	DO	SPI chip select	Can be multiplexed into UART6_CST.
SPI_CLK	59	DO	SPI clock	Can be multiplexed into UART6_RTS.
SPI_MOSI	60	DO	SPI master-out slave-in	Can be multiplexed into UART6_TXD.
SPI_MISO	61	DI	SPI master-in salve-out	Can be multiplexed into UART6_RXD.
FP_SPI_CS	203	DO	SPI chip select	Can be multiplexed into I2S_WS.
FP_SPI_CLK	250	DO	SPI clock	Can be multiplexed into I2S_SCK.
FP_SPI_MOSI	249	DO	SPI master-out slave-in	Can be multiplexed into I2S_D0.
FP_SPI_MISO	251	DI	SPI master-in salve-out	Can be multiplexed into I2S_D1.

3.17. ADC Interfaces

SC600Y/SC600T provides two analog-to-digital converter (ADC) interfaces, and the pin definition is shown below.

Table 20: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PMI_ADC	153	AI	General purpose ADC interface	Maximum input voltage: 1.5V.
PMU_MPP2	151	AI	General purpose ADC interface	Maximum input voltage: 1.7V.

The resolution of the ADC is up to 15 bits.

3.18. Vibrator Drive Interface

The pin definition of vibrator drive interface is listed below.

Table 21: Pin Definition of Vibrator Drive Interface

Pin Name	Pin No	I/O	Description	Comment
VIB_GND	160		Vibrator GND (-)	Connected to the negative terminal of vibrator.
VIB_DRV	161	PO	Vibrator drive (+)	Connected to the positive terminal of vibrator.

The vibrator is driven by an exclusive circuit, and a reference circuit design is shown below.

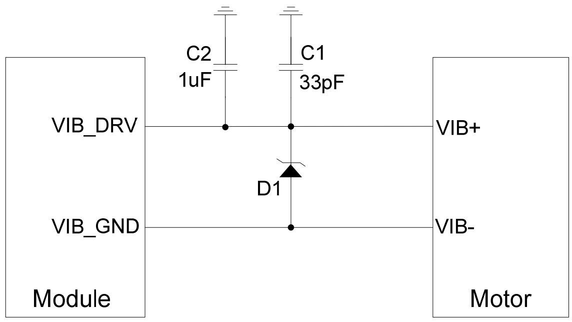

Figure 19: Reference Circuit for Vibrator Connection

3.19. LCM Interfaces

SC600Y/SC600T provides two LCM interfaces, and supports dual LCDs with WUXGA (1900×1200) display. These interfaces support high speed differential data transmission, with up to eight lanes.

Table 22: Pin Definition of LCM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
LDO6_1P8	10	PO	1.8V output power supply LCM logic circuit and DSI	
LDO17_2P85	12	PO	2.85V output power supply for LCM analog circuits	
PMU_MPP4	152	DO	PWM output	
LCD_BL_A	21	PO	Current output for LCD backlight	
LCD_BL_K1	22	AI	Current sink for LCD backlight	
LCD_BL_K2	23	AI	Current sink for LCD backlight	
LCD_BL_K3	24	AI	Current sink for LCD backlight	
LCD_BL_K4	25	AI	Current sink for LCD backlight	
LCD0_RST	127	DO	LCD0 reset	Active low.
LCD0_TE	126	DI	LCD0 tearing effect	
LCD1_RST	113	DO	LCD1 reset	Active low.
LCD1_TE	114	DI	LCD1 tearing effect	
DSI0_CLK_N	116	AO	LCD0 MIPI clock signal (-)	
DSI0_CLK_P	115	AO	LCD0 MIPI clock signal (+)	
DSI0_LN0_N	118	AO	LCD0 MIPI lane 0 data signal (-)	
DSI0_LN0_P	117	AO	LCD0 MIPI lane 0 data signal (+)	
DSI0_LN1_N	120	AO	LCD0 MIPI lane 1 data signal (-)	

DSI0_LN1_P	119	AO	LCD0 MIPI lane 1 data signal (+)
DSI0_LN2_N	122	AO	LCD0 MIPI lane 2 data signal (-)
DSI0_LN2_P	121	AO	LCD0 MIPI lane 2 data signal (+)
DSI0_LN3_N	124	AO	LCD0 MIPI lane 3 data signal (-)
DSI0_LN3_P	123	AO	LCD0 MIPI lane 3 data signal (+)
DSI1_CLK_N	103	AO	LCD1 MIPI clock signal (-)
DSI1_CLK_P	102	AO	LCD1 MIPI clock signal (+)
DSI1_LN0_N	105	AO	LCD1 MIPI lane 0 data signal (-)
DSI1_LN0_P	104	AO	LCD1 MIPI lane 0 data signal (+)
DSI1_LN1_N	107	AO	LCD1 MIPI lane 1 data signal (-)
DSI1_LN1_P	106	AO	LCD1 MIPI lane 1 data signal (+)
DSI1_LN2_N	109	AO	LCD1 MIPI lane 2 data signal (-)
DSI1_LN2_P	108	AO	LCD1 MIPI lane 2 data signal (+)
DSI1_LN3_N	111	AO	LCD1 MIPI lane 3 data signal (-)
DSI1_LN3_P	110	AO	LCD1 MIPI lane 3 data signal (+)

The following are the reference designs for LCM interfaces.

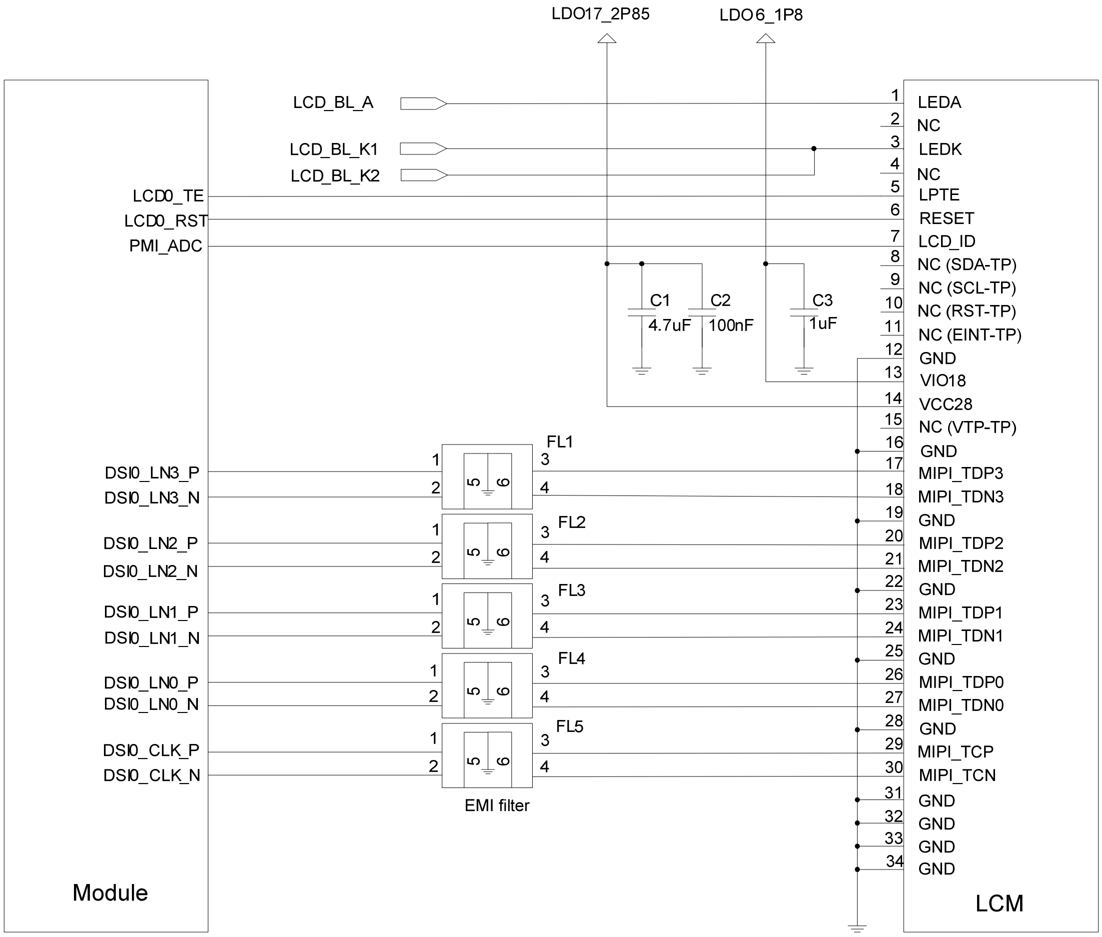

Figure 20: Reference Circuit Design for LCM0 Interface

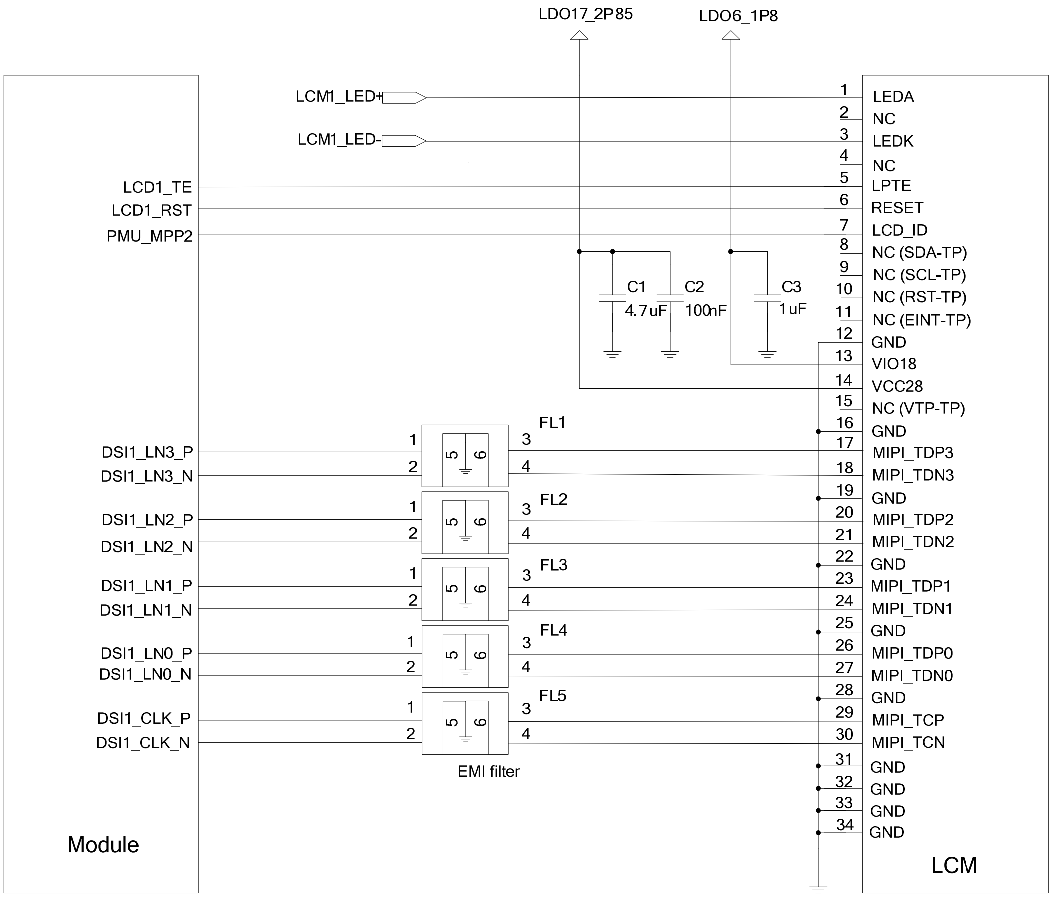

Figure 21: Reference Circuit Design for LCM1 Interface

MIPI are high speed signal lines. It is recommended that common-mode filters should be added in series near the LCM connector, so as to improve protection against electromagnetic radiation interference.

When compatible design with other displays is required, please connect the LCD_ID pin of LCM to the module's ADC pin, and please note that the output voltage of LCD_ID cannot exceed the voltage range of ADC pin.

Backlight driving circuits should be designed for LCMs. SC600Y/SC600T provide backlight driving output which can be used to drive LCM backlight WLEDs directly. The features are listed below:

- Use the high voltage output (LCD_BL_A) for powering WLED strings, and the output voltage can be configured from VBAT to 29.5V.
- Support 4 current sinks (LCD_BL_K1, LCD_BL_K2, LCD_BL_K3, LCD_BL_K4), with maximum sink current up to 25mA for each.

- Power two strings of WLEDs (about 14 WLEDs) with two current sink drivers, or power four strings of WLEDs (about 24 WLEDs) with four current sink drivers.
- The duty ratio of PWM can be configured by software to adjust the backlight brightness.

LCM0 uses the internal backlight driving circuit provided by SC600Y/SC600T by default. LCM1 can use the internal circuit or an external backlight driving circuit according to customers' demands. The following is a reference design for LCM1 external backlight driving circuit where PMU_MPP4 is used to adjust the backlight brightness.

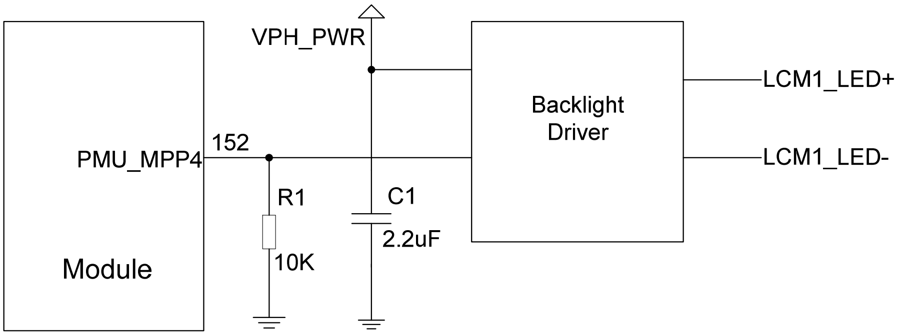

Figure 22: Reference Design of LCM1 External Backlight Driving Circuit

3.20. Touch Panel Interfaces

SC600Y/SC600T provides two I2C interfaces for connection with touch panel, and also provides the corresponding power supply and interrupt pins. The pin definition of touch panel interfaces is illustrated below.

Table 23: Pin Definition of Touch Panel Interfaces

Pin Name	Pin No	I/O	Description	Comment
LDO10_2P8	11	PO	2.8V output power supply.	Vnorm=2.8V $I_O$max=150mA
LDO6_1P8	10	PO	1.8V output power supply.	Pull-up power supply of I2C Vnorm=1.8V $I_O$max=300mA
TP0_INT	139	DI	TP0 Interrupt	1.8V power domain.
TP0_RST	138	DO	TP0 reset	1.8V power domain. Active low.

TP0_I2C_SCL	140	OD	TP0 I2C clock	1.8V power domain.
TP0_I2C_SDA	206	OD	TP0 I2C data	1.8V power domain.
TP1_INT	137	DI	TP1 Interrupt	1.8V power domain.
TP1_RST	136	DO	TP1 reset	Active low.
TP1_I2C_SCL	205	OD	TP1 I2C clock	1.8V power domain.
TP1_I2C_SDA	204	OD	TP1 I2C data	1.8V power domain.

A reference design for touch panel interfaces is shown below.

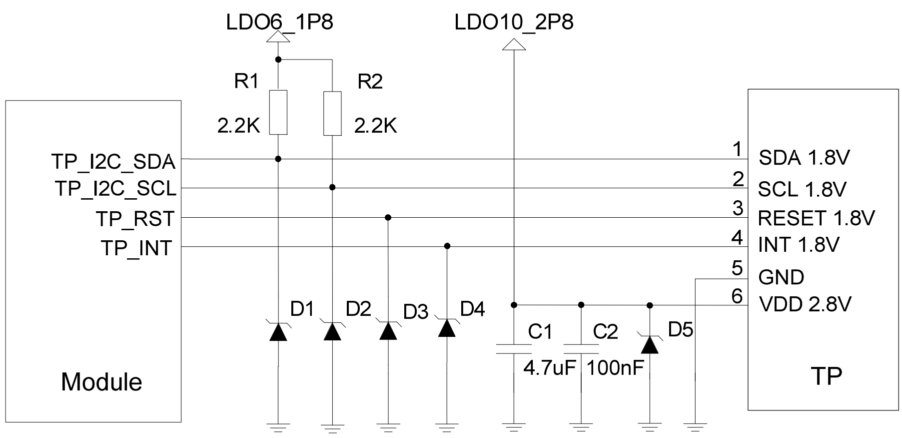

Figure 23: Reference Circuit Design for Touch Panel Interfaces

NOTE

TP is powered by LDO10_2P8 by default and LDO10_2P8 can output 150mA current. It is recommended to use an external LDO power supply if dual-TP or other applications need to be supported.

3.21. Camera Interfaces

Based on standard MIPI CSI input interface, SC600Y/SC600T supports 3 cameras (4-lane + 4-lane + 4-lane) or 4 cameras (4-lane + 4-lane + 2-lane + 1-lane), with maximum pixels up to 21MP for SC600Y and 24MP for SC600T. The video and photo quality are determined by various factors such as camera sensor, camera lens quality, etc.

Table 24: Pin Definition of Camera Interfaces

Pin Name	Pin No.	I/O	Description	Comment
LDO2_1P1	13	PO	1.1V output power supply for digital core circuit of rear camera	Vnorm=1.1V $I_O$max=1200mA
LDO6_1P8	10	PO	1.8V output power supply for digital I/O circuit of camera	Vnorm=1.8V $I_O$max=300mA
LDO17_2P85	12	PO	2.85V output power supply auto focus circuit	Vnorm=2.85V $I_O$max=300mA
LDO22_2P8	14	PO	2.8V output power supply for AVDD of cameras	Vnorm=2.8V $I_O$max=150mA
LDO23_1P2	15	PO	1.2V output power supply for digital core circuit of front camera	Vnorm=1.2V $I_O$max=600mA
CSI0_CLK_N	89	AO	MIPI clock signal of rear camera (-)	
CSI0_CLK_P	88	AO	MIPI clock signal of rear camera (+)	
CSI0_LN0_N	91	AI	MIPI lane 0 data signal of rear camera (-)	
CSI0_LN0_P	90	AI	MIPI lane 0 data signal of rear camera (+)	
CSI0_LN1_N	93	AI	MIPI lane 1 data signal of rear camera (-)	
CSI0_LN1_P	92	AI	MIPI lane 1 data signal of rear camera (+)	
CSI0_LN2_N	95	AI	MIPI lane 2 data signal of rear camera (-)	
CSI0_LN2_P	94	AI	MIPI lane 2 data signal of rear camera (+)	
CSI0_LN3_N	97	AI	MIPI lane 3 data signal of rear camera (-)	

CSI0_LN3_P	96	AI	MIPI lane 3 data signal of rear camera (+)	
CSI1_CLK_N	184	AO	MIPI clock signal of depth camera (-)	
CSI1_CLK_P	183	AO	MIPI clock signal of depth camera (+)	
CSI1_LN0_N	186	AI	MIPI lane 0 data signal of depth camera (-)	
CSI1_LN0_P	185	AI	MIPI lane 0 data signal of depth camera (+)	
CSI1_LN1_N	188	AI	MIPI lane 1 data signal of depth camera (-)	
CSI1_LN1_P	187	AI	MIPI lane 1 data signal of depth camera (+)	
CSI1_LN2_N	190	AI	MIPI lane 2 data signal of depth camera (-)	Can be multiplexed into differential data of the fourth camera (-).
CSI1_LN2_P	189	AI	MIPI lane 2 data signal of depth camera (+)	Can be multiplexed into differential data of the fourth camera (+).
CSI1_LN3_N	192	AI	MIPI lane 3 data signal of depth camera (-)	Can be multiplexed into differential clock of the fourth camera (-).
CSI1_LN3_P	191	AI	MIPI lane 3 data signal of depth camera (+)	Can be multiplexed into differential clock of the fourth camera (+).
CSI2_CLK_N	78	AO	MIPI clock signal of front camera (-)	
CSI2_CLK_P	77	AO	MIPI clock signal of front camera (+)	
CSI2_LN0_N	80	AI	MIPI lane 0 data signal of front camera (-)	
CSI2_LN0_P	79	AI	MIPI lane 0 data signal of front camera (+)	
CSI2_LN1_N	82	AI	MIPI lane 1 data signal of front camera (-)	
CSI2_LN1_P	81	AI	MIPI lane 1 data signal of front camera (+)	
CSI2_LN2_N	84	AI	MIPI lane 2 data signal of front camera (-)	
CSI2_LN2_P	83	AI	MIPI lane 2 data signal of front camera (+)	

CSI2_LN3_N	86	AI	MIPI lane 3 data signal of front camera (-)	
CSI2_LN3_P	85	AI	MIPI lane 3 data signal of front camera (+)	
MCAM_MCLK	99	DO	Master clock of rear camera	1.8V power domain.
SCAM_MCLK	100	DO	Master clock of front camera	1.8V power domain.
MCAM_RST	74	DO	Reset of rear camera	1.8V power domain.
MCAM_PWDN	73	DO	Power down of rear camera	1.8V power domain.
SCAM_RST	72	DO	Reset of front camera	1.8V power domain.
SCAM_PWDN	71	DO	Power down of front camera	1.8V power domain.
CAM_I2C_SCL	75	OD	I2C clock for camera	1.8V power domain.
CAM_I2C_SDA	76	OD	I2C data for camera	1.8V power domain.
DCAM_MCLK	194	DO	Clock of depth camera	1.8V power domain.
CAM4_MCLK	236	DO	Master clock of fourth camera	1.8V power domain.
DCAM_RST	180	DO	Reset of depth camera	1.8V power domain.
DCAM_PWDN	181	DO	Power down of depth camera	1.8V power domain.
DCAM_I2C_SDA	197	OD	I2C data for depth camera	1.8V power domain.
DCAM_I2C_SCL	196	OD	I2C clock for depth camera	1.8V power domain.

The following is a reference circuit design for dual camera applications.

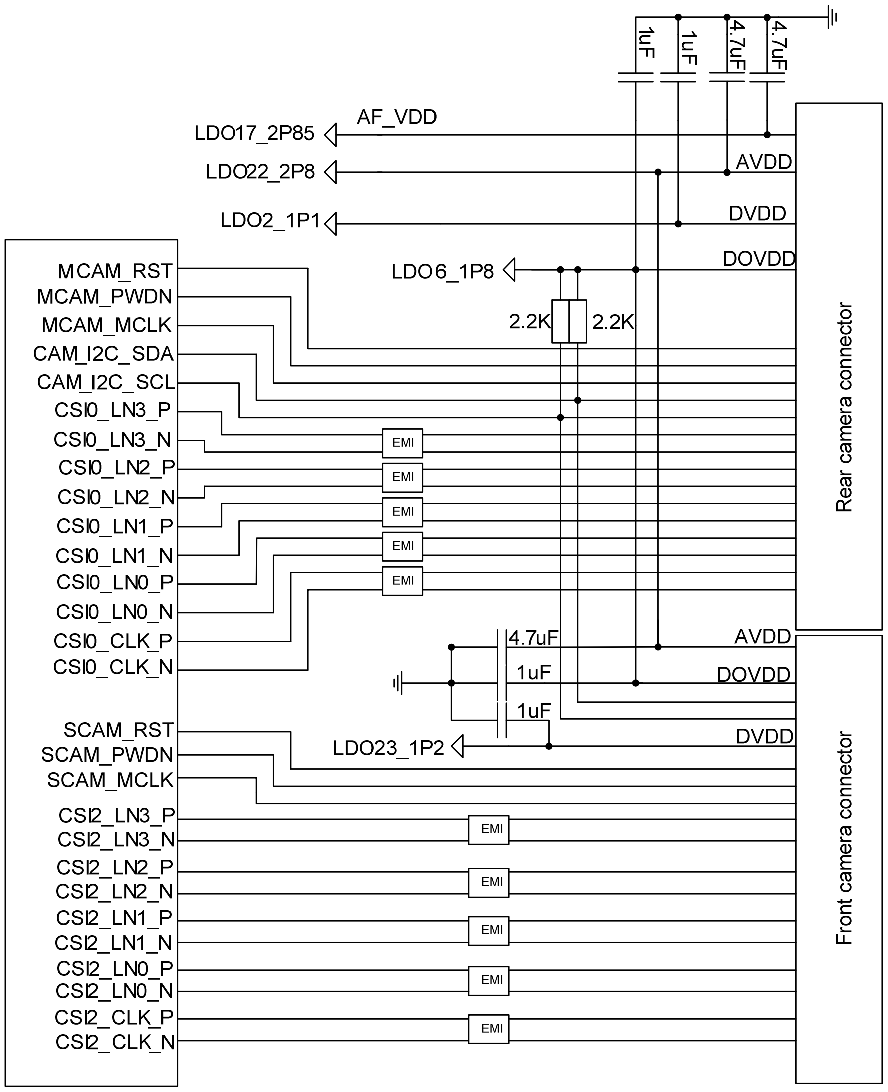

Figure 24: Reference Circuit Design for Dual Camera Applications

NOTE

CSI0 is used for rear camera, CSI1 is used for depth camera, and CSI2 is used for front camera.

The following is a reference circuit design for triple camera applications.

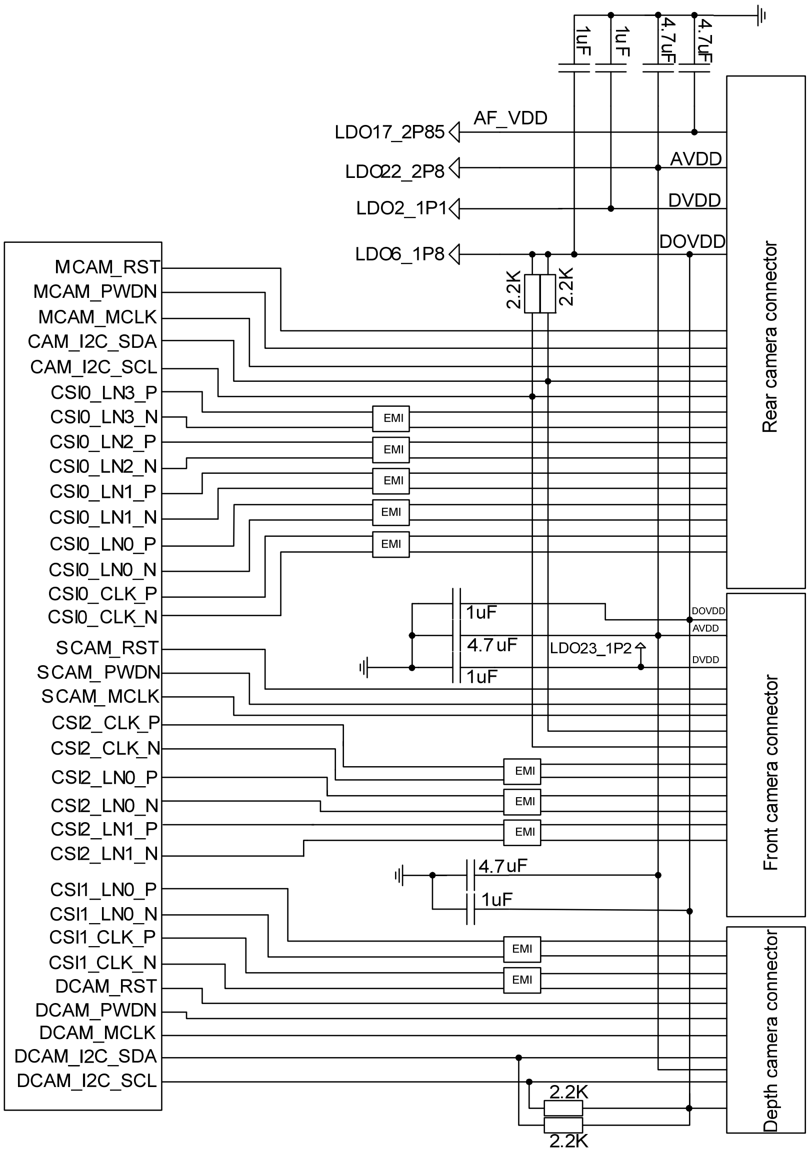

Figure 25: Reference Circuit Design for Triple Camera Applications

NOTE

CSI1 data lines CSI1_LN2_P, CSI1_LN2_N, CSI1_LN3_P and CSI1_LN3_N can be multiplexed into MIPI signals for the fourth camera in four-camera application.

3.21.1. Design Considerations

- Special attention should be paid to the pin definition of LCM/camera connectors. Assure the SC600Y/SC600T and the connectors are correctly connected.
- MIPI are high speed signal lines, supporting maximum data rate up to 2.1Gbps. The differential impedance should be controlled as 100Ω. Additionally, it is recommended to route the trace on the inner layer of PCB, and do not cross it with other traces. For the same group of DSI or CSI signals, all the MIPI traces should keep the same length. In order to avoid crosstalk, it is recommended to maintain the intra-lane spacing as trace width and the inter-lane spacing as two times of the trace width. Any cut or hole on GND reference plane under MIPI signals should be avoided.
- It is recommended to select a low capacitance TVS for ESD protection and the recommended parasitic capacitance is below 1pF.
- Route MIPI traces according to the following rules:

  a) The total trace length should not exceed 305mm;
  b) Control the differential impedance to 100Ω±10%;
  c) Control intra-lane length difference within 0.67mm;
  d) Control inter-lane length difference within 1.3mm.

Table 25: MIPI Trace Length Inside the Module

Pin No.	Pin Name	Length (mm)	Length Difference (P-N)
116	DSI0_CLK_N	20.82	-0.45
115	DSI0_CLK_P	20.37	
118	DSI0_LN0_N	24.84	0
117	DSI0_LN0_P	24.84	
120	DSI0_LN1_N	24.85	-0.03
119	DSI0_LN1_P	24.82	
122	DSI0_LN2_N	25.94	0.24
121	DSI0_LN2_P	26.18	
124	DSI0_LN3_N	29.31	0.2
123	DSI0_LN3_P	29.51	
103	DSI1_CLK_N	9.52	-0.05
102	DSI1_CLK_P	9.47	

105	DSI1_LN0_N	10.27	-0.11
104	DSI1_LN0_P	10.16	
107	DSI1_LN1_N	11.75	-0.17
106	DSI1_LN1_P	11.58	
109	DSI1_LN2_N	14.86	-0.36
108	DSI1_LN2_P	14.5	
111	DSI1_LN3_N	15.73	0.15
110	DSI1_LN3_P	15.88	
89	CSI0_CLK_N	16.54	0.03
88	CSI0_CLK_P	16.57	
91	CSI0_LN0_N	17.47	-0.07
90	CSI0_LN0_P	17.4	
93	CSI0_LN1_N	12.13	-0.05
92	CSI0_LN1_P	12.08	
95	CSI0_LN2_N	9.56	0.14
94	CSI0_LN2_P	9.7	
97	CSI0_LN3_N	8.73	0.13
96	CSI0_LN3_P	8.86	
184	CSI1_CLK_N	20.32	-0.23
183	CSI1_CLK_P	20.09	
186	CSI1_LN0_N	12.09	0.57
185	CSI1_LN0_P	12.66	
188	CSI1_LN1_N	11.33	0.37
187	CSI1_LN1_P	11.70	
190	CSI1_LN2_N	5.86	0.19
189	CSI1_LN2_P	6.05	

192	CSI1_LN3_N	10.49	-0.43
191	CSI1_LN3_P	10.06	
78	CSI2_CLK_N	22.00	0.17
77	CSI2_CLK_P	22.17	
80	CSI2_LN0_N	22.07	-0.07
79	CSI2_LN0_P	22.00	
82	CSI2_LN1_N	22.54	-0.49
81	CSI2_LN1_P	22.05	
84	CSI2_LN2_N	22.03	-0.11
83	CSI2_LN2_P	21.92	
86	CSI2_LN3_N	21.90	0.59
85	CSI2_LN3_P	22.49	

3.21.2. Flashlight Interfaces

SC600Y/SC600T supports 2 flash LED drivers. In Flash mode, the maximum output current is 0.75A each for two LEDs and 1.5A for one LED. In torch mode, the maximum output current is 300mA each for two LEDs and 300mA for one LED.

Table 26: Pin Definition of Flashlight Interfaces

Pin Name	Pin No.	I/O	Description	Comment
FLASH_LED1	26	AO	Flash/torch current driver output	Support flash and torch modes.
FLASH_LED2	162	AO	Flash/torch current driver output	

A reference circuit design is shown below.

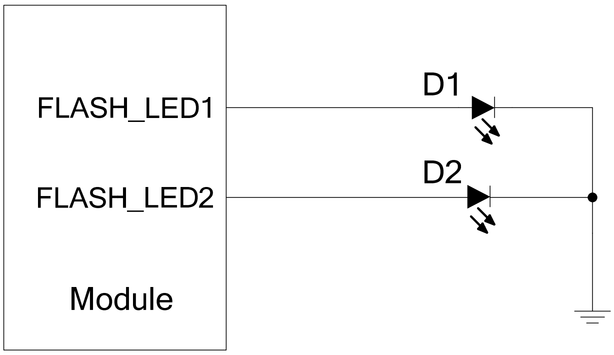

Figure 26: Reference Circuit Design for Flashlight Interfaces

3.22. Sensor Interfaces

SC600Y/SC600T modules support communication with sensors via I2C interface, and it supports various sensors such as acceleration sensor, gyroscopic sensor, compass, optical sensor, temperature sensor.

Table 27: Pin Definition of Sensor Interfaces

Pin Name	Pin No.	I/O	Description	Comment
SENSOR_I2C_SCL	131	OD	I2C clock for external sensors	Dedicated for external sensors. Cannot be used for other devices such as touch panel, NFC, keypad, etc.
SENSOR_I2C_SDA	132	OD	I2C data for external sensors	
GPIO_43	253	DI	Interrupt signal of optical sensor	
GPIO_44	254	DI	Interrupt signal of direction sensor (compass)	
GPIO_42	252	DI	Interrupt signal of acceleration sensor	
GPIO_45	255	DI	Interrupt signal of gyroscopic sensor	

3.23. Audio Interfaces

SC600Y/SC600T provides three analog input channels and three analog output channels. The following table shows the pin definition.

Table 28: Pin Definition of Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MIC1_P	44	AI	Microphone input for channel 1 (+)	
MIC1_N	45	AI	Microphone input for channel 1 (-)	
MIC_GND	168		Microphone reference ground	If unused, connect this pin to the ground.
MIC2_P	46	AI	Microphone input for headset (+)	
MIC3_P	169	AI	Microphone input for channel 2 (+)	
MIC_BIAS	167	AO	Microphone bias voltage	
EAR_P	53	AO	Earpiece output (+)	
EAR_N	52	AO	Earpiece output (-)	
SPK_P	55	AO	Speaker output (+)	
SPK_N	54	AO	Speaker output (-)	
HPH_R	51	AO	Headphone right channel output	
HPH_REF	50	AI	Headphone reference ground	It should be connected to main GND.
HPH_L	49	AO	Headphone left channel output	
HS_DET	48	AI	Headset insertion detection	High level by default.

- The module offers three audio input channels, including one differential input pair and two single-ended channels. The three sets of MICs are integrated with internal bias voltage.
- The output voltage range of MIC_BIAS is programmable between 1.6V and 2.85V, and the maximum output current is 3mA.
- The earpiece interface uses differential output.
- The loudspeaker interface uses differential output as well. The output channel is available with a Class-D amplifier whose maximum output power is 1.5W when load is 8Ω.
- The headphone interface features stereo left and right channel output, and headphone insertion detection function is supported.

3.23.1. Reference Circuit Design for Microphone Interfaces

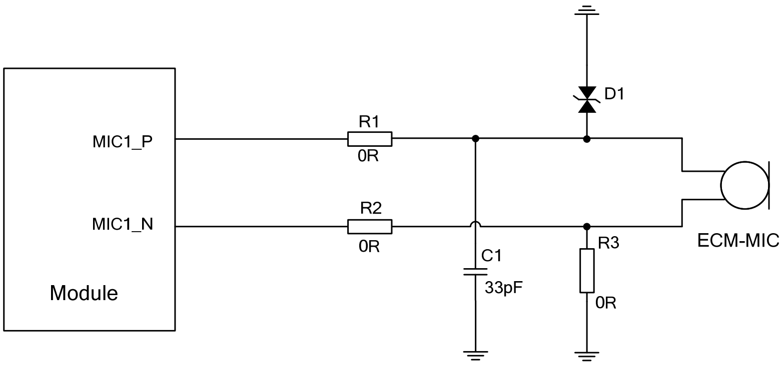

Figure 27: Reference Circuit Design for Analog ECM-type Microphone

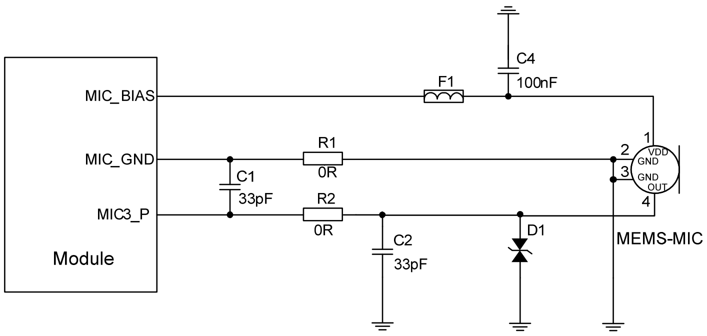

Figure 28: Reference Circuit Design for MEMS-type Microphone

3.23.2. Reference Circuit Design for Earpiece Interface

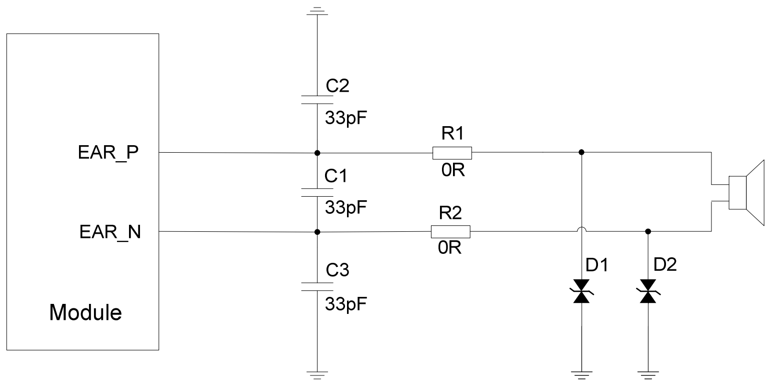

Figure 29: Reference Circuit Design for Earpiece Interface

3.23.3. Reference Circuit Design for Headphone Interface

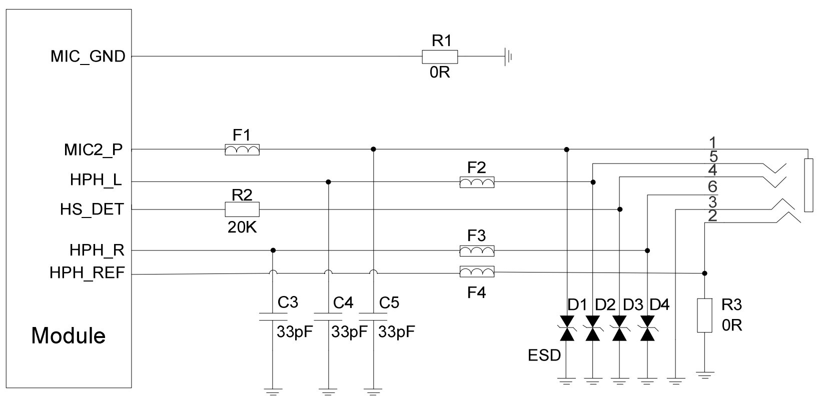

Figure 30: Reference Circuit Design for Headphone Interface with a NO Jack

3.23.4. Reference Circuit Design for Loudspeaker Interface

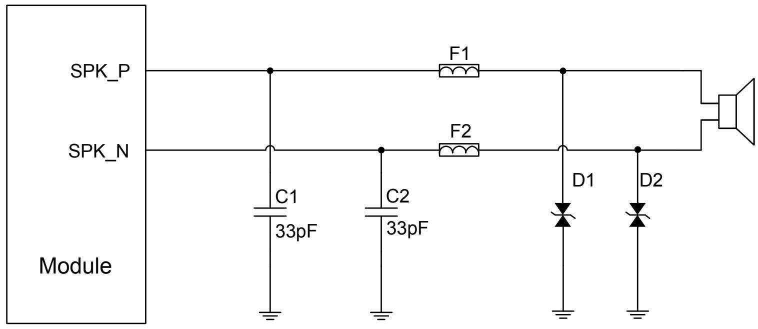

Figure 31: Reference Circuit Design for Loudspeaker Interface

3.23.5. Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10pF and 33pF) for filtering out RF interference, thus reducing TDD noise. The 33pF capacitor is applied for filtering out RF interference when the module is transmitting at EGSM900. Without placing this capacitor, TDD noise could be heard. The 10pF capacitor here is used for filtering out RF interference at DCS1800. Please note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, customers would have to discuss with their capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. In some cases, EGSM900 TDD noise is more severe; while in other cases, DCS1800 TDD noise is more obvious. Therefore, a suitable capacitor can be selected based on the test results. Sometimes, even no RF filtering capacitor is required.

In order to decrease radio or other signal interference, RF antennas should be placed away from audio interfaces and audio traces. Power traces cannot be parallel with and also should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

3.24. Emergency Download Interface

USB_BOOT is an emergency download interface. Pull up to LDO5_1P8 during power-up will force the module enter into emergency download mode. This is an emergency option when there are failures such as abnormal startup or operation. For convenient firmware upgrade and debugging in the future, please reserve the reference circuit design shown as below.

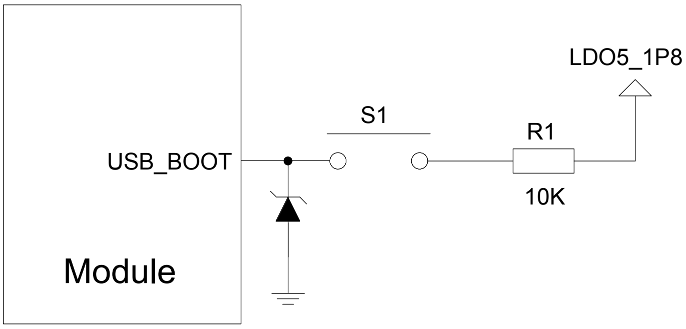

Figure 32: Reference Circuit Design for Emergency Download Interface

4 Wi-Fi and BT

SC600Y/SC600T provides a shared antenna interface ANT_WIFI/BT for Wi-Fi and Bluetooth (BT) functions. The interface impedance is 50Ω. External antennas such as PCB antenna, sucker antenna and ceramic antenna can be connected to the module via the interface, so as to achieve Wi-Fi and BT functions.

4.1. Wi-Fi Overview

SC600Y/SC600T supports 2.4GHz and 5GHz dual-band WLAN wireless communication based on IEEE 802.11a/b/g/n/ac standard protocols. The maximum data rate is up to 433Mbps.

The features are as below:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI SMS4 hardware encryption
- Support AP mode
- Support Wi-Fi Direct
- Support MCS 0-7 for HT20 and HT40
- Support MCS 0-8 for VHT20
- Support MCS 0-9 for VHT40 and VHT80

4.1.1. Wi-Fi Performance

The following table lists the Wi-Fi transmitting and receiving performance of SC600Y/SC600T module.

Table 29: Wi-Fi Transmitting Performance

	Standard	Rate	Output Power
2.4GHz	802.11b	1Mbps	16dBm±2.5dB
	802.11b	11Mbps	16dBm±2.5dB
	802.11g	6Mbps	16dBm±2.5dB

	802.11g	54Mbps	14dBm±2.5dB
	802.11n HT20	MCS0	15dBm±2.5dB
	802.11n HT20	MCS7	13dBm±2.5dB
	802.11n HT40	MCS0	14dBm±2.5dB
	802.11n HT40	MCS7	13dBm±2.5dB
5GHz	802.11a	6Mbps	14dBm±2.5dB
	802.11a	54Mbps	13dBm±2.5dB
	802.11n HT20	MCS0	15dBm±2.5dB
	802.11n HT20	MCS7	13dBm±2.5dB
	802.11n HT40	MCS0	15dBm±2.5dB
	802.11n HT40	MCS7	13dBm±2.5dB
	802.11ac VHT20	MCS0	15dBm±2.5dB
	802.11ac VHT20	MCS8	13dBm±2.5dB
	802.11ac VHT40	MCS0	14dBm±2.5dB
	802.11ac VHT40	MCS9	13dBm±2.5dB
	802.11ac VHT80	MCS0	13dBm±2.5dB
	802.11ac VHT80	MCS9	12dBm±2.5dB

Table 30: Wi-Fi Receiving Performance

	Standard	Rate	Sensitivity
2.4GHz	802.11b	1Mbps	-94dBm
	802.11b	11Mbps	-86dBm
	802.11g	6Mbps	-88dBm
	802.11g	54Mbps	-71dBm
	802.11n HT20	MCS0	-87dBm

	802.11n HT20	MCS7	-69dBm
	802.11n HT40	MCS0	-85dBm
	802.11n HT40	MCS7	-67dBm
5GHz	802.11a	6Mbps	-90dBm
	802.11a	54Mbps	-71dBm
	802.11n HT20	MCS0	-86dBm
	802.11n HT20	MCS7	-66dBm
	802.11n HT40	MCS0	-84dBm
	802.11n HT40	MCS7	-65dBm
	802.11ac VHT20	MCS8	-65dBm
	802.11ac VHT40	MCS9	-61dBm
	802.11ac VHT80	MCS9	-56dBm

Reference specifications are listed below:

- IEEE 802.11n WLAN MAC and PHY, October 2009 + IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- IEEE Std 802.11b, IEEE Std 802.11d, IEEE Std 802.11e, IEEE Std 802.11g, IEEE Std 802.11i: IEEE 802.11-2007 WLAN MAC and PHY, June 2007

4.2. BT Overview

SC600Y/SC600T supports BT4.2 (BR/EDR+BLE) specifications, as well as GFSK, 8-DPSK, π/4-DQPSK modulation modes.

- Maximally support up to 7 wireless connections
- Maximally support up to 3.5 piconets at the same time
- Support one SCO or eSCO (Extended Synchronous Connection Oriented) connection

The BR/EDR channel bandwidth is 1MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2MHz, and can accommodate 40 channels.

Table 31: BT Data Rate and Versions

Version	Data rate	Maximum Application	Throughput	Comment
1.2	1Mbit/s	> 80Kbit/s		
2.0+EDR	3Mbit/s	> 80Kbit/s		
3.0+HS	24Mbit/s	Reference to 3.0+HS		
4.0	24Mbit/s	Reference to 4.0 LE		
4.2	60Mbit/s	Reference to 4.2 LE		

Reference specifications are listed below:

- Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 + HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009
- Bluetooth Low Energy RF PHY Test Specification, Core_v4.2, December 12, 2014

4.2.1. BT Performance

The following table lists the BT transmitting and receiving performance of SC600Y/SC600T module.

Table 32: BT Transmitting and Receiving Performance

Transmitter Performance			
Packet Types	DH5	2-DH5	3-DH5
Transmitting Power	10dBm±2.5dB	8dBm±2.5dB	8dBm±2.5dB
Receiver Performance			
Packet Types	DH5	2-DH5	3-DH5
Receiving Sensitivity	-90dBm	-90dBm	-85dBm

5 GNSS

SC600Y/SC600T integrates a Qualcomm IZat™ GNSS engine (Gen 8C) which supports multiple positioning and navigation systems including GPS, GLONASS and BeiDou. With an embedded LNA, the module provides greatly improved positioning accuracy.

5.1. GNSS Performance

The following table lists the GNSS performance of SC600Y/SC600T module in conduction mode.

Table 33: GNSS Performance

Parameter	Description	Typ.	Unit
Sensitivity (GNSS)	Cold start	-142	dBm
	Reacquisition	-153	dBm
	Tracking	-153	dBm
TTFF (GNSS)	Cold start	86	s
	Warm start	70	s
	Hot start	<10	s
Static Drift (GNSS)	CEP-50	<80	m

5.2. GNSS RF Design Guidelines

Bad design of antenna and layout may cause reduced GNSS receiving sensitivity, longer GNSS positioning time, or reduced positioning accuracy. In order to avoid these, please follow the design rules listed below:

- Maximize the distance between the GNSS RF part and the GPRS RF part (including trace routing and antenna layout) to avoid mutual interference.
- In user systems, GNSS RF signal lines and RF components should be placed far away from high speed circuits, switched-mode power supplies, power inductors, the clock circuit of single-chip microcomputers, etc.
- For applications with harsh electromagnetic environment or high ESD-protection requirements, it is recommended to add ESD protective diodes for the antenna interface. Only diodes with ultra-low junction

capacitance such as 0.5pF can be selected. Otherwise, there will be effects on the impedance characteristic of RF circuit loop, or attenuation of bypass RF signal may be caused.

- Control the impedance of either feeder line or PCB trace as 50Ω, and keep the trace length as short as possible.
- Refer to ***Chapter 6.3*** for GNSS antenna reference circuit designs.

6 Antenna Interfaces

SC600Y/SC600T provides five antenna interfaces for main antenna, Rx-diversity/MIMO antenna, GNSS antenna, Wi-Fi/BT antenna and FM antenna respectively. The antenna ports have an impedance of 50Ω.

6.1. Main/Rx-diversity Antenna Interfaces

The pin definition of main/Rx-diversity antenna interfaces is shown below.

Table 34: Pin Definition of Main/Rx-diversity Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	19	AI/AO	Main antenna interface	50Ω impedance
ANT_DRX	149	AI	Diversity and MIMO antenna interface	50Ω impedance

The operating frequencies of SC600Y/SC600T module are listed in the following table.

删除的内容: **Table 35: SC600Y-JP/SC600T-JP Operating Frequencies 3GPP Band** ... [9]

6.2. Wi-Fi/BT/FM Antenna Interface

The pin definition of Wi-Fi/BT/FM antenna interfaces and operating frequencies is shown below.

Table 35: Pin Definition of Wi-Fi/BT/FM Antenna Interface

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Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI/BT	129	AI/AO	Wi-Fi/BT antenna interface	50Ω impedance
ANT_FM	244	AI	FM antenna interface	50Ω impedance

Table 36: Wi-Fi/BT/FM Frequency

删除的内容: 39

Type	Frequency	Unit
802.11a/b/g/n/ac	2402~2482 5180~5825	MHz
BT4.2 LE	2402~2480	MHz
FM	76~108	MHz

A reference circuit design for Wi-Fi/BT/FM antenna interface is shown below. A π-type matching circuit is recommended to be reserved for better RF performance. The capacitors are not mounted by default and resistors are 0Ω.

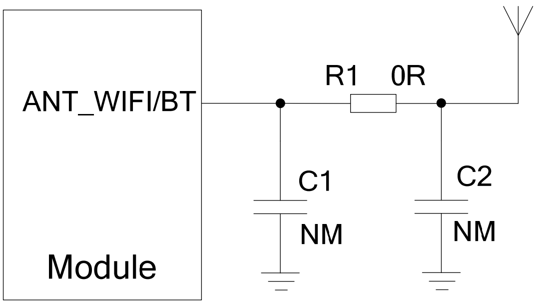

Figure 33: Reference Circuit Design for Wi-Fi/BT Antenna Interface

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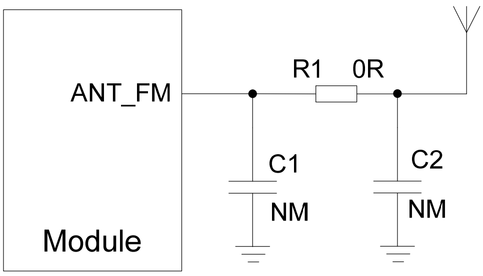

Figure 34: Reference Circuit Design for FM Antenna Interface

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6.3. GNSS Antenna Interface

The pin definition of GNSS antenna interfaces and operating frequencies is shown below.

Table 37: Pin Definition of GNSS Antenna

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Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	134	AI	GNSS antenna Interface	50Ω impedance
GNSS_LNA_EN	202	DO	LNA enable control	For test purpose only. If unused, keep it open.

Table 38: GNSS Frequ

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ency

Type	Frequency	Unit
GPS	1575.42±1.023	MHz
GLONASS	1597.5~1605.8	MHz
BeiDou	1561.098±2.046	MHz

6.3.1. Recommended Circuit for Passive Antenna

GNSS antenna interface supports passive ceramic antennas and other types of passive antennas. A reference circuit design is given below.

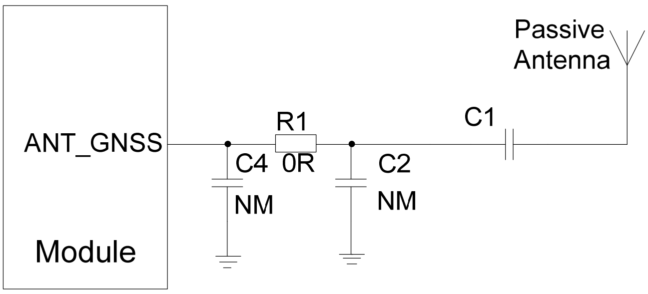

Figure 35: Reference Circuit Design for GNSS Passive Antenna

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NOTE

passive antenna is placed far away from the module (that is, the antenna trace is long), it is recommended to add an external LNA circuit for better GNSS receiving performance, and the LNA should be placed close to the antenna.

6.3.2. Recommended Circuit for Active Antenna

The active antenna is powered by a 56nH inductor through the antenna's signal path. The common power supply voltage ranges from 3.3V to 5.0V. Although featuring low power consumption, the active antenna still requires stable and clean power supplies. It is recommended to use high performance LDO as the power supply. A reference design of GNSS active antenna is shown below.

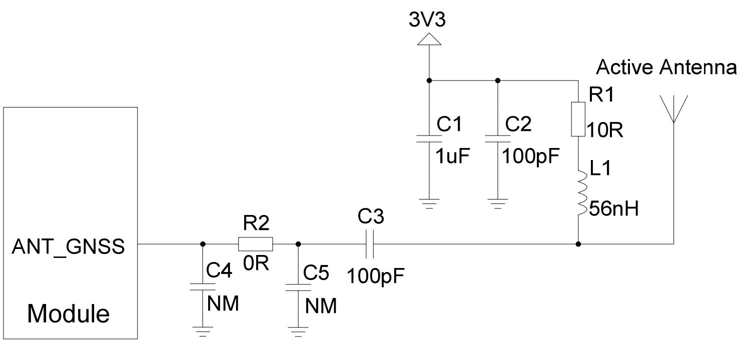

Figure 36: Reference Circuit Design for GNSS Active Antenna

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6.4. Antenna Installation

6.4.1. Antenna Requirements

The following table shows the requirements on main antenna, Rx-diversity, Wi-Fi/BT antenna and GNSS antenna.

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Table 39: Antenna Requirements

带格式表格

删除的内容: GSM/WCDMA/ LTE ... [10]

Antenna Type	Requirements
Wi-Fi/BT	VSWR: ≤2 Gain (dBi): 1 Max Input Power (W): 50 Input Impedance (Ω): 50 Polarization Type: Vertical Cable Insertion Loss: <1dB
GNSS [1]	Frequency range: 1559MHz~1609MHz Polarization: RHCP or linear VSWR: <2 (Typ.) Passive Antenna Gain: >0dBi Active Antenna Noise Figure: <1.5dB (Typ.) Active Antenna Gain: >-2dBi Active Antenna Embedded LNA Gain: <17dB (Typ.) Active Antenna Total Gain: <17dBi (Typ.)

NOTE

[1] It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

6.4.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by HIROSE.

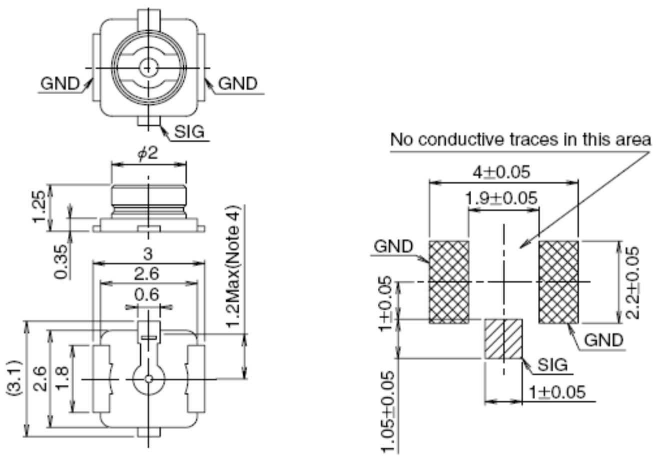


Figure 37: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

删除的内容: 42

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

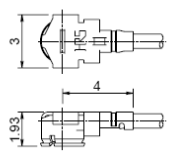
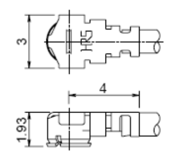
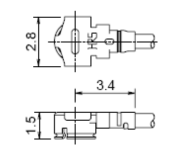
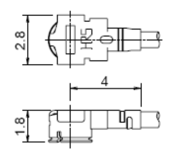
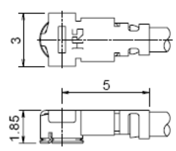
	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Part No.					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 38: Mechanicals of U.FL-LP Connectors

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The following figure describes the space factor of mated connector.

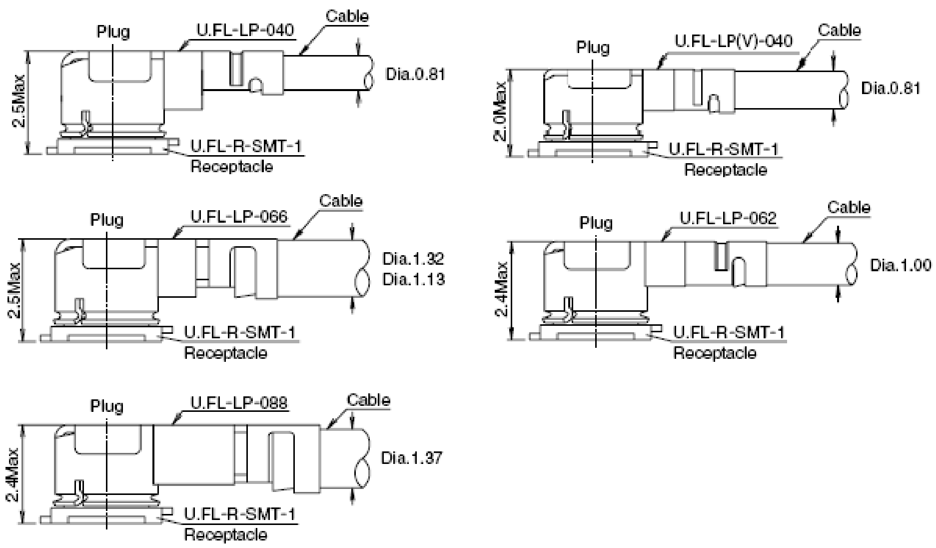

Figure 39: Space Factor of Mated Connector (Unit: mm)

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For more details, please visit http://www.hirose.com.

Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the space between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

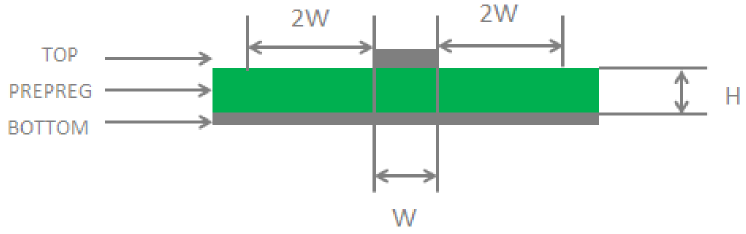

Figure 34: Microstrip Design on a 2-layer PCB

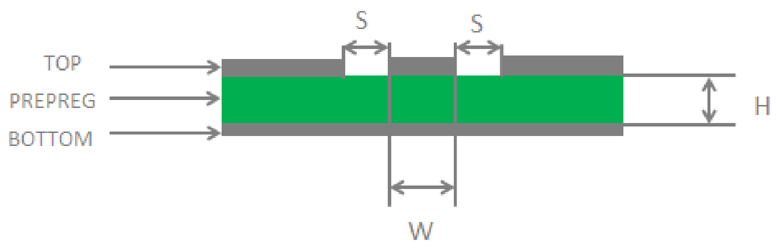

Figure 35: Coplanar Waveguide Design on a 2-layer PCB

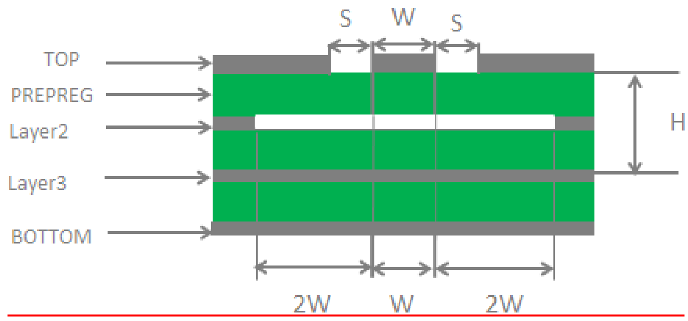

Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

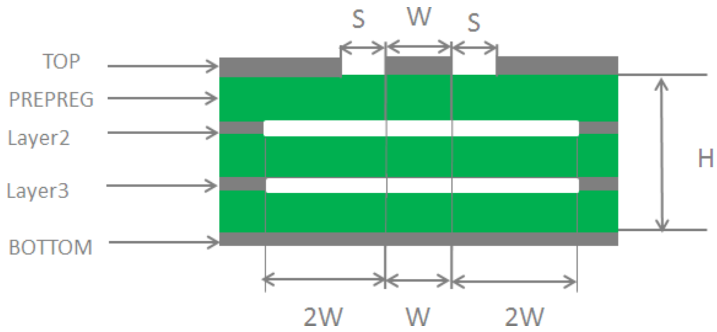

Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pins, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and

all the right-angle traces should be changed to curved ones.

- There should be clearance under the signal pin of the antenna connector or solder joint.

- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times as wide as RF signal traces (2 W).

带格式的: 列表段落, 列出段落, 缩进: 左侧: 2.49 厘米, 右侧: 1.51 厘米, 段落间距段前: 3.55 磅, 行距: 多倍行距 1.29 字行, 不调整西文与中文之间的空格, 不调整中文和数字之间的空格, 制表位: 3.62 字符, 左对齐 + 3.62 字符, 左对齐

带格式的: Quectel正文文本样式

带格式的: (中文) 中文(简体, 中国), (其他) 英语(美国)

7 Electrical, Reliability and Radio Characteristics

7.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

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Table 40: Absolute Maximum Ratings

Parameter	Min	Max	Unit
VBAT	-0.5	6	V
USB_VBUS	-0.3	16	V
Current on VBAT	0	3	A
Voltage on Digital Pins	-0.3	2.16	V

7.2. Power Supply Ratings

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Table 41: SC600Y/SC600T Power Supply Ratings

Parameter	Description	Conditions	Min	Typ.	Max	Unit
VBAT	VBAT	The actual input voltages must fall between the minimum and maximum values	3.55	3.8	4.4	V
	Voltage drop during transmitting burst	Maximum power control level at EGSM900			400	mV

I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level at EGSM900		1.8	3.0	A
USB_VBUS			4.0	5.0	10	V
VRTC	Power supply voltage of backup battery		2.0	3.0	3.25	V

7.3. Operation and Storage Temperatures

The operation and storage temperatures are listed in the following table.

Table 42: Operation and Storage Temperatures

Parameter	Min	Typ.	Max	Unit
Operating temperature range 1)	-35	+25	+65	°C
Extended temperature range 2)	-40		+75	°C
Storage temperature range	-40		+90	°C

NOTES

1. 1) Within operating temperature range, the module is 3GPP compliant.
2. 2) Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

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删除的内容: <#>Current Consumption

The current consumption of different conditions is listed in the following table.

删除的内容: Table 46: SC600Y-JP/SC600T-JP Current Consumption Parameter ... [1]

带格式表格

删除的内容: Table 49: SC600Y-JP/SC600T-JP RF Output Power Frequency

7.4. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it should be subject to ESD handling precautions that are typically applied to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the electrostatic discharge characteristics of SC600Y/SC600T module.

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Table 43: ESD Characteristics (Temperature: 25°C, Humidity: 45%)

Test Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	+/-5	+/-10	KV
All Antenna Interfaces	+/-5	+/-10	KV
Other Interfaces	+/-0.5	+/-1	KV

8 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimension tolerances are ±0.05mm unless otherwise specified.

8.1. Mechanical Dimensions of the Module

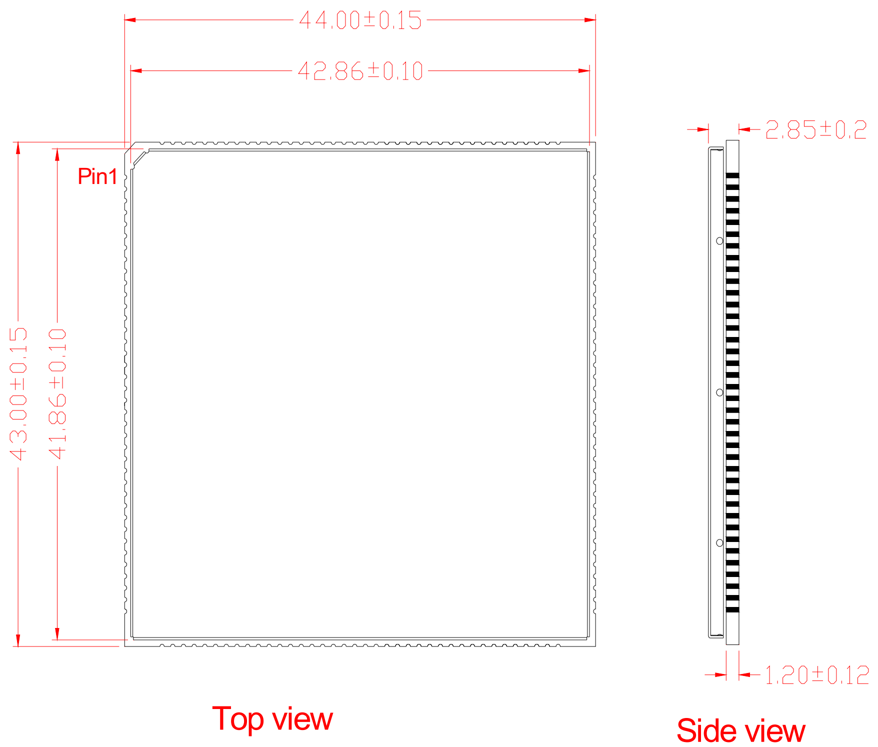

Figure 40: Module Top and Side Dimensions

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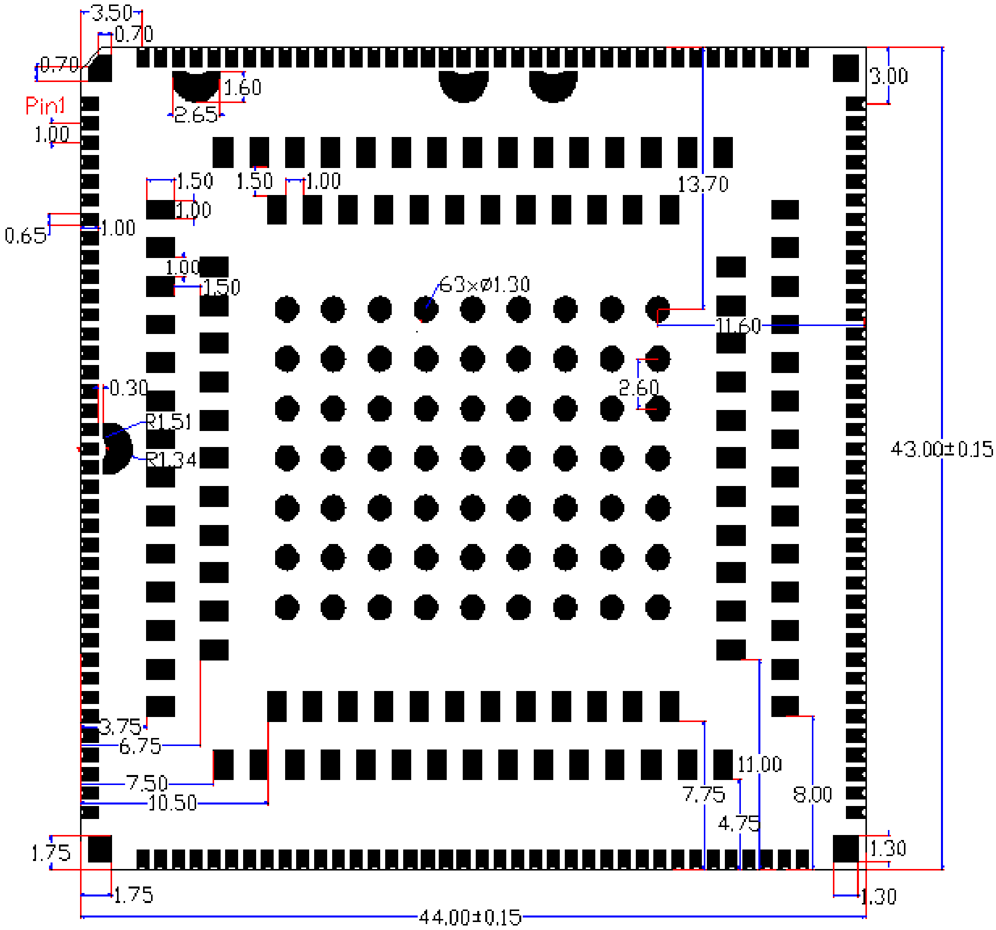

Figure 41: Module Bottom Dimensions (Top View)

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8.2. Recommended Footprint

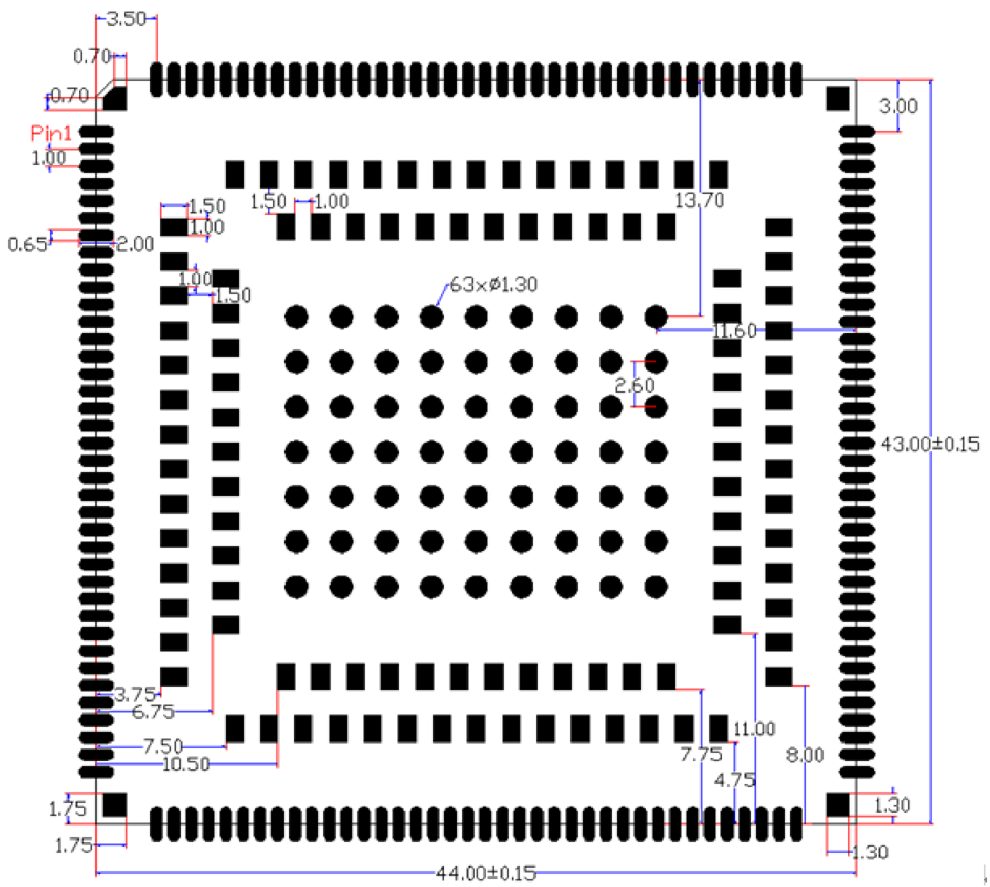

Figure 42: Recommended Footprint (Top View)

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NOTES

1. For easy maintenance of the module, keep about 3mm between the module and other components on host PCB.
2. All RESERVED pins should be kept open and MUST NOT be connected to ground.

8.3. Top and Bottom View of the Module

Figure 43: Top View of SC600Y/SC600T Module

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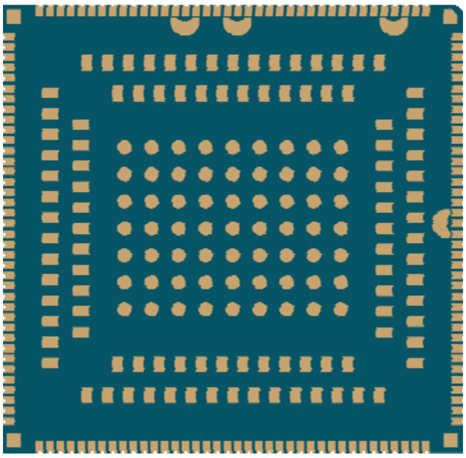

Figure 44: Bottom View of SC600Y/SC600T Module

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NOTE

These are renderings of SC600Y/SC600T module. For authentic appearance, please refer to the module that you receive from Quectel.

9 Storage, Manufacturing and Packaging

9.1. Storage

SC600Y/SC600T is stored in a vacuum-sealed bag. They are rated at MSL 3, and their storage restrictions are shown as below.

1. Shelf life in the vacuum-sealed bag: 12 months at <40ºC/90%RH.

2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:
   - Mounted within 168 hours at the factory environment of ≤30ºC/60%RH.
   - Stored at <10%RH.

3. Devices require baking before mounting, if any circumstance below occurs.
   - When the ambient temperature is 23ºC±5ºC and the humidity indication card shows the humidity is >10% before opening the vacuum-sealed bag.
   - Device mounting cannot be finished within 168 hours at factory conditions of ≤30ºC/60%RH.

4. If baking is required, devices may be baked for 8 hours at 120ºC±5ºC.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devices before high temperature (120ºC) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for baking procedure.

9.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18mm~0.20mm. It is recommended to slightly reduce the amount of solder paste for LGA pads, thus avoiding short-circuit. For more details, please refer to ***document [4]***.

It is suggested that the peak reflow temperature is 238°C~245ºC, and the absolute maximum reflow temperature is 245ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

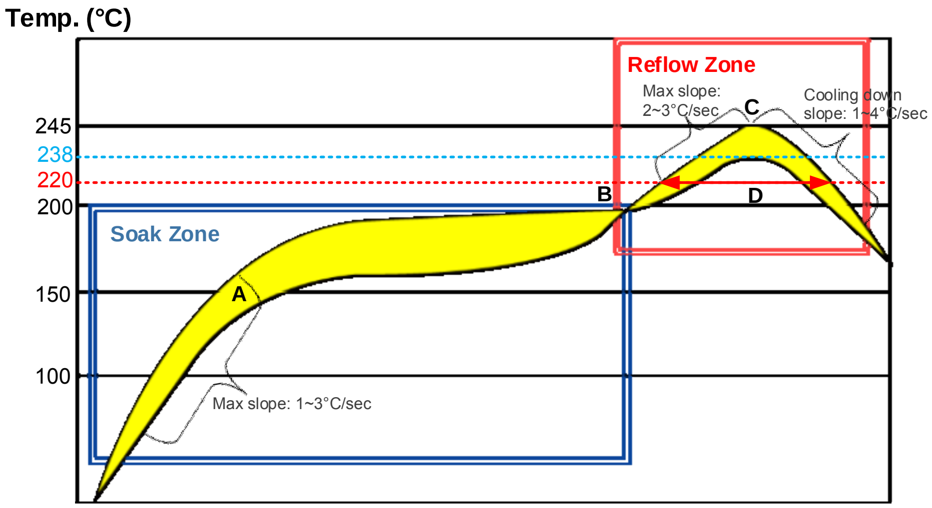

Figure 45: Recommended Reflow Soldering Thermal Profile

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Table 44: Recommended Thermal Profile Parameters

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Factor	Recommendation
Soak Zone	
Max slope	1 to 3°C/sec
Soak time (between A and B: 150°C and 200°C)	60 to 120 sec

Reflow Zone	
Max slope	2 to 3°C/sec
Reflow time (D: over 220°C)	40 to 60 sec
Max temperature	238°C ~ 245°C
Cooling down slope	1 to 4°C/sec
Reflow Cycle	
Max reflow cycle	1

9.3. Packaging

SC600Y/SC600T is packaged in tape and reel carriers. Each reel is 330mm in diameter and contains 200 modules. The following figures show the package details, measured in mm.

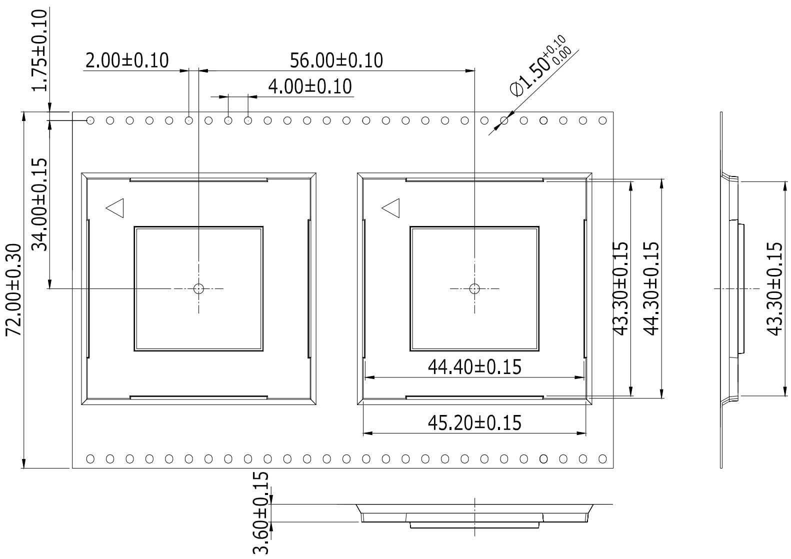

Figure 46: Tape Dimensions

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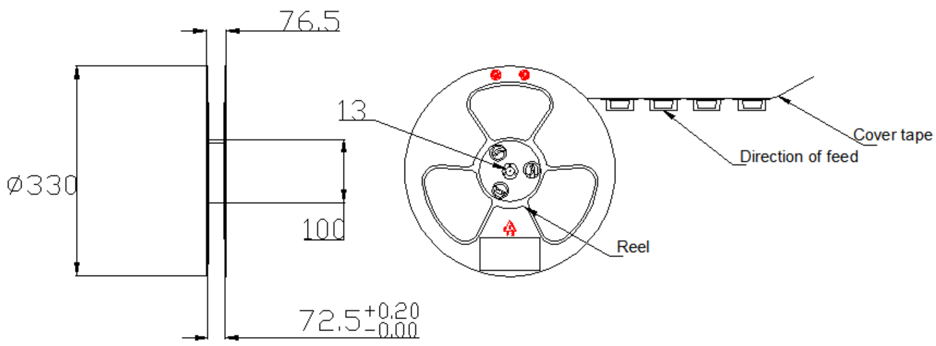

Figure 47: Reel Dimensions

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Table 45: Reel Packaging

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Model Name	MOQ for MP	Minimum Package: 200pcs	Minimum Package×4=800pcs
SC600Y/ SC600T	200	Size: 398mm × 383mm × 83mm N.W: 1.92kg G.W: 3.67kg	Size: 420mm × 350mm × 405mm N.W: 8.18kg G.W: 15.18kg

10 Appendix A References

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Table 46: Related Documents

SN	Document Name	Remark
[1]	Quectel_Smart_EVB-G2_User_Guide	EVB User Guide for SC600Y/SC600T
[2]	Quectel_SC600Y&SC600T_GPIO_Configuration	GPIO Configuration of SC600Y/SC600T
[3]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[4]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide
[5]	Quectel_ SC600Y&SC600T_Reference_Design	Reference Design for SC600Y/SC600T

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Table 47: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-rate
BLE	Bluetooth Low Energy
bps	Bits per Second
BR	Basic Rate
EDR	Enhanced Data Rate
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DL	Downlink

DRX	Discontinuous Reception
EFR	Enhanced Full Rate
ESR	Equivalent Series Resistance
ESD	Electrostatic Discharge
ERM	Eccentric Rotating Mass
FR	Full Rate
GLONASS	Globalnaya Navigazionnaya Sputnikovaya Sistema, the Russian Global Navigation Satellite System
GPS	Global Positioning System
GPU	Graphics Processing Unit
HR	Half Rate
IO	Input / Output
IQ	Inphase and Quadrature
ISP	Image Signal Processing
LCD	Liquid Crystal Display
LCM	LCD Module
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LRA	Linear Resonant Actuator
MIPI	Mobile Industry Processor Interface
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PMI	Power Management Interface
PMU	Power Management Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation

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删除的内容: GMSK ... [14]
删除的内容: GSM ... [15]
删除的内容: HSDPA ... [16]
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RF	Radio Frequency
RH	Relative Humidity
RHCP	Right Hand Circularly Polarized
RTC	Real Time Clock
Rx	Receive
SMS	Short Message Service
TE	Terminal Equipment
TX	Transmitting Direction
UART	Universal Asynchronous Receiver & Transmitter
UL	Uplink
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_I	Voltage Input
V_{IH}min	Minimum Input High Level Voltage Value

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删除的内容: V_{IL}max ... [20]

FCC Certification Requirements.

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.

And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based time-averaging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.

2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

3.A label with the following statements must be attached to the host end product: This device contains FCC ID: XMR201911SC600WF.

4. This module must not transmit simultaneously with any other antenna or transmitter

5. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

For this device, OEM integrators must be provided with labeling instructions of finished products. Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module:"Contains Transmitter Module FCC ID: XMR201911SC600WF" or "Contains FCC ID: XMR201911SC600WF" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

带格式的：缩进：左侧： 0 厘米

§15.19 Labeling requirements.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

§15.21 Information to user.

The users manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment

带格式的: 英语(美国)

带格式的: 缩进: 左侧: 0 厘米

带格式的: 缩进: 左侧: 0 厘米

带格式的: (中文) 中文(简体，中国), (其他) 英语(美国)

带格式的: Quectel正文文本样式

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LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B20/B28A/B28B
LTE-TDD	B38/B39/B40/B41
WCDMA	B1/B2/B4/B5/B8
GSM	850/900/1800/1900MHz

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LTE-FDD	B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/B66/B71
LTE-TDD	B41
WCDMA	B2/B4/B5
GSM	/

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LTE-FDD	B1/B3/B5/B8/B11/B18/B19/B21/B26/B28A/B28B
LTE-TDD	B41
WCDMA	B1/B6/B8/B19
GSM	/

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LTE-FDD	/
LTE-TDD	/
WCDMA	/
GSM	/

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Memory	16GB eMMC + 2GB LPDDR3 (default) 32GB eMMC + 3GB LPDDR3 (optional) 64GB eMMC + 4GB LPDDR3 (optional)

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Transmitting Power	Class 4 (33dBm±2dB) for GSM850 Class 4 (33dBm±2dB) for EGSM900 Class 1 (30dBm±2dB) for DCS1800 Class 1 (30dBm±2dB) for PCS1900 Class E2 (27dBm±3dB) for GSM850 8-PSK Class E2 (27dBm±3dB) for EGSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class E2 (26dBm±3dB) for PCS1900 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (23dBm±2dB) for LTE-FDD bands Class 3 (23dBm±2dB) for LTE-TDD bands
LTE Features	Support 3GPP R10 Cat 6 and Cat 4 Support 1.4 to 20MHz RF bandwidth Support Multiuser MIMO in DL direction Cat 6 FDD: Max 300Mbps (DL)/Max 50Mbps (UL) Cat 6 TDD: Max 265Mbps (DL)/Max 30Mbps (UL) Cat 4 FDD: Max 150Mbps (DL)/Max 50Mbps (UL) Cat 4 TDD: Max 130Mbps (DL)/Max 30Mbps (UL)

UMTS Features	Support 3GPP R9 DC-HSDPA/DC-HSUPA/HSPA+/HSDPA/HSUPA/WCDMA Support QPSK, 16-QAM and 64-QAM modulation DC-HSDPA: Max 42Mbps (DL) DC-HSUPA: Max 11.2Mbps (UL) WCDMA: Max 384Kbps (DL)/Max 384Kbps (UL)
GSM Features	**R99** CSD: 9.6kbps, 14.4kbps **GPRS** Support GPRS multi-slot class 33 (33 by default) Coding scheme: CS-1, CS-2, CS-3 and CS-4 Max 107Kbps (DL), 85.6Kbps (UL) **EDGE** Support EDGE multi-slot class 33 (33 by default) Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: CS 1-4 and MCS 1-9 Uplink coding schemes: CS 1-4 and MCS 1-9 Max 296Kbps (DL), 236.8Kbps (UL)

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Table 35: SC600Y-JP/SC600T-JP Operating Frequencies

3GPP Band	Receive	Transmit	Unit
WCDMA B1	2110~2170	1920~1980	MHz
WCDMA B6	875~885	830~840	MHz
WCDMA B8	925~960	880~915	MHz
WCDMA B19	875~890	830~845	MHz
LTE-FDD B1	2110~2170	1920~1980	MHz
LTE-FDD B3	1805~1880	1710~1785	MHz
LTE-FDD B5	869~894	824~849	MHz
LTE-FDD B8	925~960	880~915	MHz
LTE-FDD B11	1476~496	1428~1448	MHz
LTE-FDD B18	860~875	815~830	MHz
LTE-FDD B19	875~890	830~845	MHz

LTE-TDD B26	758~788	703~733	MHz
LTE-FDD B28A	758~788	703~733	MHz
LTE-FDD B28B	773~803	718~748	MHz
LTE-TDD B41 1)	2496~2690	2496~2690	MHz

Table 36: SC600Y-EM/SC600T-EM Operating Frequencies

3GPP Band	Receive	Transmit	Unit
GSM850	869~894	824~849	MHz
EGSM900	925~960	880~915	MHz
DCS1800	1805~1880	1710~1785	MHz
PCS1900	1930~1990	1850~1910	MHz
WCDMA B1	2110~2170	1920~1980	MHz
WCDMA B2	1930~1990	1850~1910	MHz
WCDMA B4	2110~2155	1710~1755	MHz
WCDMA B5	869~894	824~849	MHz
WCDMA B8	925~960	880~915	MHz
LTE-FDD B1	2110~2170	1920~1980	MHz
LTE-FDD B2	1930~1990	1850~1910	MHz
LTE-FDD B3	1805~1880	1710~1785	MHz
LTE-FDD B5	869~894	824~849	MHz
LTE-FDD B7	2620~2690	2500~2570	MHz
LTE-FDD B8	925~960	880~915	MHz
LTE-FDD B20	791~821	832~862	MHz
LTE-FDD B28A	758~788	703~733	MHz

LTE-FDD B28B	773~803	718~748	MHz
LTE-TDD B38	2570~2620	2570~2620	MHz
LTE-TDD B39	1880~1920	1880~1920	MHz
LTE-TDD B40	2300~2400	2300~2400	MHz
LTE-TDD B41 [1)]	2496~2690	2496~2690	MHz

Table 37: SC600Y-NA/SC600T-NA Operating Frequencies

3GPP Band	Receive	Transmit	Unit
WCDMA B2	1930~1990	1850~1910	MHz
WCDMA B4	2110~2155	1710~1755	MHz
WCDMA B5	869~894	824~849	MHz
LTE-FDD B2	1930~1990	1850~1910	MHz
LTE-FDD B4	2110~2155	1710~1755	MHz
LTE-FDD B5	869~894	824~849	MHz
LTE-FDD B7	2620~2690	2500~2570	MHz
LTE-FDD B12	729~746	699~716	MHz
LTE-FDD B13	746~756	777~787	MHz
LTE-FDD B14	758~768	788~798	MHz
LTE-FDD B17	734~746	704~716	MHz
LTE-FDD B25	1930~1995	1850~1915	MHz
LTE-FDD B26	859~894	814~849	MHz
LTE-FDD B66	2110~2200	1710~1780	MHz
LTE-FDD B71	617 – 652	663 – 698	MHz
LTE-TDD B41 [1)]	2496~2690	2496~2690	MHz

NOTE

[1] The bandwidth of LTE-TDD B41 for SC600Y-EM/SC600T-EM, SC600Y-JP/SC600T-JP, SC600Y-NA/SC600T-NA is 200MHz (2496MHz~2690MHz), and the corresponding channel ranges from 39650 to 41589.

Main and Rx-diversity Antenna Interfaces Reference Design

A reference circuit design for main and Rx-diversity antenna interfaces is shown as below. A π-type matching circuit should be reserved for better RF performance, and the π-type matching components (R1/C1/C2, R2/C3/C4) should be placed as close to the antennas as possible. The capacitors are not mounted by default and resistors are 0Ω.

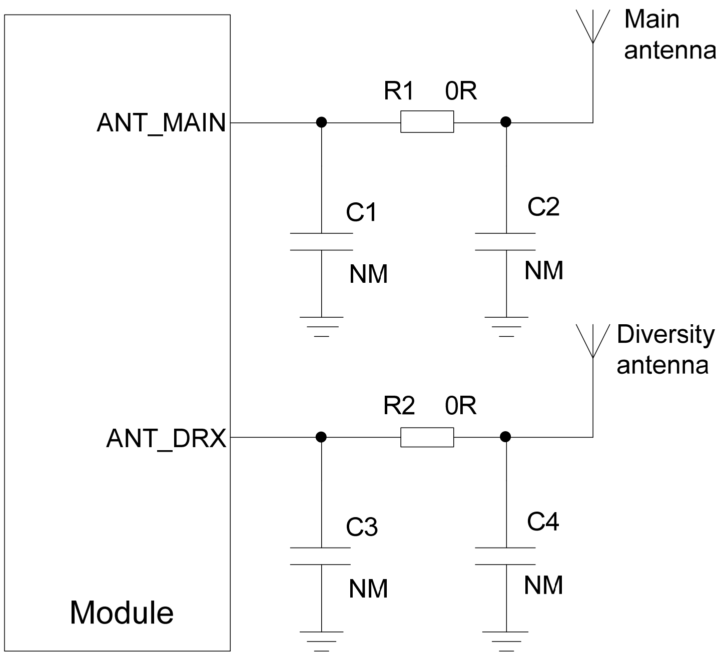

Figure 33: Reference Circuit Design for Main and Rx-diversity Antenna Interfaces

Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the space between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic structures.

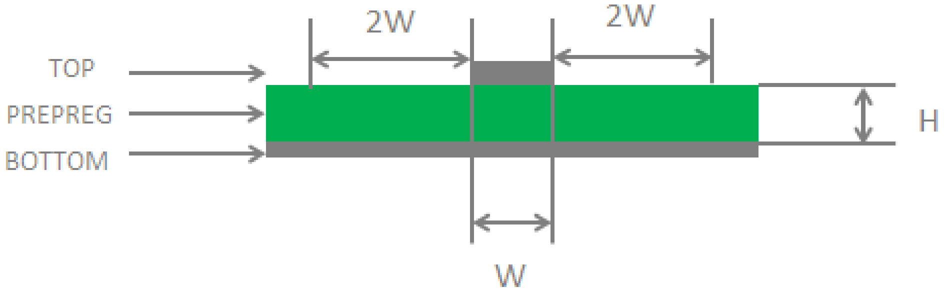

Figure 34: Microstrip Design on a 2-layer PCB

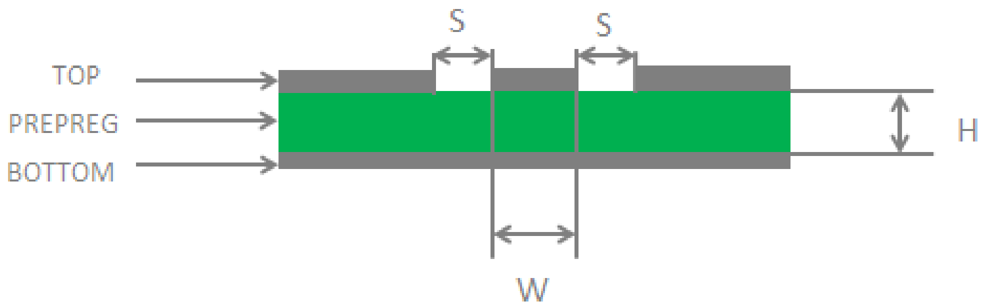

Figure 35: Coplanar Waveguide Design on a 2-layer PCB

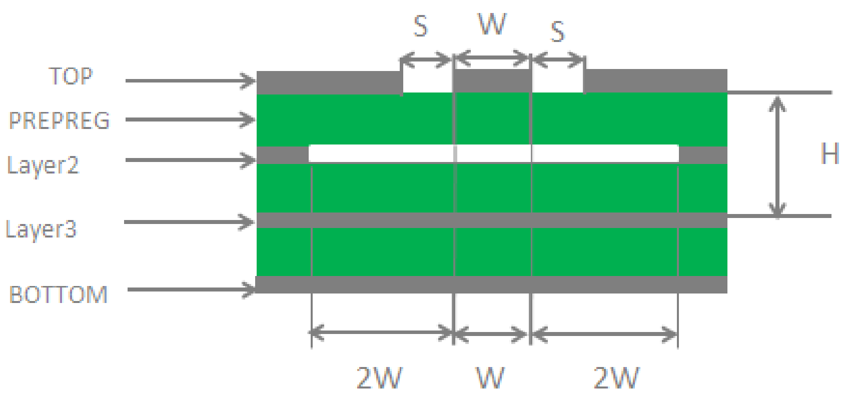

Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

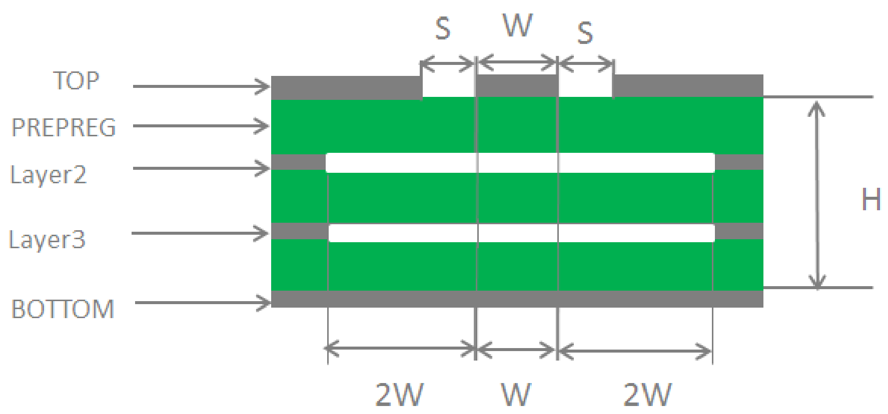

Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50Ω.
The GND pins adjacent to RF pins should not be designed as thermal relief pins, and should be fully connected to ground.
The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
There should be clearance under the signal pin of the antenna connector or solder joint.
The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times as wide as RF signal traces (2 × W).

For more details about RF layout, please refer to ***document [3]***.

页 **102: [10]** 删除的内容	**dell**	**2019/12/6 9:42:00**

GSM/WCDMA/ LTE	VSWR:≤2 Gain (dBi): 1 Max Input Power (W): 50 Input Impedance (Ω): 50 Polarization Type: Vertical Cable Insertion Loss: <1dB (GSM850, EGSM900, WCDMA B5/B6/B8/B19, LTE B5/B8/B12/B13/B14/B17/B18/B19/B20/B26/B28A/B28B/B71) Cable Insertion Loss: <1.5dB (DCS1800, PCS1900, WCDMA B1/B2/B4,

Cable Insertion Loss: <2dB (LTE-FDD B7, LTE-TDD B38/B40/B41)

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Table 46: SC600Y-JP/SC600T-JP Current Consumption

Parameter	Description	Conditions	Min	Typ.	Max	Unit
I_{VBAT}	OFF state	Power down		80		uA
	WCDMA supply current	Sleep (USB disconnected) @DRX=6		4.57		mA
		Sleep (USB disconnected) @DRX=8		3.1		mA
		Sleep (USB disconnected) @DRX=9		3.0		mA
	LTE-FDD supply current	Sleep (USB disconnected) @DRX=6		4.13		mA
		Sleep (USB disconnected) @DRX=8		3.15		mA
	LTE-TDD supply current	Sleep (USB disconnected) @DRX=6		3.95		mA
		Sleep (USB disconnected) @DRX=8		3.03		mA
	WCDMA voice call	B1 @max power		597		mA
		B6 @max power		620		mA
		B8 @max power		584		mA
		B19 @max power		610		mA
	WCDMA data transfer	B1 (HSDPA) @max power		550		mA
		B6 (HSDPA) @max power		580		mA
		B8 (HSDPA) @max power		550		mA
		B19 (HSDPA) @max power		580		mA
		B1 (HSUPA) @max power		562		mA
		B6 (HSUPA) @max power		595		mA

		B19 (HSUPA) @max power		600		mA
	LTE data transfer	LTE-FDD B1 @max power		570		mA
		LTE-FDD B3 @max power		610		mA
		LTE-FDD B5 @max power		530		mA
		LTE-FDD B8 @max power		540		mA
		LTE-TDD B11 @max power		550		mA
		LTE-TDD B18 @max power		595		mA
		LTE-TDD B19 @max power		540		mA
		LTE-TDD B21 @max power		560		mA
		LTE-TDD B26 @max power		570		mA
		LTE-TDD B28A @max power		680		mA
		LTE-TDD B28B @max power		625		mA
		LTE-TDD B41 @max power		530		mA

Table 47: SC600Y-EM/SC600T-EM Current Consumption

Parameter	Description	Conditions	Min	Typ.	Max	Unit
I_{VBAT}	OFF state	Power down		80		uA
	GSM supply current	Sleep (USB disconnected) @DRX=2		4.5		mA
		Sleep (USB disconnected) @DRX=5		3.5		mA
		Sleep (USB disconnected) @DRX=9		3		mA
	WCDMA supply current	Sleep (USB disconnected) @DRX=6		3.47		mA
		Sleep (USB disconnected) @DRX=8		3.11		mA
		Sleep (USB disconnected) @DRX=9		2.75		mA
	LTE-FDD supply	Sleep (USB disconnected)				

		Sleep (USB disconnected) @DRX=8	2.96	mA
	LTE-TDD supply current	Sleep (USB disconnected) @DRX=6	4.27	mA
		Sleep (USB disconnected) @DRX=8	3.17	mA
	GSM voice call	GSM850 @PCL 5	280	mA
		GSM850 @PCL 12	125	mA
		GSM850 @PCL 19	110	mA
		EGSM900 @PCL 5	280	mA
		EGSM900 @PCL 12	120	mA
		EGSM900 @PCL 19	100	mA
		DCS1800 @PCL 0	210	mA
		DCS1800 @PCL 7	140	mA
		DCS1800 @PCL 15	130	mA
		PCS1900 @PCL 0	210	mA
		PCS1900 @PCL 7	130	mA
		PCS1900 @PCL 15	125	mA
	WCDMA voice call	B1 @max power	620	mA
		B2 @max power	550	mA
		B4 @max power	580	mA
		B5 @max power	590	mA
		B8 @max power	560	mA
	GPRS data transfer	GSM850 (1UL/4DL) @PCL 5	240	mA
		GSM850 (2UL/3DL) @PCL 5	370	mA
		GSM850 (3UL/2DL) @PCL 5	440	mA
		GSM850 (4UL/1DL) @PCL 5	500	mA

	EGSM900 (2UL/3DL) @PCL 5	380	mA
	EGSM900 (3UL/2DL) @PCL 5	490	mA
	EGSM900 (4UL/1DL) @PCL 5	520	mA
	DCS1800 (1UL/4DL) @PCL 0	190	mA
	DCS1800 (2UL/3DL) @PCL 0	280	mA
	DCS1800 (3UL/2DL) @PCL 0	350	mA
	DCS1800 (4UL/1DL) @PCL 0	420	mA
	PCS1900 (1UL/4DL) @PCL 0	190	mA
	PCS1900 (2UL/3DL) @PCL 0	290	mA
	PCS1900 (3UL/2DL) @PCL 0	370	mA
	PCS1900 (4UL/1DL) @PCL 0	420	mA
EDGE data transfer	GSM850 (1UL/4DL) @PCL 8	170	mA
	GSM850 (2UL/3DL) @PCL 8	250	mA
	GSM850 (3UL/2DL) @PCL 8	320	mA
	GSM850 (4UL/1DL) @PCL 8	370	mA
	EGSM900 (1UL/4DL) @PCL 8	170	mA
	EGSM900 (2UL/3DL) @PCL 8	260	mA
	EGSM900 (3UL/2DL) @PCL8	340	mA
	EGSM900 (4UL/1DL) @PCL 8	380	mA
	DCS1800 (1UL/4DL) @PCL 2	170	mA
	DCS1800 (2UL/3DL) @PCL 2	260	mA
	DCS1800 (3UL/2DL) @PCL 2	330	mA
	DCS1800 (4UL/1DL) @PCL 2	400	mA
	PCS1900 (1UL/4DL) @PCL 2	170	mA
	PCS1900 (2UL/3DL) @PCL 2	260	mA

		PCS1900 (3UL/2DL) @PCL 2	400	mA
		PCS1900 (4UL/1DL) @PCL 2	410	mA
	WCDMA data transfer	B1 (HSDPA) @max power	550	mA
		B2 (HSDPA) @max power	510	mA
		B4 (HSDPA) @max power	530	mA
		B5 (HSDPA) @max power	550	mA
		B8 (HSDPA) @max power	510	mA
		B1 (HSUPA) @max power	580	mA
		B2 (HSUPA) @max power	530	mA
		B4 (HSUPA) @max power	550	mA
		B5 (HSUPA) @max power	520	mA
		B8 (HSUPA) @max power	520	mA
	LTE data transfer	LTE-FDD B1 @max power	550	mA
		LTE-FDD B2 @max power	530	mA
		LTE-FDD B3 @max power	650	mA
		LTE-FDD B4 @max power	530	mA
		LTE-FDD B5 @max power	560	mA
		LTE-FDD B7 @max power	680	mA
		LTE-FDD B8 @max power	550	mA
		LTE-FDD B20 @max power	530	mA
		LTE-FDD B28A @max power	580	mA
		LTE-FDD B28B @max power	570	mA
		LTE-TDD B38 @max power	600	mA
		LTE-TDD B39 @max power	420	mA
		LTE-TDD B40 @max power	430	mA

		LTE-TDD B41 @max power		580		mA

Table 48: SC600Y-NA/SC600T-NA Current Consumption

Parameter	Description	Conditions	Min	Typ.	Max	Unit
I_{VBAT}	OFF state	Power down		80		uA
	WCDMA supply current	Sleep (USB disconnected) @DRX=6		3.72		mA
		Sleep (USB disconnected) @DRX=8		3.08		mA
		Sleep (USB disconnected) @DRX=9		2.60		mA
	LTE-FDD supply current	Sleep (USB disconnected) @DRX=6		3.84		mA
		Sleep (USB disconnected) @DRX=8		3.0		mA
	LTE-TDD supply current	Sleep (USB disconnected) @DRX=6		4.19		mA
		Sleep (USB disconnected) @DRX=8		2.99		mA
	WCDMA voice call	B2 @max power		600		mA
		B4@max power		600		mA
		B5 @max power		540		mA
	WCDMA data transfer	B2 (HSDPA) @max power		570		mA
		B4 (HSDPA) @max power		580		mA
		B5 (HSDPA) @max power		530		mA
		B2 (HSUPA) @max power		590		mA
		B4 (HSUPA) @max power		585		mA
		B5 (HSUPA) @max power		530		mA
	LTE data transfer	LTE-FDD B2 @max power		590		mA
		LTE-FDD B4 @max power		640		mA

	LTE-FDD B7 @max power	710	mA
	LTE-FDD B12 @max power	520	mA
	LTE-FDD B13 @max power	540	mA
	LTE-TDD B14 @max power	560	mA
	LTE-TDD B17 @max power	470	mA
	LTE-TDD B25 @max power	530	mA
	LTE-TDD B26 @max power	590	mA
	LTE-TDD B66 @max power	620	mA
	LTE-TDD B71 @max power	580	mA
	LTE-TDD B41 @max power	450	mA

RF Output Power

The following table shows the RF output power of SC600Y/SC600T module.

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Table 49: SC600Y-JP/SC600T-JP RF Output Power

Frequency	Max	Min
WCDMA B1	**24dBm+1/-3dB**	**<-49dBm**
WCDMA B6	**24dBm +1/-3dB**	**<-49dBm**
WCDMA B8	**24dBm +1/-3dB**	**<-49dBm**
WCDMA B19	**24dBm +1/-3dB**	**<-49dBm**
LTE-FDD B1	**23dBm±2dB**	**<-39dBm**
LTE-FDD B3	**23dBm±2dB**	**<-39dBm**
LTE-FDD B5	**23dBm±2dB**	**<-39dBm**

LTE-FDD B11	**23dBm±2dB**	**<-39dBm**
LTE-FDD B18	**23dBm±2dB**	**<-39dBm**
LTE-FDD B19	**23dBm±2dB**	**<-39dBm**
LTE-FDD B21	**23dBm±2dB**	**<-39dBm**
LTE-FDD B26	**23dBm±2dB**	**<-39dBm**
LTE-FDD B28A	**23dBm±2dB**	**<-39dBm**
LTE-FDD B28B	**23dBm±2dB**	**<-39dBm**
LTE-TDD B41	**23dBm±2dB**	**<-39dBm**

Table 50: SC600Y-EM/SC600T-EM RF Output Power

Frequency	Max	Min
GSM850	33dBm±2dB	5dBm±5dB
EGSM900	33dBm±2dB	5dBm±5dB
DCS1800	30dBm±2dB	0dBm±5dB
PCS1900	30dBm±2dB	0dBm±5dB
WCDMA B1	24dBm+1/-3dB	<-49dBm
WCDMA B2	24dBm+1/-3dB	<-49dBm
WCDMA B4	24dBm+1/-3dB	<-49dBm
WCDMA B5	24dBm+1/-3dB	<-49dBm
WCDMA B8	24dBm+1/-3dB	<-49dBm
LTE-FDD B1	23dBm±2dB	<-39dBm
LTE-FDD B2	23dBm±2dB	<-39dBm
LTE-FDD B3	23dBm±2dB	<-39dBm
LTE-FDD B4	23dBm±2dB	<-39dBm
LTE-FDD B5	23dBm±2dB	<-39dBm

LTE-FDD B8	23dBm±2dB	<-39dBm
LTE-FDD B20	23dBm±2dB	<-39dBm
LTE-FDD B28A	23dBm±2dB	<-39dBm
LTE-FDD B28B	23dBm±2dB	<-39dBm
LTE-TDD B38	23dBm±2dB	<-39dBm
LTE-TDD B39	23dBm±2dB	<-39dBm
LTE-TDD B40	23dBm±2dB	<-39dBm
LTE-TDD B41	23dBm±2dB	<-39dBm

Table 51: SC600Y-NA/SC600T-NA RF Output Power

Frequency	Max	Min
WCDMA B2	24dBm+1/-3dB	<-49dBm
WCDMA B4	24dBm+1/-3dB	<-49dBm
WCDMA B5	24dBm+1/-3dB	<-49dBm
LTE-FDD B2	23dBm±2dB	<-39dBm
LTE-FDD B4	23dBm±2dB	<-39dBm
LTE-FDD B5	23dBm±2dB	<-39dBm
LTE-FDD B7	23dBm±2dB	<-39dBm
LTE-FDD B12	23dBm±2dB	<-39dBm
LTE-FDD B13	23dBm±2dB	<-39dBm
LTE-FDD B14	23dBm±2dB	<-39dBm
LTE-FDD B17	23dBm±2dB	<-39dBm
LTE-FDD B25	23dBm±2dB	<-39dBm
LTE-FDD B26	23dBm±2dB	<-39dBm
LTE-FDD B66	23dBm±2dB	<-39dBm
LTE-FDD B71	23dBm±2dB	<-39dBm
LTE-TDD B41	23dBm±2dB	<-39dBm

NOTE

In GPRS 4 slots TX mode, the maximum output power is reduced by 3dB. This design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

RF Receiving Sensitivity

The following table shows the conducted RF receiving sensitivity of SC600Y/SC600T module.

Table 52: SC600Y-JP/SC600T-JP RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
WCDMA B1	-108.5	-109.5	-110.5	-106.7dBm
WCDMA B6	-109.5	-108	-111	-106.7dBm
WCDMA B8	-109.5	-109.5	-111	-104.7dBm
WCDMA B19	-109.5	-108	-110.5	-106.7dBm
LTE-FDD B1 (10M)	-97	-98	-99.5	-96.3dBm
LTE-FDD B3 (10M)	-97	-97	-99.5	-93.3dBm
LTE-FDD B5 (10M)	-97	-97	-99	-94.3dBm
LTE-FDD B8 (10M)	-97	-97	-99.5	-93.3dBm
LTE-FDD B11 (10M)	-96	-97	-99	-96.3dBm
LTE-FDD B18(10M)	-97	-98	-100	-96.3dBm
LTE-FDD B19 (10M)	-97	-98	-100	-96.3dBm
LTE-FDD B21(10M)	-97	-96.5	-99.5	-96.3dBm
LTE-FDD B26 (10M)	-97	-98	-100	-93.8dBm
LTE-FDD B28A (10M)	-95	-97	-98.5	-94.8dBm

LTE-TDD B41 (10M)	-95	-96	-98	-94.3dBm

Table 53: SC600Y-EM/SC600T-EM RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
GSM850	-109	/	/	-102.4dBm
EGSM900	-108	/	/	-102.4dBm
DCS1800	-107	/	/	-102.4dBm
PCS1900	-107	/	/	-102.4dBm
WCDMA B1	-109	-109	-110	-106.7dBm
WCDMA B2	-109	-109	-110	-106.7dBm
WCDMA B4	-109	-108.5	-110	-104.7dBm
WCDMA B5	-109.5	-108	-110.5	-104.7dBm
WCDMA B8	-109	-109	-110.5	-104.7dBm
LTE-FDD B1 (10M)	-97	-97	-100	-96.3dBm
LTE-FDD B2 (10M)	-97	-97	-100	-94.3dBm
LTE-FDD B3 (10M)	-96.5	-96.5	-99	-93.3dBm
LTE-FDD B4 (10M)	-97	-97	-100	-96.3dBm
LTE-FDD B5 (10M)	-97.5	-98	-100	-94.3dBm
LTE-FDD B7 (10M)	-96	-96	-99	-94.3dBm
LTE-FDD B8 (10M)	-97.5	-97.5	-100.5	-93.3dBm
LTE-FDD B20 (10M)	-96.5	-97.5	-100	-93.3dBm
LTE-FDD B28A (10M)	-97	-96.5	-99.5	-94.8dBm
LTE-FDD B28B (10M)	-97	-95.5	-99	-94.8dBm
LTE-TDD B38 (10M)	-96.5	-96	-99	-96.3dBm
LTE-TDD B39 (10M)	-97	-98	-100	-96.3dBm
LTE-TDD B40 (10M)	-96.5	-95.5	-99	-96.3dBm

Table 54: SC600Y-NA/SC600T-NA RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
WCDMA B2	-109	-109	-111	-106.7dBm
WCDMA B4	-109	-109	-110.5	-104.7dBm
WCDMA B5	-109.5	-109.5	-111	-104.7dBm
LTE-FDD B2 (10M)	-97	-97	-99.5	-94.3dBm
LTE-FDD B4 (10M)	-97	-96.5	-98.5	-96.3dBm
LTE-FDD B5 (10M)	-98	-97.5	-100	-94.3dBm
LTE-FDD B7 (10M)	-96	-96	-98	-94.3dBm
LTE-FDD B12 (10M)	-96	-97.5	-98.5	-93.3dBm
LTE-FDD B13 (10M)	-95.5	-97.5	-98	-93.3dBm
LTE-FDD B14 (10M)	-97	-97	-99	-93.3dBm
LTE-FDD B17 (10M)	-96	-97	-98	-93.3dBm
LTE-FDD B25 (10M)	-97	-97	-99	-92.8dBm
LTE-FDD B26 (10M)	-97.5	-98	-99.5	-93.8dBm
LTE-FDD B66 (10M)	-97	-96.5	-98.5	-95.8dBm
LTE-FDD B71 (10M)	-96.5	-96.5	-99	-93.5dBm
LTE-TDD B41 (10M)	-96	-96	-98	-94.3dBm

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EGSM	Extended GSM900 band (includes standard GSM900 band)

页 **119: [14]** 删除的内容	**dell**	**2019/12/6 10:22:00**

GMSK	Gaussian Minimum Shift Keying

页 **119: [15]** 删除的内容	**dell**	**2019/12/6 10:22:00**

GSM	Global System for Mobile Communications

页 **119: [16]** 删除的内容	**dell**	**2019/12/6 10:22:00**

HSDPA	High Speed Down Link Packet Access
HSPA	High Speed Packet Access

页 **119: [17]** 删除的内容	**dell**	**2019/12/6 10:22:00**

LTE-TDD	Long-Term Evolution Time-Division Duplex

页 **120: [18]** 删除的内容	**dell**	**2019/12/6 10:23:00**

TDD	Time Division Distortion

页 **120: [19]** 删除的内容	**dell**	**2019/12/6 10:23:00**

UMTS	Universal Mobile Telecommunications System

页 **120: [20]** 删除的内容	**dell**	**2019/12/6 10:21:00**

$V_{IL}max$	Maximum Input Low Level Voltage Value
V_O	Voltage Output
$V_{OH}min$	Minimum Output High Level Voltage Value
$V_{OL}max$	Maximum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLED	White Light-Emitting Diode

Appendix B GPRS Coding Schemes

Table 60: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

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Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 61: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA
14	4	4	NA

15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

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Appendix D EDGE Modulation and Coding Schemes

Table 62: EDGE Modulation and Coding Schemes

Coding Schemes	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1:	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2:	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3:	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4:	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.60kbps	35.20kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps