SC20 Hardware Design

Smart LTE Module Series

Rev: SC20_Hardware_Design_V1.0

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About the Document

History

Revision	Date	Author	Description
1.0	2019-12-03	Tony GAO	Initial

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OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part
15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text:
“Contains FCC ID: XMR201911SC20AL”
“Contains IC: 10224A-2019SC20AL “
The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and
(2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Industry Canada Statement

This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

The device could automatically discontinue transmission in case of absence of information to transmit, or operational failure. Note that this is not intended to prohibit transmission of control or signaling information or the use of repetitive codes where required by the technology.

The device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;
The maximum antenna gain permitted for devices in the bands 5250–5350 MHz and 5470–5725 MHz shall comply with the e.i.r.p. limit; and
The maximum antenna gain permitted for devices in the band 5725–5825 MHz shall comply with the e.i.r.p. limits specified for point-to-point and non point-to-point operation as appropriate.

L'appareil peut interrompre automatiquement la transmission en cas d'absence d'informations à transmettre ou de panne opérationnelle. Notez que ceci n'est pas destiné à interdire la transmission d'informations de contrôle ou de signalisation ou l'utilisation de codes répétitifs lorsque cela est requis par la technologie.

Le dispositif utilisé dans la bande 5150-5250 MHz est réservé à une utilisation en intérieur afin de réduire le risque de brouillage préjudiciable aux systèmes mobiles par satellite dans le même canal;
Le gain d'antenne maximal autorisé pour les dispositifs dans les bandes 5250-5350 MHz et 5470-5725 MHz doit être conforme à la norme e.r.p. limite; et
Le gain d'antenne maximal autorisé pour les appareils de la bande 5725-5825 MHz doit être conforme à la norme e.i.r.p. les limites spécifiées pour un fonctionnement point à point et non point à point, selon le cas.

CAN ICES-3(B)/ NMB-3(B)

Radiation Exposure Statement

This equipment complies with FCC/IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

1 Introduction

This document defines the SC20 module and its air interfaces and hardware interfaces which are connected with customers' application.

This document can help customers quickly understand module interface specifications, electrical and mechanical details as well as other related information of SC20 module. Associated with application note and user guide, customers can use SC20 module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating SC20 module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

	Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

SC20 is a series of Smart LTE module based on Qualcomm platform and Linux operating system, and provides industrial grade performance. Its general features are listed below:

- Support worldwide LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, TD-SCDMA, EVDO/CDMA, EDGE and GPRS coverage.
- Support short-range wireless communication via Wi-Fi 802.11a/b/g/n and BT4.2 LE.
- Integrate GPS/GLONASS/BeiDou satellite positioning systems.
- Support multiple audio and video codecs.
- Built-in high performance Adreno™ 304 graphics processing unit.
- Enable smooth play of 720P videos.
- Provide multiple audio and video input/output interfaces as well as abundant GPIO interfaces.

SC20 module contains six variants: SC20-CE R1.1, SC20-EL, SC20-AL, SC20-AUL and SC20-JL. The following tables show the supported frequency bands and network standards of SC20.

Table 1: SC20-CE R1.1 Frequency Bands

Type	Frequency
LTE-FDD	B1/B3/B5/B8
LTE-TDD	B38/B39/B40/B41
WCDMA	B1/B8
TD-SCDMA	B34/B39
EVDO/CDMA	BC0
GSM	900/1800MHz
Wi-Fi 802.11a/b/g/n	2400MHz~2482MHz 5180MHz~5825MHz

BT	2402MHz~2480MHz
GNSS	GPS: 1575.42MHz±1.023MHz GLONASS: 1597.5MHz~1605.8MHz BeiDou: 1561.098MHz±2.046MHz

Table 2: SC20-EL Frequency Bands

Type	Frequency
LTE-FDD	B1/B3/B5/B7/B8/B20
LTE-TDD	B38/B40/B41
WCDMA	B1/B5/B8
GSM	850/900/1800/1900MHz
Wi-Fi 802.11a/b/g/n	2400MHz~2482MHz 5180MHz~5825MHz
BT4.2 LE	2402MHz~2480MHz
GNSS	GPS: 1575.42MHz±1.023MHz GLONASS: 1597.5MHz~1605.8MHz BeiDou: 1561.098MHz±2.046MHz

Table 3: SC20-AL Frequency Bands

Type	Frequency
LTE-FDD	B2/B4/B5/B7/B12/B13/B25/B26
WCDMA	B1/B2/B4/B5/B8
GSM	850/1900MHz
Wi-Fi 802.11a/b/g/n	2400MHz~2482MHz 5180MHz~5825MHz
BT4.2 LE	2402MHz~2480MHz
GNSS	GPS: 1575.42MHz±1.023MHz GLONASS: 1597.5MHz~1605.8MHz BeiDou: 1561.098MHz±2.046MHz

Table 4: SC20-AUL Frequency Bands

Type	Frequency
LTE-FDD	B1/B3/B5/B7/B8/B28
LTE-TDD	B40
WCDMA	B1/B2/B5/B8
GSM	850/900/1800/1900MHz
Wi-Fi 802.11a/b/g/n	2400MHz~2482MHz 5180MHz~5825MHz
BT4.2 LE	2402MHz~2480MHz
GNSS	GPS: 1575.42MHz±1.023MHz GLONASS: 1597.5MHz~1605.8MHz BeiDou: 1561.098MHz±2.046MHz

Table 5: SC20-JL Frequency Bands

Type	Frequency
LTE-FDD	B1/B3/B8/B18/B19/B26
LTE-TDD	B41
WCDMA	B1/B6/B8/B19
Wi-Fi 802.11a/b/g/n	2400MHz~2496MHz 5180MHz~5825MHz
BT4.2 LE	2402MHz~2480MHz
GNSS	GPS: 1575.42MHz±1.023MHz GLONASS: 1597.5MHz~1605.8MHz BeiDou: 1561.098MHz±2.046MHz

SC20 is an SMD type module, which can be embedded into applications through its 210-pin pads including 146 LCC signal pads and 64 LGA pads. With a compact profile of 40.5mm × 40.5mm × 2.8mm, SC20 can meet almost all requirements for M2M applications such as CPE, wireless POS, smart metering, router, data card, automotive, smart phone, digital signage, alarm panel, security and industry PDA, etc.

2.2. Key Features

The following table describes the detailed features of SC20 module.

Table 6: SC20 Key Features

Feature	Details
Applications Processor	ARM Cortex-A7 microprocessor cores (quad-core) up to 1.1GHz 512KB L2 cache
Modem DSP	QDSP6 v5 core up to 691.2MHz 768KB L2 cache
Memory	8GB eMMC+8Gb LPDDR3
Operating System	Linux
Power Supply	Supply voltage: 3.5V~4.2V Typical supply voltage: 3.8V
Transmitting Power	Class 4 (33dBm±2dB) for GSM850 and EGSM900 Class 1 (30dBm±2dB) for DCS1800 and PCS1900 Class E2 (27dBm±3dB) for GSM850 and EGSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 and PCS1900 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (24dBm+3/-1dB) for EVDO/CDMA BC0 Class 2 (24dBm+1/-3dB) for TD-SCDMA bands Class 3 (23dBm±2dB) for LTE-FDD bands Class 3 (23dBm±2dB) for LTE-TDD bands
LTE Features	Support 3GPP R8 Cat.4 FDD and TDD Support 1.4 to 20 MHz RF bandwidth Support DL 2 x 2 MIMO ● FDD: Max 150Mbps (DL)/Max 50Mbps (UL) ● TDD: Max 130Mbps (DL)/Max 30Mbps (UL)
UMTS Features	Support 3GPP R8 DC-HSDPA/HSPA+/HSDPA/HSUPA/WCDMA Support 16-QAM, 64-QAM and QPSK modulation ● DC-HSDPA: Max 42Mbps (DL) ● HSUPA: Max 5.76Mbps (UL) ● WCDMA: Max 384Kbps (DL)/Max 384Kbps (UL)
TD-SCDMA Features	Support CCSA Release 3 ● Max 4.2Mbps (DL)/Max 2.2Mbps (UL)
CDMA2000 Features	Support 3GPP2 CDMA2000 1X Advanced, CDMA2000 1x EV-DO Rev.A ● EVDO: Max 3.1Mbps (DL)/Max 1.8Mbps (UL) ● 1X Advanced: Max 307.2Kbps (DL)/Max 307.2Kbps (UL)

GSM Features	**R99:** CSD: 9.6kbps, 14.4kbps **GPRS:** Support GPRS multi-slot class 33 (33 by default) Coding scheme: CS-1, CS-2, CS-3 and CS-4 Max 85.6Kbps (UL)/Max 107Kbps (DL) **EDGE:** Support EDGE multi-slot class 33 (33 by default) Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: CS 1-4 and MCS 1-9 Uplink coding schemes: CS 1-4 and MCS 1-9 Max 236.8Kbps (UL)/Max 296Kbps (DL)
WLAN Features	Support 2.4GHz and 5GHz frequency bands Support 802.11a/b/g/n, maximally up to 150Mbps Support AP mode
Bluetooth Feature	BT4.2 LE
GNSS Features	GPS/GLONASS/BeiDou
SMS	Text and PDU mode Point-to-point MO and MT SMS cell broadcast SMS storage: ME by default
LCM Interface	4-lane MIPI_DSI, up to 1.5Gbps per lane Support WVGA (2-lane MIPI_DSI), up to 720p (4-lane MIPI_DSI) 24bit color depth
Camera Interfaces	Use MIPI_CSI, up to 1.5Gbps per lane Support two cameras: 2-lane MIPI_CSI for rear camera, max pixel up to 8MP 1-lane MIPI_CSI for front camera, max pixel up to 2MP
Video Codec	**Video encoding:** H.264 BP/MP – 720p @30fps MPEG-4 SP/H.263 P0 – WVGA @30fps VP8 – WVGA @30fps **Video decoding:** H.264 BP/MP/HP – 1080P @30fps MPEG-4 SP/ASP –1080P @30fps DivX 4x/5x/6x –1080P @30fps H.263 P0 – WVGA @30fps VP8 –1080P @30 fps (HEVC) H.265 MP 8 bit –1080P @30fps
Audio Interfaces	**Audio input:** Two analog microphone inputs, integrating internal bias voltage

	Audio output: Class AB stereo headphone output Class AB earpiece differential output Class D speaker differential amplifier output
Audio Codec	HR, FR, EFR, AMR, AMR-WB
USB Interface	Compliant with USB 2.0 specification; the data transfer rate can reach up to 480Mbps Used for AT command communication, data transmission, software debugging and firmware upgrade Support USB OTG (Need additional 5V power supply chip) USB Driver: Support Windows XP, Windows Vista, Windows 7/8/8.1
(U)SIM Interfaces	Two (U)SIM interfaces Support USIM/SIM card: 1.8V and 2.95V Support Dual SIM Dual Standby (supported by default)
UART Interfaces	Two UART interfaces: UART1 and UART2 ● UART1: 4-wire UART interface with RTS/CTS hardware flow control; baud rate up to 3.75Mbps ● UART2: 2-wire UART interface used for debugging
Motor Drive Interface	Drive ERM motor
SD Card Interface	Support SD 3.0, 4-bit SDIO Support hot-plug
I2C Interfaces	Three I2C interfaces Used for peripherals such as camera, sensor, touch panel, etc.
ADC Interfaces	Support three ADC interfaces Used for input voltage sense, battery temperature detection and general-purpose ADC
Real Time Clock	Supported
Antenna Interfaces	Main antenna, DRX antenna, GNSS antenna and Wi-Fi/BT antenna
Physical Characteristics	Size: (40.5±0.15) × (40.5±0.15) × (2.8±0.2)mm Package: LCC Weight: approx. 9.8g
Temperature Range	Operating temperature range: -35°C~+65°C [1)] Extended temperature range: -40°C~+75°C [2)] Storage temperature range: -40°C ~ +90°C
Firmware Upgrade	Over USB interface
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1] Within operation temperature range, the module is 3GPP compliant.
2. [2] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

2.3. Functional Diagram

The following figure shows a block diagram of SC20 and illustrates the major functional parts.

- Power management
- Radio frequency
- Baseband
- LPDDR3+eMMC flash
- Peripheral interfaces
  --USB interface
  --UART interfaces
  --(U)SIM interfaces
  --SD card interface
  --GPIO interfaces
  --I2C interfaces
  --ADC interfaces
  --LCM (MIPI) interface
  --Touch panel interface
  --CAM (MIPI) interfaces
  --Audio interfaces

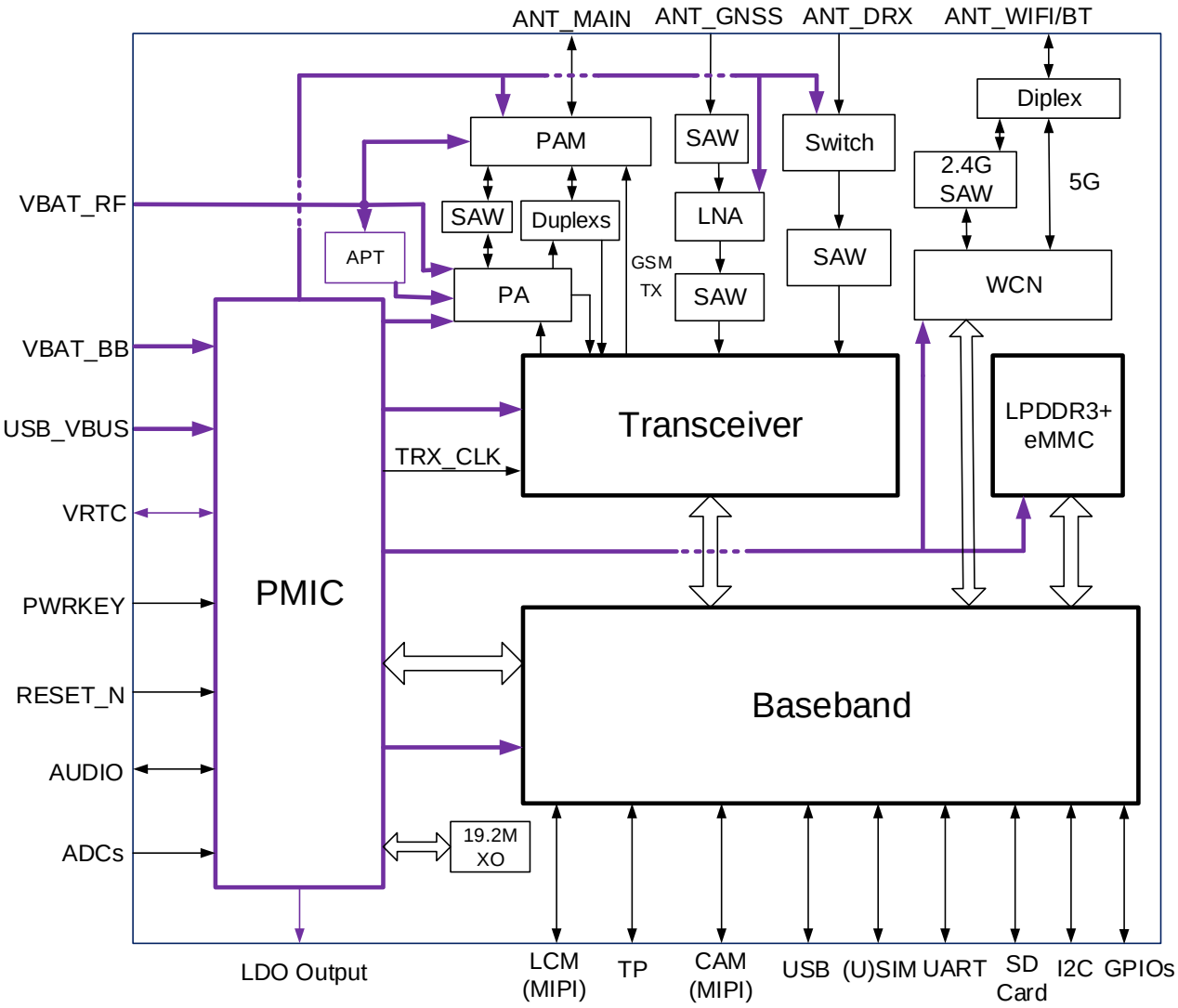


Figure 1: Functional Diagram

2.4. Evaluation Board

In order to help customers to develop applications with SC20, Quectel supplies the evaluation board (SMART EVB), USB to RS232 converter cable, USB data cable, power adapter, earphone, antenna and other peripherals to control or test the module. For more details, please refer to ***document [1]***.

3 Application Interfaces

3.1. General Description

SC20 is an SMD type module with 146 LCC pads and 64 LGA pads. The following chapters provide the detailed description of pins/interfaces listed below.

- Power supply
- VRTC interface
- USB interface
- UART interfaces
- (U)SIM interfaces
- SD card interface
- GPIO interfaces
- SPI interface
- I2C interfaces
- ADC interfaces
- Motor drive interface
- LCM interface
- Touch panel interface
- Camera interfaces
- Sensor interfaces
- Audio interfaces
- Emergency download interface

3.2. Pin Assignment

The following figure shows the pin assignment of SC20 module.

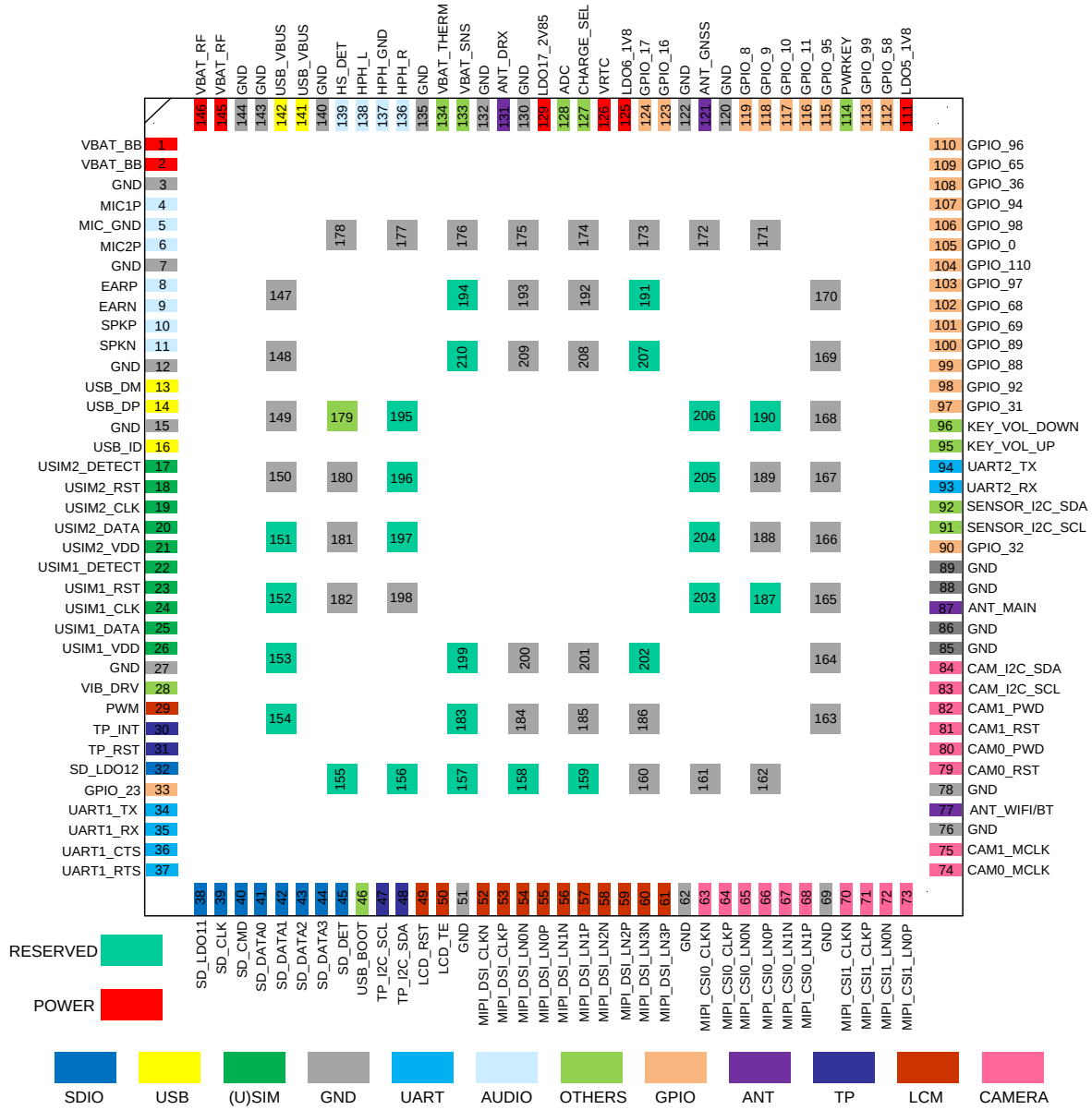


Figure 2: Pin Assignment (Top View)

3.3. Pin Description

The following tables show the SC20's pin definition.

Table 7: I/O Parameters Definition

Type	Description
IO	Bidirectional
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain

The following tables show the SC20's pin definition and electrical characteristics.

Table 8: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	1, 2	PI	Power supply for module's baseband part.	Vmax=4.2V Vmin=3.5V Vnorm=3.8V	It must be able to provide sufficient current up to 3.0A. It is suggested to use a zener diode for voltage stabilization.
VBAT_RF	145, 146	PI	Power supply for module's RF part.	Vmax=4.2V Vmin=3.5V Vnorm=3.8V	
VRTC	126	PI/PO	Power supply for internal RTC circuit.	$V_O$max=3.2V V_I=2.0V~3.25V	If unused, keep this pin open.
LDO5_1V8	111	PO	1.8V output power supply	Vnorm=1.8V $I_O$max=20mA	Power supply for external GPIO's pull up circuits and level

					shift circuit.
LDO6_1V8	125	PO	1.8V output power supply	Vnorm=1.8V $I_O$max=100mA	Power supply for peripherals. 2.2uF~4.7uF capacitor is recommended to be applied to the LDO6_1V8 pin. If unused, keep this pin open.
LDO17_2V85	129	PO	2.85V output power supply	Vnorm=2.85V $I_O$max=300mA	Power supply for peripherals. 2.2uF~4.7uF capacitor is recommended to be applied to the LDO17_2V85 pin. If unused, keep this pin open.
SD_LDO11	38	PO	Power supply for SD card.	Vnorm=2.95V $I_O$max=600mA	
SD_LDO12	32	PO	1.8V/2.95V output power supply	Vnorm=2.95V $I_O$max=50mA	Power supply for SD's pull up circuits.
GND	3, 7, 12, 15, 27, 51, 62, 69, 76, 78, 85, 86, 88, 89, 120, 122, 130, 132, 135, 140, 143, 144, 147~150, 160~178, 180~182, 184~186, 188~189, 192~193,		GND		

	198~200, 201~208, 209				
Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC1P	4	AI	Microphone positive input for channel 1		
MIC_GND	5		MIC reference ground		
MIC2P	6	AI	Microphone positive input for channel 2		
EARP	8	AO	Earpiece positive output		
EARN	9	AO	Earpiece negative output		
SPKP	10	AO	Speaker positive output		
SPKN	11	AO	Speaker negative output		
HPH_R	136	AO	Headphone right channel output		
HPH_GND	137	AI	Headphone virtual ground		
HPH_L	138	AO	Headphone left channel output		
HS_DET	139	AI	Headset insertion detection		High level by default.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	141, 142	PI	USB power supply	Vmax=6.3V Vmin=4.35V Vnorm=5.0V	Used for USB 5V power input and USB detection.
USB_DM	13	IO	USB differential data bus (minus)	Compliant with USB 2.0 standard specification.	Require differential impedance of 90Ω.
USB_DP	14	IO	USB differential data bus (plus)		

USB_ID	16	AI	USB ID detection		High level by default.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM2_ DETECT	17	DI	(U)SIM2 card hot-plug detection	V_{IL}max=0.63V V_{IH}min=1.17V	Active Low. External pull-up resistor is required. If unused, keep this pin open.
USIM2_RST	18	DO	(U)SIM2 card reset signal	V_{OL}max=0.4V V_{OH}min= 0.8×USIM2_VDD	
USIM2_CLK	19	DO	(U)SIM2 card clock signal	V_{OL}max=0.4V V_{OH}min= 0.8×USIM2_VDD	
USIM2_DATA	20	IO	(U)SIM2 card data signal	V_{IL}max= 0.2×USIM2_VDD V_{IH}min= 0.7×USIM2_VDD V_{OL}max=0.4V V_{OH}min= 0.8×USIM2_VDD	
USIM2_VDD	21	PO	(U)SIM2 card power supply	**For 1.8V (U)SIM:** Vmax=1.85V Vmin=1.75V **For 2.95V (U)SIM:** Vmax=3.1V Vmin=2.8V	Either 1.8V or 2.95V (U)SIM card is supported by the module automatically.
USIM1_ DETECT	22	DI	(U)SIM1 card hot-plug detection	V_{IL}max=0.63V V_{IH}min=1.17V	Active low. External pull-up resistor is required. If unused, keep this pin open.
USIM1_RST	23	DO	(U)SIM1 card reset signal	V_{OL}max=0.4V V_{OH}min= 0.8×USIM1_VDD	
USIM1_CLK	24	DO	(U)SIM1 card clock signal	V_{OL}max=0.4V V_{OH}min= 0.8×USIM1_VDD	
USIM1_DATA	25	IO	(U)SIM1 card data signal	V_{IL}max= 0.2×USIM1_VDD	

				V_{IH}min= 0.7×USIM1_VDD V_{OL}max=0.4V V_{OH}min= 0.8×USIM1_VDD	
USIM1_VDD	26	PO	(U)SIM1 card power supply	**For 1.8V (U)SIM:** Vmax=1.85V Vmin=1.75V **For 2.95V (U)SIM:** Vmax=3.1V Vmin=2.8V	Either 1.8V or 2.95V (U)SIM card is supported by the module automatically
UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART1_TX	34	DO	UART1 transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
UART1_RX	35	DI	UART1 receive data	V_{IL}max=0.63V V_{IH}min=1.17V	1.8V power domain. If unused, keep this pin open.
UART1_CTS	36	DI	UART1 clear to send	V_{IL}max=0.63V V_{IH}min=1.17V	1.8V power domain. If unused, keep this pin open.
UART1_RTS	37	DO	UART1 request to send	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
UART2_RX	93	DI	UART2 receive data. Debug port by default.	V_{IL}max=0.63V V_{IH}min=1.17V	1.8V power domain. If unused, keep this pin open.
UART2_TX	94	DO	UART2 transmit data. Debug port by default.	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_CLK	39	DO	High speed digital clock signal of SD card	**1.8V SD card:** V_{OL}max=0.45V V_{OH}min=1.4V	

				2.95V SD card: V_{OL}max=0.37V V_{OH}min=2.2V	
SD_CMD	40	IO	Command signal of SD card	**1.8V SD card:** V_{IL}max=0.58V V_{IH}min=1.27V V_{OL}max=0.45V V_{OH}min=1.4V **2.95V SD card:** V_{IL}max=0.73V V_{IH}min=1.84V V_{OL}max=0.37V V_{OH}min=2.2V	
SD_DATA0	41	IO	High speed bidirectional digital signal lines of SD card	**1.8V SD card:** V_{IL}max=0.58V V_{IH}min=1.27V V_{OL}max=0.45V V_{OH}min=1.4V **2.95V SD card:** V_{IL}max=0.73V V_{IH}min=1.84V V_{OL}max=0.37V V_{OH}min=2.2V	
SD_DATA1	42	IO			
SD_DATA2	43	IO			
SD_DATA3	44	IO			
SD_DET	45	DI	SD card insertion detection	V_{IL}max=0.63V V_{IH}min=1.17V	Active low
Touch Panel (TP) Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TP_INT	30	DI	Interrupt signal of TP	V_{IL}max=0.63V V_{IH}min=1.17V	1.8V power domain.
TP_RST	31	DO	Reset signal of TP	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. Active low.
TP_I2C_SCL	47	OD	I2C clock signal of TP		1.8V power domain.
TP_I2C_SDA	48	OD	I2C data signal of TP		1.8V power domain.

LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWM	29	DO	Adjust the backlight brightness. PWM control signal.	V_{OL}max=0.45V V_{OH}max=VBAT_BB	
LCD_RST	49	DO	LCD reset signal	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. Active low.
LCD_TE	50	DI	LCD tearing effect signal	V_{IL}max=0.63V V_{IH}min=1.17V	1.8V power domain.
MIPI_DSI_CLKN	52	AO	MIPI DSI clock signal (negative)		
MIPI_DSI_CLKP	53	AO	MIPI DSI clock signal (positive)		
MIPI_DSI_LN0N	54	AO	MIPI DSI data signal (negative)		
MIPI_DSI_LN0P	55	AO	MIPI DSI data signal (positive)		
MIPI_DSI_LN1N	56	AO	MIPI DSI data signal (negative)		
MIPI_DSI_LN1P	57	AO	MIPI DSI data signal (positive)		
MIPI_DSI_LN2N	58	AO	MIPI DSI data signal (negative)		
MIPI_DSI_LN2P	59	AO	MIPI DSI data signal (positive)		
MIPI_DSI_LN3N	60	AO	MIPI DSI data signal (negative)		
MIPI_DSI_LN3P	61	AO	MIPI DSI data signal (positive)		
Camera Interfaces					
Pin Name	**Pin No**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIPI_CSI0_CLKN	63	AI	MIPI CSI clock signal (negative)		

MIPI_CSI0_CLKP	64	AI	MIPI CSI clock signal (positive)		
MIPI_CSI0_LN0N	65	AI	MIPI CSI data signal (negative)		
MIPI_CSI0_LN0P	66	AI	MIPI CSI data signal (positive)		
MIPI_CSI0_LN1N	67	AI	MIPI CSI data signal (negative)		
MIPI_CSI0_LN1P	68	AI	MIPI CSI data signal (positive)		
MIPI_CSI1_CLKN	70	AI	MIPI CSI clock signal (negative)		
MIPI_CSI1_CLKP	71	AI	MIPI CSI clock signal (positive)		
MIPI_CSI1_LN0N	72	AI	MIPI CSI data signal (negative)		
MIPI_CSI1_LN0P	73	AI	MIPI CSI data signal (positive)		
CAM0_MCLK	74	DO	Clock signal of rear camera	V_{OL}max=0.45V V_{OH}min=1.35V	
CAM1_MCLK	75	DO	Clock signal of front camera	V_{OL}max=0.45V V_{OH}min=1.35V	
CAM0_RST	79	DO	Reset signal of rear camera	V_{OL}max=0.45V V_{OH}min=1.35V	
CAM0_PWD	80	DO	Power down signal of rear camera	V_{OL}max=0.45V V_{OH}min=1.35V	
CAM1_RST	81	DO	Reset signal of front camera	V_{OL}max=0.45V V_{OH}min=1.35V	
CAM1_PWD	82	DO	Power down signal of front camera	V_{OL}max=0.45V V_{OH}min=1.35V	
CAM_I2C_SCL	83	OD	I2C clock signal of camera		1.8V power domain.

CAM_I2C_SDA	84	OD	I2C data signal of camera		1.8V power domain.
Keypad Interfaces					
Pin Name	**Pin No**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	114	DI	Turn on/off the module	V_{IL}max=0.63V V_{IH}min=1.17V	Pull-up to 1.8V internally, active low.
KEY_VOL_UP	95	DI	Volume up	V_{IL}max=0.63V V_{IH}min=1.17V	If unused, keep this pin open.
KEY_VOL_DOWN	96	DI	Volume down	V_{IL}max=0.63V V_{IH}min=1.17V	If unused, keep this pin open.
SENSOR_I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SENSOR_I2C_SCL	91	OD	I2C clock signal for external sensor		1.8V power domain.
SENSOR_I2C_SDA	92	OD	I2C data signal for external sensor		1.8V power domain.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC	128	AI	General purpose ADC		Maximum voltage not exceeding 1.7V.
VBAT_SNS	133	AI	Input voltage sense		Maximum input voltage is 4.5V.
VBAT_THERM	134	AI	Battery temperature detection		
RF Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	87	IO	Main antenna		50Ω impedance
ANT_DRX	131	AI	Diversity antenna		
ANT_GNSS	121	AI	GNSS antenna		
ANT_WIFI/BT	77	IO	Wi-Fi/BT antenna		

GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_23	33	IO	GPIO		1.8V power domain.
GPIO_32	90	IO	GPIO		1.8V power domain.
GPIO_31	97	IO	GPIO		1.8V power domain.
GPIO_92	98	IO	GPIO		1.8V power domain.
GPIO_88 [1)]	99	IO	GPIO		1.8V power domain.
GPIO_89	100	IO	GPIO		1.8V power domain.
GPIO_69	101	IO	GPIO		1.8V power domain.
GPIO_68 [1)]	102	IO	GPIO		1.8V power domain.
GPIO_97	103	IO	GPIO		1.8V power domain.
GPIO_110	104	IO	GPIO		1.8V power domain.
GPIO_0	105	IO	GPIO	V_{IL}max=0.63V V_{IH}min=1.17V V_{OL}max=0.45V V_{OH}min=1.4V	1.8V power domain.
GPIO_98	106	IO	GPIO		1.8V power domain.
GPIO_94	107	IO	GPIO		1.8V power domain.
GPIO_36	108	IO	GPIO		1.8V power domain.
GPIO_65	109	IO	GPIO		1.8V power domain.
GPIO_96	110	IO	GPIO		1.8V power domain.
GPIO_58	112	IO	GPIO		1.8V power domain.
GPIO_99	113	IO	GPIO		1.8V power domain.
GPIO_95	115	IO	GPIO		1.8V power domain.
GPIO_11	116	IO	GPIO		Can be multiplexed into SPI_CLK.
GPIO_10	117	IO	GPIO		Can be multiplexed into SPI_CS_N.
GPIO_9	118	IO	GPIO		Can be multiplexed into SPI_MISO.
GPIO_8	119	IO	GPIO		Can be multiplexed

					into SPI_MOSI.
GPIO_16	123	IO	GPIO		1.8V power domain.
GPIO_17	124	IO	GPIO		1.8V power domain.
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VIB_DRV	28	PO	Motor drive	Imax=0~175mA Vmax=1.2V~3.1V	Connected to the negative terminal of the motor.
RESET_N [2)]	179	DI	Reset the module		Disabled by default and can be enabled through software configuration.
USB_BOOT	46	DI	Force the module to boot from USB port		Set USB_BOOT to high level will force the module to enter into emergency download mode.
CHARGE_SEL	127	DI	Used for charger selection		If it is open, internal charger is used. If it is connected to GND, external charger is used.
Reserved Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	151, 152, 153, 154, 155, 156, 157, 158, 159, 183, 187, 190, 191, 194, 195, 196, 197, 199, 202, 203, 204, 205, 206, 207, 210		Reserved pins		Keep these pins open.

NOTES

1. [1)] GPIO_68 and GPIO_88 cannot be pulled up during start-up.
2. [2)] RESET_N is disabled by default and can be enabled through software configuration.

3.4. Power Supply

3.4.1. Power Supply Pins

SC20 provides two VBAT_RF pins and two VBAT_BB pins for connecting with an external power supply. The VBAT_RF pins are used for the RF part of the module and the VBAT_BB pins are used for the baseband part of the module.

3.4.2. Decrease Voltage Drop

The power supply range of the module is 3.5V~4.2V, and the recommended value is 3.8V. The power supply performance, such as load capacity, voltage ripple, etc. directly influences the module's performance and stability. Under ultimate conditions, the transient peak current of the module may surge up to 3A. If the supply voltage is not enough, there will be voltage drops, and if the voltage drops below 3.1V, the module will be turned off automatically. Therefore, please make sure the input voltage will never drop below 3.1V.

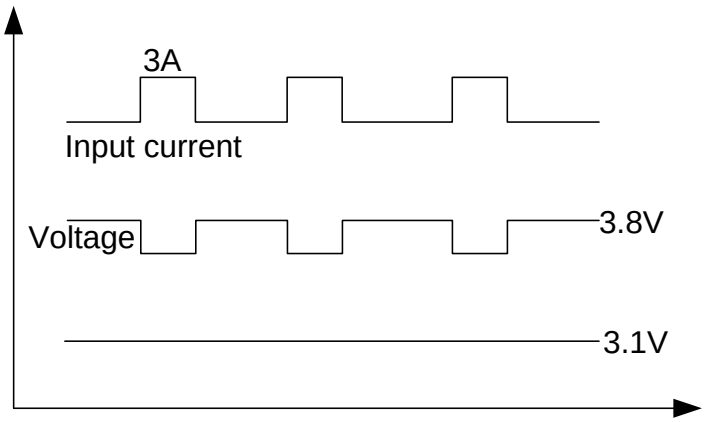


Figure 3: Voltage Drop Sample

To decrease voltage drop, a bypass capacitor of about 100μF with low ESR (ESR=0.7Ω) should be used, and a multi-layer ceramic chip capacitor (MLCC) should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100nF, 33pF, 10pF) for composing the MLCC array, and place these capacitors close to VBAT_BB/RF pins. The main power supply from an external application

has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1.5mm, and the width of VBAT_RF trace should be no less than 2mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to get a stable power source, it is suggested to use a 0.5W zener diode and place it as close to the VBAT_BB/RF pins as possible to increase voltage surge withstand capability. The following figure shows the star structure of the power supply.

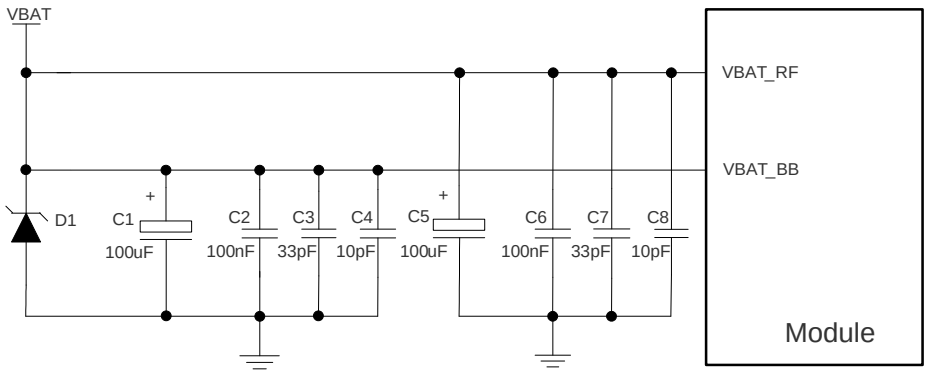


Figure 4: Star Structure of the Power Supply

3.4.3. Reference Design for Power Supply

The power design for the module is very important, as the performance of module largely depends on the power source. The power supply of SC20 should be able to provide sufficient current up to 3A at least. If the voltage drop between the input and output is not too high, it is suggested to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5V input power source which adopts an LDO (MIC29302WU) from MICREL. The typical output voltage is 3.8V and the maximum load current is 3.0A.

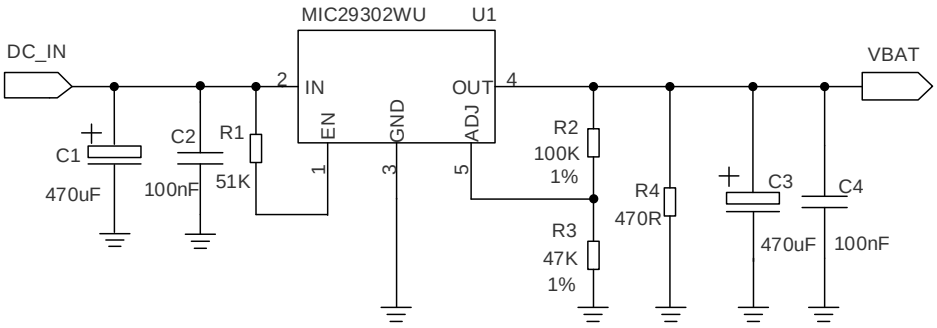


Figure 5: Reference Circuit of Power Supply

NOTES

1. It is suggested that customers should switch off the power supply for module in abnormal state, and then switch on the power to restart the module.
2. The module supports battery charging function by default. If the above power supply design is adopted, please make sure the charging function is disabled by software or connect VBAT to Schottky diode in series to avoid the reverse current to the power supply chip.

3.5. Turn on and off Scenarios

3.5.1. Turn on Module Using the PWRKEY

The module can be turned on by driving PWRKEY pin to a low level for at least 1.6s. PWRKEY pin is pulled to 1.8V internally. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

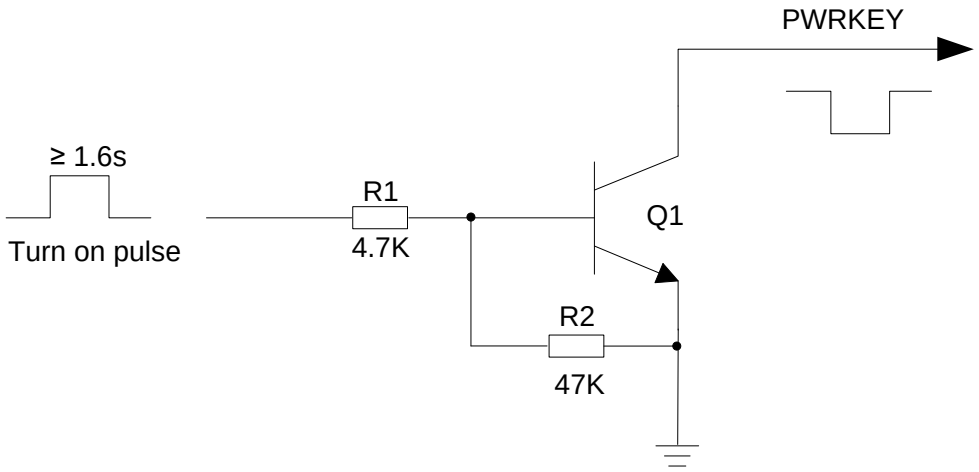


Figure 6: Turn on the Module Using Driving Circuit

The other way to control the PWRKEY is using a button directly. A TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

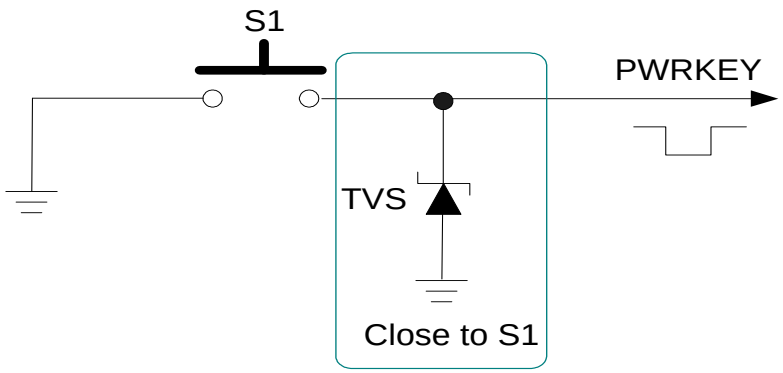


Figure 7: Turn on the Module Using Keystroke

The turning on scenario is illustrated in the following figure.

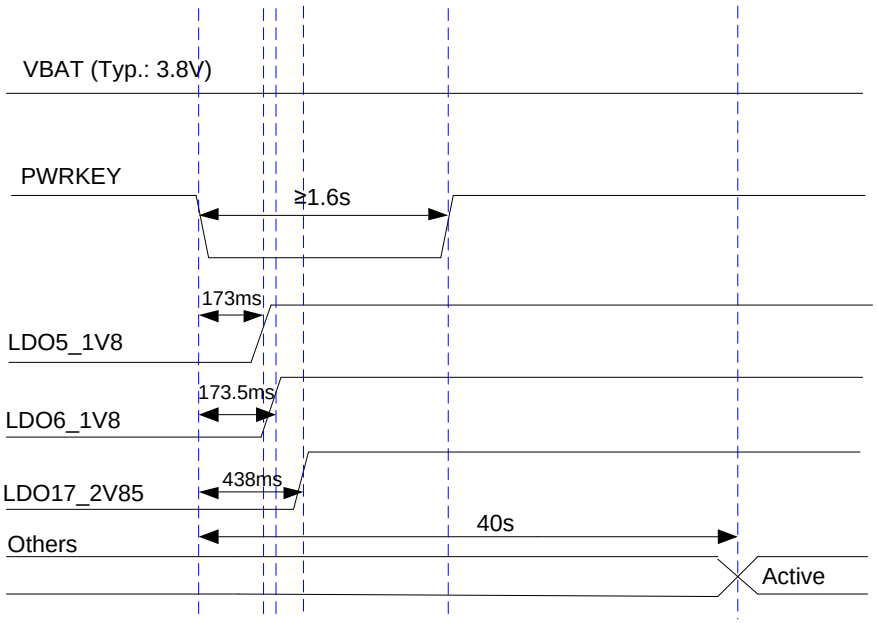


Figure 8: Timing of Turning on Module

NOTES

1. When the module is powered on for the first time, its timing of turning on will be 45ms longer than that shown above.
2. Make sure that VBAT is stable before pulling down PWRKEY pin. The recommended time between them is no less than 30ms. PWRKEY pin cannot be pulled down all the time.

3.5.2. Turn off Module

Set the PWRKEY pin low for at least 1s, and then choose to turn off the module when the prompt window comes up.

The other way to turn off the module is to drive PWRKEY to a low level for at least 8s. The module will execute forced shutdown. The forced power-down scenario is illustrated in the following figure.

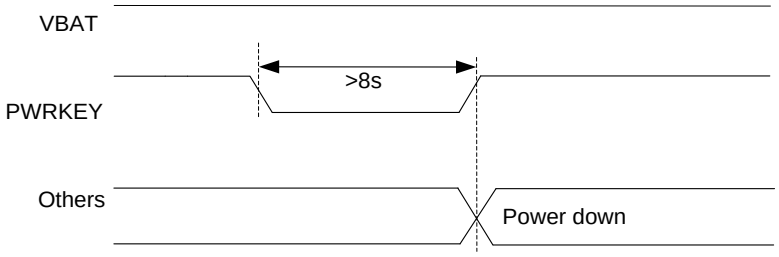


Figure 9: Timing of Turning off Module

3.6. VRTC Interface

The RTC (Real Time Clock) can be powered by an external power source through VRTC when the module is powered down and there is no power supply for the VBAT. The external power source can be capacitor or rechargeable battery (such as coil cells) according to application demands. The following are some reference circuit designs when an external battery or capacitor is utilized for powering RTC.

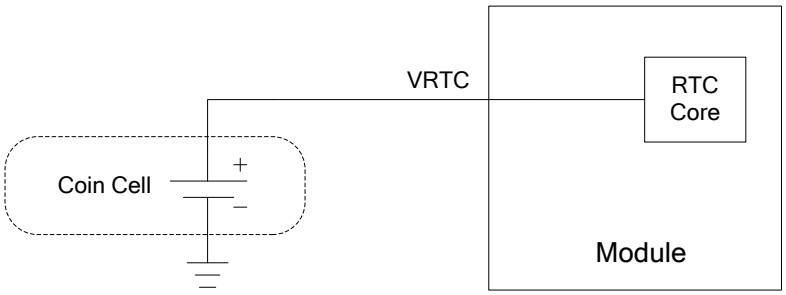


Figure 10: RTC Powered by Coin Cell

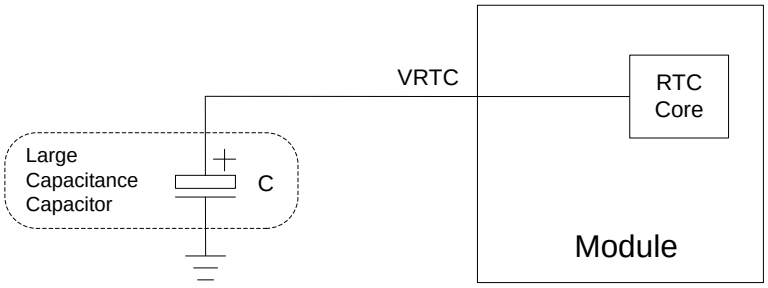


Figure 11: RTC Powered by Capacitor

If RTC is ineffective, it can be synchronized through network after the module is powered on.

- 2.0V~3.25V input voltage range and 3.0V typical value for VRTC. When VBAT is disconnected, the average consumption is about 5uA.
- When powered by VBAT, the RTC error is 50ppm. When powered by VRTC, the RTC error is 200ppm.
- If the rechargeable battery is used, the ESR of the battery should be less than 2K, and it is recommended to use the MS621FE FL11E of SEIKO.
- If large capacitance capacitor is selected, it is recommended to use a 100uF capacitor with low ESR. The capacitor will be able to power the real-time clock for 45 seconds.

3.7. Power Output

SC20 supports output of regulated voltages for peripheral circuits. During application, it is recommended to use parallel capacitors (33pF and 10pF) in the circuit to suppress high frequency noise.

Table 9: Power Description

Pin Name	Default Voltage (V)	Driving Current (mA)	IDLE
LDO5_1V8	1.8	20	KEEP
LDO6_1V8	1.8	100	/
LDO17_2V85	2.85	300	/
SD_LDO12	2.95	50	/
SD_LDO11	2.95	600	/
USIM1_VDD	1.80/2.95	50	
USIM2_VDD	1.80/2.95	50	

3.8. Battery Charge and Management

SC20 module can recharge batteries. The battery charger in SC20 module supports trickle charging, constant current charging and constant voltage charging modes, which optimize the charging procedure for Li-ion batteries.

- **Trickle charging:** There are two steps in this mode. When the battery voltage is below 2.8V, a 90mA trickle charging current is applied to the battery. When the battery voltage is charged up and is between 2.8V and 3.2V, the charging current can be set to 450mA maximally.
- **Constant current mode (CC mode):** When the battery is increased to between 3.2V and 4.2V, the system will switch to CC mode. The maximum charging current is 1.44A when adapter is used for battery charging; and the maximum charging current is 450mA while USB charging.
- **Constant voltage mode (CV mode):** When the battery voltage reaches the final value 4.2V, the system will switch to CV mode and the charging current will decrease gradually. When the battery level reaches 100%, the charging is completed.

SC20 module supports battery temperature detection in the condition that the battery integrates a thermistor (47K 1% NTC thermistor with B-constant of 4050K by default; SDNT1608X473F4050FTF of SUNLORD is recommended) and the thermistor is connected to VBAT_THERM pin. The default battery temperature range is -3.0°C~48.5°C. If VBAT_THERM pin is not connected, there will be malfunctions such as battery charging failure, battery level display error, etc.

A reference design for battery charging circuit is shown as below.

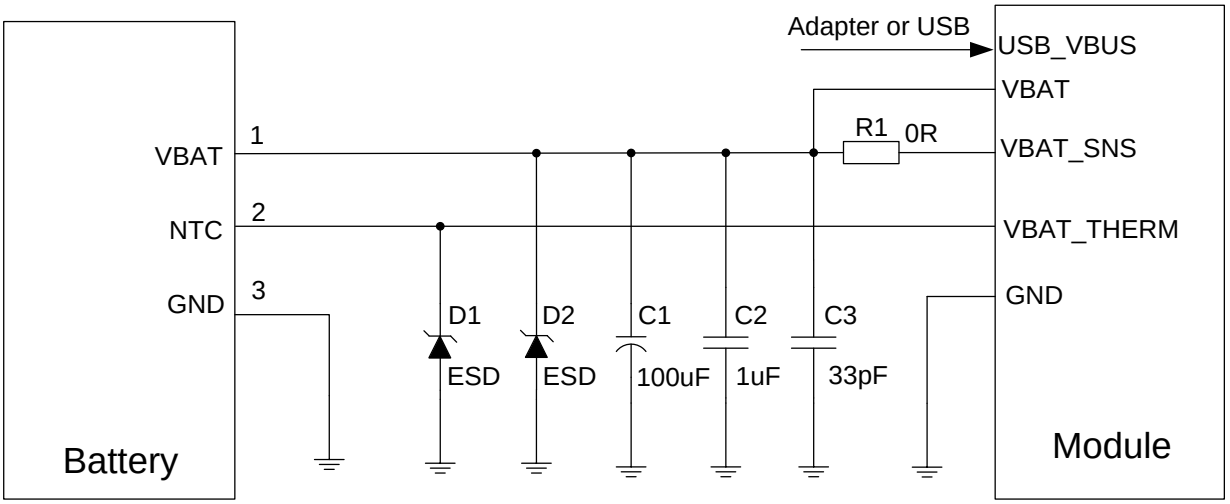


Figure 12: Reference Design for Battery Charging Circuit

Mobile devices such as mobile phones and handheld POS systems are powered by batteries. When different batteries are utilized, the charging and discharging curve has to be modified correspondingly so as to achieve the best effect.

If thermistor is not available in the battery, or adapter is utilized for powering module, then there is only need for VBAT and GND connection. In this case, the system may mistakenly judge that the battery temperature is abnormal, which will cause battery charging failure. In order to avoid this, VBAT_THERM should be connected to GND via a 47KΩ resistor. If VBAT_THERM is unconnected, the system will be unable to detect the battery, making battery cannot be charged.

VBAT_SNS pin must be connected. Otherwise, the module will have abnormalities in voltage detection, as well as associated power on/off and battery charging and discharging issues.

3.9. USB Interface

SC20 contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high speed (480Mbps) and full speed (12Mbps) modes. The USB interface is used for AT command communication, data transmission, software debugging and firmware upgrade.

The following table shows the pin definition of USB interface.

Table 10: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	141, 142	PI	USB power supply	4.35V~6.3V. Typical 5.0V.
USB_DM	13	IO	USB differential data bus (minus)	Require differential impedance of 90Ω
USB_DP	14	IO	USB differential data bus (plus)	
USB_ID	16	AI	USB ID detection	High level by default

USB_VBUS can be powered by USB power or adapter. It can also be used for detecting USB connection, as well as for battery charging via the internal PMU. The input voltage of power supply ranges from 4.35 to 6.3V, and the typical value is 5V. SC20 module supports charging management for a single Li-ion battery, but varied charging parameters should be set for batteries with varied models or capacities. The module is available a built-in linear-charging circuit which supports maximally 1.44A charging current.

The following are two USB interface reference designs for customers to choose from.

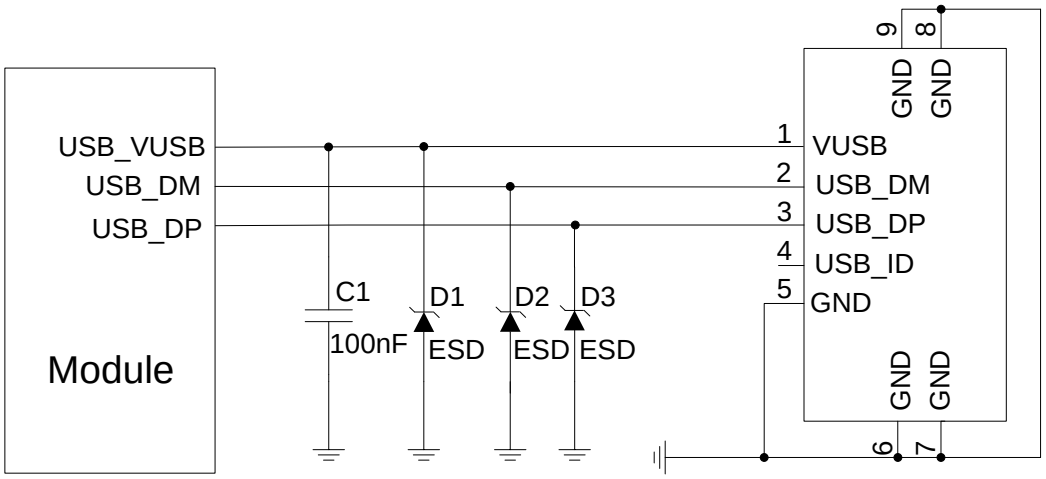


Figure 13: USB Interface Reference Design (OTG is not Supported)

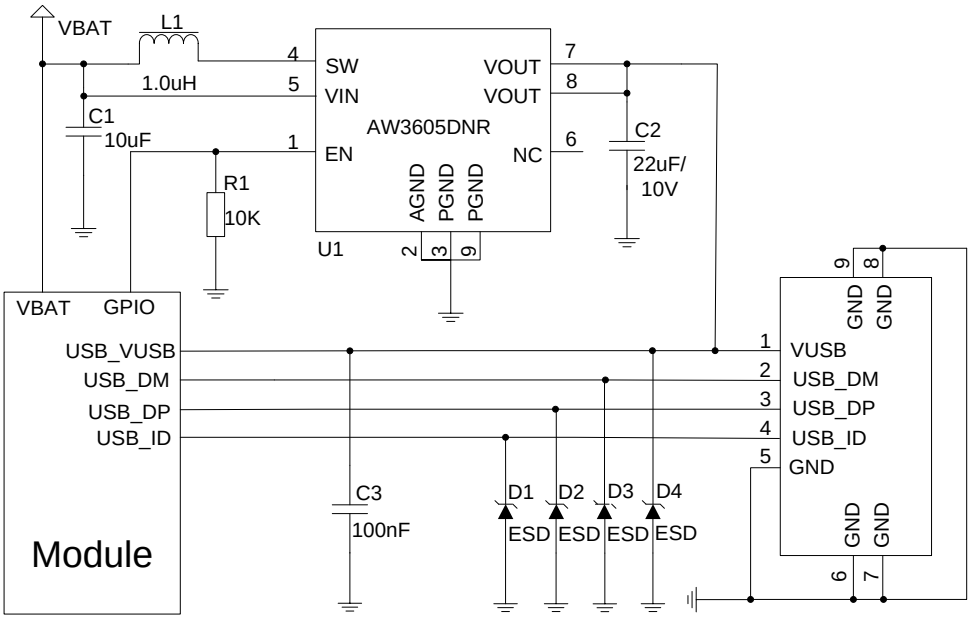


Figure 14: USB Interface Reference Design (OTG is Supported)

SC20 supports OTG protocol. If OTG function is needed, please refer to the above figure for the reference design. AW3605DNR is a high efficiency DC-DC chip manufactured by AWINIC, and customers can choose according to their own demands.

In order to ensure USB performance, please comply with the following principles while designing USB interface.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance

of USB differential trace is 90Ω.

- Keep the ESD protection devices as close as possible to the USB connector. Pay attention to the influence of junction capacitance of ESD protection devices on USB data lines. Typically, the capacitance value should be less than 2pF.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layer but also right and left sides.
- Make sure the trace length difference between USB_DM and USB_DP is not exceeding 6.6mm.

Table 11: USB Trace Length Inside the Module

PIN	Signal	Length (mm)	Length Difference (DP-DM)
13	USB_DM	29.43	-0.07
14	USB_DP	29.36	

3.10. UART Interfaces

The module provides two UART interfaces:

- **UART1:** 4-wire UART interface which supports hardware flow control
- **UART2:** 2-wire UART interface and is used for debugging

Table 12: Pin Definition of UART Interfaces

Pin Name	Pin No	I/O	Description	Comment
UART1_TX	34	DO	UART1 transmit data	1.8V power domain. If it is unused, keep it open.
UART1_RX	35	DI	UART1 receive data	1.8V power domain. If it is unused, keep it open.
UART1_CTS	36	DI	UART1 clear to send	1.8V power domain. If it is unused, keep it open.
UART1_RTS	37	DO	UART1 request to send	1.8V power domain. If it is unused, keep it open.
UART2_RX	93	DI	UART2 receive data. Debug port by default.	1.8V power domain. If it is unused, keep it open.
UART2_TX	94	DO	UART2 transmit data. Debug port by default.	1.8V power domain. If it is unused, keep it open.

UART1 provides 1.8V logic level. A level translator should be used if customers' application is equipped with a 3.3V UART interface. A level translator TXS0104PWR provided by *Texas Instruments* is recommended. The following figure shows the reference design.

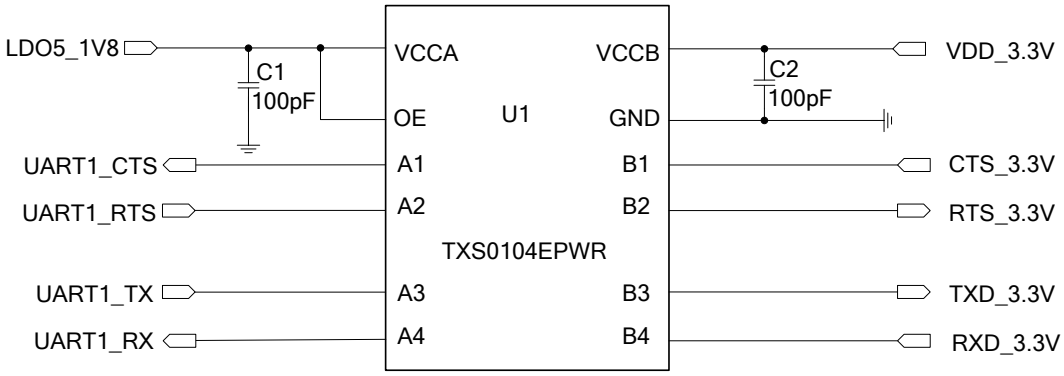


Figure 15: Reference Circuit with Level Translator Chip (for UART1)

The following figure is an example of connection between SC20 and PC. A voltage level translator and a RS-232 level translator chip are also recommended to be added between the module and PC, as these two UART interfaces do not support the RS-232 level, while support the 1.8V CMOS level only.

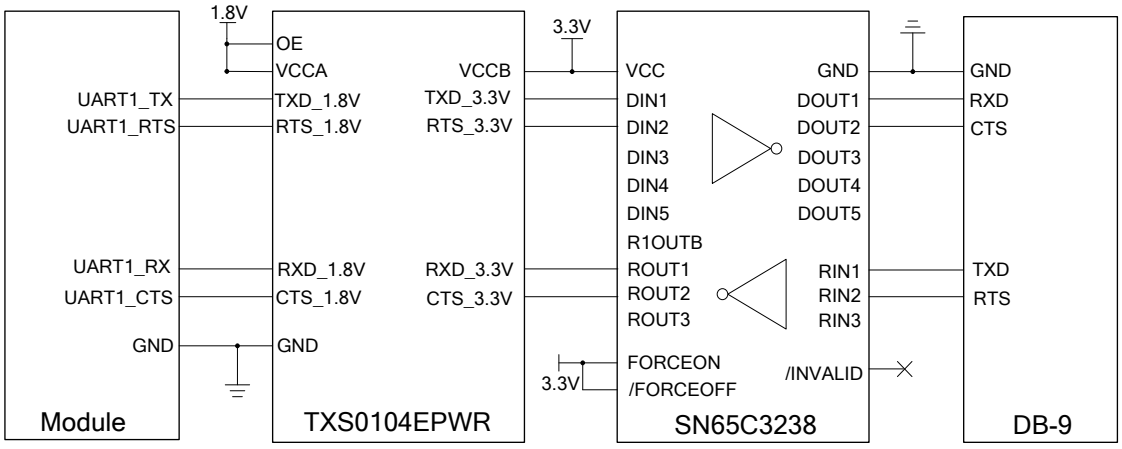


Figure 16: RS-232 Level Match Circuit (for UART1)

NOTE

UART2 is similar to UART1. Please refer to UART1 reference circuit designs for UART2's.

3.11. (U)SIM Interfaces

SC20 provides 2 (U)SIM interfaces which circuitry meet ETSI and IMT-2000 requirements. Dual SIM Card Dual Standby is supported by default. Both 1.8V and 2.95V (U)SIM cards are supported, and the (U)SIM card interfaces are powered by the internal power supply of SC20 module.

Table 13: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No	I/O	Description	Comment
USIM2_DETECT	17	DI	(U)SIM2 card hot-plug detection	Active Low. External pull-up resistor is required. If unused, keep this pin open.
USIM2_RST	18	DO	(U)SIM2 card reset signal	
USIM2_CLK	19	DO	(U)SIM2 card clock signal	
USIM2_DATA	20	IO	(U)SIM2 card data signal	Pull-up to USIM2_VDD with a 10K resistor.
USIM2_VDD	21	PO	(U)SIM2 card power supply	Either 1.8V or 2.95V (U)SIM card is supported by the module automatically.
USIM1_DETECT	22	DI	(U)SIM1 card hot-plug detection	Active low. External pull-up resistor is required. If unused, keep this pin open.
USIM1_RST	23	DO	(U)SIM1 card reset signal	
USIM1_CLK	24	DO	(U)SIM1 card clock signal	
USIM1_DATA	25	IO	(U)SIM1 card data signal	Pull-up to USIM1_VDD with a 10K resistor.
USIM1_VDD	26	PO	(U)SIM1 card power supply	Either 1.8V or 2.95V (U)SIM card is supported by the module automatically.

SC20 supports (U)SIM card hot-plug via the USIM_DETECT pin. A reference circuit for (U)SIM interface with an 8-pin (U)SIM card connector is shown below.

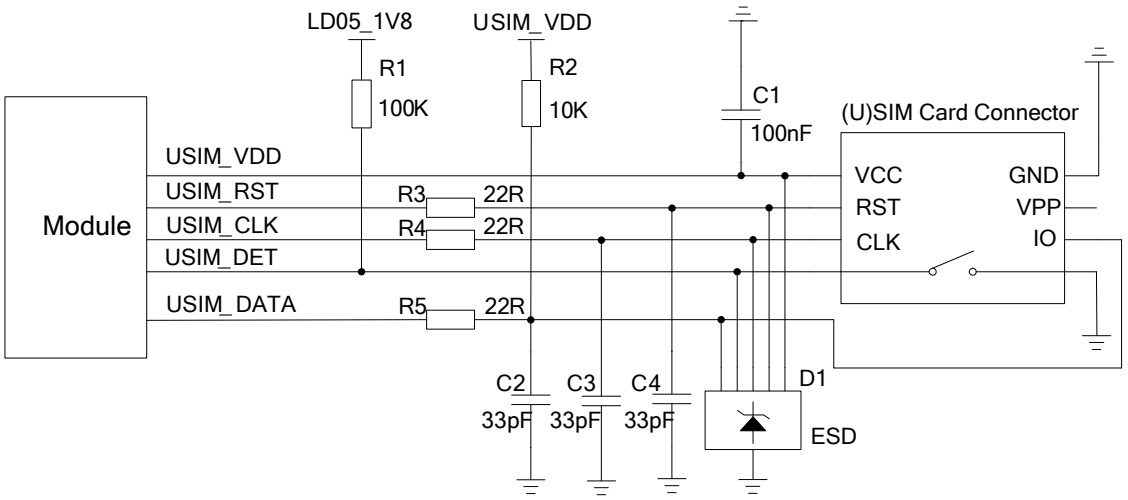


Figure 17: Reference Circuit for (U)SIM Interface with an 8-pin (U)SIM Card Connector

If there is no need to use USIM_DETECT, please keep it open. The following is a reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector.

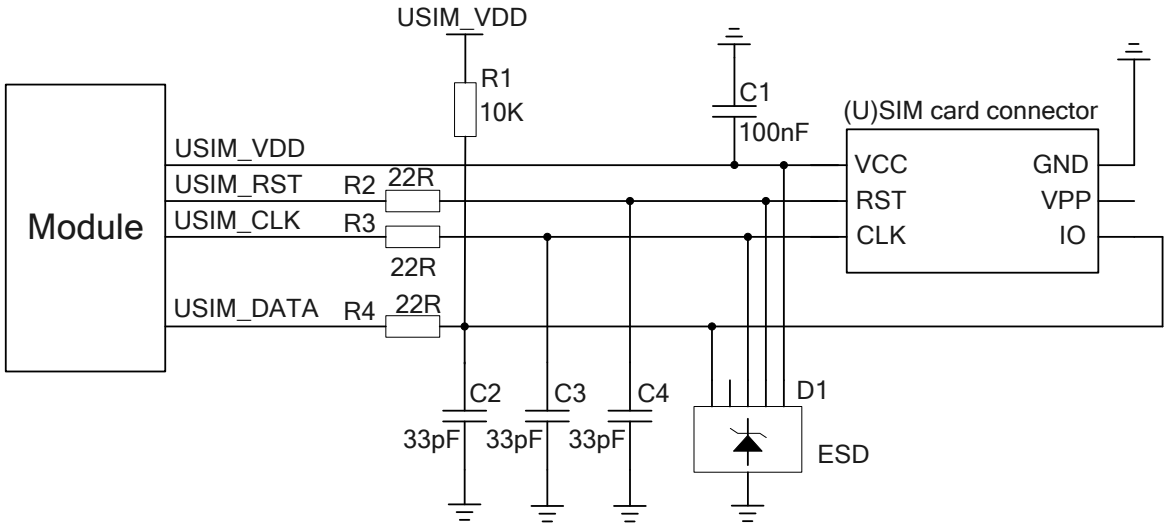


Figure 18: Reference Circuit for (U)SIM Interface with a 6-pin (U)SIM Card Connector

In order to ensure good performance and avoid damage of (U)SIM cards, please follow the criteria below in (U)SIM circuit design:

- Keep placement of (U)SIM card connector as close to the module as possible. Keep the trace length of (U)SIM card signals as less than 200mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- A 100nF filter capacitor shall be reserved for USIM_VDD, and its maximum capacitance should not exceed 1uF. The capacitor should be placed near to (U)SIM card.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with ground. USIM_RST also needs ground protection.

- In order to offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 50pF. The 22Ω resistors should be added in series between the module and (U)SIM card so as to suppress EMI spurious transmission and enhance ESD protection. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The 33pF capacitors should be added in parallel on USIM_DATA, USIM_CLK and USIM_RST signal lines so as to filter RF interference, and they should be placed as close to the (U)SIM card connector as possible.

3.12. SD Card Interface

SC20 module supports SD cards with 4-bit data interfaces or SDIO devices. The pin definition of the SD card interface is shown below.

Table 14: Pin Definition of SD Card Interface

Pin Name	Pin No	I/O	Description	Comment
SD_LDO11	38	PO	Power supply for SD card	Vnorm=2.95V $I_O$max=600mA
SD_LDO12	32	PO	1.8V/2.95V output power supply	Support 1.8V or 2.95V power supply. The maximum drive current is 50mA.
SD_CLK	39	DO	High speed digital clock signal of SD card	Control characteristic impedance as 50Ω.
SD_CMD	40	I/O	Command signal of SD card	
SD_DATA0	41	I/O	High speed bidirectional digital signal lines of SD card	
SD_DATA1	42	I/O		
SD_DATA2	43	I/O		
SD_DATA3	44	I/O		
SD_DET	45	DI	SD card insertion detection	Active low

A reference circuit for SD card interface is shown as below.

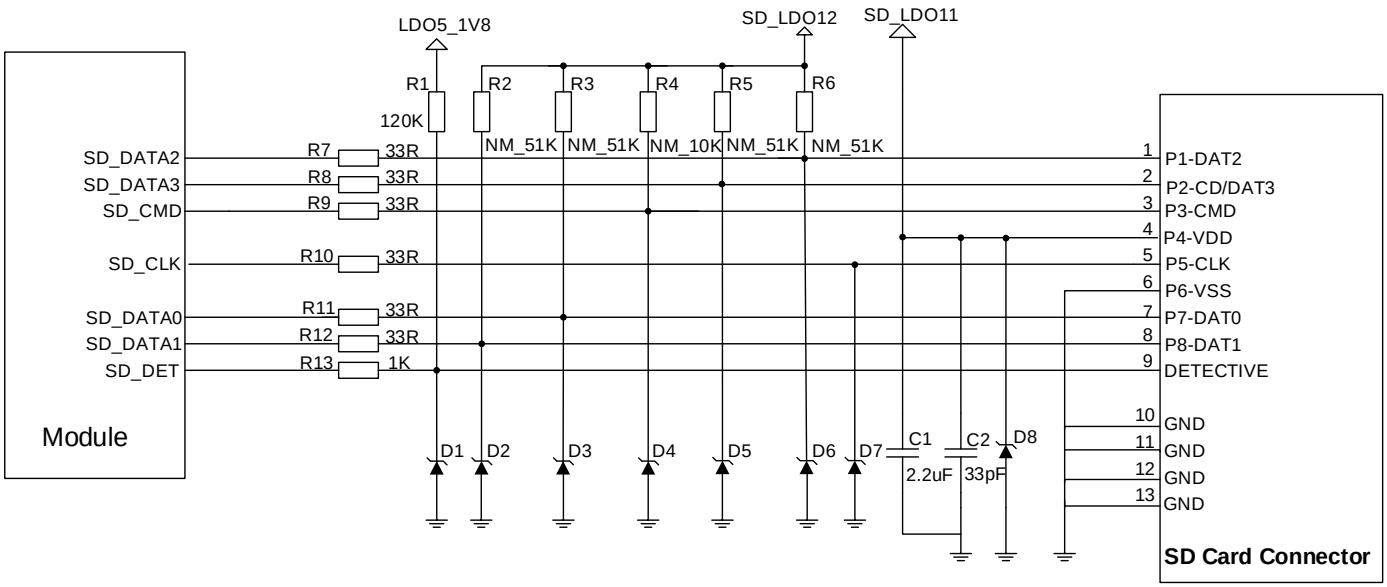


Figure 19: Reference Circuit for SD Card Interface

SD_LDO11 is a peripheral driver power supply for SD card. The maximum drive current is approx. 600mA. Because of the high drive current, it is recommended that the trace width is 0.6mm or more. In order to ensure the stability of drive power, a 2.2uF capacitor should be added in parallel near the SD card connector.

CMD, CLK, DATA0, DATA1, DATA2 and DATA3 are all high-speed signal lines. In PCB design, please control the characteristic impedance of them to 50Ω, and do not cross with other traces. It is recommended to route the trace on the inner layer of PCB, and keep the same trace length for CLK, CMD, DATA0, DATA1, DATA2 and DATA3. CLK additionally needs ground shielding.

Layout guidelines:

- Control impedance as 50Ω±10%, and ground shielding is required.
- The total trace length difference between CLK and other signal line traces should not exceed 1mm.

Table 15: SD Card Trace Length Inside the Module

Pin No.	Signal	Length (mm)	Comment
39	SD_CLK	14.60	
40	SD_CMD	14.55	
41	SD_DATA0	14.53	
42	SD_DATA1	14.56	

43	SD_DATA2	14.53
44	SD_DATA3	14.57

3.13. GPIO Interfaces

SC20 has abundant GPIO interfaces with logic level of 1.8V. The pin definition is listed below.

Table 16: Pin Definition of GPIO Interfaces

PIN	Pin Name	GPIO	Default state	Comment
30	TP_INT	GPIO_13	B-PD: nppukp [1)]	Wakeup [2)]
31	TP_RST	GPIO_12	B-PD: nppukp	Wakeup
33	GPIO_23	GPIO_23	B-PD: nppukp	
34	UART1_TX	GPIO_20	B-PD: nppukp	Wakeup
35	UART1_RX	GPIO_21	B-PD: nppukp	UART1_RX Wakeup
36	UART1_CTS	GPIO_111	B-PD: nppukp	Wakeup
37	UART1_RTS	GPIO_112	B-PD: nppukp	Wakeup
45	SD_DET	GPIO_38	B-PD: nppukp	Wakeup
47	TP_I2C_SCL	GPIO_19	B-PD: nppukp	
48	TP_I2C_SDA	GPIO_18	B-PD: nppukp	
49	LCD_RST	GPIO_25	B-PD: nppukp	Wakeup
50	LCD_TE	GPIO_24	B-PD: nppukp	
74	CAM0_CLK	GPIO_26	B-PD: nppukp	
75	CAM1_CLK	GPIO_27	B-PD: nppukp	
79	CAM0_RST	GPIO_35	B-PD: nppukp	Wakeup
80	CAM0_PWD	GPIO_34	B-PD: nppukp	Wakeup
81	CAM1_RST	GPIO_28	B-PD: nppukp	Wakeup

82	CAM1_PWD	GPIO_33	B-PD: nppukp	
83	CAM_I2C_SCL	GPIO_30	B-PD: nppukp	
84	CAM_I2C_SDA	GPIO_29	B-PD: nppukp	
90	GPIO_32	GPIO_32	B-PD: nppukp	
91	SENSOR_I2C_SCL	GPIO_7	B-PD: nppukp	
92	SENSOR_I2C_SDA	GPIO_6	B-PD: nppukp	
93	UART2_RX	GPIO_5	B-PD: nppukp	Wakeup
94	UART2_TX	GPIO_4	B-PD: nppukp	
95	KEY_VOL_UP	GPIO_90	B-PD: nppukp	Wakeup
96	KEY_VOL_DOWN	GPIO_91	B-PD: nppukp	Wakeup
97	GPIO_31	GPIO_31	B-PD: nppukp	Wakeup
98	GPIO_92	GPIO_92	B-PD: nppukp	Wakeup
99	GPIO_88 [3)]	GPIO_88 [3)]	B-PD: nppukp	
100	GPIO_89	GPIO_89	B-PD: nppukp	
101	GPIO_69	GPIO_69	B-PD: nppukp	
102	GPIO_68 [3)]	GPIO_68 [3)]	B-PD: nppukp	
103	GPIO_97	GPIO_97	B-PD: nppukp	Wakeup
104	GPIO_110	GPIO_110	B-PD: nppukp	Wakeup
105	GPIO_0	GPIO_0	B-PD: nppukp	
106	GPIO_98	GPIO_98	B-PD: nppukp	Wakeup
107	GPIO_94	GPIO_94	B-PD: nppukp	Wakeup
108	GPIO_36	GPIO_36	B-PD: nppukp	Wakeup
109	GPIO_65	GPIO_65	B-PD: nppukp	Wakeup
110	GPIO_96	GPIO_96	B-PD: nppukp	Wakeup
112	GPIO_58	GPIO_58	B-PD: nppukp	Wakeup

113	GPIO_99	GPIO_99	B-PD: nppukp	
115	GPIO_95	GPIO_95	B-PD: nppukp	Wakeup
116	GPIO_11	GPIO_11	B-PD: nppukp	Wakeup
117	GPIO_10	GPIO_10	B-PD: nppukp	
118	GPIO_9	GPIO_9	B-PD: nppukp	
119	GPIO_8	GPIO_8	B-PD: nppukp	
123	GPIO_16	GPIO_16	B-PD: nppukp	
124	GPIO_17	GPIO_17	B-PD: nppukp	

NOTES

1. [1)] B: Bidirectional digital with CMOS input. PD: nppukp=default pull-down with programmable options following the colon (:).
2. [2)] Wakeup: interrupt pins that can wake up the system.
3. [3)] GPIO_68 and GPIO_88 cannot be pulled up during start-up.

3.14. SPI Interface

SC20 module provide one SPI interface multiplexed from GPIO interfaces. The interface only supports the master mode.

Table 17: Pin Definition of SPI Interface

Pin Name	Pin No	I/O	Description	Comment
GPIO_8	119	IO	GPIO by default. Can be multiplexed into SPI_MOSI.	Master out slave in of SPI
GPIO_9	118	IO	GPIO by default. Can be multiplexed into SPI_MISO.	Master in slave out of SPI
GPIO_10	117	DO	GPIO by default. Can be multiplexed into SPI_CS_N.	SPI chip select
GPIO_11	116	DO	GPIO by default. Can be multiplexed into SPI_CLK.	SPI clock

3.15. I2C Interfaces

SC20 module provides three I2C interfaces which only support the master mode. As an open drain output, the I2C interfaces need a pull-up resistor on its external circuit, and the recommended logic level is 1.8V.

Table 18: Pin Definition of I2C Interfaces

Pin Name	Pin No	I/O	Description	Comment
TP_I2C_SCL	47	OD	I2C clock signal of touch panel	Used for touch panel
TP_I2C_SDA	48	OD	I2C data signal of touch panel	
CAM_I2C_SCL	83	OD	I2C clock signal of camera	Used for camera
CAM_I2C_SDA	84	OD	I2C data signal of camera	
SENSOR_I2C_SCL	91	OD	I2C clock signal for external sensor	Used for external sensor
SENSOR_I2C_SDA	92	OD	I2C data signal for external sensor	

3.16. ADC Interfaces

SC20 module provides three analog-to-digital converter (ADC) interfaces, and the pin definition is shown below.

Table 19: Pin Definition of ADC Interfaces

Pin Name	Pin No	I/O	Description	Comment
ADC	128	AI	General purpose ADC	Max input voltage is 1.7V
VBAT_SNS	133	AI	Input voltage sense	Max input voltage is 4.5V
VBAT_THERM	134	AI	Battery temperature detection	Internal pull-up; externally connect to GND with a 47K NTC thermistor

The resolution of the ADC is up to 16 bits and the effective resolution is 12 bits.

NOTE

When the input voltage exceeds the maximum input voltage of VBAT_SNS pin, resistor divider cannot be used in the circuit design. Instead, general purpose ADC with resistor divider input can be used.

3.17. Motor Drive Interface

The pin of motor drive interface is listed below.

Table 20: Pin Definition of Motor Drive Interface

Pin Name	Pin No	I/O	Description	Comment
VIB_DRV	28	PO	Motor drive	Connected to the negative terminal of the motor

The motor is driven by an exclusive circuit, and a reference circuit design is shown below.

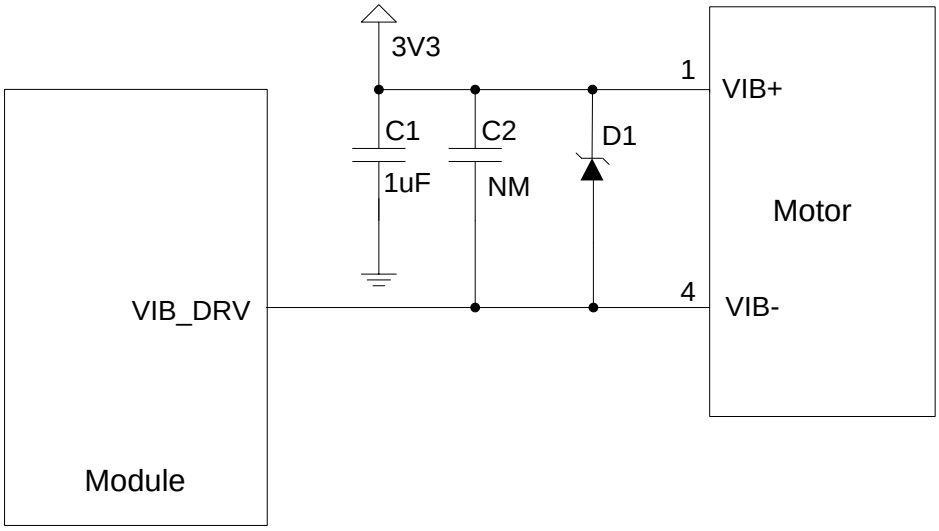


Figure 20: Reference Circuit for Motor Connection

When the motor stops, the redundant electricity can be discharged from the circuit loop formed by diodes, thus avoiding component damages.

3.18. LCM Interface

SC20 module provides an LCM interface meeting MIPI DSI specification. The interface supports high speed differential data transmission, with up to four lanes and a transmission rate up to 1.5Gbps per lane. It supports maximally 720P resolution displays.

Table 21: Pin Definition of LCM Interface

Pin Name	Pin No	I/O	Description	Comment
LDO6_1V8	125	PO	1.8V output power supply for LCM logic circuit and DSI	1.8V normal voltage. Vnorm=1.8V $I_O$max=100mA
LDO17_2V85	129	PO	2.85V output power supply for LCM analog circuits	2.85V normal voltage. Vnorm=2.85V $I_O$max=300mA
PWM	29	DO	Adjust the backlight brightness. PWM control signal.	
LCD_RST	49	DO	LCD reset signal	Active low
LCD_TE	50	DI	LCD tearing effect signal	
MIPI_DSI_CLKN	52	AO	MIPI DSI clock signal (negative)	
MIPI_DSI_CLKP	53	AO	MIPI DSI clock signal (positive)	
MIPI_DSI_LN0N	54	AO	MIPI DSI data signal (negative)	
MIPI_DSI_LN0P	55	AO	MIPI DSI data signal (positive)	
MIPI_DSI_LN1N	56	AO	MIPI DSI data signal (negative)	
MIPI_DSI_LN1P	57	AO	MIPI DSI data signal (positive)	
MIPI_DSI_LN2N	58	AO	MIPI DSI data signal (negative)	
MIPI_DSI_LN2P	59	AO	MIPI DSI data signal (positive)	
MIPI_DSI_LN3N	60	AO	MIPI DSI data signal (negative)	
MIPI_DSI_LN3P	61	AO	MIPI DSI data signal (positive)	

Four-lane MIPI DSI is needed for connection with 720P displays. The following is a reference circuit design, by taking the connection with LCM interface on LHR050H41-00 (IC: ILI9881C) from HUARUI Lighting as an example.

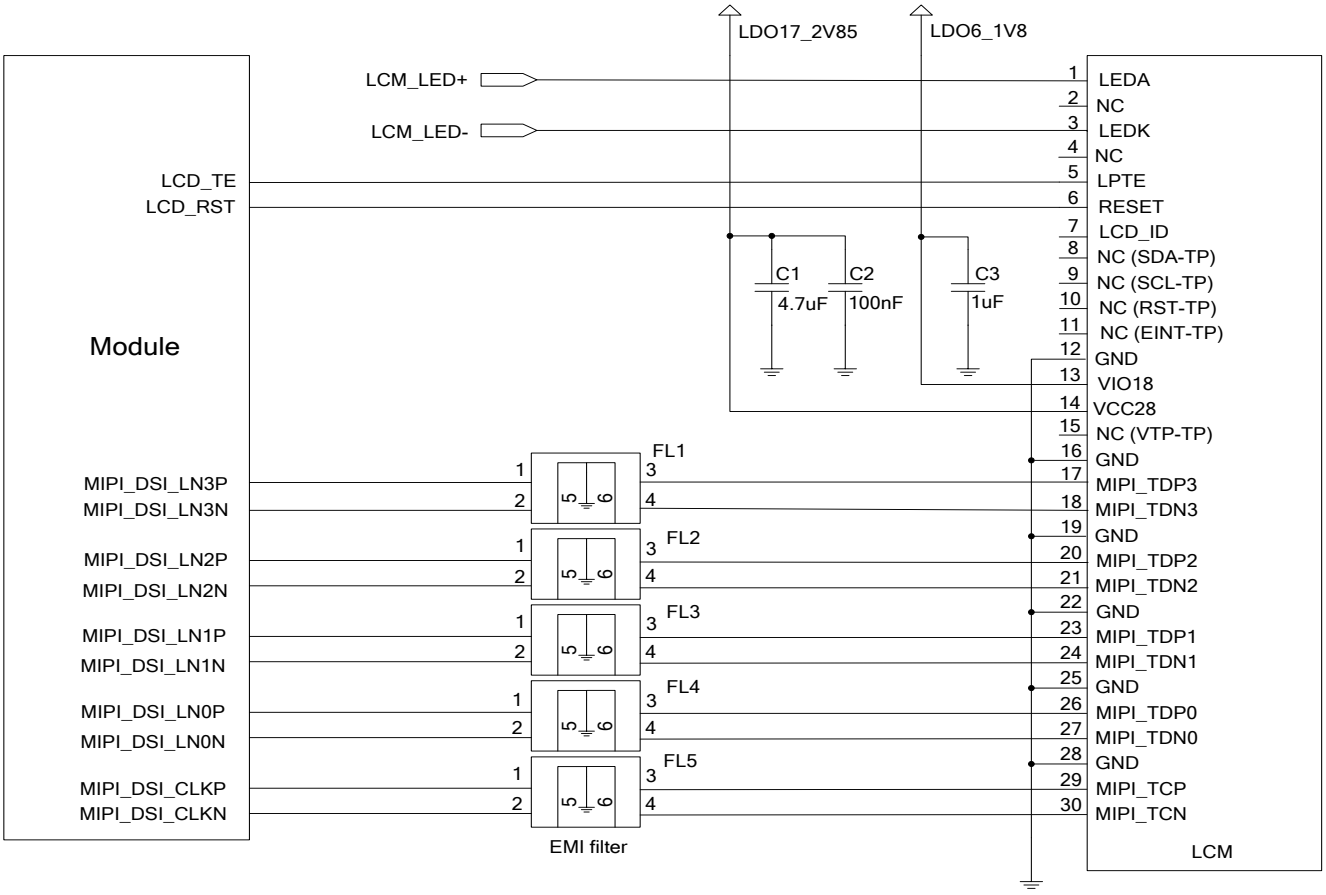


Figure 21: Reference Circuit Design for LCM Interface

MIPI are high speed signal lines. It is recommended that common-mode filters should be added in series near the LCM connector, so as to improve protection against electromagnetic radiation interference. ICMEF112P900MFR from ICT is recommended.

When compatible design with other displays is required, please connect the LCD_ID pin of LCM to the module's ADC pin, and please note that the output voltage of LCD_ID cannot exceed the voltage range of ADC pin.

External backlight driving circuit needs to be designed for LCM, and a reference circuit design is shown in the following figure. Backlight brightness adjustment can be realized by PWM pin of SC20 module through adjusting the duty ratio.

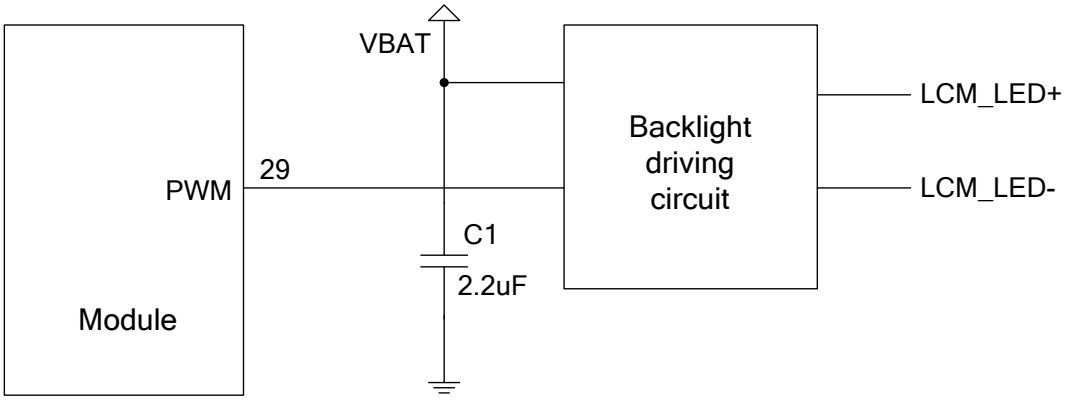


Figure 22: Reference Design for External Backlight Driving Circuit

3.19. Touch Panel Interface

SC20 provides a set of I2C interface for connection with Touch Panel (TP), and also provides the corresponding power supply and interrupt pins. The definition of TP interface pins is illustrated below.

Table 22: Pin Definition of Touch Panel Interface

Pin Name	Pin No	I/O	Description	Comment
LDO6_1V8	125	PO	1.8V output power supply for TP I/O power	Pull-up power supply of I2C. 1.8V normal voltage
LDO17_2V85	129	PO	2.85V output power supply for TP VDD power	TP power supply. 2.85V normal voltage
TP_INT	30	DI	Interrupt signal of TP	
TP_RST	31	DO	Reset signal of TP	Active low
TP_I2C_SCL	47	OD	I2C clock signal of TP	
TP_I2C_SDA	48	OD	I2C data signal of TP	

The following illustrates a TP interface reference circuit, by taking the connection with TP interface on LHR050H41-00 (IC: GT9147) from HUARUI Lighting as an example.

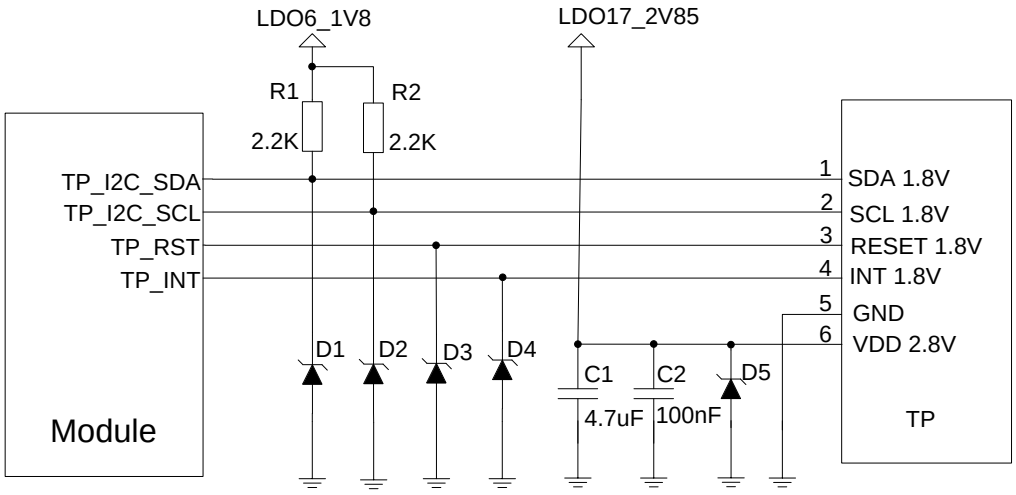


Figure 23: Reference Circuit Design for TP Interface

3.20. Camera Interfaces

Based on standard MIPI CSI video input interface, SC20 module supports two cameras, and the maximum pixel of the rear camera can be up to 8MP. The video and photo quality are determined by various factors such as the camera sensor, camera lens quality, etc. It is recommended to select a proper camera model, according to the specification of cameras verified and recommended by Quectel.

The following models of camera sensors have been verified by Quectel:

- For rear camera: Hi843 of SK Hynix, T4KA3 of TOSHIBA
- For front camera: Hi259 of SK Hynix, SP2508 of SuperPix

3.20.1. Rear Camera Interface

The rear camera realizes transmission and control via its FPC and a connector which is connected to the module. SC20 rear camera interface integrates a two-lane MIPI CSI for differential data transmission, and it maximally supports 8MP cameras.

The pin definition of rear camera interface is shown below.

Table 23: Pin Definition of Rear Camera Interface

Pin Name	Pin No	I/O	Description	Comment
LDO6_1V8	125	PO	1.8V output power supply for DOVDD of camera	1.8V normal voltage. Vnorm=1.8V

				$I_O$max=100mA
LDO17_2V85	129	PO	2.85V output power supply for AVDD of camera	2.85V normal voltage. Vnorm=2.85V $I_O$max=300mA
MIPI_CSI0_CLKN	63	AI	MIPI CSI clock signal (negative)	
MIPI_CSI0_CLKP	64	AI	MIPI CSI clock signal (positive)	
MIPI_CSI0_LN0N	65	AI	MIPI CSI data signal (negative)	
MIPI_CSI0_LN0P	66	AI	MIPI CSI data signal (positive)	
MIPI_CSI0_LN1N	67	AI	MIPI CSI data signal (negative)	
MIPI_CSI0_LN1P	68	AI	MIPI CSI data signal (positive)	
CAM0_MCLK	74	DO	Clock signal of rear camera	
CAM0_RST	79	DO	Reset signal of rear camera	
CAM0_PWD	80	DO	Power down signal of rear camera	
CAM_I2C_SCL	83	OD	I2C clock signal of camera	
CAM_I2C_SDA	84	OD	I2C data signal of camera	

The following is a reference circuit design for rear camera interface, by taking the connection with T4KA3 camera as an example.

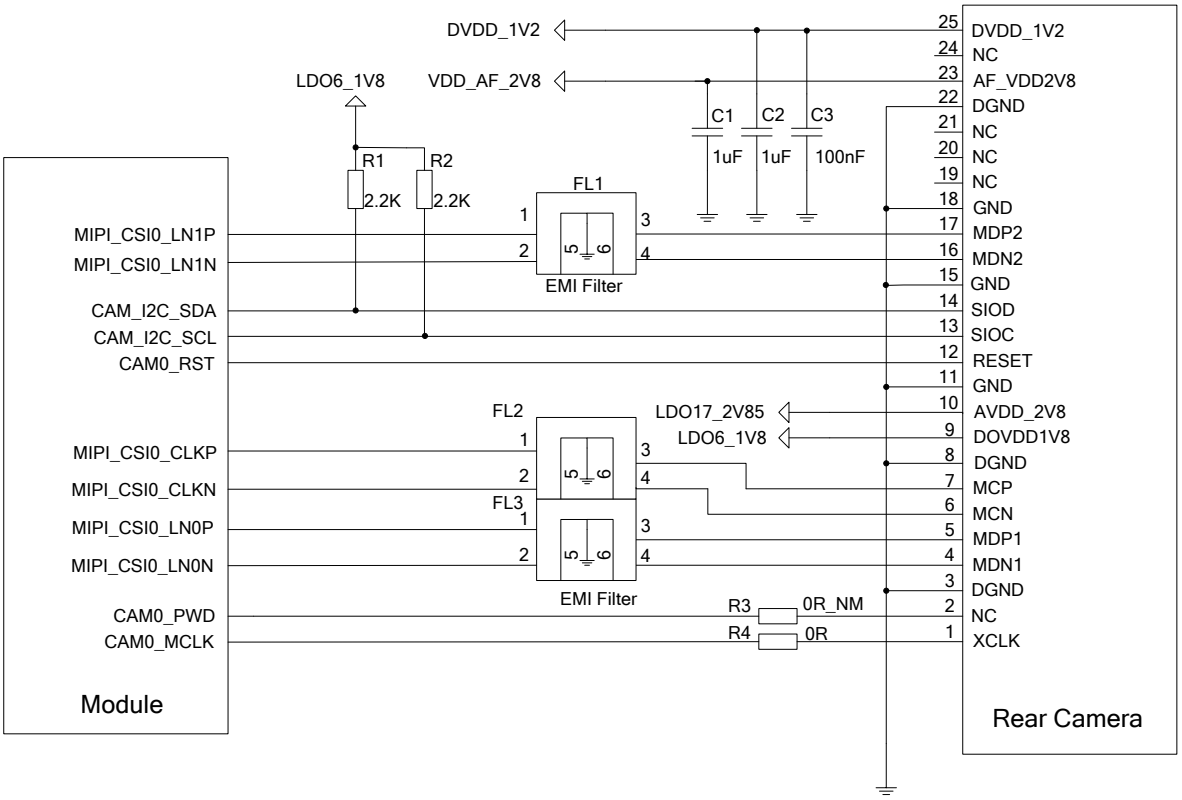


Figure 24: Reference Circuit Design for Rear Camera Interface

NOTE

DVDD_1V2 is used to power the rear camera core, and VDD_AF_2V8 is used to power the rear camera AF circuit. Both of them are powered by an external LDO.

3.20.2. Front Camera Interface

The front camera interface integrates a differential data interface meeting one-lane MIPI CSI standard, and is tested to support 2MP cameras.

The pin definition of front camera interface is shown below.

Table 24: Pin Definition of Front Camera Interface

Pin Name	Pin No	I/O	Description	Comment
LDO6_1V8	125	PO	1.8V output power supply for DOVDD of camera	1.8V normal voltage. Vnorm=1.8V $I_O$max=100mA

LDO17_2V85	129	PO	2.85V output power supply for AVDD of camera	2.85V normal voltage. Vnorm=2.85V $I_O$max=300mA
MIPI_CSI1_CLKN	70	AI	MIPI CSI clock signal (negative)	
MIPI_CSI1_CLKP	71	AI	MIPI CSI clock signal (positive)	
MIPI_CSI1_LN0N	72	AI	MIPI CSI data signal (negative)	
MIPI_CSI1_LN0P	73	AI	MIPI CSI data signal (positive)	
CAM1_MCLK	75	DO	Clock signal of front camera	
CAM1_RST	81	DO	Reset signal of front camera	
CAM1_PWD	82	DO	Power down signal of front camera	
CAM_I2C_SCL	83	OD	I2C clock signal of camera	
CAM_I2C_SDA	84	OD	I2C data signal of camera	

The following is a reference circuit design for front camera interface, by taking the connection with SP2508 camera as an example.

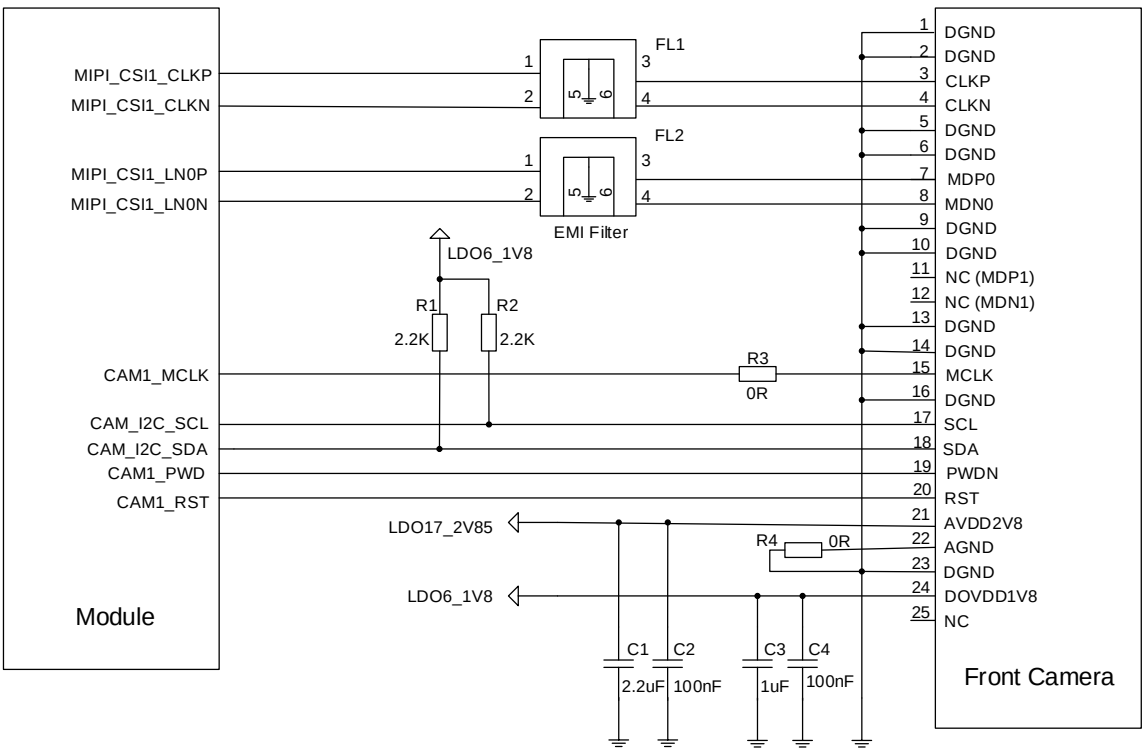


Figure 25: Reference Circuit Design for Front Camera Interface

3.20.3. Design Considerations

- Special attention should be paid to the definition of video device interface in schematic design. Different video devices will have varied definitions for their corresponding connectors. Assure the device and the connectors are correctly connected.
- MIPI are high speed signal lines, supporting maximum data rate up to 1.5Gbps. The differential impedance should be controlled as 100Ω. Additionally, it is recommended to route the trace on the inner layer of PCB, and do not cross it with other traces. For the same video device, all the MIPI traces should keep the same length. In order to avoid crosstalk, a distance of 1.5 times of the trace width is recommended to be maintained among MIPI signal lines. During impedance matching, do not connect GND on different planes so as to ensure impedance consistency.
- It is recommended to select a low capacitance TVS for ESD protection and the recommended parasitic capacitance is below 1pF.
- Route MIPI traces according to the following rules:
  a) The total trace length should not exceed 305mm;
  b) Control the differential impedance as 100Ω±10%;
  c) Control intra-lane length difference within 0.67mm;
  d) Control inter-lane length difference within 1.3mm.

Table 25: MIPI Trace Length Inside the Module

PIN	Pin Name	Length (mm)	Length Difference (P-N)
52	MIPI_DSI_CLKN	7.08	-0.63
53	MIPI_DSI_CLKP	6.45	
54	MIPI_DSI_LN0N	6.15	-0.30
55	MIPI_DSI_LN0P	5.85	
56	MIPI_DSI_LN1N	6.64	-0.04
57	MIPI_DSI_LN1P	6.60	
58	MIPI_DSI_LN2N	8.20	0.74
59	MIPI_DSI_LN2P	8.94	
60	MIPI_DSI_LN3N	9.28	0.96
61	MIPI_DSI_LN3P	10.24	
63	MIPI_CSI0_CLKN	10.55	0.54
64	MIPI_CSI0_CLKP	11.09	

65	MIPI_CSI0_LN0N	12.13	0.40
66	MIPI_CSI0_LN0P	12.53	
67	MIPI_CSI0_LN1N	13.73	0.76
68	MIPI_CSI0_LN1P	14.49	
70	MIPI_CSI1_CLKN	17.32	0.13
71	MIPI_CSI1_CLKP	17.45	
72	MIPI_CSI1_LN0N	18.89	0.35
73	MIPI_CSI1_LN0P	19.24	

3.21. Sensor Interfaces

SC20 module supports communication with sensors via I2C interfaces, and it supports ALS/PS, compass, G-sensor, and gyroscopic sensors.

Verified sensor models by Quectel include: BST-BMA223, STK3311-WV, MPU-6881 and MMC35240PJ.

Table 26: Pin Definition of Sensor Interfaces

Pin Name	Pin No	I/O	Description	Comment
SENSOR_I2C_SCL	91	OD	I2C clock signal for external sensor	
SENSOR_I2C_SDA	92	OD	I2C data signal for external sensor	
GPIO_88	99	DI	Gyroscope sensor interrupt signal 2	Default configuration; but not limited to these GPIO pins.
GPIO_89	100	DI	Gyroscope sensor interrupt signal 1	
GPIO_94	107	DI	Proximity sensor interrupt signal	
GPIO_36	108	DI	Compass sensor interrupt signal	
GPIO_65	109	DI	Gravity sensor interrupt signal 2	
GPIO_96	110	DI	Gravity sensor interrupt signal 1	

3.22. Audio Interfaces

SC20 module provides two analog input channels and three analog output channels. The following table shows the pin definition.

Table 27: Pin Definition of Audio Interfaces

Pin Name	Pin No	I/O	Description	Comment
MIC1P	4	AI	Microphone positive input for channel 1	
MIC_GND	5		MIC reference ground	
MIC2P	6	AI	Microphone positive input for channel 2	
EARP	8	AO	Earpiece positive output	
EARN	9	AO	Earpiece negative output	
SPKP	10	AO	Speaker positive output	
SPKN	11	AO	Speaker negative output	
HPH_R	136	AO	Headphone right channel output	
HPH_GND	137	AI	Headphone virtual ground	
HPH_L	138	AO	Headphone left channel output	
HS_DET	139	AI	Headset insertion detection	High level by default

- The module offers two audio input channels which are both single-ended channels.
- The earpiece interface uses differential output.
- The loudspeaker interface uses differential output as well. The output channel is available with a Class-D amplifier whose output power is 879mW when VBAT is 4.2V and load is 8Ω.
- The headphone interface features stereo left and right channel output, and headphone insert detection function is supported.

3.22.1. Reference Circuit Design for Microphone Interfaces

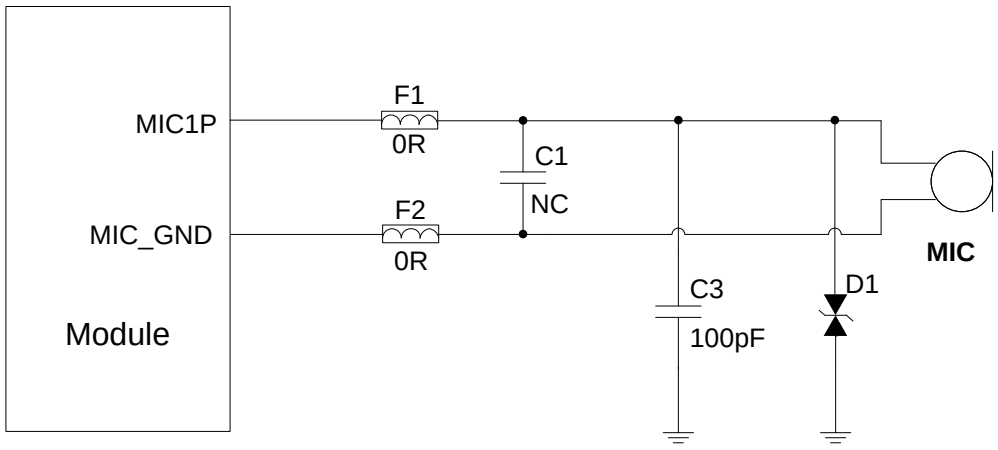


Figure 26: Reference Circuit Design for Microphone Interfaces

3.22.2. Reference Circuit Design for Receiver Interface

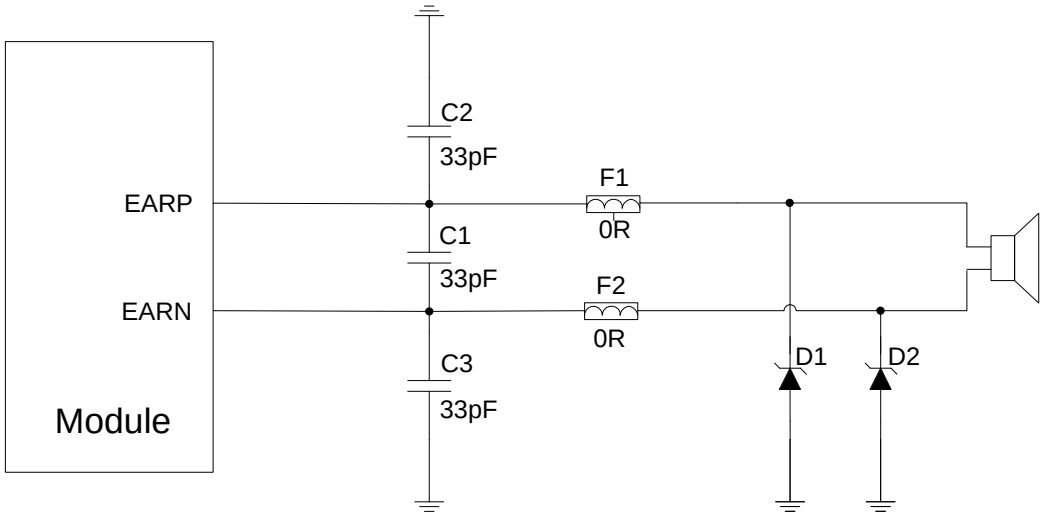


Figure 27: Reference Circuit Design for Receiver Interface

3.22.3. Reference Circuit Design for Headphone Interface

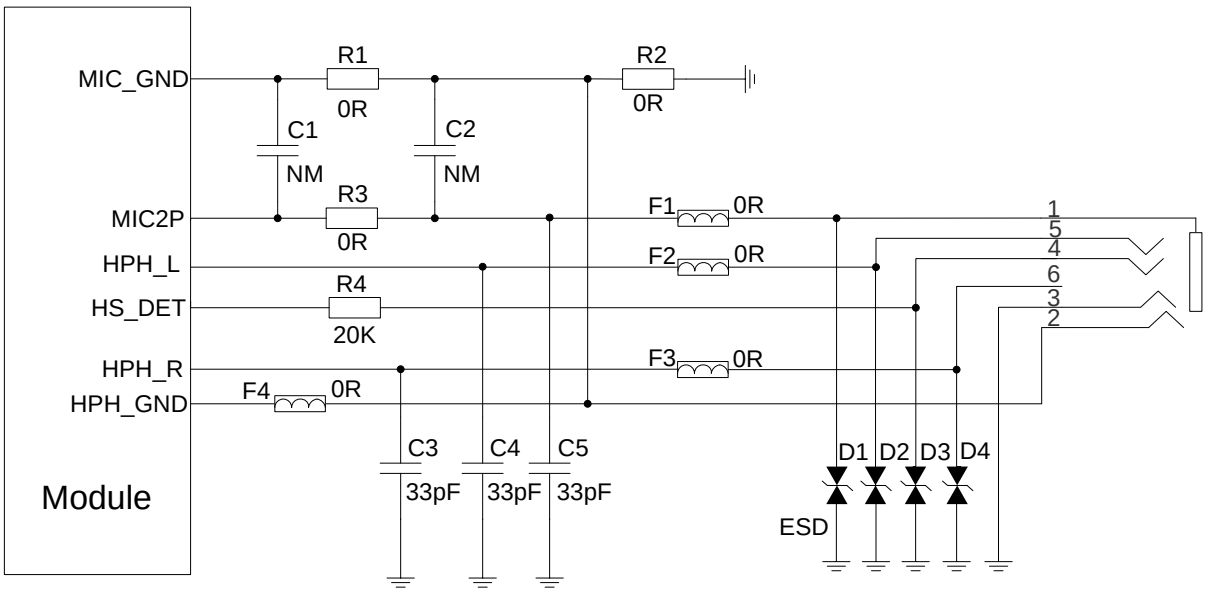


Figure 28: Reference Circuit Design for Headphone Interface

3.22.4. Reference Circuit Design for Loudspeaker Interface

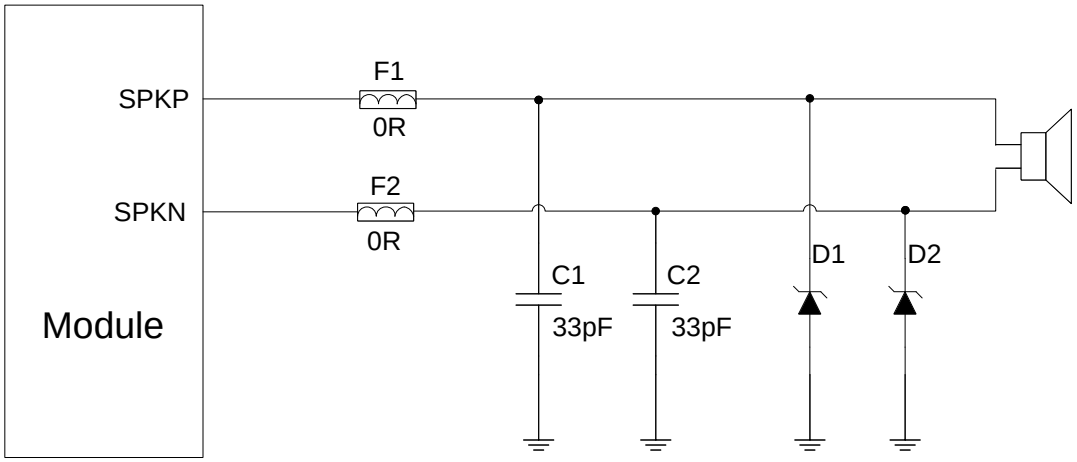


Figure 29: Reference Circuit Design for Loudspeaker Interface

3.22.5. Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10pF and 33pF) for filtering out RF interference, thus reducing TDD noise. The 33pF capacitor is applied for filtering out RF

interference when the module is transmitting at EGSM900MHz. Without placing this capacitor, TDD noise could be heard. Moreover, the 10pF capacitor here is used for filtering out 1800MHz RF interference. Please note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, customers would have to discuss with their capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. In some cases, EGSM900 TDD noise is more severe; while in other cases, DCS1800 TDD noise is more obvious. Therefore, a suitable capacitor can be selected based on the test results. Sometimes, even no RF filtering capacitor is required.

The capacitor which is used for filtering out RF noise should be close to the audio device or audio interface. The trace should be as short as possible, and it is recommended to route the trace for capacitors first and then for other points.

In order to decrease radio or other signal interference, RF antennas should be placed away from audio interfaces and audio traces. Power traces cannot be parallel with and also should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

3.23. Emergency Download Interface

USB_BOOT is an emergency download interface. Pull up to LDO5_1V8 during power-up will force the module enter into emergency download mode. This is an emergency option when there are failures such as abnormal startup or running. For convenient firmware upgrade and debugging in the future, please reverse this pin. The reference circuit design is shown as below.

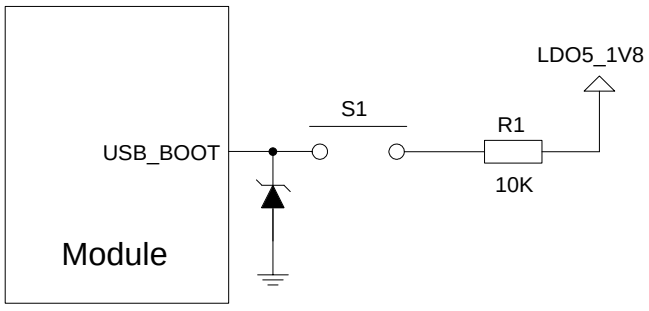


Figure 30: Reference Circuit Design for Emergency Download Interface

4 Wi-Fi and BT

SC20 module provides a shared antenna interface ANT_WIFI/BT for Wi-Fi and Bluetooth (BT) functions. The interface impedance is 50Ω. External antennas such as PCB antenna, sucker antenna and ceramic antenna can be connected to the module via the interface, so as to achieve Wi-Fi and BT functions.

4.1. Wi-Fi Overview

SC20 series module supports 2.4GHz/5GHz double-band WLAN wireless communication based on IEEE 802.11a/b/g/n standard protocols. The maximum data rate is up to 150Mbps.

The features are as below:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI SMS4 hardware encryption
- Support AP mode
- Support Wi-Fi Direct
- Support MCS 0-7 for HT20 and HT40

4.1.1. Wi-Fi Performance

The following table lists the Wi-Fi transmitting and receiving performance of SC20 module.

Table 28: Wi-Fi Receiving Performance

	Standard	Rate	Sensitivity
2.4GHz	802.11b	1Mbps	-96dBm
	802.11b	11Mbps	-87dBm
	802.11g	6Mbps	-91dBm
	802.11g	54Mbps	-74dBm

	802.11n HT20	MCS0	-90dBm
	802.11n HT20	MCS7	-72dBm
	802.11n HT40	MCS0	-87dBm
	802.11n HT40	MCS7	-68dBm
5GHz	802.11a	6Mbps	-90dBm
	802.11a	54Mbps	-71dBm
	802.11n HT20	MCS0	-88dBm
	802.11n HT20	MCS7	-69dBm
	802.11n HT40	MCS0	-86dBm
	802.11n HT40	MCS7	-66dBm

Referenced specifications are listed below:

- IEEE 802.11n WLAN MAC and PHY, October 2009 + IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- IEEE Std 802.11b, IEEE Std 802.11d, IEEE Std 802.11e, IEEE Std 802.11g, IEEE Std 802.11i: IEEE 802.11-2007 WLAN MAC and PHY, June 2007

4.2. BT Overview

SC20 module supports BT4.2 (BR/EDR+BLE) specification, as well as GFSK, 8-DPSK, π/4-DQPSK modulation modes.

- Maximally support up to 7 wireless connections.
- Maximally support up to 3.5 piconets at the same time.
- Support one SCO (Synchronous Connection Oriented) or eSCO connection.

The BR/EDR channel bandwidth is 1MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2MHz, and can accommodate 40 channels.

Table 29: BT Data Rate and Version

Version	Data rate	Maximum Application Throughput	Comment
1.2	1 Mbit/s	>80 Kbit/s	
2.0 + EDR	3 Mbit/s	>80 Kbit/s	
3.0 + HS	24 Mbit/s	Reference 3.0 + HS	
4.0	24 Mbit/s	Reference 4.0 LE	

Referenced specifications are listed below:

- Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 + HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009

5 GNSS

SC20 module integrates a Qualcomm IZat™ GNSS engine (GEN 8C) which supports multiple positioning and navigation systems including GPS, GLONASS and BeiDou. With an embedded LNA, the module provides greatly improved positioning accuracy.

5.1. GNSS Performance

The following table lists the GNSS performance of SC20 module in conduction mode.

Table 29: GNSS Performance

Parameter	Description	Typ.	Unit
Sensitivity (GNSS)	Cold start	-146	dBm
	Reacquisition	-157	dBm
	Tracking	-157	dBm
TTFF (GNSS)	Cold start	32	s
	Warm start	30	s
	Hot start	2	s
Static Drift (GNSS)	CEP-50	6	m

5.2. GNSS RF Design Guidelines

Bad design of antenna and layout may cause reduced GPS receiving sensitivity, longer GPS positioning time, or reduced positioning accuracy. In order to avoid this, please follow the reference design rules as below:

- Maximize the distance between the GNSS RF part and the GPRS RF part (including trace routing and antenna layout) to avoid mutual interference.
- In user systems, GNSS RF signal lines and RF components should be placed far away from high speed circuits, switched-mode power supplies, power inductors, the clock circuit of single-chip microcomputers, etc.
- For applications with harsh electromagnetic environment or with high requirement on ESD protection, it is recommended to add ESD protective diodes for the antenna interface. Only diodes with ultra-low junction capacitance such as 0.05pF can be selected. Otherwise, there will be effects on the impedance characteristic of RF circuit loop, or attenuation of bypass RF signal may be caused.
- Control the impedance of either feeder line or PCB trace as 50Ω, and keep the trace length as short as possible.
- Refer to ***Chapter 6.3*** for GNSS reference circuit design.

6 Antenna Interfaces

SC20 provides four antenna interfaces for main antenna, Rx-diversity/MIMO antenna, GNSS antenna and Wi-Fi/BT antenna, respectively. The antenna ports have an impedance of 50Ω.

6.1. Main/Rx-diversity Antenna Interfaces

The pin definition of main/Rx-diversity antenna interfaces is shown below.

Table 30: Pin Definition of Main/Rx-diversity Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	87	IO	Main antenna	50Ω impedance
ANT_DRX	131	AI	Diversity antenna	

6.1.1. Operating Frequency

Table 31: SC20-CE R1.1 Module Operating Frequencies

3GPP Band	Receive	Transmit	Unit
EGSM900	925~960	880~915	MHz
DCS1800	1805~1880	1710~1785	MHz
WCDMA B1	2110~2170	1920~1980	MHz
WCDMA B8	925~960	880~915	MHz
EVDO/CDMA BC0	869~894	824~849	MHz
TD-SCDMA B34	2010~2025	2010~2025	MHz
TD-SCDMA B39	1880~1920	1880~1920	MHz

LTE-FDD B1	2110~2170	1920~1980	MHz
LTE-FDD B3	1805~1880	1710~1785	MHz
LTE-FDD B5	869~894	824~849	MHz
LTE-FDD B8	925~960	880~915	MHz
LTE-TDD B38	2570~2620	2570~2620	MHz
LTE-TDD B39	1880~1920	1880~1920	MHz
LTE-TDD B40	2300~2400	2300~2400	MHz
LTE-TDD B41	2555~2655	2555~2655	MHz

Table 32: SC20-EL Module Operating Frequencies

3GPP Band	Receive	Transmit	Unit
GSM850	869~894	824~849	MHz
EGSM900	925~960	880~915	MHz
DCS1800	1805~1880	1710~1785	MHz
PCS1900	1930~1990	1850~1910	MHz
WCDMA B1	2110~2170	1920~1980	MHz
WCDMA B5	869~894	824~849	MHz
WCDMA B8	925~960	880~915	MHz
LTE-FDD B1	2110~2170	1920~1980	MHz
LTE-FDD B3	1805~1880	1710~1785	MHz
LTE-FDD B5	869~894	824~849	MHz
LTE-FDD B7	2620~2690	2500~2570	MHz
LTE-FDD B8	925~960	880~915	MHz
LTE-FDD B20	791~821	832~862	MHz
LTE-TDD B38	2570~2620	2570~2620	MHz

LTE-TDD B40	2300~2400	2300~2400	MHz
LTE-TDD B41	2555~2655	2555~2655	MHz

Table 33: SC20-AL Module Operating Frequencies

3GPP Band	Receive	Transmit	Unit
GSM850	869~894	824~849	MHz
PCS1900	1930~1990	1850~1910	MHz
WCDMA B1	2110~2170	1920~1980	MHz
WCDMA B2	1930~1990	1850~1910	MHz
WCDMA B4	2110~2155	1710~1755	MHz
WCDMA B5	869~894	824~849	MHz
WCDMA B8	925~960	880~915	MHz
LTE-FDD B2	1930~1990	1850~1910	MHz
LTE-FDD B4	2110~2155	1710~1755	MHz
LTE-FDD B5	869~894	824~849	MHz
LTE-FDD B7	2620~2690	2500~2570	MHz
LTE-FDD B12	729~746	699~716	MHz
LTE-FDD B13	746~756	777~787	MHz
LTE-FDD B25	1930~1995	1850~1915	MHz
LTE-FDD B26	859~894	814~849	MHz

Table 34: SC20-AUL Module Operating Frequencies

3GPP Band	Receive	Transmit	Unit
GSM850	869~894	824~849	MHz
EGSM900	925~960	880~915	MHz
DCS1800	1805~1880	1710~1785	MHz

PCS1900	1930~1990	1850~1910	MHz
WCDMA B1	2110~2170	1920~1980	MHz
WCDMA B2	1930~1990	1850~1910	MHz
WCDMA B5	869~894	824~849	MHz
WCDMA B8	925~960	880~915	MHz
LTE-FDD B1	2110~2170	1920~1980	MHz
LTE-FDD B3	1805~1880	1710~1785	MHz
LTE-FDD B5	869~894	824~849	MHz
LTE-FDD B7	2620~2690	2500~2570	MHz
LTE-FDD B8	925~960	880~915	MHz
LTE-FDD B28	758~803	703~748	MHz
LTE-TDD B40	2300~2400	2300~2400	MHz

Table 35: SC20-JL Module Operating Frequencies

3GPP Band	Receive	Transmit	Unit
WCDMA B1	2110~2170	1920~1980	MHz
WCDMA B6	875~885	830~840	MHz
WCDMA B8	925~960	880~915	MHz
WCDAM B19	875~890	830~845	MHz
LTE-FDD B1	2110~2170	1920~1980	MHz
LTE-FDD B3	1805~1880	1710~1785	MHz
LTE-FDD B8	925~960	880~915	MHz
LTE-FDD B18	860~875	815~830	MHz
LTE-FDD B19	875~890	830~845	MHz
LTE-FDD B26	859~894	814~849	MHz
LTE-TDD B41 [1)]	2545~2655	2545~2655	MHz

NOTE

[1] The bandwidth of LTE-TDD B41 for SC20-JL is 110MHz (2545MHz~2655MHz), and the corresponding channel range is 40140~41240.

6.1.2. Main and Rx-diversity Antenna Interfaces Reference Design

A reference circuit design for main and Rx-diversity antenna interfaces is shown as below. A π-type matching circuit should be reserved for better RF performance. The π-type matching components (R1/C1/C2, R2/C3/C4) should be placed as close to the antennas as possible and are mounted according to the actual debugging. C1, C2, C3 and C4 are not mounted and a 0Ω resistor is mounted on R1 and R2 respectively by default.

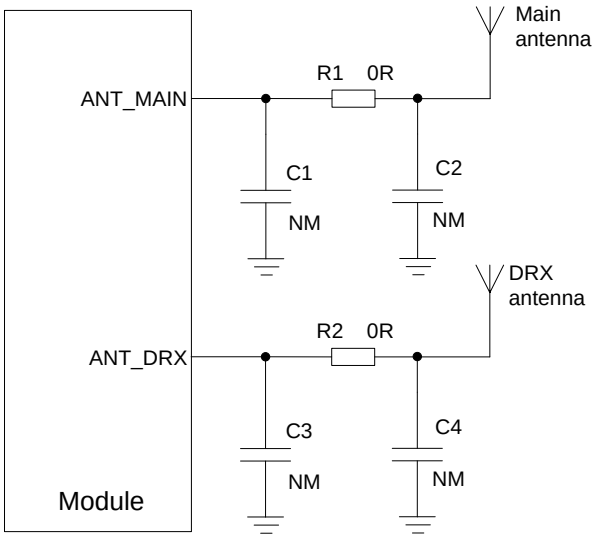


Figure 31: Reference Circuit Design for Main and Rx-diversity Antenna Interfaces

6.1.3. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the clearance between RF trace and ground (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

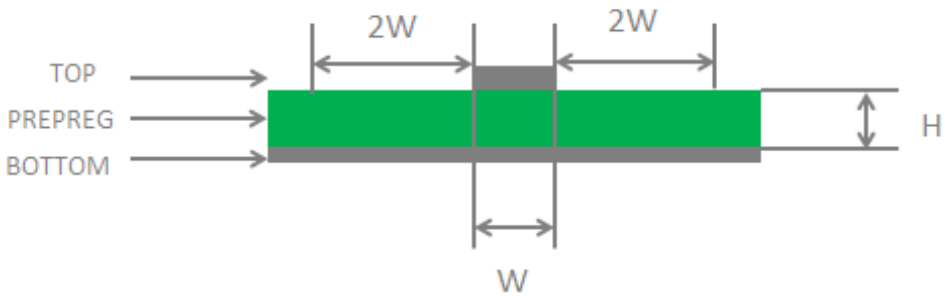


Figure 32: Microstrip Design on a 2-layer PCB

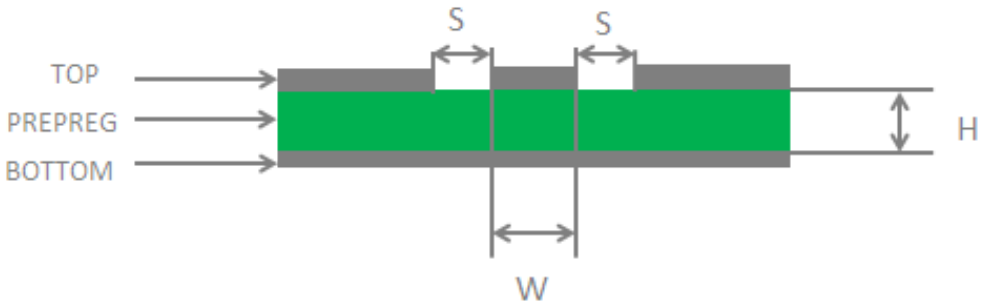


Figure 33: Coplanar Waveguide Design on a 2-layer PCB

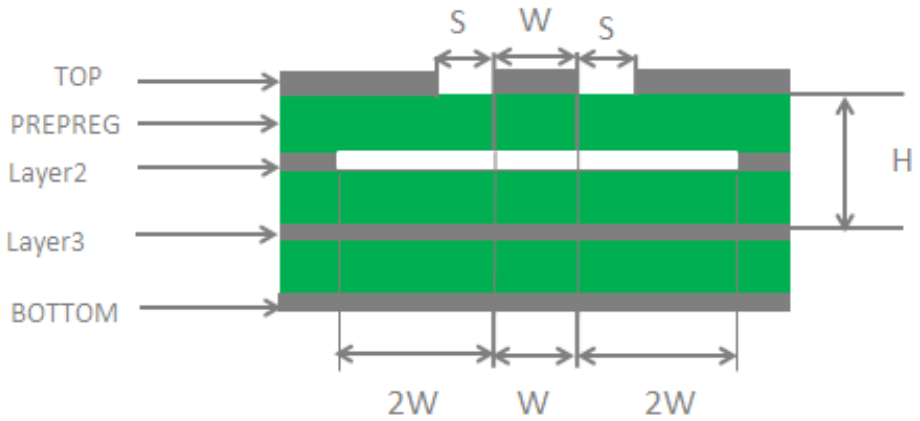


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

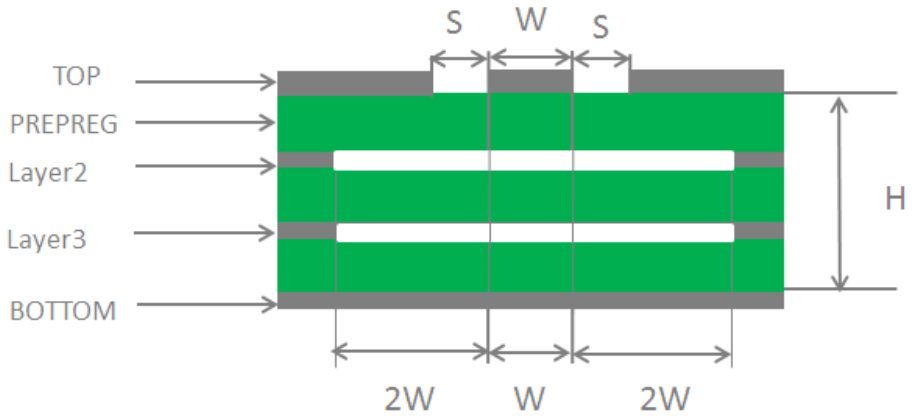


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times as wide as RF signal traces (2*W).

For more details about RF layout, please refer to ***document [2]***.

6.2. Wi-Fi/BT Antenna Interface

The following tables show the pin definition and frequency specification of the Wi-Fi/BT antenna interface.

Table 36: Pin Definition of Wi-Fi/BT Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI/BT	77	IO	Wi-Fi/BT antenna interface	50Ω impedance

Table 37: Wi-Fi/BT Frequency

Type	Frequency	Unit
802.11a/b/g/n	2400~2482 5180~5825	MHz
BT4.2 LE	2402~2480	MHz

NOTE

The supported Wi-Fi frequencies of SC20-JL are 2400MHz~2496MHz and 5180MHz~5825MHz.

A reference circuit design for Wi-Fi/BT antenna interface is shown as below. A π-type matching circuit should be reserved for better RF performance. The π-type matching components (R1, C1, C2) should be placed as close to the antenna as possible and are mounted according to the actual debugging. C1 and C2 are not mounted and a 0Ω resistor is mounted on R1 by default.

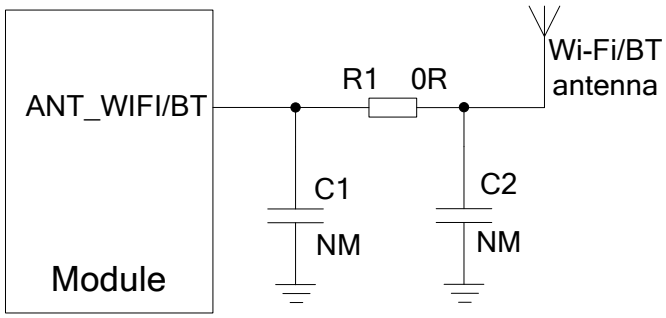


Figure 36: Reference Circuit Design for Wi-Fi/BT Antenna

6.3. GNSS Antenna Interface

The following tables show pin definition and frequency specification of GNSS antenna interface.

Table 38: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	121	AI	GNSS antenna interface	50Ω impedance

Table 39: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42±1.023	MHz
GLONASS	1597.5~1605.8	MHz
BeiDou	1561.098±2.046	MHz

6.3.1. Recommended Circuit for Passive Antenna

GNSS antenna interface supports passive ceramic antennas and other types of passive antennas. A reference circuit design is given below.

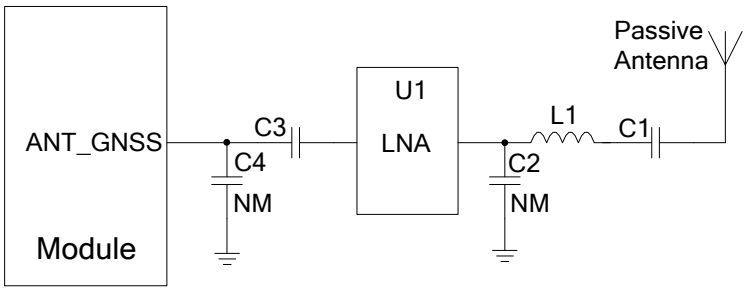


Figure 37: Reference Circuit Design for GNSS Passive Antenna

NOTE

When the passive antenna is placed far away from the module (that is, the antenna trace is long), it is recommended to add an external LNA circuit for better GNSS receiving performance, and the LNA should be placed close to the antenna.

6.3.2. Recommended Circuit for Active Antenna

The active antenna is powered by VCC power supply through the R1 and L1 power paths shown in the following figure. The common power supply voltage ranges from 3.3V to 5.0V. Although featuring low power consumption, the active antenna still requires stable and clean power supplies. It is recommended to use high performance LDO as the power supply. A reference design of GNSS active antenna is shown below.

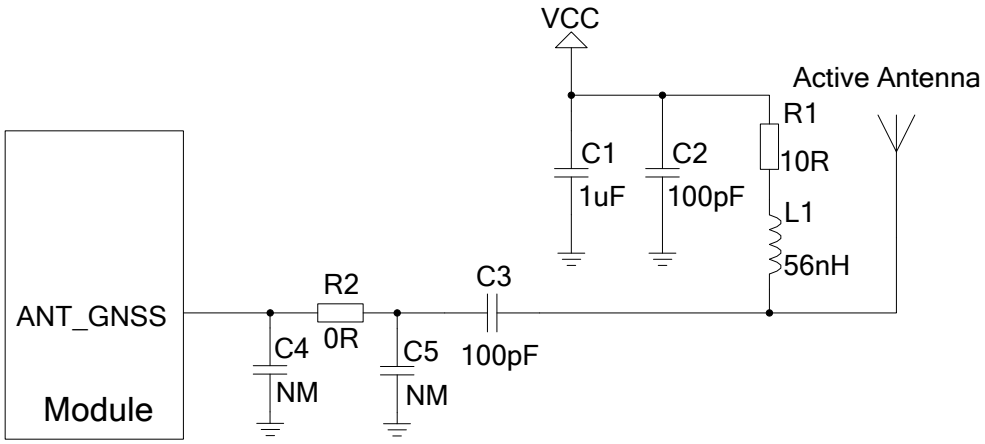


Figure 38: Reference Circuit Design for GNSS Active Antenna

6.4. Antenna Installation

6.4.1. Antenna Requirements

The following table shows the requirement on main antenna, RX-diversity antenna, Wi-Fi/BT antenna and GNSS antenna.

Table 40: Antenna Requirements

Type	Requirements
GSM/WCDMA/TD-SCDMA/ LTE	VSWR: ≤ 2 Gain (dBi): 1 Max Input Power (W): 50 Input Impedance (Ω): 50 Polarization Type: Vertical Cable Insertion Loss: < 1dB (GSM850, EGSM900, WCDMA B5/B6/B8/B19, EVDO/CDMA BC0, LTE-FDD B5/B8/B12/B13/B18/B19/B20/B26/B28) Cable Insertion Loss: < 1.5dB (DCS1800, PCS1900, WCDMA B1/B2/B4, TD-SCDMA B34/B39, LTE-FDD B1/B2/B3/B4/B25, LTE-TDD B39) Cable Insertion Loss: < 2dB (LTE-FDD B7, LTE-TDD B38/B40/B41)
Wi-Fi/BT	VSWR: ≤ 2 Gain (dBi): 1 Max Input Power (W): 50

	Input Impedance (Ω): 50 Polarization Type: Vertical Cable Insertion Loss: < 1dB
GNSS	Frequency range: 1559MHz~1609MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive Antenna Gain: > 0dBi Active Antenna Noise Figure: < 1.5dB Active Antenna Total Gain: < 17dBi (Typ.)

NOTE

[1] It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

6.4.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by HIROSE.

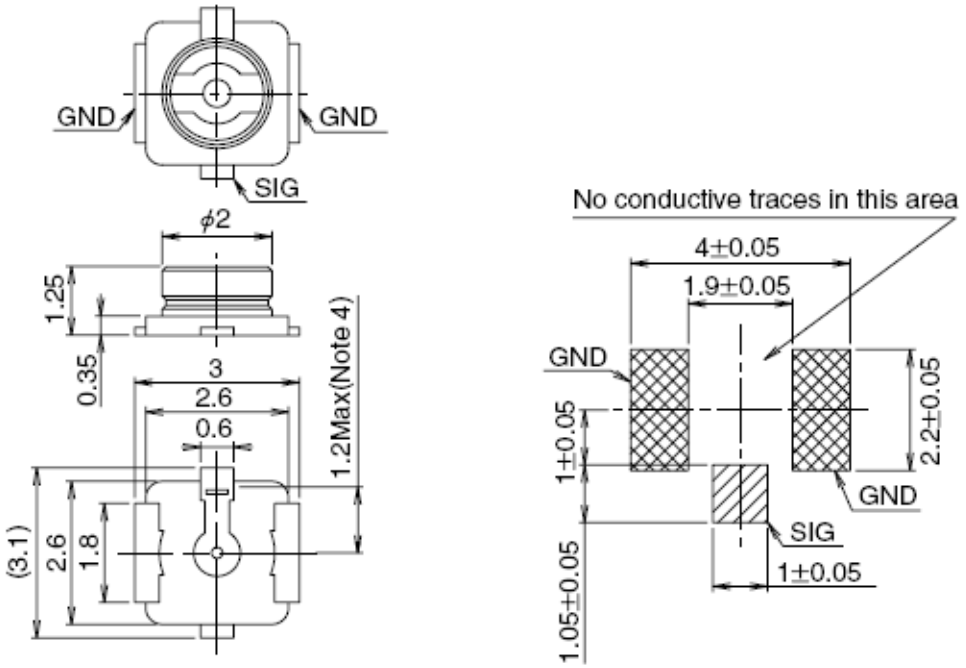


Figure 39: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

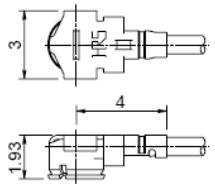
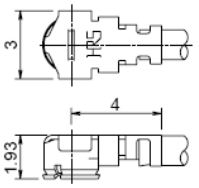
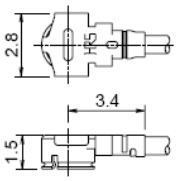
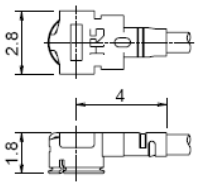
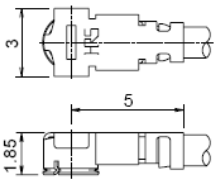
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 40: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

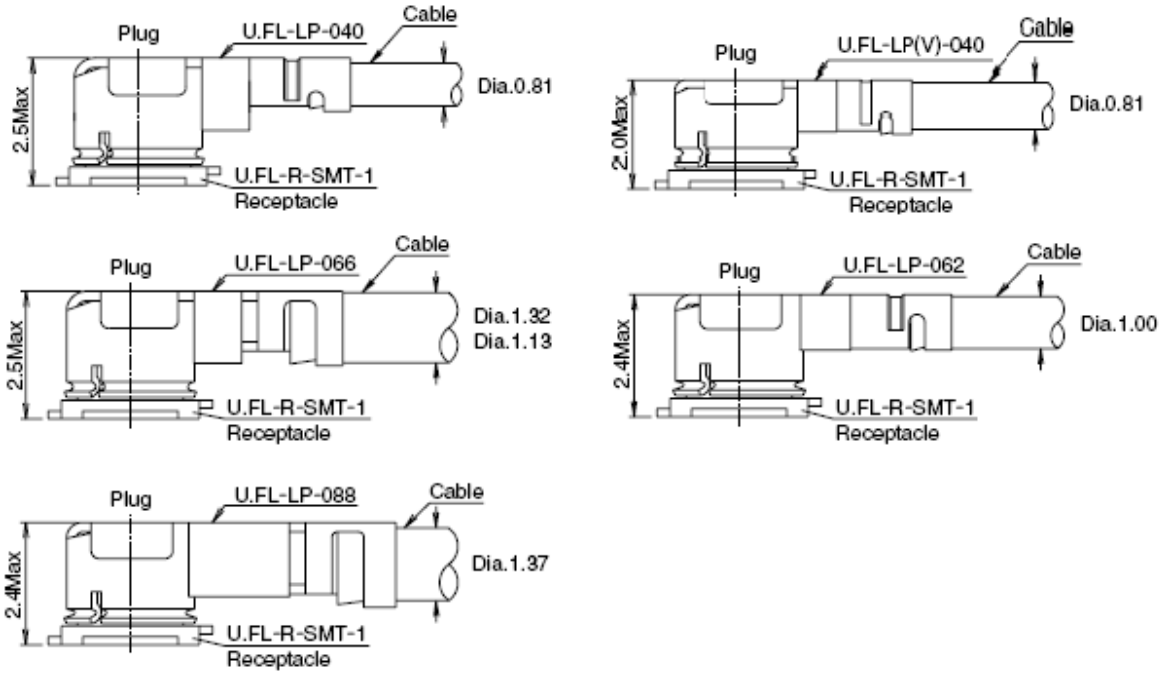


Figure 41: Space Factor of Mated Connectors (Unit: mm)

For more details, please visit http://www.hirose.com.

7 Electrical, Reliability and Radio Characteristics

7.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 41: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.5	6	V
USB_VBUS	-0.5	16	V
Peak Current of VBAT	0	3	A
Voltage on Digital Pins	-0.3	2.3	V

7.2. Power Supply Ratings

Table 42: SC20 Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT	The actual input voltages must stay between the minimum and maximum values.	3.5	3.8	4.2	V
	Voltage drop during transmitting burst	Maximum power control level at EGSM900.			400	mV

I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level at EGSM900.		1.8	3.0	A
USB_VBUS	USB detection		4.35	5.0	6.3	V
VRTC	Power supply voltage of backup battery.		2.0	3.0	3.25	V

7.3. Charging Performance Specifications

Table 43: Charging Performance Specifications

Parameter	Min.	Typ.	Max.	Unit
Trickle charging-A current	81	90	99	mA
Trickle charging-A threshold voltage range (15.62mV steps)	2.5	2.796	2.984	V
Trickle charging-B threshold voltage range (18.75mV steps)	3.0	3.2	3.581	V
Charge voltage range (25mV steps)	4	4.2	4.775	V
Charge voltage accuracy			+/-2	%
Charge current range (90mA steps)	90		1440	mA
Charge current accuracy			+/-10	%
Charge termination current: when charge current is from 90mA to 450mA		7		%
Charge termination current: when charge current is from 450mA to 1440mA		7.4		%

7.4. Operation and Storage Temperatures

The operating temperature is listed in the following table.

Table 44: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating temperature range [1)]	-35	+25	+65	ºC
Extended temperature range [2)]	-40		+75	ºC
Storage Temperature Range	-40		+90	ºC

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

7.5. Current Consumption

The values of current consumption are shown below.

Table 45: SC20-CE R1.1 Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	20	uA
	GSM/GPRS supply current	Sleep (USB disconnected) @DRX=2	3.85	mA
		Sleep (USB disconnected) @DRX=5	3.01	mA
		Sleep (USB disconnected) @DRX=9	2.91	mA

	WCDMA supply current	Sleep (USB disconnected) @DRX=6	3.30	mA
		Sleep (USB disconnected) @DRX=7	2.79	mA
		Sleep (USB disconnected) @DRX=8	2.49	mA
		Sleep (USB disconnected) @DRX=9	2.33	mA
	LTE-FDD supply current	Sleep (USB disconnected) @DRX=5	5.60	mA
		Sleep (USB disconnected) @DRX=6	3.83	mA
		Sleep (USB disconnected) @DRX=7	3.02	mA
		Sleep (USB disconnected) @DRX=8	2.65	mA
	LTE-TDD supply current	Sleep (USB disconnected) @DRX=5	5.49	mA
		Sleep (USB disconnected) @DRX=6	3.87	mA
		Sleep (USB disconnected) @DRX=7	3.05	mA
		Sleep (USB disconnected) @DRX=8	2.67	mA
	GSM voice call	EGSM900 PCL=5 @31.84dBm	290	mA
		EGSM900 PCL=12 @18.49dBm	150	mA
		EGSM900 PCL=19 @4.95dBm	104	mA
		DCS1800 PCL=0 @28.91dBm	220	mA
		DCS1800 PCL=7 @15.35dBm	150	mA
		DCS1800 PCL=15 @-0.21dBm	120	mA
	EVDO/CDMA voice call	BC0 (max power) @23.91dBm	560	mA
		BC0 (min power) @-60.28dBm	190	mA
	WCDMA voice call	B1 (max power) @22.61dBm	560	mA

		B8 (max power) @22.74dBm	580	mA
	EDGE data transfer	EGSM900 (1UL/4DL) @26.29dBm	220	mA
		EGSM900 (2UL/3DL) @26.15dBm	330	mA
		EGSM900 (3UL/2DL) @26.06dBm	420	mA
		EGSM900 (4UL/1DL) @25.92dBm	530	mA
		DCS1800 (1UL/4DL) @24.89dBm	180	mA
		DCS1800 (2UL/3DL) @24.74dBm	270	mA
		DCS1800 (3UL/2DL) @24.54dBm	360	mA
		DCS1800 (4UL/1DL) @24.44dBm	450	mA
	EVDO/CDMA data transfer	BC0 (max power) @23.68dBm	560	mA
	WCDMA data transfer	B1 (HSDPA) @21.64dBm	540	mA
		B8 (HSDPA) @21.61dBm	540	mA
		B1 (HSUPA) @21.36dBm	560	mA
		B8 (HSUPA) @21.56dBm	550	mA
	LTE data transfer	LTE-FDD B1 @22.96dBm	750	mA
		LTE-FDD B3 @22.95dBm	700	mA
		LTE-FDD B5 @22.90dBm	680	mA
		LTE-FDD B8 @23.17dBm	680	mA
		LTE-TDD B38 @22.02dBm	400	mA
		LTE-TDD B39 @22.13dBm	410	mA
		LTE-TDD B40 @22.01dBm	410	mA
		LTE-TDD B41 @22.31dBm	400	mA

Table 46: SC20-EL Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	20	uA
	GSM/GPRS supply current	Sleep (USB disconnected) @DRX=2	3.58	mA
		Sleep (USB disconnected) @DRX=5	2.46	mA
		Sleep (USB disconnected) @DRX=9	2.13	mA
	WCDMA supply current	Sleep (USB disconnected) @DRX=6	2.99	mA
		Sleep (USB disconnected) @DRX=7	2.35	mA
		Sleep (USB disconnected) @DRX=8	2.01	mA
		Sleep (USB disconnected) @DRX=9	1.85	mA
	LTE-FDD supply current	Sleep (USB disconnected) @DRX=5	5.51	mA
		Sleep (USB disconnected) @DRX=6	3.56	mA
		Sleep (USB disconnected) @DRX=7	2.62	mA
		Sleep (USB disconnected) @DRX=8	2.14	mA
	LTE-TDD supply current	Sleep (USB disconnected) @DRX=5	5.93	mA
		Sleep (USB disconnected) @DRX=6	3.74	mA
		Sleep (USB disconnected) @DRX=7	2.70	mA
		Sleep (USB disconnected) @DRX=8	2.17	mA
	GSM voice call	GSM850 PCL=5 @33.13dBm	263.8	mA
		GSM850 PCL=12 @19.15dBm	134.7	mA
		GSM850 PCL=19 @5.31dBm	109.2	mA

		EGSM900 PCL=5 @33.07dBm	271.2	mA
		EGSM900 PCL=12 @19.53dBm	137.3	mA
		EGSM900 PCL=19 @5.59dBm	110.6	mA
		DCS1800 PCL=0 @30.00dBm	203.0	mA
		DCS1800 PCL=7 @16.45dBm	150.7	mA
		DCS1800 PCL=15 @0.67dBm	130.8	mA
		PCS1900 PCL=0 @29.72dBm	195.9	mA
		PCS1900 PCL=7 @16.72dBm	151.3	mA
		PCS1900 PCL=15 @0.98dBm	130.0	mA
	WCDMA voice call	B1 (max power) @23.18dBm	544.1	mA
		B5 (max power) @23.22dBm	513.5	mA
		B8 (max power) @23.29dBm	522.7	mA
	GPRS data transfer	GSM850 (1UL/4DL) @33.12dBm	265.9	mA
		GSM850 (2UL/3DL) @33.02dBm	435.1	mA
		GSM850 (3UL/2DL) @30.50dBm	478.8	mA
		GSM850 (4UL/1DL) @29.49dBM	564.0	mA
		EGSM900 (1UL/4DL) @33.10dBm	272.7	mA
		EGSM900 (2UL/3DL) @33.00dBm	445.0	mA
		EGSM900 (3UL/2DL) @30.96dBm	512.0	mA
		EGSM900 (4UL/1DL) @29.93dBm	599.2	mA
		DCS1800 (1UL/4DL) @29.96dBm	205.8	mA

		DCS1800 (2UL/3DL) @29.86dBm	314.3	mA
		DCS1800 (3UL/2DL) @29.73dBm	420.8	mA
		DCS1800 (4UL/1DL) @29.63dBm	531.7	mA
		PCS1900 (1UL/4DL) @29.77dBm	199.3	mA
		PCS1900 (2UL/3DL) @29.64dBm	307.2	mA
		PCS1900 (3UL/2DL) @29.54dBm	411.5	mA
		PCS1900 (4UL/1DL) @29.34dBm	518.7	mA
	EDGE data transfer	GSM850 (1UL/4DL) @26.75dBm	172.2	mA
		GSM850 (2UL/3DL) @27.13dBm	266.6	mA
		GSM850 (3UL/2DL) @26.63dBm	353.1	mA
		GSM850 (4UL/1DL) @26.54dBm	446.9	mA
		EGSM900 (1UL/4DL) @27.05dBm	182	mA
		EGSM900 (2UL/3DL) @27.13dBm	177.4	mA
		EGSM900 (3UL/2DL) @27.28dBm	278.3	mA
		EGSM900 (4UL/1DL) @27.19dBm	371.0	mA
		DCS1800 (1UL/4DL) @26.04dBm	170.6	mA
		DCS1800 (2UL/3DL) @25.98dBm	260.5	mA
		DCS1800 (3UL/2DL) @25.71dBm	349.8	mA
		DCS1800 (4UL/1DL) @25.46dBm	440.2	mA
		PCS1900 (1UL/4DL) @26.14dBm	171.0	mA
		PCS1900 (2UL/3DL) @26.11dBm	260.5	mA

		PCS1900 (3UL/2DL) @26.11dBm	349.6	mA
		PCS1900 (4UL/1DL) @25.70dBm	442.3	mA
	WCDMA data transfer	B1 (HSDPA) @22.43dBm	503.8	mA
		B5 (HSDPA) @22.23dBm	471.6	mA
		B8 (HSDPA) @22.24dBm	481.6	mA
		B1 (HSUPA) @22.30dBm	504.6	mA
		B5 (HSUPA) @21.93dBm	460.5	mA
		B8 (HSUPA) @21.90dBm	464.8	mA
	LTE data transfer	LTE-FDD B1 @23.29dBm	737	mA
		LTE-FDD B3 @23.29dBm	756	mA
		LTE-FDD B5 @23.44dBm	636	mA
		LTE-FDD B7 @23.28dBm	842	mA
		LTE-FDD B8 @23.44dBm	639	mA
		LTE-FDD B20 @23.36dBm	684	mA
		LTE-TDD B38 @23.19dBm	427	mA
		LTE-TDD B40 @23.17dBm	427	mA
		LTE-TDD B41 @23.19dBm	455	mA

Table 47: SC20-AL Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	20	uA
	GSM/GPRS supply current	Sleep USB disconnected) @DRX=2	4.08	mA

		Sleep (USB disconnected) DRX=5	3.10	mA
		Sleep (USB disconnected) DRX=9	2.77	mA
	WCDMA supply current	Sleep (USB disconnected) DRX=6	3.86	mA
		Sleep (USB disconnected) DRX=7	2.90	mA
		Sleep (USB disconnected) DRX=8	2.55	mA
		Sleep (USB disconnected) DRX=9	2.43	mA
	FDD-LTE supply current	Sleep (USB disconnected) DRX=5	6.60	mA
		Sleep (USB disconnected) DRX=6	4.24	mA
		Sleep (USB disconnected) DRX=7	3.11	mA
		Sleep (USB disconnected) DRX=8	2.77	mA
	GSM voice call	GSM850 PCL=5 @32.23dBm	254.60	mA
		GSM850 PCL=12 @18.34dBm	136.30	mA
		GSM850 PCL=19 @4.87dBm	111.30	mA
		PCS1900 PCL=0 @29.14dBm	196.60	mA
		PCS1900 PCL=7 @16.23dBm	158.40	mA
		PCS1900 PCL=15 @0.62dBm	135.50	mA
	WCDMA voice call	B1 (max power) @23.24dBm	548.13	mA
		B2 (max power) @23.40dBm	575.70	mA
		B4 (max power) @23.20dBm	561.35	mA
		B5 (max power) @23.47dBm	558.00	mA
		B8 (max power) @23.5dBm	557.10	mA
	GPRS data transfer	GSM850 (1UL/4DL) @32.18dBm	254.50	mA

		GSM850 (2UL/3DL) @32.00dBm	410.70	mA
		GSM850 (3UL/2DL) @30.43dBm	496.10	mA
		GSM850 (4UL/1DL) @29.37dBm	573.90	mA
		PCS1900 (1UL/4DL) @29.13dBm	198.70	mA
		PCS1900 (2UL/3DL) @29.19dBm	306.50	mA
		PCS1900 (3UL/2DL) @29.05dBm	408.90	mA
		PCS1900 (4UL/1DL) @28.84dBm	514.60	mA
	EDGE data transfer	GSM850 (1UL/4DL) @26.39dBm	186.00	mA
		GSM850 (2UL/3DL) @26.30dBm	280.00	mA
		GSM850 (3UL/2DL) @26.30dBm	368.00	mA
		GSM850 (4UL/1DL) @26.07dBm	456.00	mA
		PCS1900 (1UL/4DL) @25.70dBm	184.40	mA
		PCS1900 (2UL/3DL) @25.55dBm	276.60	mA
		PCS1900 (3UL/2DL) @25.39dBm	365.20	mA
		PCS1900 (4UL/1DL) @25.17dBm	456.50	mA
	WCDMA data transfer	B1 (HSDPA) @22.24dBm	506.35	mA
		B2 (HSDPA) @22.44dBm	535.10	mA
		B4 (HSDPA) @22.23dBm	523.07	mA
		B5 (HSDPA) @22.38dBm	513.13	mA
		B8 (HSDPA) @22.47dBm	512.30	mA
		B1 (HSUPA) @22.2dBm	516.00	mA

		B2 (HSUPA) @22.4dBm	545.60	mA
		B4 (HSUPA) @21.93dBm	527.93	mA
		B5 (HSUPA) @22.26dBm	528.94	mA
		B8 (HSUPA) @22 dBm	507.70	mA
	LTE data transfer	LTE-FDD B2 @23.05dBm	710.01	mA
		LTE-FDD B4 @23.3dBm	736.50	mA
		LTE-FDD B5 @23.13dBm	626.18	mA
		LTE-FDD B7 @22.75dBm	733.40	mA
		LTE-FDD B12 @22.74dBm	606.02	mA
		LTE-FDD B13 @23.3dBm	674.84	mA
		LTE-FDD B25 @23.2dBm	665.62	mA
		LTE-FDD B26 @23.57dBm	718.75	mA

Table 48: SC20-AUL Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	20	uA
	GSM/GPRS supply current	Sleep (USB disconnected) DRX=2	3.31	mA
		Sleep (USB disconnected) DRX=5	2.30	mA
		Sleep (USB disconnected) DRX=9	2.01	mA
	WCDMA supply current	Sleep (USB disconnected) DRX=6	2.79	mA
		Sleep (USB disconnected) DRX=7	2.21	mA
		Sleep (USB disconnected)	1.90	mA

		DRX=8		
		Sleep (USB disconnected) DRX=9	1.75	mA
	LTE-FDD supply current	Sleep (USB disconnected) DRX=5	5.29	mA
		Sleep (USB disconnected) DRX=6	3.59	mA
		Sleep (USB disconnected) DRX=7	2.76	mA
		Sleep (USB disconnected) DRX=8	2.24	mA
	LTE-TDD supply current	Sleep (USB disconnected) DRX=5	5.52	mA
		Sleep (USB disconnected) DRX=6	3.71	mA
		Sleep (USB disconnected) DRX=7	2.76	mA
		Sleep (USB disconnected) DRX=8	2.28	mA
	GSM voice call	GSM850 PCL=5 @32.96dBm	268	mA
		GSM850 PCL=12 @18.83dBm	133	mA
		GSM850 PCL=19 @5.31dBm	109	mA
		EGSM900 PCL=5 @32.96dBm	267	mA
		EGSM900 PCL=12 @19.21dBm	137	mA
		EGSM900 PCL=19 @5.60dBm	108	mA
		DCS1800 PCL=0 @29.93dBm	202	mA
		DCS1800 PCL=7 @16.29dBm	152	mA
		DCS1800 PCL=15 @0.62dBm	131	mA
		PCS1900 PCL=0 @29.67dBm	194	mA
		PCS1900 PCL=7 @16.74dBm	149	mA

		PCS1900 PCL=15 @1.09dBm	130	mA
	WCDMA voice call	B1 (max power) @23.33dBm	561	mA
		B2 (max power) @23.51dBm	521	mA
		B5 (max power) @23.37dBm	551	mA
		B8 (max power) @23.38dBm	478	mA
	GPRS data transfer	GSM850 (1UL/4DL) @32.91dBm	267	mA
		GSM850 (2UL/3DL) @32.26dBm	388	mA
		GSM850 (3UL/2DL) @30.72dBm	503	mA
		GSM850 (4UL/1DL) @29.38dBm	574	mA
		EGSM900 (1UL/4DL) @32.92dBm	266	mA
		EGSM900 (2UL/3DL) @32.74dBm	396	mA
		EGSM900 (3UL/2DL) @30.85dBm	509	mA
		EGSM900 (4UL/1DL) @29.58dBm	583	mA
		DCS1800 (1UL/4DL) @39.81dBm	205	mA
		DCS1800 (2UL/3DL) @39.70dBm	316	mA
		DCS1800 (3UL/2DL) @29.50dBm	398	mA
		DCS1800 (4UL/1DL) @29.34dBm	530	mA
		PCS1900 (1UL/4DL) @29.58dBm	182	mA
		PCS1900 (2UL/3DL) @29.48dBm	285	mA
		PCS1900 (3UL/2DL) @29.31dBm	385	mA
		PCS1900 (4UL/1DL) @29.40dBm	498	mA

		GSM850 (1UL/4DL) @26.70dBm	166	mA
		GSM850 (2UL/3DL) @27.02dBm	300	mA
		GSM850 (3UL/2DL) @26.60dBm	389	mA
		GSM850 (4UL/1DL) @26.33dBm	457	mA
		EGSM900 (1UL/4DL) @26.87dBm	178	mA
		EGSM900 (2UL/3DL) @27.27dBm	276	mA
		EGSM900 (3UL/2DL) @26.85dBm	394	mA
		EGSM900 (4UL/1DL) @26.53dBm	490	mA
	EDGE data transfer	DCS1800 (1UL/4DL) @25.39dBm	197	mA
		DCS1800 (2UL/3DL) @25.40dBm	287	mA
		DCS1800 (3UL/2DL) @25.35dBm	373	mA
		DCS1800 (4UL/1DL) @25.05dBm	461	mA
		PCS1900 (1UL/4DL) @26.03dBm	168	mA
		PCS1900 (2UL/3DL) @26.07dBm	257	mA
		PCS1900 (3UL/2DL) @25.81dBm	345	mA
		PCS1900 (4UL/1DL) @25.70dBm	436	mA
		B1 (HSDPA) @23.02dBm	517	mA
		B2 (HSDPA) @23.11dBm	550	mA
	WCDMA data transfer	B5 (HSDPA) @22.68dBm	486	mA
		B8 (HSDPA) @22.72dBm	466	mA
		B1 (HSUPA) @22.39dBm	521	mA

		B2 (HSUPA) @23.19dBm	509	mA
		B5 (HSUPA) @22.44dBm	503	mA
		B8 (HSUPA) @22.25dBm	474	mA
	LTE data transfer	LTE-FDD B1 @23.37dBm	698	mA
		LTE-FDD B3 @23.06dBm	709	mA
		LTE-FDD B5 @23.25dBm	643	mA
		LTE-FDD B7 @22.82dBm	802	mA
		LTE-FDD B8 @23.47dBm	620	mA
		LTE-FDD B28 @23.13dBm	756	mA
		LTE-TDD B40 @23.24dBm	388	mA

Table 49: SC20-JL Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	20	uA
	WCDMA supply current	Sleep (USB disconnected) DRX=6	3.07	mA
		Sleep (USB disconnected) DRX=7	2.41	mA
		Sleep (USB disconnected) DRX=8	2.11	mA
		Sleep (USB disconnected) DRX=9	1.95	mA
	LTE-FDD supply current	Sleep (USB disconnected) DRX=5	5.17	mA
		Sleep (USB disconnected) DRX=6	3.50	mA
		Sleep (USB disconnected) DRX=7	2.60	mA
		Sleep (USB disconnected)	2.16	mA

		DRX=8		
	LTE-TDD supply current	Sleep (USB disconnected) DRX=5	5.40	mA
		Sleep (USB disconnected) DRX=6	3.53	mA
		Sleep (USB disconnected) DRX=7	2.62	mA
		Sleep (USB disconnected) DRX=8	2.17	mA
	WCDMA voice call	B1 (max power) @22.80dBm	460	mA
		B6 (max power) @23.09dBm	505	mA
		B8 (max power) @23.02dBm	504	mA
		B19 (max power) @23.07dBm	505	mA
	WCDMA data transfer	B1 (HSDPA) @22.13dBm	482	mA
		B6 (HSDPA) @22.05dBm	477	mA
		B8 (HSDPA) @22.17dBm	471	mA
		B19 (HSDPA) @22.31dBm	500	mA
		B1 (HSUPA) @21.4dBm	494	mA
		B6 (HSUPA) @22.05dBm	499	mA
		B8 (HSUPA) @21.57dBm	472	mA
		B19 (HSUPA) @22.14dBm	496	mA
	LTE data transfer	LTE-FDD B1 @23.64dBm	636	mA
		LTE-FDD B3 @23.52dBm	673	mA
		LTE-FDD B8 @23.40dBm	637	mA
		LTE-FDD B18 @23.45dBm	650	mA

	LTE-FDD B19 @23.42dBm	642	mA
	LTE-FDD B26 @23.36dBm	645	mA
	LTE-TDD B41 @23.23dBm	451	mA

7.6. RF Output Power

The following table shows the RF output power of SC20 module.

Table 50: RF Output Power

Frequency	Max.	Min.
GSM850	33dBm±2dB	5dBm±5dB
EGSM900	33dBm±2dB	5dBm±5dB
DCS1800	30dBm±2dB	0dBm±5dB
PCS1900	30dBm±2dB	0dBm±5dB
WCDMA B1	24dBm+1/-3dB	<-49dBm
WCDMA B2	24dBm+1/-3dB	<-49dBm
WCDMA B4	24dBm+1/-3dB	<-49dBm
WCDMA B5	24dBm+1/-3dB	<-49dBm
WCDMA B6	24dBm+1/-3dB	<-49dBm
WCDMA B8	24dBm+1/-3dB	<-49dBm
WCDMA B19	24dBm+1/-3dB	<-49dBm
EVDO/CDMA BC0	24dBm+3/-1dB	<-49dBm
TD-SCDMA B34	24dBm+1/-3dB	<-49dBm
TD-SCDMA B39	24dBm+1/-3dB	<-49dBm

LTE-FDD B1	23dBm±2dB	<-39dBm
LTE-FDD B2	23dBm±2dB	<-39dBm
LTE-FDD B3	23dBm±2dB	<-39dBm
LTE-FDD B4	23dBm±2dB	<-39dBm
LTE-FDD B5	23dBm±2dB	<-39dBm
LTE-FDD B7	23dBm±2dB	<-39dBm
LTE-FDD B8	23dBm±2dB	<-39dBm
LTE-FDD B12	23dBm±2dB	<-39dBm
LTE-FDD B13	23dBm±2dB	<-39dBm
LTE-FDD B18	23dBm±2dB	<-39dBm
LTE-FDD B19	23dBm±2dB	<-39dBm
LTE-FDD B20	23dBm±2dB	<-39dBm
LTE-FDD B25	23dBm±2dB	<-39dBm
LTE-FDD B26	23dBm±2dB	<-39dBm
LTE-FDD B28	23dBm±2dB	<-39dBm
LTE-TDD B38	23dBm±2dB	<-39dBm
LTE-TDD B39	23dBm±2dB	<-39dBm
LTE-TDD B40	23dBm±2dB	<-39dBm
LTE-TDD B41	23dBm±2dB	<-39dBm

NOTE

In GPRS 4 slots TX mode, the maximum output power is reduced by 3dB. This design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

7.7. RF Receiving Sensitivity

The following table shows the RF receiving sensitivity of SC20 module.

Table 51: SC20-CE R1.1 RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
EGSM900	-109dBm	/	/	-102dBm
DCS1800	-109dBm	/	/	-102dBm
WCDMA B1	-110dBm	/	/	-106.7dBm
WCDMA B8	-110dBm	/	/	-103.7dBm
EVDO/CDMA BC0	-108dBm	/	/	-104dBm
TD-SCDMA B34	-113dBm	/	/	-108dBm
TD-SCDMA B39	-113dBm	/	/	-108dBm
LTE-FDD B1 (10M)	-98dBm	-99.1dBm	-100.6dBm	-96.3dBm
LTE-FDD B3 (10M)	-98dBm	-98.1dBm	-101dBm	-93.3dBm
LTE-FDD B5 (10M)	-98.3dBm	-99.5dBm	-101.7dBm	-94.3dBm
LTE-FDD B8 (10M)	-98.2dBm	-99dBm	-101dBm	-93.3dBm
LTE-TDD B38 (10M)	-98.3dBm	-98dBm	-99dBm	-96.3dBm
LTE-TDD B39 (10M)	-98.5dBm	-98.8dBm	-99.5dBm	-96.3dBm
LTE-TDD B40 (10M)	-98.8dBm	-98.6dBm	-101dBm	-96.3dBm
LTE-TDD B41 (10M)	-98.5dBm	-98dBm	-101dBm	-94.3dBm

Table 52: SC20-EL RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
GSM850	-109dBm	/	/	-102dBm
EGSM900	-109dBm	/	/	-102dBm
DCS1800	-109dBm	/	/	-102dBm
PCS1900	-109dBm	/	/	-102dBm
WCDMA B1	-110dBm	/	/	-106.7dBm
WCDMA B5	-110dBm	/	/	-104.7dBm
WCDMA B8	-110dBm	/	/	-103.7dBm
LTE-FDD B1 (10M)	-98dBm	-99dBm	-102dBm	-96.3dBm
LTE-FDD B3 (10M)	-97dBm	-98dBm	-101dBm	-93.3dBm
LTE-FDD B5 (10M)	-99dBm	-98dBm	-102dBm	-94.3dBm
LTE-FDD B7 (10M)	-97dBm	-97dBm	-102dBm	-94.3dBm
LTE-FDD B8 (10M)	-98dBm	-98dBm	-101dBm	-93.3dBm
LTE-FDD B20 (10M)	-98dBm	-98dBm	-101dBm	-93.3dBm
LTE-TDD B38 (10M)	-97dBm	-98dBm	-100dBm	-96.3dBm
LTE-TDD B40 (10M)	-97dBm	-98dBm	-100dBm	-96.3dBm
LTE-TDD B41 (10M)	-96dBm	-98dBm	-100dBm	-94.3dBm

Table 53: SC20-AL RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
GSM850	-109.5dBm	/	/	-102dBm
PCS1900	-109dBm	/	/	-102dBm
WCDMA B1	-110dBm	-110dBm	-113dBm	-106.7dBm
WCDMA B2	-110dBm	-110dBm	-113dBm	-104.7dBm

WCDMA B4	-110dBm	-110dBm	-113dBm	-106.7dBm
WCDMA B5	-110dBm	-111dBm	-113dBm	-104.7dBm
WCDMA B8	-110dBm	/	/	-103.7dBm
LTE-FDD B2 (10M)	-98dBm	-99dBm	-102dBm	-94.3dBm
LTE-FDD B4 (10M)	-97.5dBm	-98dBm	-101dBm	-96.3dBm
LTE-FDD B5 (10M)	-99.5dBm	-99.5dBm	-102.5dBm	-94.3dBm
LTE-FDD B7 (10M)	-97dBm	-99dBm	-100dBm	-94.3dBm
LTE-FDD B12 (10M)	-98.5dBm	-98.5dBm	-101dBm	-93.3dBm
LTE-FDD B13 (10M)	-96.5dBm	-99dBm	-101dBm	-93.3dBm
LTE-TDD B25 (10M)	-99dBm	-99dBm	-102dBm	-92.8dBm
LTE-TDD B26 (10M)	-99dBm	-100dBm	-102.5dBm	-93.8dBm

Table 54: SC20-AUL RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
GSM850	-109dBm	/	/	-102dBm
EGSM900	-109dBm	/	/	-102dBm
DCS1800	-108dBm	/	/	-102dBm
PCS1900	-109dBm	/	/	-102dBm
WCDMA B1	-110dBm	-110dBm	-113dBm	-106.7dBm
WCDMA B2	-110dBm	/	/	-104.7dBm
WCDMA B5	-110dBm	-110dBm	-113dBm	-104.7dBm
WCDMA B8	-110dBm	-110dBm	-113dBm	-103.7dBm
LTE-FDD B1 (10M)	-98dBm	-99dBm	-101dBm	-96.3dBm
LTE-FDD B3 (10M)	-97dBm	-98dBm	-101.8dBm	-93.3dBm
LTE-FDD B5 (10M)	-99dBm	-100dBm	-103dBm	-94.3dBm

LTE-FDD B7 (10M)	-97dBm	-99dBm	-100.6dBm	-94.3dBm
LTE-FDD B8 (10M)	-98dBm	-100dBm	-102dBm	-93.3dBm
LTE-FDD B28 (10M)	-97.5dBm	-100dBm	-101.8dBm	-94.8dBm
LTE-TDD B40 (10M)	-97dBm	-98dBm	-100.7dBm	-96.3dBm

Table 55: SC20-JL RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
WCDMA B1	-110dBm	-110dBm	-113dBm	-106.7dBm
WCDMA B6	-110dBm	-112dBm	-113dBm	-106.7dBm
WCDMA B8	-110dBm	-110dBm	-113dBm	-103.7dBm
WCDMA B19	-110dBm	-111dBm	-113dBm	-106.7dBm
LTE-FDD B1 (10M)	-97dBm	-97.5dBm	-100dBm	-96.3dBm
LTE-FDD B3 (10M)	-97dBm	-98dBm	-101.8dBm	-93.3dBm
LTE-FDD B8 (10M)	-97dBm	-98dBm	-100dBm	-93.3dBm
LTE-FDD B18 (10M)	-98dBm	-99dBm	-101.5dBm	-96.3dBm
LTE-TDD B19 (10M)	-98dBm	-99dBm	-101.5dBm	-96.3dBm
LTE-TDD B26 (10M)	-98dBm	-99dBm	-101.5dBm	-93.8dBm
LTE-TDD B41 (10M)	-96dBm	-96.5dBm	-100dBm	-94.3dBm

7.8. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it should be subject to ESD handling precautions that are typically applied to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the electrostatic discharge characteristics of SC20 module.

Table 56: ESD Characteristics (Temperature: 25ºC, Humidity: 45%)

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	+/-5	+/-10	KV
All Antenna Interfaces	+/-5	+/-10	KV
USB Interface	+/-0.5	+/-1	KV
Other Interfaces	+/-0.5	+/-1	KV

8 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the tolerances for dimensions without tolerance values are ±0.05mm.

8.1. Mechanical Dimensions of the Module

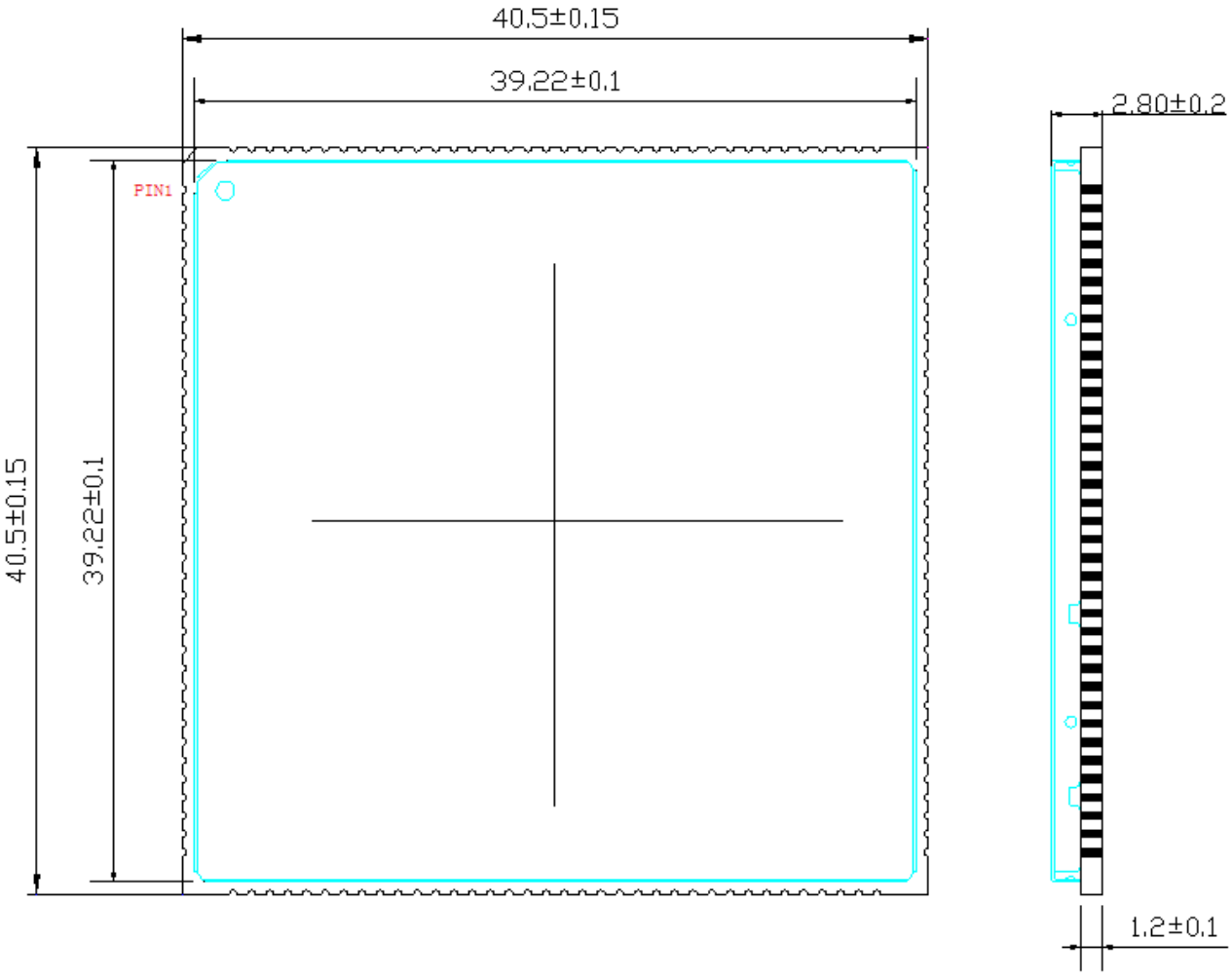


Figure 42: Module Top and Side Dimensions

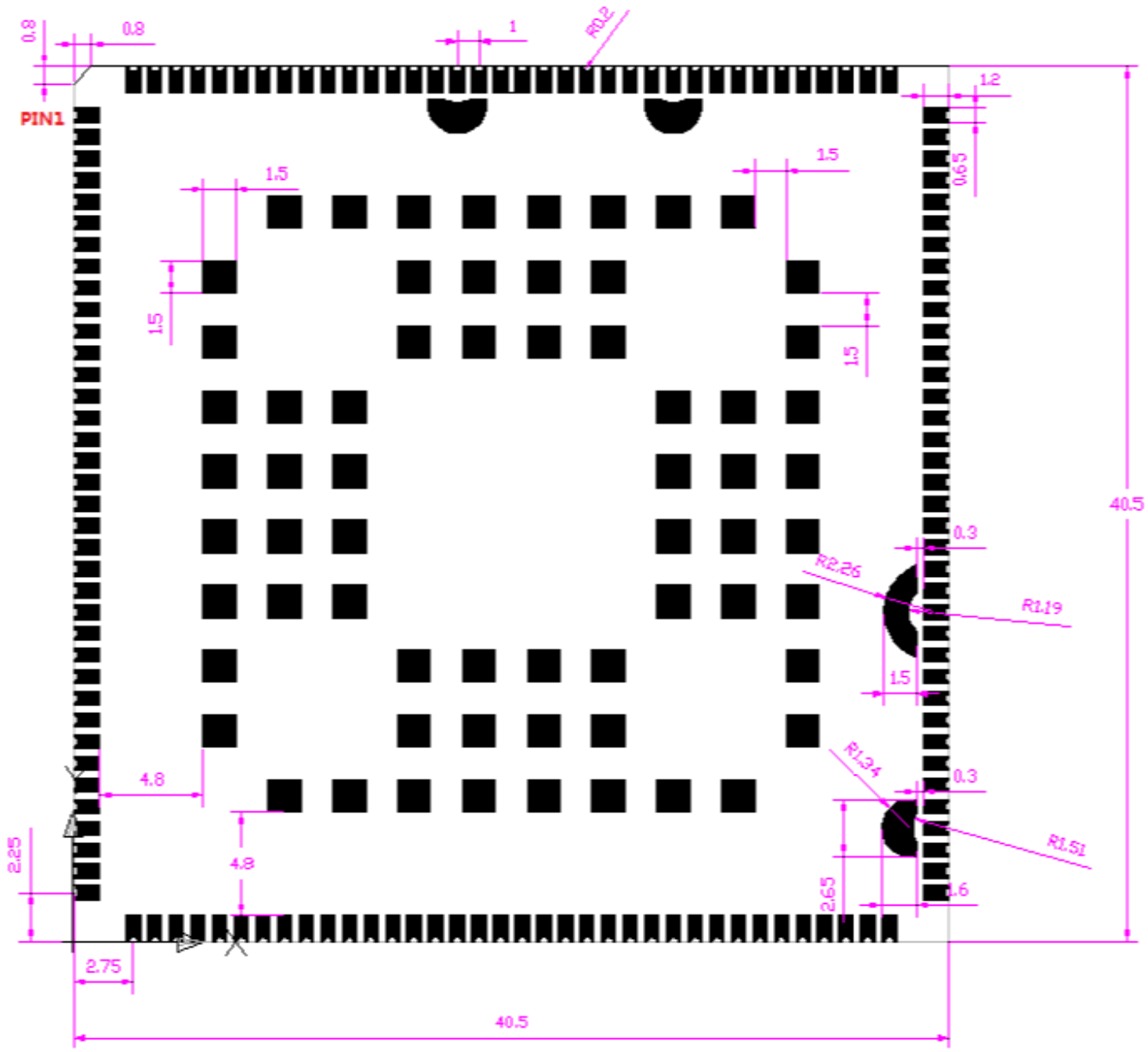


Figure 43: Module Bottom Dimensions (Top View)

8.2. Recommended Footprint

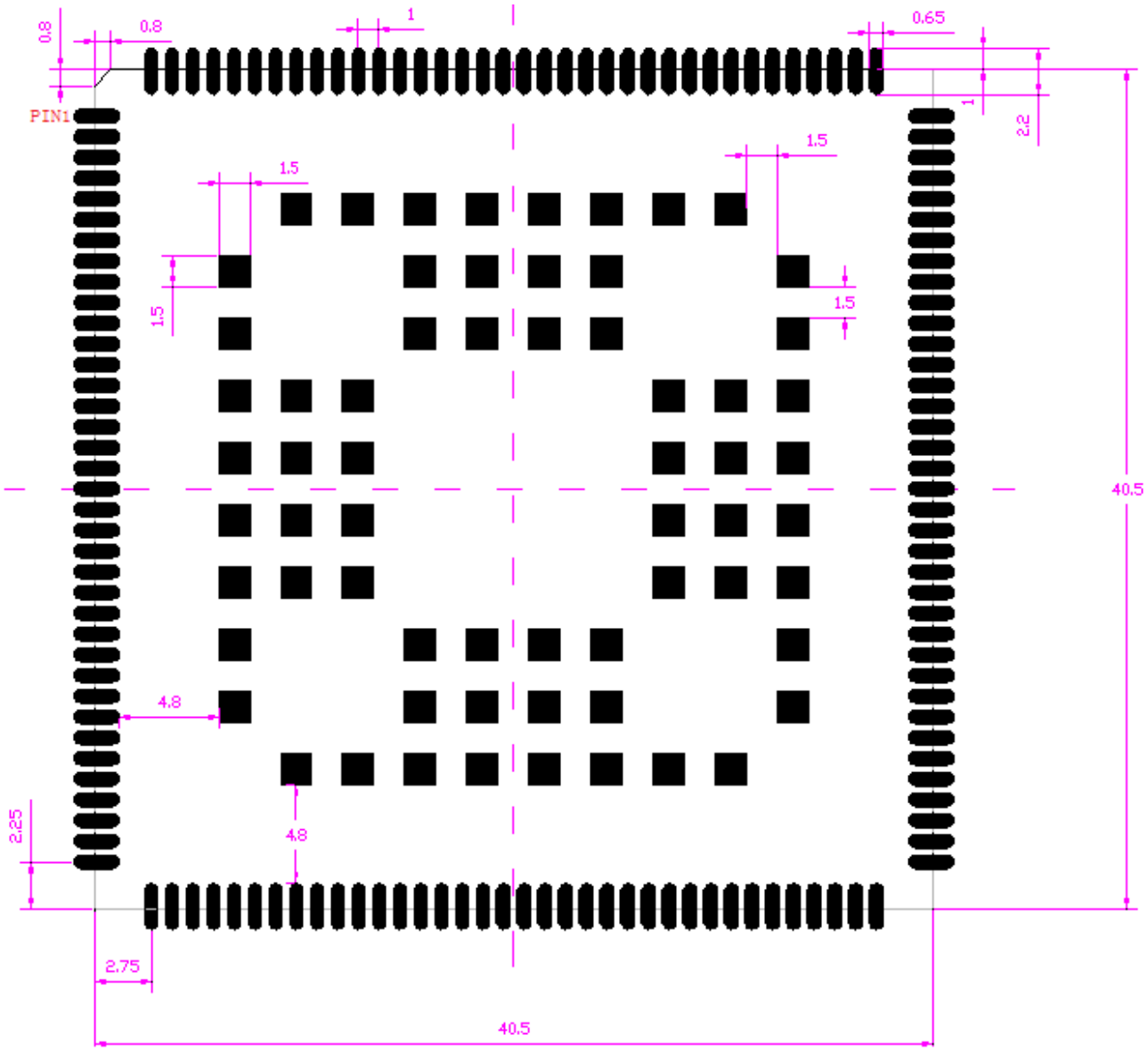


Figure 44: Recommended Footprint (Top View)

NOTES

1. For easy maintenance of the module, keep about 3mm between the module and other components on host PCB.
2. All RESERVED pins should be kept open and MUST NOT be connected to ground.

8.3. Top and Bottom Views of the Module

Figure 45: Top View of the Module

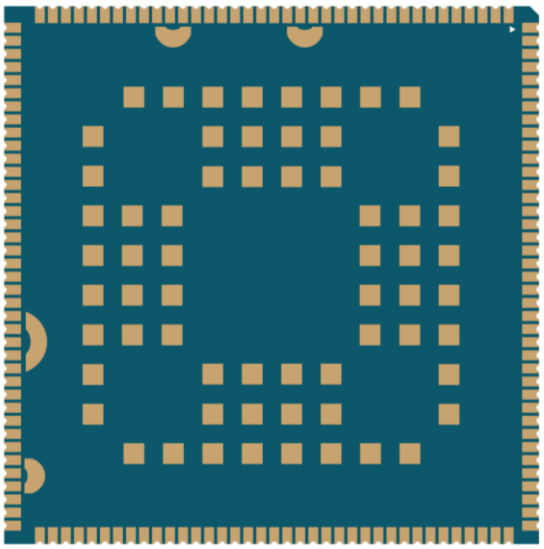


Figure 46: Bottom View of the Module

NOTE

These are renderings of SC20 module. For authentic dimension and appearance, please refer to the module that you receive from Quectel.

9 Storage, Manufacturing and Packaging

9.1. Storage

SC20 is stored in a vacuum-sealed bag. It is rated at MSL 3, and its storage restrictions are shown as below.

1. Shelf life in the vacuum-sealed bag: 12 months at <40ºC/90%RH.

2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:
   - Mounted within 168 hours at the factory environment of ≤30ºC/60%RH.
   - Stored at <10%RH.

3. Devices require baking before mounting, if any circumstance below occurs.
   - When the ambient temperature is 23ºC±5ºC and the humidity indication card shows the humidity is >10% before opening the vacuum-sealed bag.
   - Device mounting cannot be finished within 168 hours at factory conditions of ≤30ºC/60%RH.

4. If baking is required, devices may be baked for 8 hours at 120ºC±5ºC.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devic es before high temperature (120ºC) baking. If shorter baking time is desired, please refer to *IPC/J EDECJ-STD-033* for baking procedure.

9.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18mm~0.20mm. It is recommended to slightly reduce the amount of solder paste for LGA pads, thus avoiding short-circuit. For more details, please refer to ***document [3]***.

It is suggested that the peak reflow temperature is 240~245ºC, and the absolute maximum reflow temperature is 245ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below:

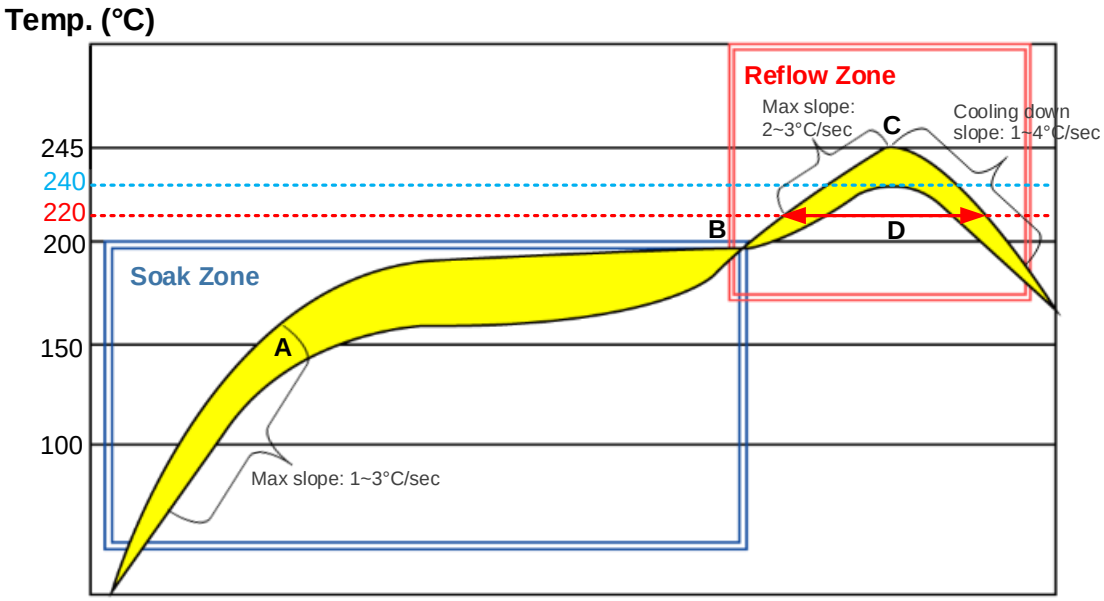


Figure 47: Recommended Reflow Soldering Thermal Profile

Table 57: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1 to 3°C/sec

Soak time (between A and B: 150°C and 200°C)	60 to 120 sec
Reflow Zone	
Max slope	2 to 3°C/sec
Reflow time (D: over 220°C)	40 to 60 sec
Max temperature	240°C ~ 245°C
Cooling down slope	1 to 4°C/sec
Reflow Cycle	
Max reflow cycle	1

9.3. Packaging

SC20 is packaged in tape and reel carriers. Each reel is 12.32m long and contains 200 modules. The following figures show the package details, measured in mm.

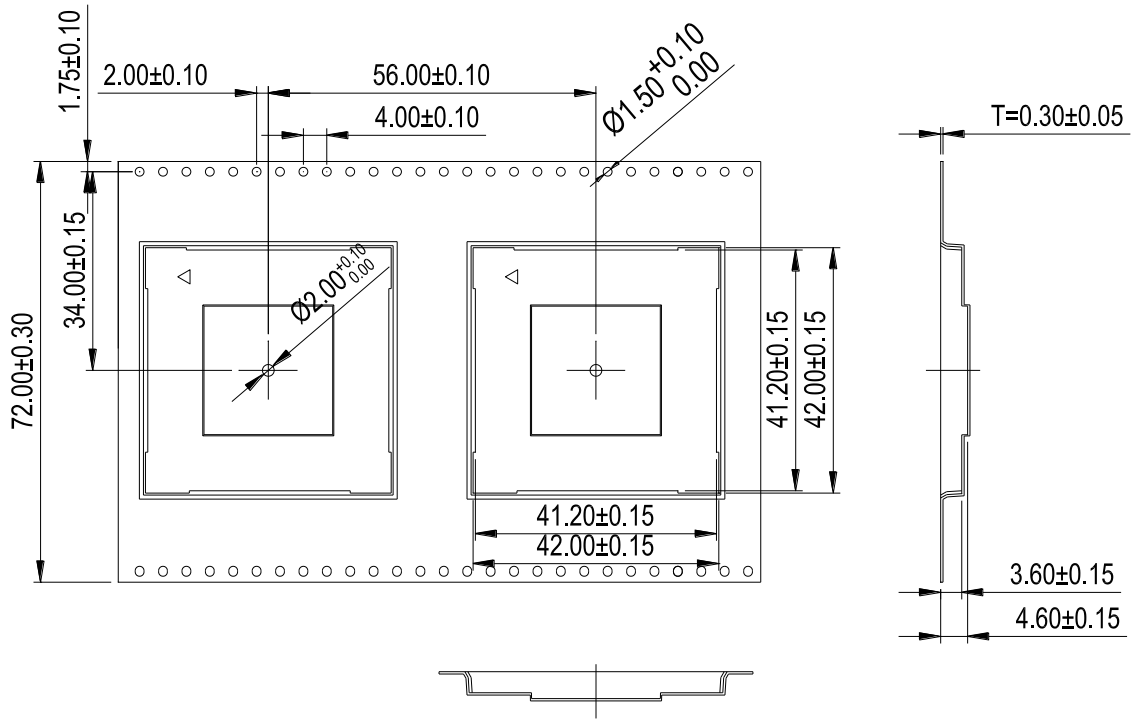


Figure 48: Tape Dimensions

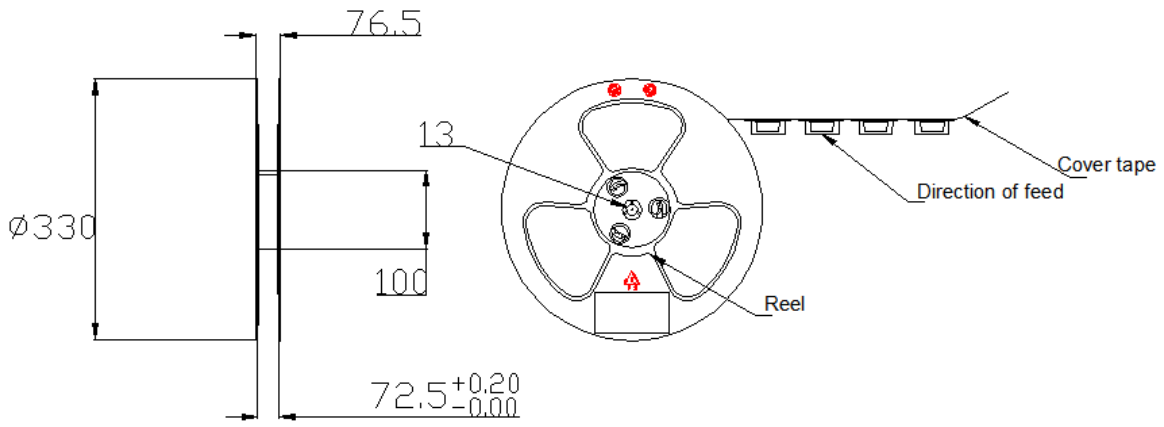


Figure 49: Reel Dimensions

Table 58: Reel Packaging

Model Name	MOQ for MP	Minimum Package: 200pcs	Minimum Package × 4=800pcs
SC20	200	Size: 370mm × 350mm × 85mm N.W: 1.92kg G.W: 3.17kg	Size: 380mm × 365mm × 365mm N.W: 7.68kg G.W: 13.63kg

10 Appendix A References

Table 59: Related Documents

SN	Document Name	Remark
[1]	Quectel_Smart_EVB_User_Guide	Smart EVB user guide
[2]	Quectel_RF_Layout_Application_Note	RF layout application note
[3]	Quectel_Module_Secondary_SMT_User_Guide	Module secondary SMT user guide
[4]	Quectel_SC20_Reference_Design	SC20 reference design

Table 60: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-rate
ARP	Antenna Reference Point
bps	Bits Per Second
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DRX	Discontinuous Reception
EFR	Enhanced Full Rate
EGSM	Extended GSM900 band (includes standard GSM900 band)
eSCD	Enhanced Synchronous Connection Oriented

ESD	Electrostatic Discharge
FR	Full Rate
GMSK	Gaussian Minimum Shift Keying
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
I/O	Input/Output
LNA	Low Noise Amplifier
MO	Mobile Originated
MS	Mobile Station (GSM engine)
MT	Mobile Terminated
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RH	Room Humidity
RHCP	Right Hand Circularly Polarized
RTC	Real Time Clock
Rx	Receive
SDIO	Secure Digital Input and Output
SIM	Subscriber Identification Module
SMS	Short Message Service

TP	Touch Panel
TX	Transmit
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
(U)SIM	Universal Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

11 Appendix B GPRS Coding Schemes

Table 61: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	C4-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

12 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 62: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA
14	4	4	NA

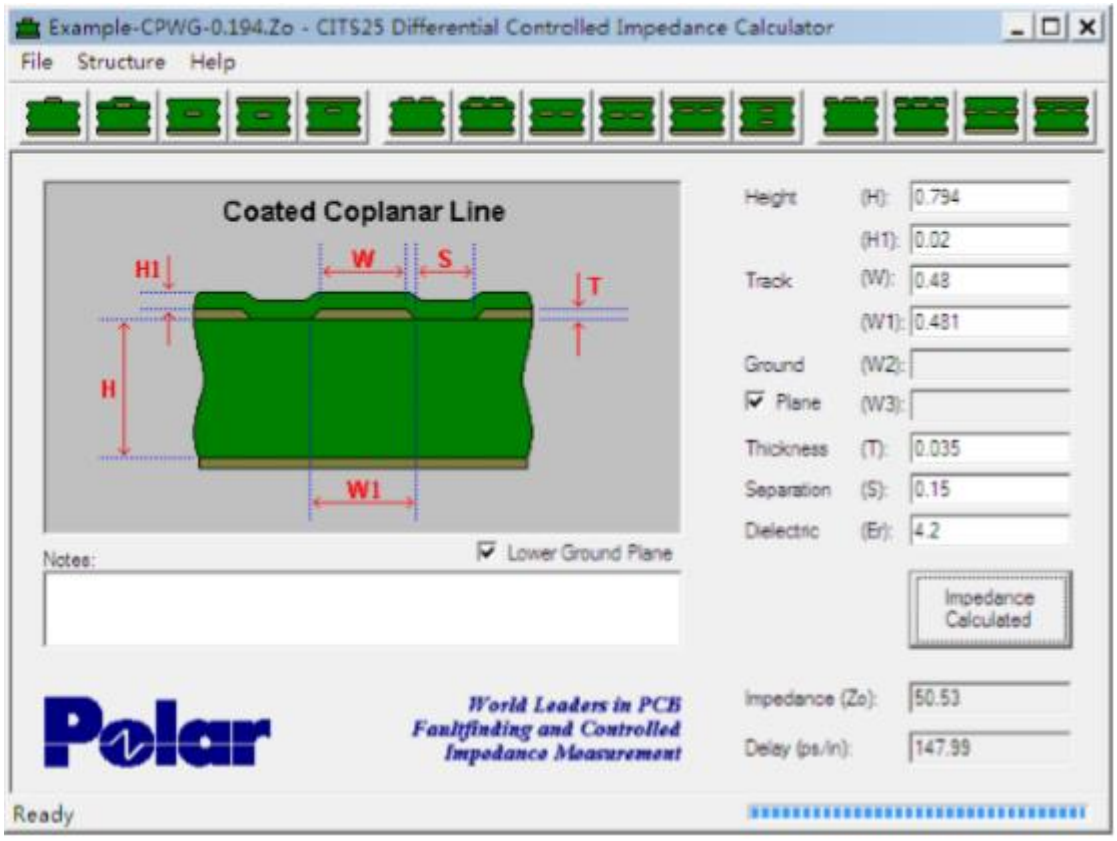
15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

13 Appendix D EDGE Modulation and Coding Schemes

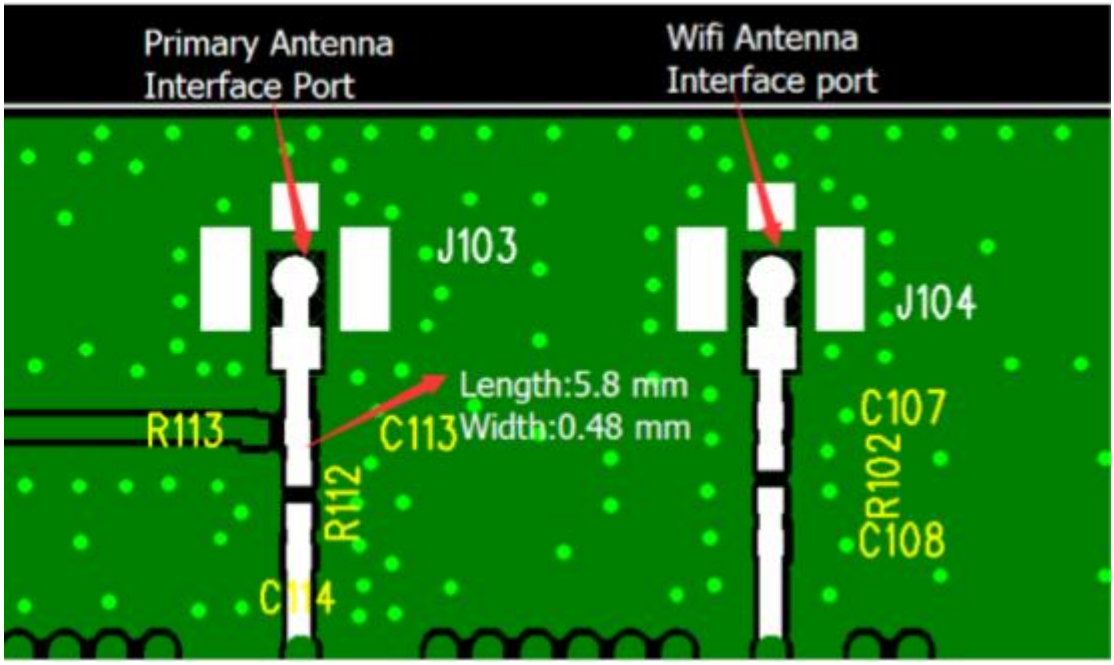
Table 63: EDGE Modulation and Coding Schemes

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.60kbps	35.20kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps

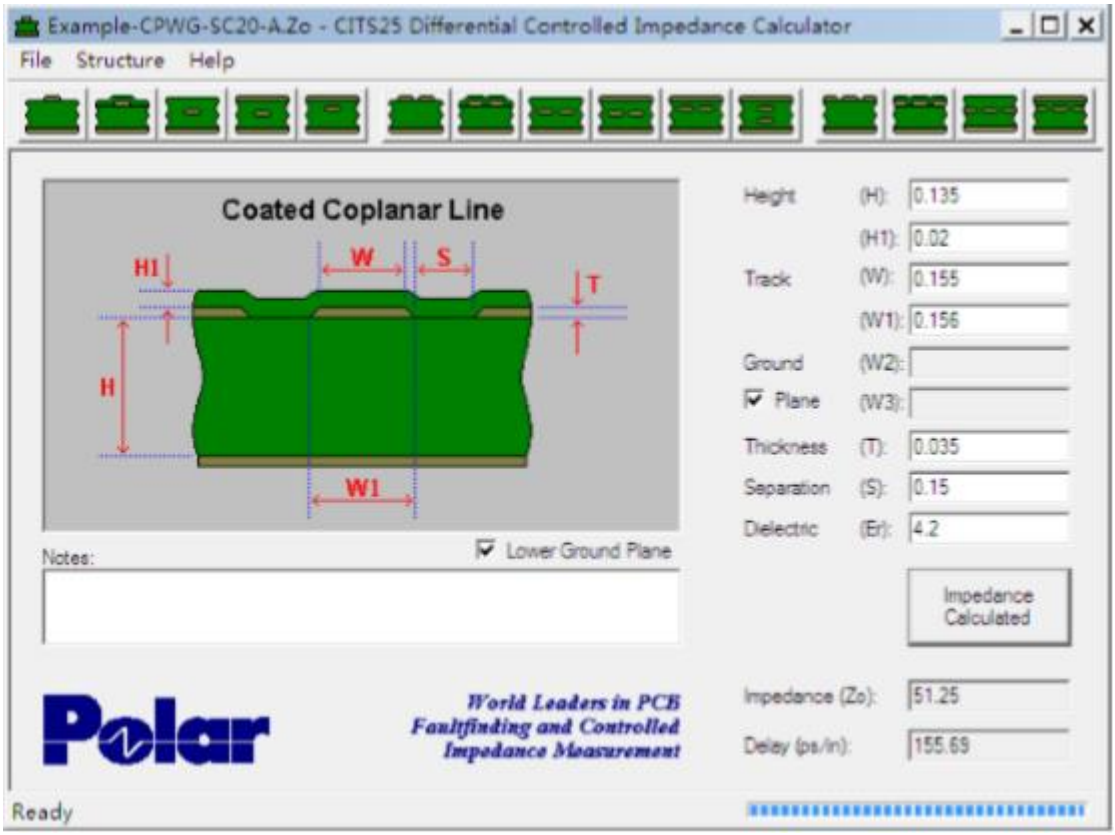
1、 the characteristic impedence depends on the dielectric of PCB, the trace width and the grand plane spacing,Coated Coplanar Line is required.the detail simulation as below.



2、the RF trace of the test board which was used in the FCC test is defined as below.



3、the characteristic impedence depends on the dielectric of PCB, the trace width and the grand plane spacing,Coated Coplanar Line is required.the detail simulation as below.



4、the RF trace of the test board which was used in the FCC test is defined as below.