EC25Hardware Design

LTE Module Series

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About the Document

History

Revision	Date	Author	Description
1.0	2016-04-01	Woody WU	Initial
1.1	2016-09-22	Lyndon LIU/ Frank WANG	1. Updated EC25 series frequency bands in Table 1. 2. Updated transmitting power, supported maximum baud rate of main UART/internal protocols/USB drivers of USB interface, firmware upgrade and temperature range in Table 2. 3. Updated timing of turning on module in Figure 12. 4. Updated timing of turning off module in Figure 13. 5. Updated timing of resetting module in Figure 16. 6. Updated supported baud rates of main UART in Chapter 3.11. 7. Added notes for ADC interface in Chapter 3.13. 8. Updated GNSS performance in Table 21. 9. Updated operating frequencies of module in Table 23. 10. Added current consumption in Chapter 6.4. 11. Updated RF output power in Chapter 6.5. 12. Added RF receiving sensitivity in Chapter 6.6.
1.2	2016-11-04	Lyndon LIU/ Michael ZHANG	1. Added SGMII and WLAN interfaces in Table 2. 2. Updated function diagram in Figure 1. 3. Updated pin assignment (Top View) in Figure 2. 4. Added description of SGMII and WLAN interfaces in Table 4. 5. Added SGMII interface in Chapter 3.17. 6. Added WLAN interface in Chapter 3.18. 7. Added USB_BOOT interface in Chapter 3.19. 8. Added reference design of RF layout in Chapter 5.1.4. 9. Added note about SIMO in Chapter 6.6.
1.3	2017-01-24	Lyndon LIU/ Frank WANG	1. Updated function diagram in Figure 1. 2. Updated pin assignment (top view) in Figure 2.

	3. Added BT interface in Chapter 3.18.2. 4. Updated GNSS performance in Table 24. 5. Updated reference circuit of wireless connectivity interfaces with FC20 module in Figure 29. 6. Updated current consumption of EC25-E module in Table 33. 7. Updated EC25-A conducted RF receiving sensitivity in Table 38. 8. AddedEC25-J conducted RF receiving sensitivity in Table 40.

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1 Introduction

This document defines the EC25module and describes its air interface and hardware interface which are connected with your application.

This document can help you quickly understand module interface specifications, electrical and mechanical details, as well as other related information of EC25 module. Associated with application note and user guide, you can use EC25 module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of the operation, such as usage, service or repair of any cellular terminal or mobile incorporating EC25 module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectelassumes no liability for the customer's failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. You must comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it is switched off. The operation of wireless appliances in an aircraft is forbidden, so as to prevent interference with communication systems. Consult the airline staff about the use of wireless devices on boarding the aircraft, if your device offers an Airplane Mode which must be enabled prior to boarding an aircraft.
	Switch off your wireless device when in hospitals,clinics or other health care facilities. These requests are desinged to prevent possible interference with sensitive medical equipment.
	Cellular terminals or mobiles operatingover radio frequency signal and cellular network cannot be guaranteed to connect in all conditions, for example no mobile fee or with an invalid USIM/SIM card. While you are in this condition and need emergent help, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength.
	Your cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency energy. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

EC25 is a series of LTE-FDD/LTE-TDD/WCDMA/GSM wireless communication module with receive diversity, which provides data connectivity on LTE-FDD,LTE-TDD,DC-HSPA+, HSPA+, HSDPA, HSUPA, WCDMA,EDGE andGPRSnetworks. It also provides GNSS[1)] and voice functionality[2)] for your specific application.EC25 contains fivevariants:EC25-E, EC25-A, EC25-V, EC25-Jand EC25-AU. You can choose a dedicated type based on the region or operator. The following table shows the frequency bands of EC25 series module.

Table 1: Frequency Bands of EC25 Series Module

Modules[2)]	LTE Bands	3G Bands	GSM	Rx-diversity	GNSS[1)]
EC25-E	FDD:B1/B3/B5/B7/B8/B20 TDD: B38/B40/B41	WCDMA: B1/B5/B8	900/1800	Supported	GPS, GLONASS, BeiDou/ Compass, Galileo, QZSS
EC25-A	FDD: B2/B4/B12	WCDMA: B2/B4/B5	Not supported	Supported	
EC25-V	FDD: B4/B13	Not supported	Not supported	Supported	
EC25-J	FDD: B1/B3/B8/B18/B19/B26 TDD: B41	WCDMA: B1/B6/B8/B19	Not supported	Supported	
EC25-AU[3)]	FDD: B1/B2/B3/B4/B5/B7/B8/B28 TDD: B40	WCDMA: B1/B2/B5/B8	850/900/1800/1900	Supported	

NOTES

1. [1)] GNSS function is optional.
2. [2)] EC25 series module (EC25-E/EC25-A/EC25-V/EC25-J/EC25-AU) includes **Data-only** and **Telematics** versions. **Data-only** version does not support voice function, while **Telematics** version supports it.
3. [3)] B2 band on EC25-AU module does not support Rx-diversity.

With a tiny profile of 32.0mm ×29.0mm ×2.4mm, EC25 can meet almost all requirements for M2M applications such as automotive, metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, tablet PC, etc.

EC25 is an SMD type module which can be embedded in applications through its 144-pin pads, including 80 LCC signal pads and 64 other pads.

2.2. Key Features

The following table describes the detailed features of EC25 module.

Table 2: Key Features of EC25 Module

Feature	Details
Power Supply	Supply voltage: 3.3V~4.3VTypical supply voltage: 3.8V
Transmitting Power	Class 4 (33dBm±2dB) for GSM900 Class 1 (30dBm±2dB) for DCS1800 Class E2 (27dBm±3dB) for GSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class 3 (23dBm+1/-3dB) for WCDMA bands Class 3 (23dBm+1/-3dB) for LTE-FDD band5 Class 3 (22.5dBm+1/-3dB) for LTE-FDD band7 Class 3 (23dBm+1/-3dB) for LTE-TDD bands
LTE Features	Support up to non-CA CAT4 Support 1.4 to 20MHz RF bandwidth Support MIMO in DL direction FDD: Max 50Mbps (UL), 150Mbps (DL) TDD: Max 35Mbps (UL), 130Mbps (DL)
WCDMA Features	Support 3GPP R8 DC-HSPA+ Support 16-QAM, 64-QAM and QPSKmodulation 3GPP R6 CAT6 HSUPA: Max 5.76Mbps (UL) 3GPP R8 CAT24 DC-HSPA+: Max 42Mbps (DL)
GSMFeatures	**R99:** CSD: 9.6kbps, 14.4kbps **GPRS:** Support GPRS multi-slot class 12 (12 by default) Coding scheme: CS-1, CS-2, CS-3 and CS-4 Maximum of four Rx time slots per frame **EDGE:** Support EDGE multi-slot class 12 (12 by default)

	Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: CS 1-4 and MCS 1-9 Uplink coding schemes: CS 1-4 and MCS 1-9
Internet Protocol Features	SupportTCP/UDP/PPP/FTP/HTTP/NTP/PING/QMI/HTTPS*/SMTP*/MMS*/FTPS*/SMTPS*/SSL*protocols Support the protocols PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) usually used for PPP connections
SMS	Text and PDU mode Point to point MO and MT SMS cell broadcast SMS storage: ME by default
USIM Interface	Support USIM/SIM card: 1.8V, 3.0V
Audio Features	Support one digital audio interface: PCM interface GSM: HR/FR/EFR/AMR/AMR-WB WCDMA: AMR/AMR-WB LTE: AMR/AMR-WB Support echo cancellation and noise suppression
PCM Interface	Used for audio function with external codec Support 8-bit A-law*, μ-law*and 16-bit linear data formats Support long frame synchronization and short frame synchronization Support master and slave modes, but must be the master in long frame synchronization
USB Interface	Compliant with USB 2.0 specification (slave only);the data transfer rate can reach up to 480Mbps Used for AT command communication, data transmission, GNSS NMEA output, software debugging, firmware upgrade and voiceover USB* Support USB drivers for: Windows XP, Windows Vista, Windows 7, Windows 8/8.1, Windows 10, Linux 2.6 or later, Android 4.0/4.2/4.4/5.0/5.1/6.0
UART Interface	**Main UART:** Used for AT command communication and data transmission Baud rate reach up to 3000000bps, 115200bps by default Support RTS and CTS hardware flow control **Debug UART:** Used for Linux console, log output 115200bps baud rate
SGMII Interface	Support 10/100/1000Mbps Ethernet connectivity
Wireless Connectivity Interfaces	Support a low-power SDIO 3.0 interface for WLAN and UART/PCM interface for Bluetooth*

Rx-diversity	Support LTE/WCDMA Rx-diversity
GNSS Features	Gen8CLite of Qualcomm Protocol: NMEA 0183
AT Commands	Compliant with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands
Network Indication	Two pins including NET_MODE and NET_STATUS to indicate network connectivity status
Antenna Interface	Including main antenna interface (ANT_MAIN), Rx-diversityantenna interface (ANT_DIV) and GNSS antenna interface (ANT_GNSS)
Physical Characteristics	Size: 32.0±0.15×29.0±0.15×2.4±0.2mm Weight: approx. 4.9g
Temperature Range	Operation temperature range: -35°C ~ +75°C[1)] Extended temperature range: -40°C ~ +85°C[2)]
Firmware Upgrade	USB interface and DFOTA*
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP compliant again.
3. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of EC25 and illustrates the major functional parts.

- Power management
- Baseband
- DDR+NAND flash
- Radio frequency
- Peripheral interfaces

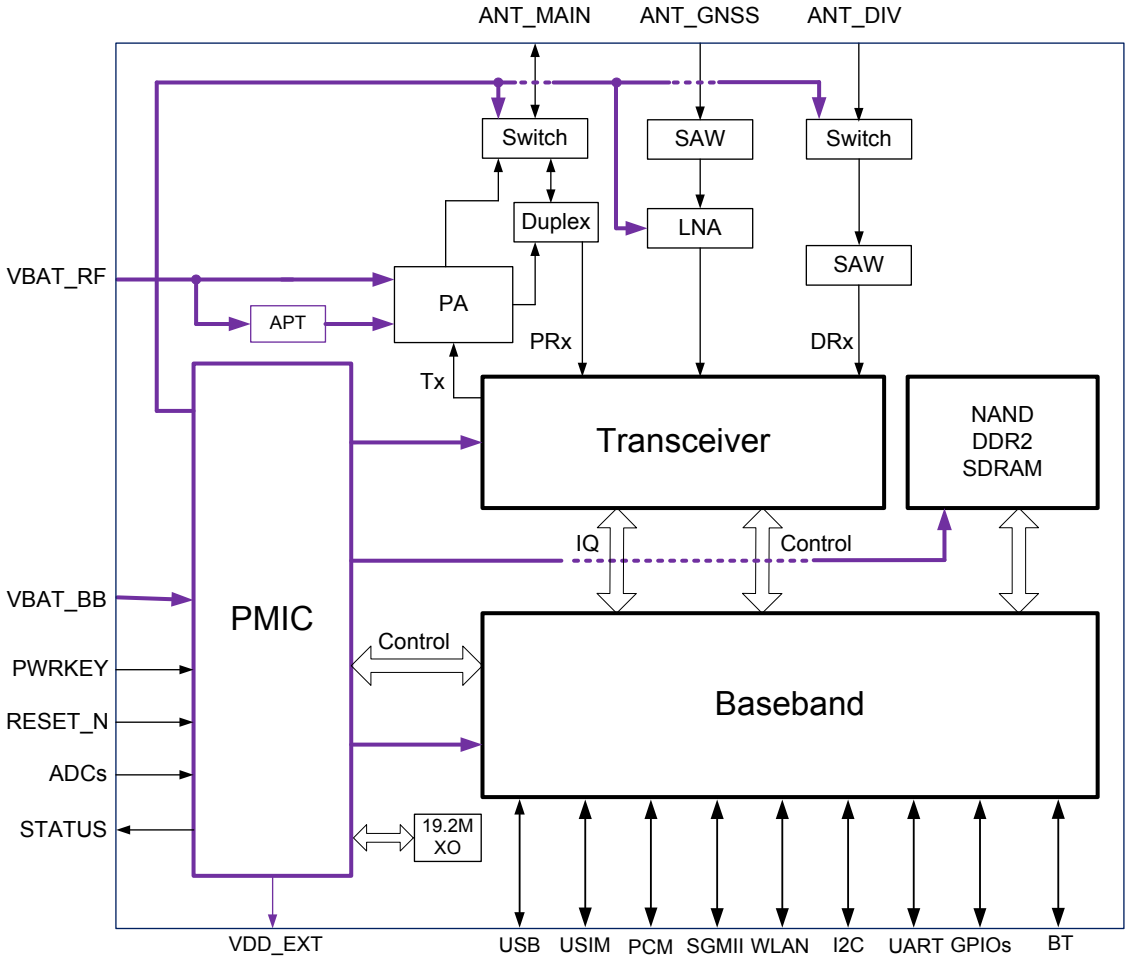


Figure 1: Functional Diagram

2.4. Evaluation Board

In order to help youto develop applications with EC25, Quectel supplies an evaluation board (EVB), USB data cable, earphone, antenna and other peripherals to control or test the module.

3 Application Interface

3.1. General Description

EC25 is equipped with 80-pin SMT pads plus 64-pin ground pads and reserved pads that can beconnected to cellular application platform. Sub-interfaces included in these pads are described in detail in the following chapters:

- Power supply
- USIM interface
- USB interface
- UART interfaces
- PCM interface
- ADC interface
- Status indication
- SGMII interface
- Wireless connectivityinterfaces
- USB_BOOT interface

3.2. Pin Assignment

The following figure shows the pin assignment of EC25 module.

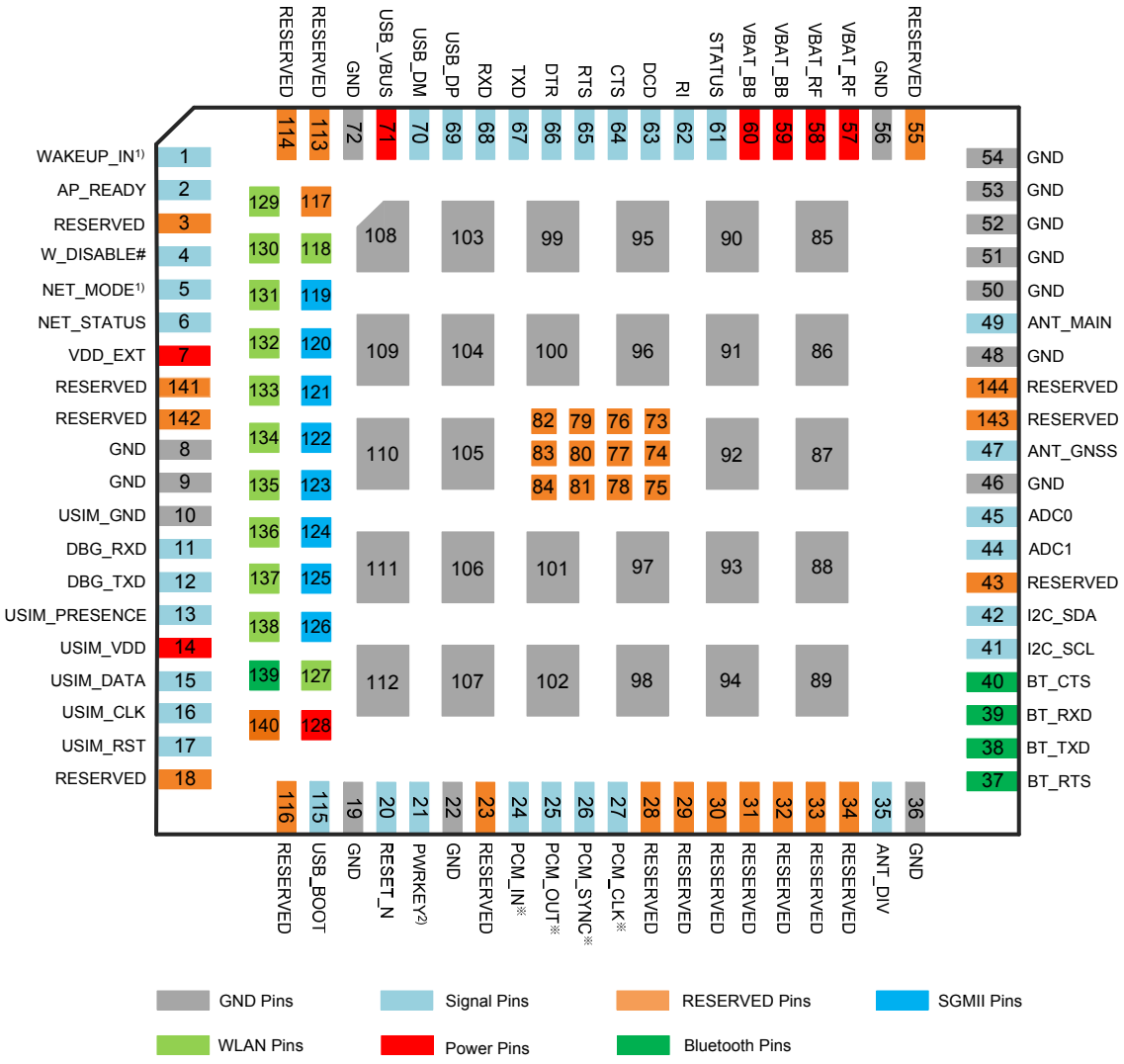


Figure 2: Pin Assignment (Top View)

NOTES

1. 1)meansthat these pins cannot be pulled up before startup.
2. 2) PWRKEY output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
3. Pads 119~126 are SGMII function pins.
4. Pads 37~40, 118, 127 and 129~139 are wireless connectivity interfaces, among which pads 127 and 129~138 are WLAN function pins, and others are Bluetooth (BT) function pins. BT function is under development.

5. Pads 24~27 are multiplexing pins used for audio design on EC25 module and BT function on FC20 module.
6. Keep all RESERVEDpins and unused pins unconnected.
7. GND pads 85~112 should be connected to ground in the design, and RESERVED pads 73~84should not be designed in schematic and PCB decal.
8. "※"means these interface functions are only supported on **Telematics** version.

3.3. Pin Description

The following tables show the pin definition of EC25 modules.

Table 3: I/O Parameters Definition

Type	Description
IO	Bidirectional
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	59,60	PI	Power supply for module baseband part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	It must be able to provide sufficient current up to 0.8A.
VBAT_RF	57,58	PI	Power supply for module RF part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	It must be able to provide sufficient current up to 1.8A in a

					bursttransmission.
VDD_EXT	7	PO	Provide 1.8V for external circuit	Vnorm=1.8V $I_O$max=50mA	Power supply for external GPIO's pull up circuits.
GND	8,9,19,22,36,46,48,50~54,56,72,85~112		Ground		
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	21	DI	Turnon/off the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
RESET_N	20	DI	Reset the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	61	OD	Indicate the module operating status	The drive current should be less than 0.9mA.	Require external pull-up. If unused, keep it open.
NET_MODE	5	DO	Indicate the module network registration mode	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. Cannot be pulled up before startup. If unused, keep it open.
NET_ STATUS	6	DO	Indicate the module network activity status	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. If unused, keep it open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	71	PI	USB detection	Vmax=5.25V Vmin=3.0V Vnorm=5.0V	
USB_DP	69	IO	USB differential data bus	Compliant with USB 2.0 standard specification.	Require differential impedance of 90ohm.

USB_DM	70	IO	USB differential data bus	Compliant with USB 2.0 standard specification.	Require differential impedance of 90ohm.
USIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	10		Specified ground for USIM card		
USIM_VDD	14	PO	Power supply for USIM card	For 1.8V USIM: Vmax=1.9V Vmin=1.7V For 3.0V USIM: Vmax=3.05V Vmin=2.7V $I_O$max=50mA	Either 1.8V or 3.0V is supported by the module automatically.
USIM_DATA	15	IO	Data signal of USIM card	For 1.8V USIM: V_{IL}max=0.6V V_{IH}min=1.2V V_{OL}max=0.45V V_{OH}min=1.35V For 3.0V USIM: V_{IL}max=1.0V V_{IH}min=1.95V V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_CLK	16	DO	Clock signal of USIM card	For 1.8V USIM: V_{OL}max=0.45V V_{OH}min=1.35V For 3.0V USIM: V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_RST	17	DO	Reset signal of USIM card	For 1.8V USIM: V_{OL}max=0.45V V_{OH}min=1.35V For 3.0V USIM: V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_ PRESENCE	13	DI	USIM card insertion detection	V_{IL}min=-0.3V V_{IL}max=0.6V	1.8V power domain. If unused, keep it

				V_{IH}min=1.2V V_{IH}max=2.0V	open.
UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RI	62	DO	Ring indicator	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
DCD	63	DO	Data carrier detection	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
CTS	64	DO	Clear to send	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
RTS	65	DI	Request to send	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
DTR	66	DI	Data terminal ready,sleep mode control	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Pull-up by default. Low level wakes up the module. If unused, keep it open.
TXD	67	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
RXD	68	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	12	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
DBG_RXD	11	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.

ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	45	AI	General purpose analog to digital converter	Voltage range: 0.3V to VBAT_BB	If unused, keep it open.
ADC1	44	AI	General purpose analog to digital converter	Voltage range: 0.3V to VBAT_BB	If unused, keep it open.
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_IN	24	DI	PCM data input	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
PCM_OUT	25	DO	PCM data output	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
PCM_SYNC	26	IO	PCM data frame synchronization signal	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_CLK	27	IO	PCM clock	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	41	OD	I2C serial clock Used for external codec.		External pull-up resistor is required. 1.8V only. If unused, keep it open.
I2C_SDA	42	OD	I2C serial dataUsed for external codec.		External pull-up resistor is required. 1.8V only. If unused, keep it open.

SGMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
EPHY_RST_N	119	DO	Ethernet PHY reset	For 1.8V: V_{OL}max=0.45V V_{OH}min=1.4V For 2.85V: V_{OL}max=0.35V V_{OH}min=2.14V	1.8V/2.85V power domain. If unused, keep it open.
EPHY_INT_N	120	DI	Ethernet PHY interrupt	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SGMII_MDATA	121	IO	SGMII MDIO (Management Data Input/Output) data	For 1.8V: V_{OL}max=0.45V V_{OH}min=1.4V V_{IL}max=0.58V V_{IH}min=1.27V For 2.85V: V_{OL}max=0.35V V_{OH}min=2.14V V_{IL}max=0.71V V_{IH}min=1.78V	1.8V/2.85V power domain. If unused, keep it open.
SGMII_MCLK	122	DO	SGMII MDIO (Management Data Input/Output) clock	For 1.8V: V_{OL}max=0.45V V_{OH}min=1.4V For2.85V: V_{OL}max=0.35V V_{OH}min=2.14V	1.8V/2.85V power domain. If unused, keep it open.
USIM2_VDD	128	PO	SGMII MDIO pull-up power source		Configurable power source. 1.8V/2.85V power domain. External pull-up for SGMII MDIO pins. If unused, keep it open.
SGMII_TX_M	123	AO	SGMII transmission - minus		If unused, keep it open.
SGMII_TX_P	124	AO	SGMII transmission		If unused, keep it

			- plus		open.
SGMII_RX_P	125	AI	SGMII receiving - plus		If unused, keep it open.
SGMII_RX_M	126	AI	SGMII receiving -minus		If unused, keep it open.
Wireless Connectivity Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDC1_ DATA3	129	IO	SDIO data bus D3	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SDC1_ DATA2	130	IO	SDIO data bus D2	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SDC1_ DATA1	131	IO	SDIO data bus D1	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SDC1_ DATA0	132	IO	SDIO data bus D0	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
SDC1_CLK	133	DO	SDIO clock	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
SDC1_CMD	134	DO	SDIO command	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
PM_ENABLE	127	DO	External power control	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
WAKE_ON_ WIRELESS	135	DI	Wake up the host (EC25 module) by	V_{IL}min=-0.3V V_{IL}max=0.6V	1.8V power domain. Active low.

			FC20 module.	V_{IH}min=1.2V V_{IH}max=2.0V	If unused, keep it open.
WLAN_EN	136	DO	WLAN function control via FC20 module	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. Active high. If unused, keep it open.
COEX_UART_RX	137	DI	LTE/WLAN&BT coexistence signal	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
COEX_UART_TX	138	DO	LTE/WLAN&BT coexistence signal	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
WLAN_SLP_CLK	118	DO	WLAN sleep clock		If unused, keep it open.
BT_RTS*	37	DI	BT UART request to send	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
BT_TXD*	38	DO	BT UART transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
BT_RXD*	39	DI	BT UART receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
BT_CTS*	40	DO	BT UART clear to send	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
BT_EN*	139	DO	BT function control via FC20 module	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep it open.
RF Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_DIV	35	AI	Diversity antenna	50ohm impedance	If unused, keep it open.
ANT_MAIN	49	IO	Main antenna	50ohm impedance	
ANT_GNSS	47	AI	GNSS antenna	50 ohm impedance	If unused, keep it open.
GPIO Pins					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
WAKEUP_IN	1	DI	Sleep mode control	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Cannot be pulled up before startup. Low level wakes up the module. If unused, keep it open.
W_DISABLE#	4	DI	Airplane mode control	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. Pull-up by default. In low voltage level, module can enter into airplane mode. If unused, keep it open.
AP_READY	2	DI	Application processor sleep state detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
USB_BOOT Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	115	DI	Force the module to boot from USB port	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	3, 18, 23, 28~34, 43, 55, 73~84, 113, 114, 116, 117, 140~144		Reserved		Keep these pins unconnected.

NOTES

1. “*” means under development.
2. Pads 24~27 are multiplexing pins used for audio design on EC25 module and BT function on FC20 module.

3.4. Operating Modes

The table below briefly summarizes the various operating modes referred in the following chapters.

Table 5: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module hasregistered onthe network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network settingand data transfer rate.
Minimum Functionality Mode	**AT+CFUN** command can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and USIM card will be invalid.	
Airplane Mode	**AT+CFUN** command or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interface is not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

3.5. Power Saving

3.5.1. Sleep Mode

EC25 is able to reduce its current consumption to a minimum value during the sleep mode. The following section describes power saving procedure of EC25 module.

3.5.1.1. UART Application

If the host communicates with module via UART interface, the following preconditions can let the module enter into sleep mode.

- Execute **AT+QSCLK=1**command to enable sleep mode.
- Drive DTR to high level.

The following figure shows the connection between the module and the host.

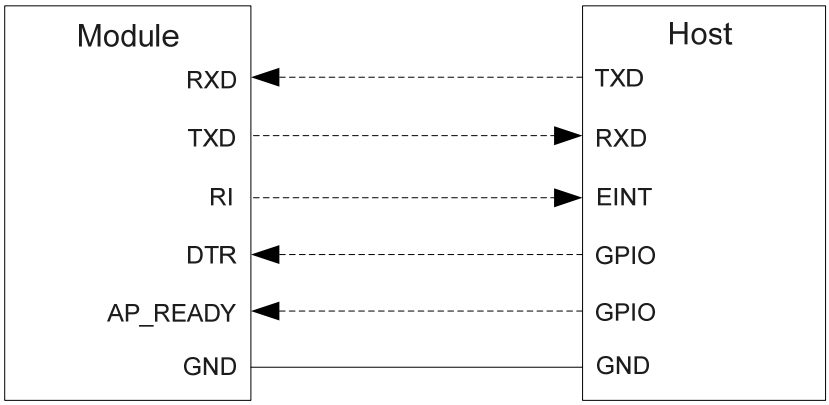


Figure 3: Sleep Mode Application via UART

- Driving the host DTR to low level will wake up the module.
- When EC25 has URC to report, RI signal will wake up the host. Refer to ***Chapter 3.16*** for details about RI behavior.
- AP_READY will detect the sleep state of the host (can be configured to high level or low level detection). Please refer to **AT+QCFG="apready"**command for details.

NOTE

AT+QCFG="apready"commandis under development.

3.5.1.2. USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup function, the followingthreepreconditions must be met tolet the module enter into the sleep mode.

- Execute **AT+QSCLK=1**command to enable the sleep mode.
- Ensure the DTR is held in high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters into suspended state.

The following figure shows the connection between the module and the host.

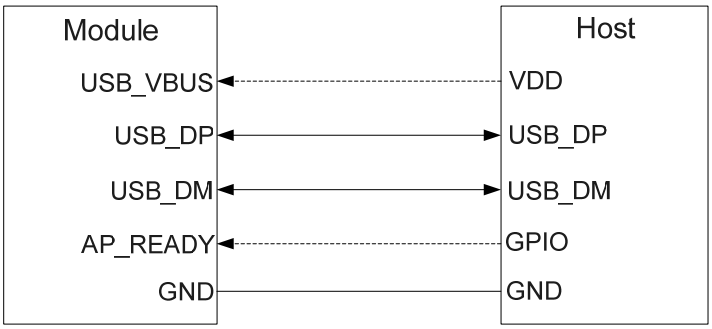


Figure 4: Sleep ModeApplication with USB Remote Wakeup

- Sending data to EC25through USB will wake up the module.
- When EC25has URC to report, the module will send remote wake-up signals viaUSB bus so as to wake up the host.

3.5.1.3. USB Application with USB Suspend/Resume and RI Function

If the host supports USB suspend/resume, but does not support remote wake-up function, the RI signal is needed to wake up the host.

There are threepreconditions to let the module enter into the sleep mode.

- Execute **AT+QSCLK=1**command to enable the sleep mode.
- Ensure the DTR is held in high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters into suspended state.

The following figure shows the connection between the module and the host.

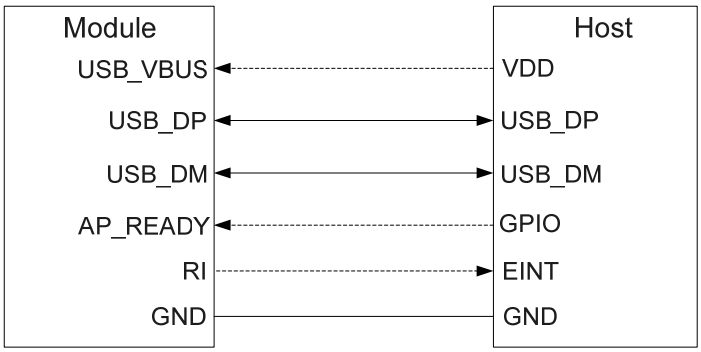


Figure 5: Sleep Mode Application with RI

- Sending data to EC25through USB will wake up the module.
- When EC25has URC to report, RI signal will wake up the host.

3.5.1.4. USB Application without USB Suspend Function

If the host does not support USB suspend function, you should disconnect USB_VBUS with additional control circuit to let the module enter into sleep mode.

- Execute **AT+QSCLK=1**commandto enable the sleep mode.
- Ensure the DTR is held in high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

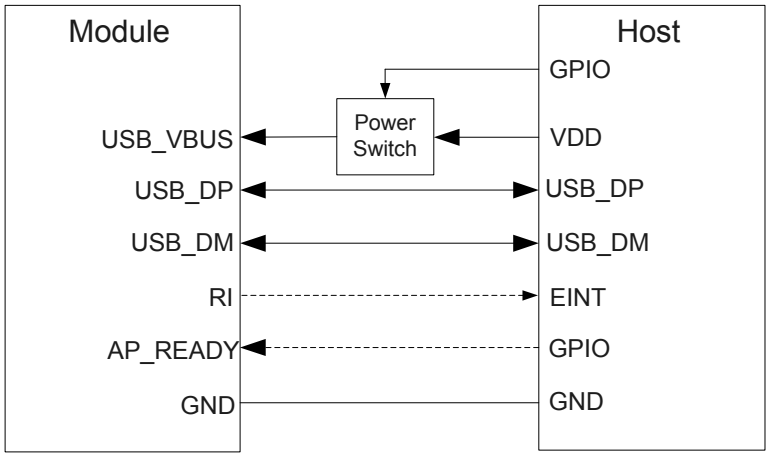


Figure 6: Sleep Mode Application without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

Please pay attention to the level match shown in dotted line between the module and the host.Refer to ***document [1]*** for more details about EC25 power management application.

3.5.2. Airplane Mode

When the module enters into airplane mode, the RF function does not work, and all AT commands correlative with RF function will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default; driving it to low level will let the module enter into airplane mode.

Software:

AT+CFUNcommand provides the choice of the functionality level.

- **AT+CFUN=0:** Minimum functionality mode; both USIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

NOTES

1. The W_DISABLE# control function is disabled in firmware by default. It can be enabled by**AT+QCFG="airplanecontrol"**command. This commandis under development.
2. The execution of **AT+CFUN** command will not affect GNSS function.

3.6. Power Supply

3.6.1. Power Supply Pins

EC25 provides four VBAT pins dedicated to connect with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module RF part
- Two VBAT_BB pins for module baseband part

The following table shows the details of VBAT pins and ground pins.

Table 6: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	57,58	Power supply for module RF part	3.3	3.8	4.3	V
VBAT_BB	59,60	Power supply for module baseband part	3.3	3.8	4.3	V
GND	8,9,19,22, 36,46, 48,50~54,56,	Ground	-	0	-	V

	72, 85~112

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.3Vto4.3V. Please make sure that the input voltage will never drop below 3.3V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G and 4G networks.

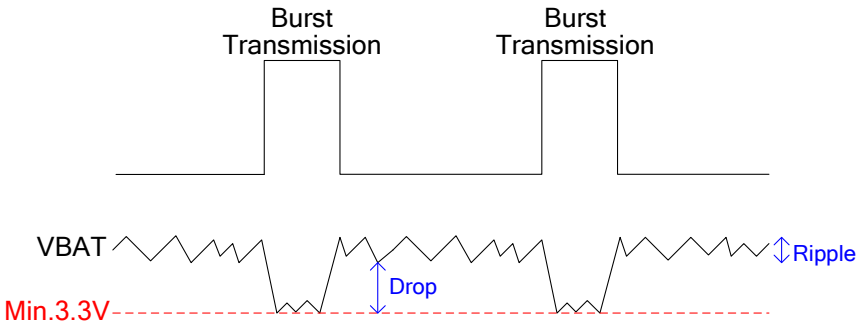


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100μF with low ESR should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be used toprovide the low ESR. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1mm; andthe width of VBAT_RF trace should be no less than 2mm.In principle, the longer the VBAT trace is, the wider it will be.

Three ceramic capacitors (100nF, 33pF, 10pF) are recommended to be applied to the VBAT pins. These capacitors should be placed close to the VBAT pins. In addition, in order to get a stable power source, it is suggested that you should use a zener diode of which reverse zener voltage is 5.1V and dissipation power is more than 0.5W. The following figure shows the star structure of the power supply.

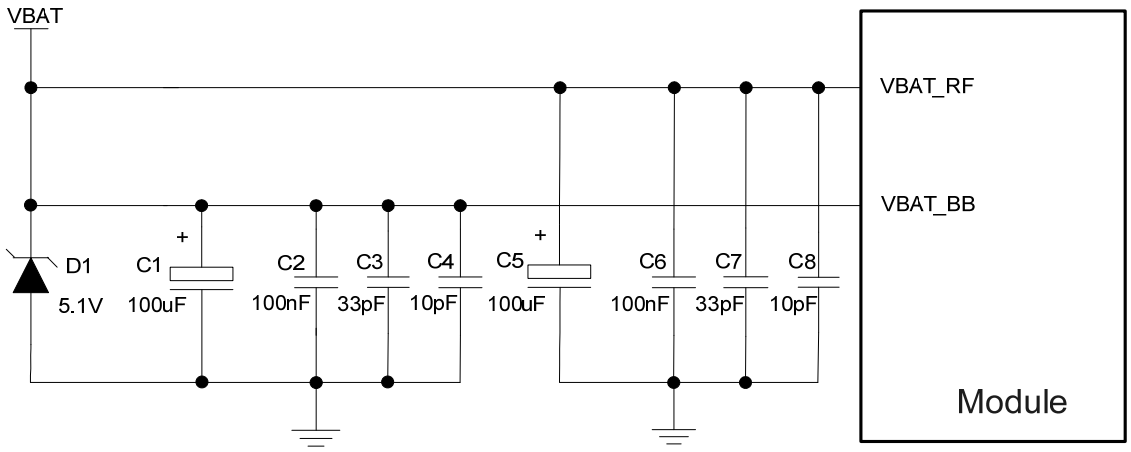


Figure 8: Star Structure of the Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, asthe performance of the module largely depends on the power source. The power supply is capable of providing sufficient current up to 2A at least. If the voltage drop between the input and output is not too high, it is suggested that you shoulduse an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as thepower supply.

The following figure shows a reference design for +5V input power source. The typical output of the power supplyis about 3.8V and the maximum load current is 3A.

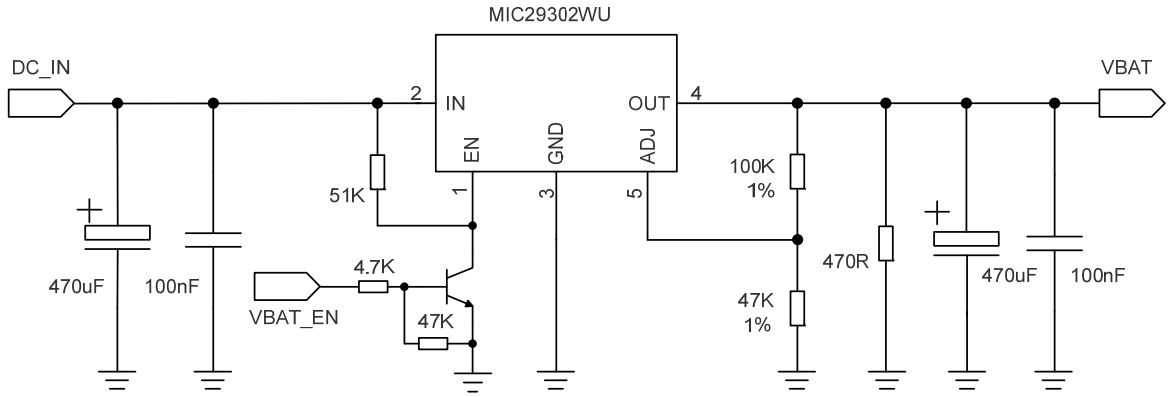


Figure 9: Reference Circuit of Power Supply

NOTE

In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shutdown by PWRKEY or AT command, the power supply can be cut off.

3.6.4. Monitor the Power Supply

AT+CBC command can be used to monitor the VBAT_BB voltage value. For more details, please refer to ***document [2]***.

3.7. Turn on and off Scenarios

3.7.1. Turn on Module Using the PWRKEY

The following table shows the pin definition of PWRKEY.

Table 7: PWRKEY Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRKEY	21	Turn on/off the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.

When EC25 is in power down mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 100ms. It is recommended to use an open drain/collector driver to control the PWRKEY.After STATUS pin (require external pull-up) outputting a low level, PWRKEY pin can be released. A simple reference circuit is illustrated in the following figure.

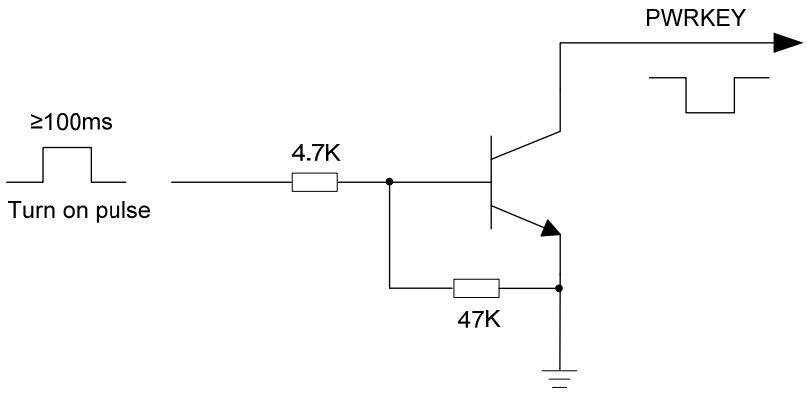


Figure 10: Turn on the Module Using Driving Circuit

The other way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from finger. Therefore, aTVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shownin the following figure.

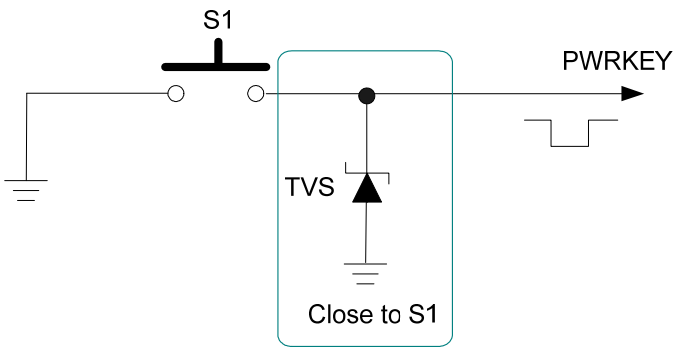


Figure 11: Turn on the Module Using Keystroke

The turn on scenario is illustrated in the following figure.

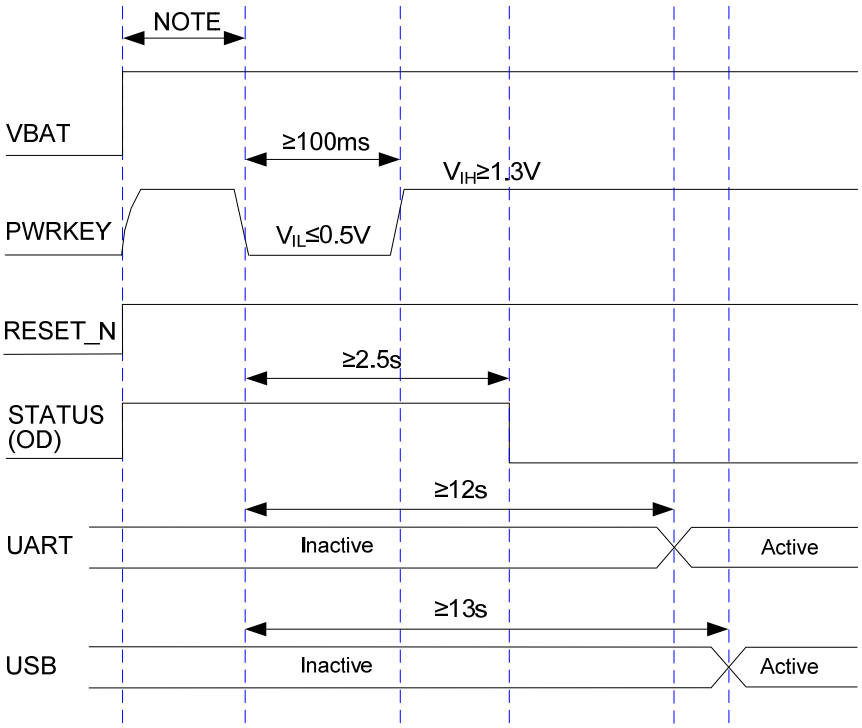


Figure 12: Timing of Turning on Module

NOTE

Please make sure that VBAT is stable before pulling down PWRKEY pin. The time between them is no less than 30ms.

3.7.2. Turn off Module

The following procedures can be used to turn off the module:

- Normal power down procedure: Turn off the module using the PWRKEY pin.
- Normal power down procedure: Turn off the module using **AT+QPOWD**command.

3.7.2.1. Turn off Module Using the PWRKEY Pin

Driving the PWRKEY pin to a low level voltage for at least 650ms, the module will execute power-down procedure after the PWRKEY is released. The power-down scenario is illustrated inthe following figure.

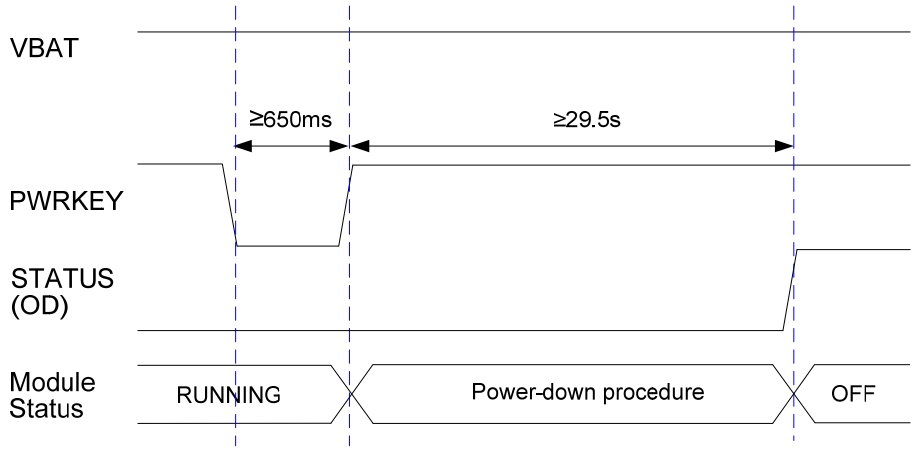


Figure 13: Timing of Turning off Module

3.7.2.2. Turn off Module Using AT Command

It is also a safe way to use **AT+QPOWD**command to turn off the module, which is similar to turning off the module via PWRKEY pin.

Please refer to***document [2]*** for details about **AT+QPOWD** command.

NOTE

Inorder to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shutdown by PWRKEY or AT command, the power supply can be cut off.

3.8. Reset the Module

The RESET_N pin can be used to reset the module.The module can be reset by driving RESET_N to a low level voltage for time between 150ms and 460ms.

Table 8: RESET_N Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET_N	20	Reset the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

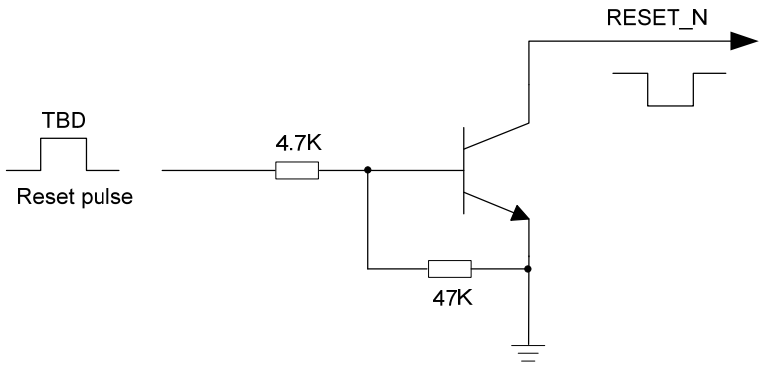


Figure 14: Reference Circuit of RESET_N by Using Driving Circuit

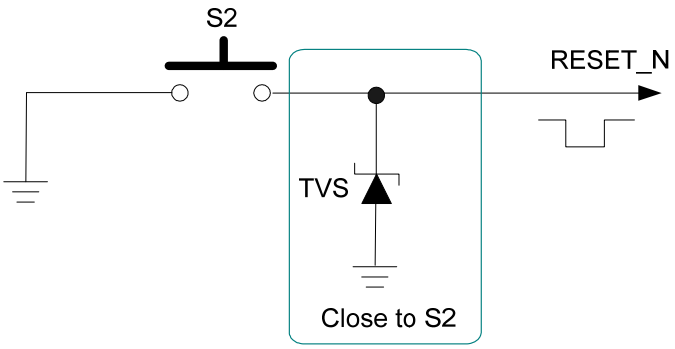


Figure 15: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated inthe following figure.

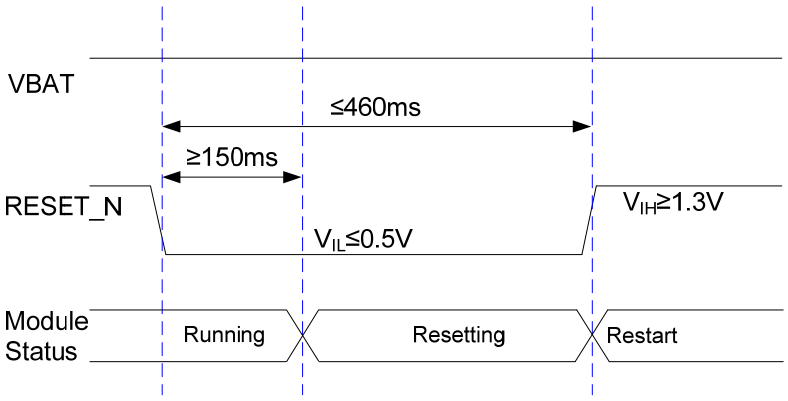


Figure 16: Timing of Resetting Module

NOTES

1. Use RESET_N only when turning off the module by **AT+QPOWD**command and PWRKEY pin failed.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

3.9. USIM Card Interface

The USIM card interface circuitrymeets ETSI and IMT-2000 SIM interface requirements. Both 1.8V and 3.0V USIM cards are supported.

Table 9: Pin Definition of the USIM Card Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	14	PO	Power supply for USIM card	Either 1.8V or 3.0V is supported by the module automatically.
USIM_DATA	15	IO	Data signal of USIM card	
USIM_CLK	16	DO	Clock signal of USIM card	
USIM_RST	17	DO	Reset signal of USIM card	
USIM_ PRESENCE	13	DI	USIM card insertion detection	
USIM_GND	10		Specified ground for USIM card	

EC25 supports USIM card hot-plug via the USIM_PRESENCE pin. The function supports low level and high level detections, and isdisabled by default. Please refer to ***document [2]*** about **AT+QSIMDET** command for details.

The following figure shows a reference design for USIM card interface with an 8-pin USIM card connector.

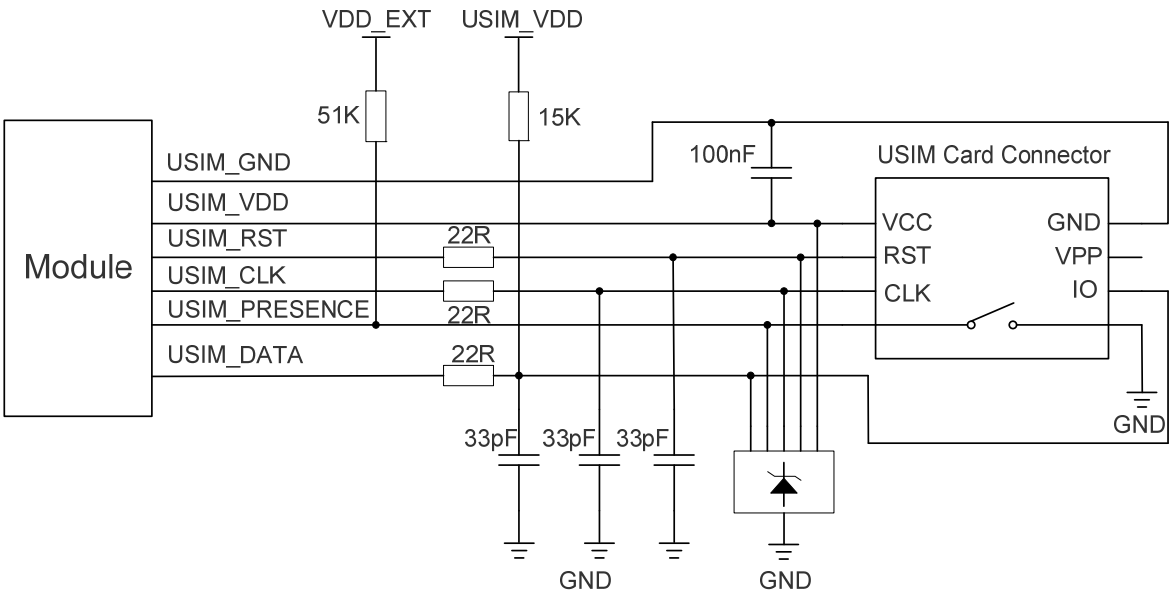


Figure 17: Reference Circuit of USIM Card Interface with an 8-Pin USIM Card Connector

If USIM card detection function is not needed, please keep USIM_PRESENCE unconnected. Areference circuit for USIM card interface witha 6-pin USIM card connector is illustrated inthe following figure.

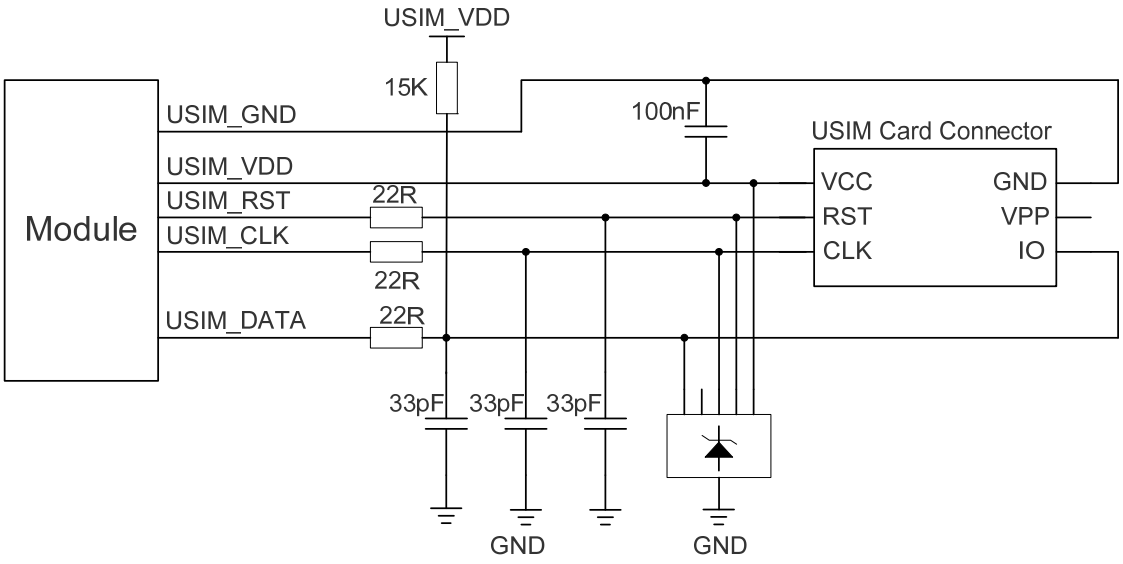


Figure 18: Reference Circuit of USIM Card Interface with a 6-Pin USIM Card Connector

In order to enhance the reliability and availability of the USIM card in your application, please follow the criteria below in USIM circuit design:

- Keep layout of USIM card as close to the module as possible. Keep the trace length as less than 200mm as possible.
- Keep USIM card signals away from RF and VBAT traces.
- Assure the ground between the module and the USIM card connector short and wide. Keep thetrace width of ground and USIM_VDD no less than 0.5mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away fromeach other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not be more than 50pF. The 22ohmresistors should be added in series between the module and the USIM card so as to suppress EMI spurious transmission and enhance ESD protection. The 33pFcapacitors are used for filtering interference of GSM900.Please note that the USIM peripheral circuit should be close to the USIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion areapplied, and should be placed close to the USIM card connector.

3.10. USB Interface

EC25 contains one integrated Universal Serial Bus (USB) transceiver which complies with the USB 2.0 specification and supports high-speed (480Mbps) and full-speed (12Mbps)modes. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB*. The following table shows the pin definition of USB interface.

Table 10: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB Signal Part				
USB_DP	69	IO	USB differential data bus (positive)	Require differential impedance of 90Ω
USB_DM	70	IO	USB differential data bus (minus)	Require differential impedance of 90Ω
USB_VBUS	71	PI	Used for detecting the USB connection	Typical 5.0V
GND	72		Ground	

For more details about the USB 2.0 specifications, please visithttp://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade in your design. The following figure shows areference circuit of USB interface.

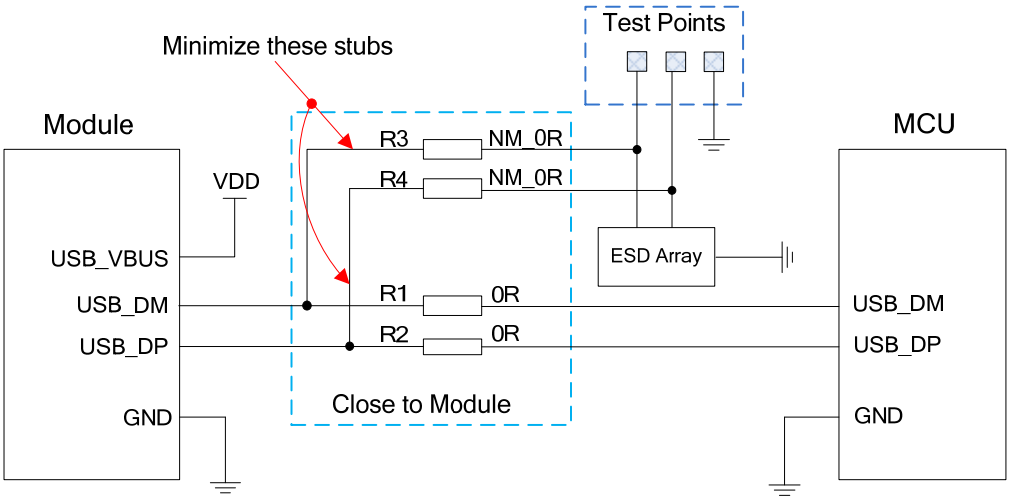


Figure 19: Reference Circuit of USB Application

In order to ensurethe integrity of USB data line signal, components R1, R2, R3 and R4 must be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

In order to ensure the USB interface design corresponding with the USB 2.0 specification, please comply with the following principles:

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90ohm.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding onnot only upper and lower layers but also right and left sides.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 2pF.
- Keep the ESD protection components to the USB connector as close as possible.

NOTES

1. EC25 module can only be used as a slave device.
2. “*” means under development.

3.11. UART Interfaces

The module provides two UART interfaces: the main UART interface and the debug UART interface. The following shows their features.

- The main UART interface supports4800, 9600, 19200,38400,57600,115200,230400,460800,921600 and3000000bps baud rates, and the default is 115200bps. This interface is used for data transmission and AT command communication.
- The debug UART interface supports 115200bps baud rate. It is used forLinux console and log output.

The following tables show the pin definition.

Table 11: Pin Definition of the Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
RI	62	DO	Ring indicator	1.8V power domain
DCD	63	DO	Data carrier detection	1.8V power domain
CTS	64	DO	Clear to send	1.8V power domain
RTS	65	DI	Request to send	1.8V power domain
DTR	66	DI	Sleep mode control	1.8V power domain
TXD	67	DO	Transmit data	1.8V power domain
RXD	68	DI	Receive data	1.8V power domain

Table 12: Pin Definition of the Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	12	DO	Transmit data	1.8V power domain
DBG_RXD	11	DI	Receive data	1.8V power domain

The logic levels are described in the following table.

Table 13:Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The module provides 1.8V UART interface. A level translator should be used if your application is equipped with a 3.3V UART interface. A level translator TXS0108EPWR provided by *Texas Instrument* is recommended. The following figure shows a reference design.

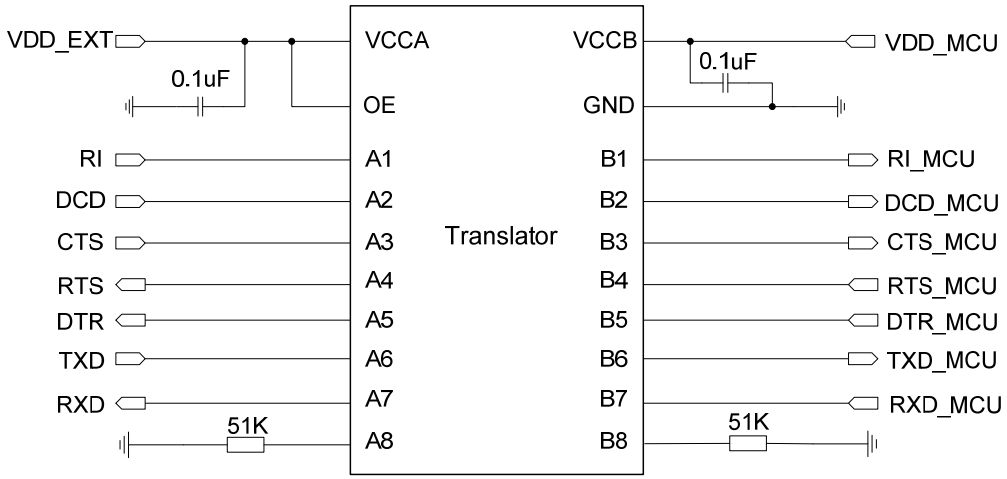


Figure 20: Reference Circuit with Translator Chip

Please visit http://www.ti.comfor more information.

Another example with transistor translation circuit is shown as below. Thecircuit design of dotted line section can refer to the design of solid line section, in terms of both module input and output circuit designs, but please pay attention to the direction of connection.

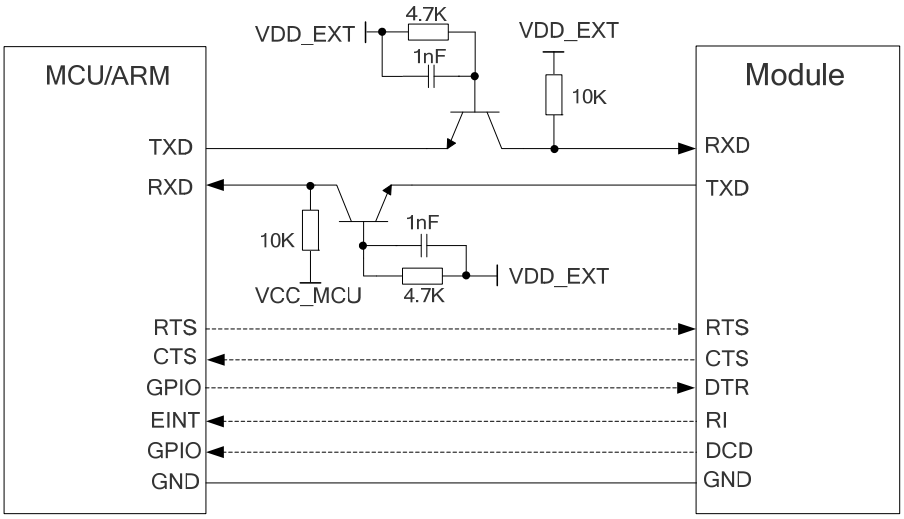


Figure 21: Reference Circuit with Transistor Circuit

NOTE

Transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.

3.12. PCM and I2C Interfaces

EC25 provides one Pulse Code Modulation (PCM) digital interface for audio design, which supports the following modes:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, PCM_CLK supports 128,256,512,1024 and2048kHz for different speech codecs.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge.The PCM_SYNC rising edge represents the MSB. In this mode, PCM interface operates with a 128kHz PCM_CLK and an 8kHz, 50% duty cycle PCM_SYNC only.

EC25 supports 8-bit A-law* andμ-law*, and also 16-bit linear data formats. The following figures show theprimary mode's timing relationship with 8kHz PCM_SYNC and 2048kHz PCM_CLK, as well asthe auxiliary mode's timing relationship with 8kHz PCM_SYNC and 128kHz PCM_CLK.

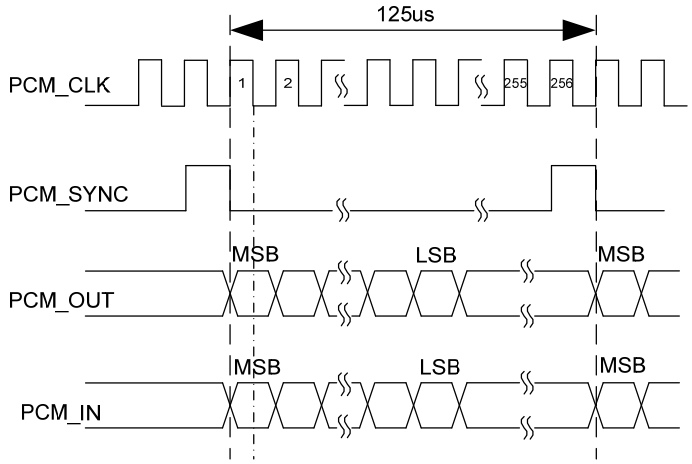


Figure 22: Primary Mode Timing

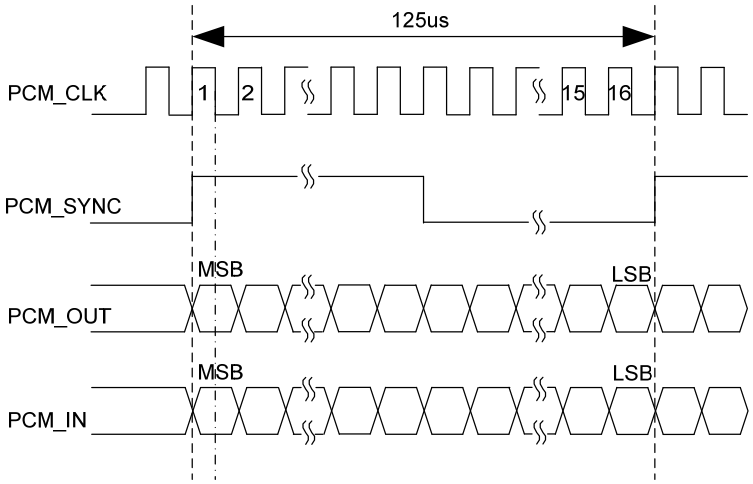


Figure 23: Auxiliary Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 14: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_IN	24	DI	PCM data input	1.8V power domain
PCM_OUT	25	DO	PCM data output	1.8V power domain
PCM_SYNC	26	IO	PCM data frame sync signal	1.8V power domain

PCM_CLK	27	IO	PCM data bit clock	1.8V power domain
I2C_SCL	41	OD	I2C serial clock	Require external pull-up to 1.8V
I2C_SDA	42	OD	I2C serial data	Require external pull-up to 1.8V

Clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048kHzPCM_CLK and 8kHz PCM_SYNC.Please refer to ***document [2]*** about **AT+QDAI**command for details.

The following figure shows areference design of PCM interface with external codec IC.

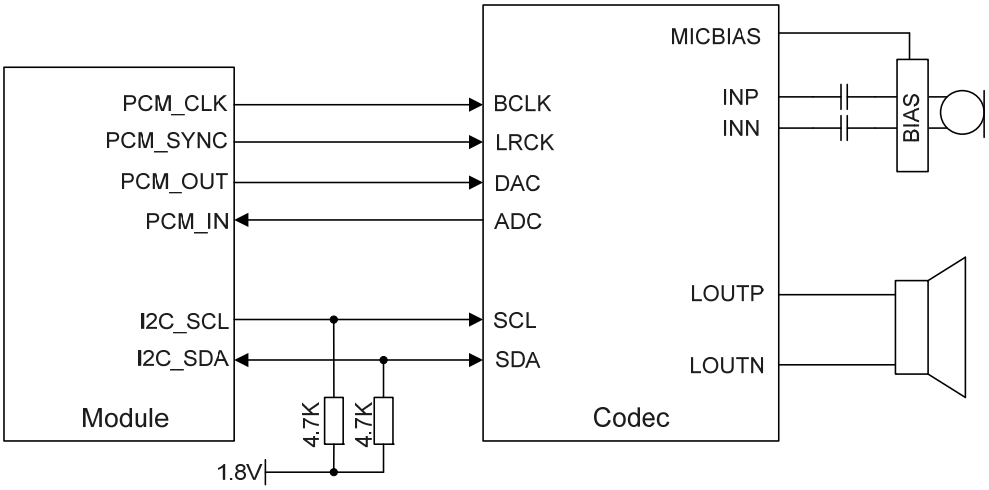


Figure 24: Reference Circuit of PCM Application with Audio Codec

NOTES

1. "*" means under development.
2. It is recommended to reserve RC (R=22ohm, C=22pF) circuit on the PCM lines, especially for PCM_CLK.
3. EC25 works as a master device pertaining to I2C interface.

3.13. ADC Function

The module provides two analog-to-digital converters (ADC).**AT+QADC=0**command can be used toread the voltage value on ADC0 pin. **AT+QADC=1**command can be used to read the voltage value on ADC1 pin. For more details about these AT commands, please refer to***document [2]***.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 15: Pin Definition of the ADC

Pin Name	Pin No.	Description
ADC0	45	General purpose analog to digital converter
ADC1	44	General purpose analog to digital converter

The following table describes the characteristic of the ADC function.

Table 16: Characteristic of the ADC

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0.3		VBAT_BB	V
ADC1 Voltage Range	0.3		VBAT_BB	V
ADC Resolution			15	bits

NOTES

1. ADC input voltage must not exceed VBAT_BB.
2. It is prohibited to supply any voltage to ADC pinswhen VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.

3.14. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides two pins which are NET_MODE and NET_STATUS. The following tables describe pin definition and logic level changes in different network status.

Table 17: Pin Definition of Network Connection Status/Activity Indicator

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE[1)]	5	DO	Indicate the module network registration mode.	1.8V power domain
NET_STATUS	6	DO	Indicate the module network activity status.	1.8V power domain

NOTE

[1)]meansthat this pin cannot be pulled up before startup.

Table 18: Working State of the Network Connection Status/Activity Indicator

Pin Name	Logic Level Changes	Network Status
NET_MODE	Always High	Registered on LTE network
	Always Low	Others
NET_STATUS	Flicker slowly (200ms High/1800ms Low)	Network searching
	Flicker slowly (1800ms High/200ms Low)	Idle
	Flicker quickly (125ms High/125ms Low)	Data transfer is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

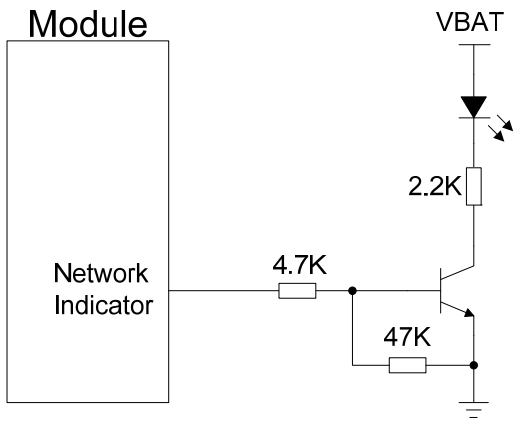


Figure 25: Reference Circuit of the Network Indicator

3.15. STATUS

The STATUS pin is an open drain output for indicating the module's operation status. You can connect it to a GPIO of DTE with a pulled up resistor, or as LED indication circuit as below. When the module is turned on normally, the STATUS will present the low state. Otherwise, the STATUS will present high-impedance state.

Table 19: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	61	OD	Indicate the module operation status	Require external pull-up

The following figure shows different circuitdesigns of STATUS, and you can choose either one according to your application demands.

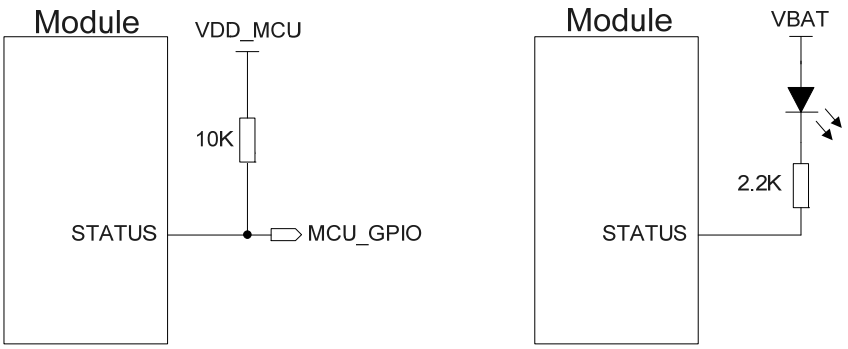


Figure 26: Reference Circuits of STATUS

3.16. Behavior of the RI

AT+QCFG="risignaltype","physical"command can be used to configure RI behavior.

No matter on which port URC is presented, URC will trigger the behavior of RI pin.

NOTE

URC can be output from UART port, USB AT port and USB modem port by **AT+QURCCFG** command. The default port is USB AT port.

In addition, RI behavior can be configured flexibly. The default behavior of the RI is shown as below.

Table 20: Behavior of the RI

State	Response
Idle	RI keeps in high level
URC	RI outputs 120ms low pulse when new URC returns

The RI behavior can be changed by **AT+QCFG="urc/ri/ring"** command. Please refer to ***document [2]*** for details.

3.17. SGMII Interface

EC25 includes an integrated Ethernet MAC with an SGMII interface and twomanagement interfaces,key features of the SGMII interface are shown below:

- IEEE802.3 compliance
- Full duplex at 1000Mbps
- Half/full duplex for 10/100Mbps
- Support VLAN tagging
- Support IEEE1588 and Precision Time Protocol(PTP)
- Can be used to connect toexternal Ethernet PHY like AR8033, or to an external switch
- Management interfaces support dual voltage 1.8V/2.85V

The following table shows the pin definition of SGMII interface.

Table 21: Pin Definition of the SGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
Control Signal Part				
EPHY_RST_N	119	DO	Ethernet PHY reset	1.8V/2.85V power domain
EPHY_INT_N	120	DI	Ethernet PHY interrupt	1.8V power domain
SGMII_MDATA	121	IO	SGMII MDIO(Management Data Input/Output) data	1.8V/2.85V power domain
SGMII_MCLK	122	DO	SGMII MDIO (Management Data Input/Output) clock	1.8V/2.85V power domain
USIM2_VDD	128	PO	SGMII MDIO pull-up power source	Configurable power source. 1.8V/2.85V power domain. External pull-up power source for SGMII MDIO pins.
SGMII Signal Part				
SGMII_TX_M	123	AO	SGMII transmission-minus	Connect with a 0.1uF capacitor, close to the PHY side.
SGMII_TX_P	124	AO	SGMII transmission-plus	Connect with a 0.1uF capacitor, close to the PHY side.

SGMII_RX_P 125	AI	SGMII receiving-plus	Connect with a 0.1uF capacitor, close to EC25 module.
SGMII_RX_M 126	AI	SGMII receiving-minus	Connect with a 0.1uF capacitor, close to EC25 module.

The following figure shows the simplified block diagram for Ethernet application.

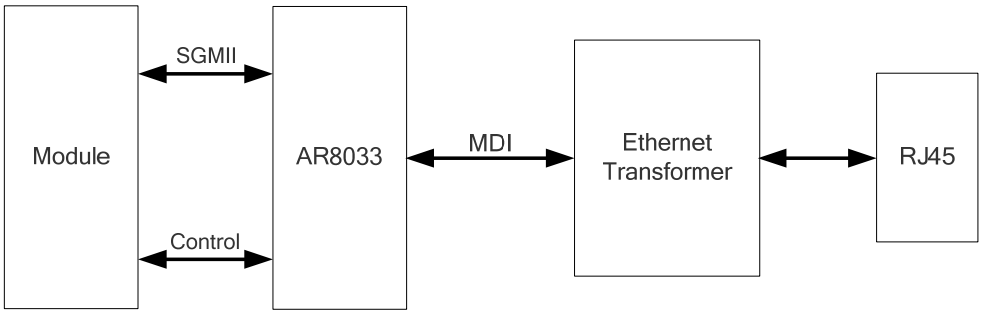


Figure 27: Simplified Block Diagram for Ethernet Application

The following figure shows a reference design ofSGMII interface with PHY AR8033 application.

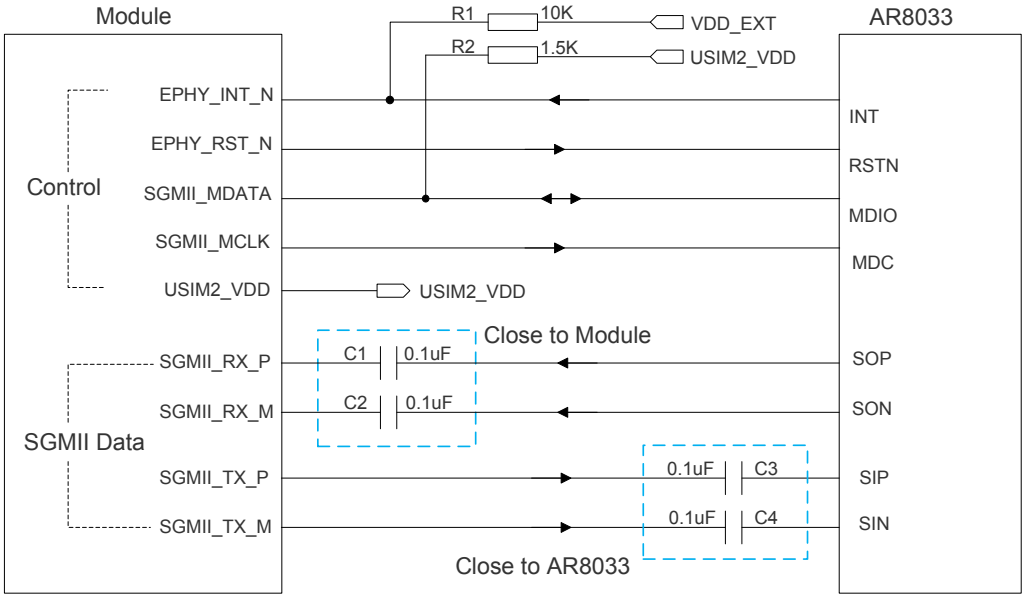


Figure 28: Reference Circuit of SGMII Interface with PHY AR8033 Application

In order to enhance the reliability and availability in your application, please follow the criteria below in the Ethernet PHY circuit design:

- Keep SGMII data and control signals away from RF and VBAT trace.
- Keep the maximum trace length less than 10inch and keep skew on the differential pairs less than

20mil.

- The differential impedance of SGMII data trace is 100ohm±10%.
- To minimize crosstalk, the distance between separate adjacent pairs that are on the same layer must be equal to or larger than 40mil.

NOTE

For more information about SGMII application, please refer to ***document [5]***and ***document [7]***.

3.18. Wireless Connectivity Interfaces

EC25supports a low-power SDIO 3.0 interface for WLAN and a UART/PCM interface for BT.

The following table shows the pin definition of wireless connectivity interfaces.

Table 22: Pin Definition of Wireless Connectivity Interfaces

Pin Name	Pin No.	I/O	Description	Comment
WLAN Part				
SDC1_DATA3	129	IO	SDIO data bus D3	1.8V power domain
SDC1_DATA2	130	IO	SDIO data bus D2	1.8V power domain
SDC1_DATA1	131	IO	SDIO data bus D1	1.8V power domain
SDC1_DATA0	132	IO	SDIO data bus D0	1.8V power domain
SDC1_CLK	133	DO	SDIO clock	1.8V power domain
SDC1_CMD	134	IO	SDIO command	1.8V power domain
WLAN_EN	136	DO	WLAN function control via FC20 module. Active high.	1.8V power domain
Coexistence and Control Part				
PM_ENABLE	127	DO	External power control	1.8V power domain
WAKE_ON_WIRELESS	135	DI	Wake up the host (EC25 module) by FC20 module.	1.8V power domain
COEX_UART_RX	137	DI	LTE/WLAN&BT coexistence signal	1.8V power domain

COEX_UART_TX	138	DO	LTE/WLAN&BT coexistence signal	1.8V power domain
WLAN_SLP_CLK	118	DO	WLAN sleep clock	
BT Part*				
BT_RTS*	37	DI	BT UART request to send	1.8V power domain
BT_TXD*	38	DO	BT UART transmit data	1.8V power domain
BT_RXD*	39	DI	BT UART receive data	1.8V power domain
BT_CTS*	40	DO	BT UART clear to send	1.8V power domain
PCM_IN[1)]	24	DI	PCM data input	1.8V power domain
PCM_OUT[1)]	25	DO	PCM data output	1.8V power domain
PCM_SYNC[1)]	26	IO	PCM data frame sync signal	1.8V power domain
PCM_CLK[1)]	27	IO	PCM data bit clock	1.8V power domain
BT_EN*	139	DO	BT function control via FC20 module. Active high.	1.8V power domain

NOTES

1. "*" means under development.
2. [1)] Pads 24~27 are multiplexing pins used for audio design on EC25 module and BT function on FC20 module.

The following figure shows a reference design of Wireless Connectivity interfaces with QuectelFC20 module.

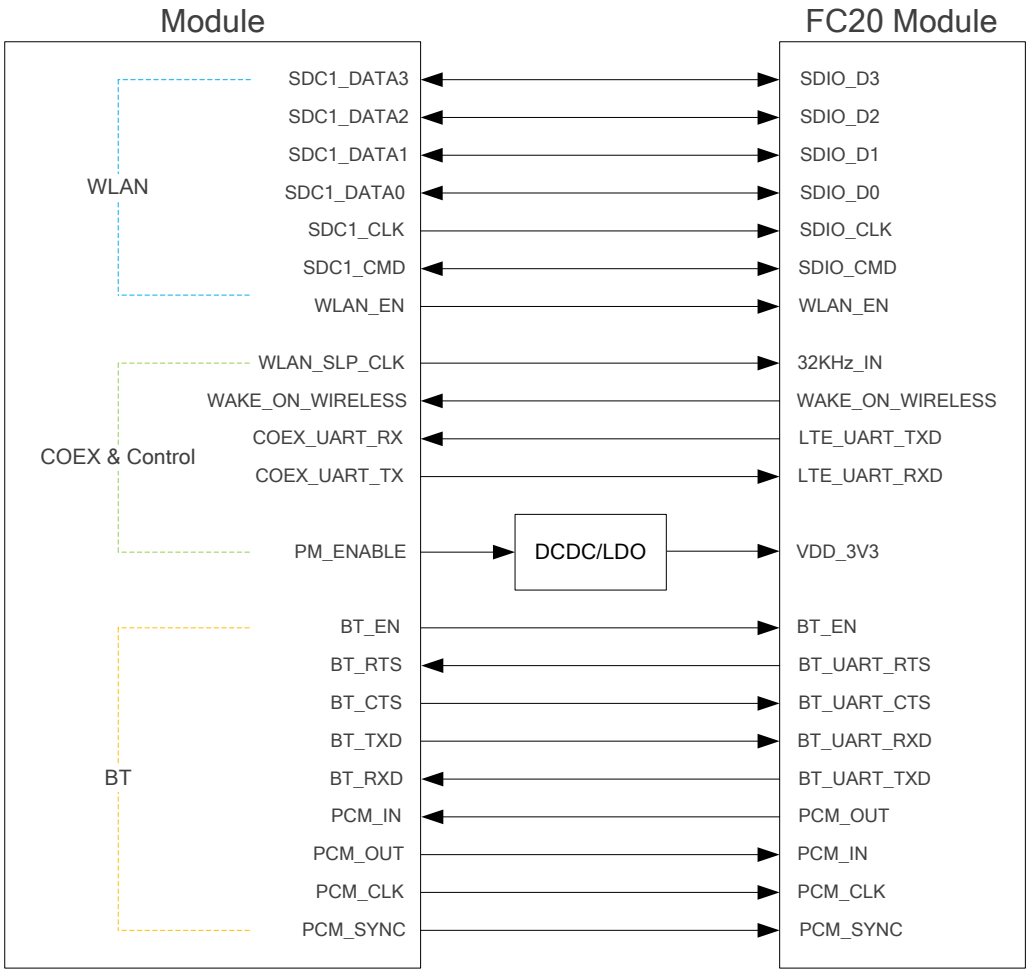


Figure 29: Reference Circuit of Wireless Connectivity Interfaces with FC20 Module

NOTES

1. FC20 module can only be used as a slave device,
2. When BT function is enabled on EC25 module, PCM_SYNC and PCM_CLK pins are only used to output signals.
3. For more information about wireless connectivity interfaces application, please refer to ***document [5]***.

3.18.1. WLAN Interface

EC25 provides a low power SDIO 3.0 interface and control interface for WLAN design.

SDIO interface supports the following modes:

- Single data rate(SDR) mode (up to 200MHz)
- Double data rate(DDR) mode (up to 52MHz)

As SDIO signals are very high-speed, in order to ensure the SDIO interface design corresponds with the SDIO 3.0 specification, please comply with the following principles:

- It is important to route the SDIO signal traces with total grounding. The impedance of SDIOsignal trace is 50ohm(±10%).
- Protect other sensitive signals/circuits(RF, analog signals, etc.) from SDIO corruption and protect SDIO signals from noisy signals (clocks, DCDCs, etc.).
- It is recommended to keep matching lengthbetween CLK andDATA/CMD less than 1mm and total routing length less than 50mm.
- Keep termination resistorswithin 15~24ohm on clock lines near the module and keep the route distance from the module clock pins to termination resistorsless than 5mm.
- Make sure the adjacent trace spacing is 2x line width and bus capacitance is less than 15pF.

3.18.2. BT Interface*

EC25 supportsa dedicated UART interface and a PCM interface for BT application.

Further information about BT interface will be added in future version of this document.

NOTE

"*" means under development.

3.19. USB_BOOT Interface

EC25 provides a USB_BOOT pin. During development or factory production, USB_BOOT pin can force the module to boot from USB port for firmware upgrade.

Table 23: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Force the module to boot from USB port	1.8V power domain. Active high. If unused, keep it open.

The following figure shows a reference circuit of USB_BOOT interface.

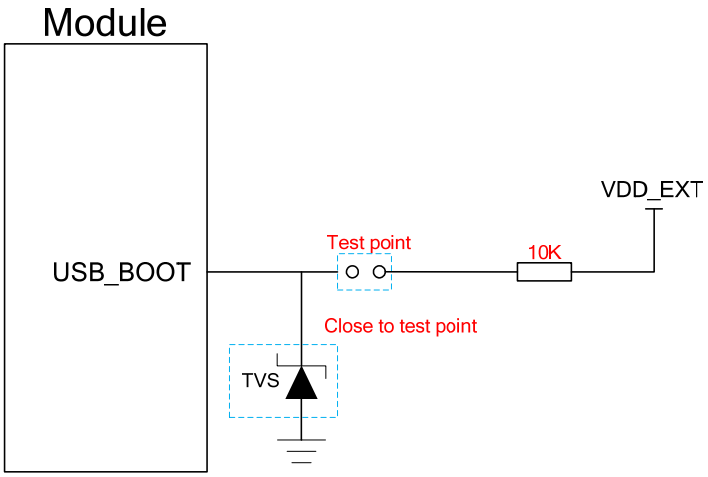


Figure 30: Reference Circuit of USB_BOOT Interface

4 GNSS Receiver

4.1. General Description

EC25 includes a fully integrated global navigation satellite system solution that supports Gen8C-Lite of Qualcomm (GPS, GLONASS, BeiDou, Galileo and QZSS).

EC25 supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1Hz data update rate via USB interface by default.

By default, EC25 GNSS engine is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, please refer to ***document [3]***.

4.2. GNSS Performance

The following table shows GNSS performance of EC25.

Table 24: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-146	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-157	dBm
TTFF (GNSS)	Cold start @open sky	Autonomous	35	s
		XTRA enabled	18	s
	Warm start @open sky	Autonomous	26	s
		XTRA enabled	2.2	s
	Hot start	Autonomous	2.5	s

	@open sky	XTRA enabled	1.8	s
Accuracy (GNSS)	CEP-50	Autonomous @open sky	<1.5	m

NOTES

1. Tracking sensitivity: the lowest GNSSsignal value at the antenna port on which the module can keep on positioning for 3 minutes.
2. Reacquisition sensitivity: the lowest GNSS signal value at the antenna port on which the module can fix position again within 3 minutes after loss of lock.
3. Cold start sensitivity: the lowest GNSS signal value at the antenna port on which the module fixes position within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in your design.

- Maximize the distance among GNSS antenna, main antenna and Rx-diversity antenna.
- Digital circuits such as USIM card, USB interface, camera module, display connector and SD card should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50ohm characteristic impedance for the ANT_GNSS trace.

Please refer to ***Chapter 5*** for GNSS antenna reference design and antenna installation information.

5 Antenna Interfaces

EC25 antenna interfaces include a main antenna interface,anRx-diversity antennainterface which is used toresist the fall of signals caused by high speed movement and multipath effect, and a GNSS antenna interface. The antenna interfaces have an impedance of 50ohm.

5.1. Main/Rx-diversityAntenna Interface

5.1.1. Pin Definition

The pin definition of main antenna and Rx-diversityantenna interfaces are shown below.

Table 25: Pin Definition of the RF Antenna

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	49	IO	Main antenna pad	50ohmimpedance
ANT_DIV	35	AI	Receive diversityantenna pad	50ohm impedance

5.1.2. Operating Frequency

Table 26: Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
B1	1920~1980	2110~2170	MHz
B2 (1900)	1850~1910	1930~1990	MHz
B3 (1800)	1710~1785	1805~1880	MHz
B4	1710~1755	2110~2155	MHz
B5 (850)	824~849	869~894	MHz
B6	830~840	875~885	MHz

B7	2500~2570	2620~2690	MHz
B8 (900)	880~915	925~960	MHz
B12	699~716	729~746	MHz
B13	777~787	746~756	MHz
B18	815~830	860~875	MHz
B19	830~845	875~890	MHz
B20	832~862	791~821	MHz
B26	814~849	859~894	MHz
B28	703~748	758~803	MHz
B38	2570~2620	2570~2620	MHz
B40	2300~2400	2300~2400	MHz
B41	2555~2655	2555~2655	MHz

5.1.3. Reference Design of RF Antenna Interface

Areference design of ANT_MAIN and ANT_DIVantenna pads is shown as below. It should reserve a π-type matching circuit for better RF performance. The capacitors are not mounted by default.

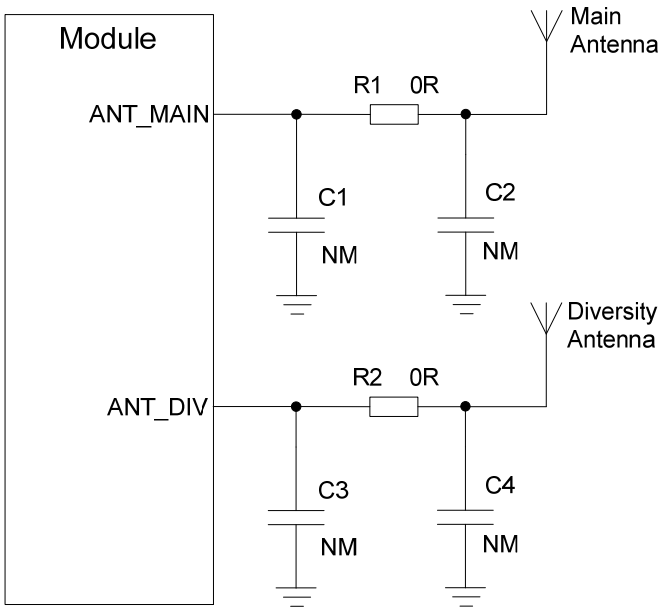


Figure 31: Reference Circuit of RF Antenna Interface

NOTES

1. Keep a proper distance between the main antenna and theRx-diversityantenna to improve the receiving sensitivity.
2. ANT_DIV function is enabledby default.
3. Place theπ-type matching components (R1, C1, C2, R2, C3, C4) as close to the antenna as possible.

5.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 ohm. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the distance between signal layer and reference ground (H), and the clearance between RF trace and ground (S). Microstrip line or coplanar waveguide line is typically used in RF layout for characteristic impedance control. The following are reference designs of microstrip line or coplanar waveguide line with different PCB structures

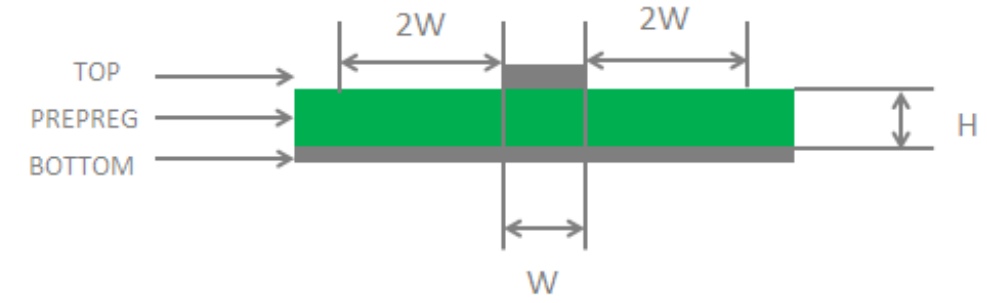


Figure 32: Microstrip Line Design on a 2-layer PCB

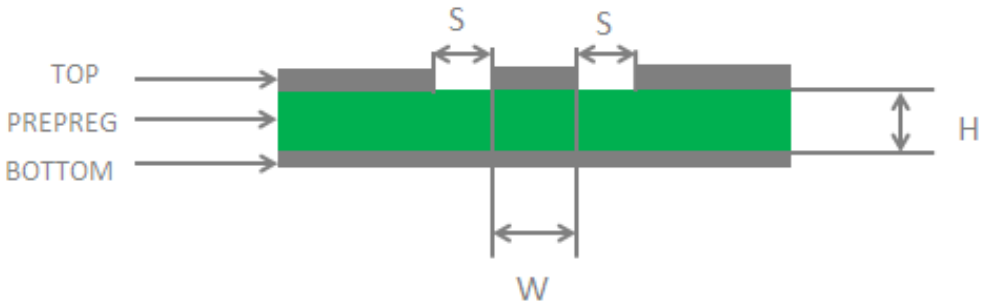


Figure 33: Coplanar Waveguide Line Design on a 2-layer PCB

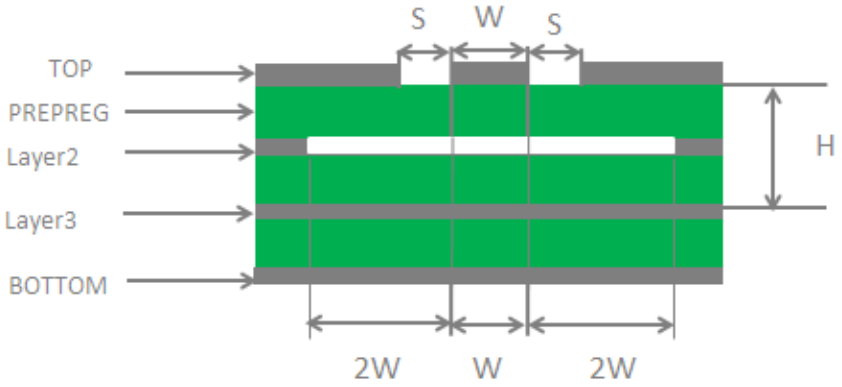


Figure 34: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 3 as Reference Ground)

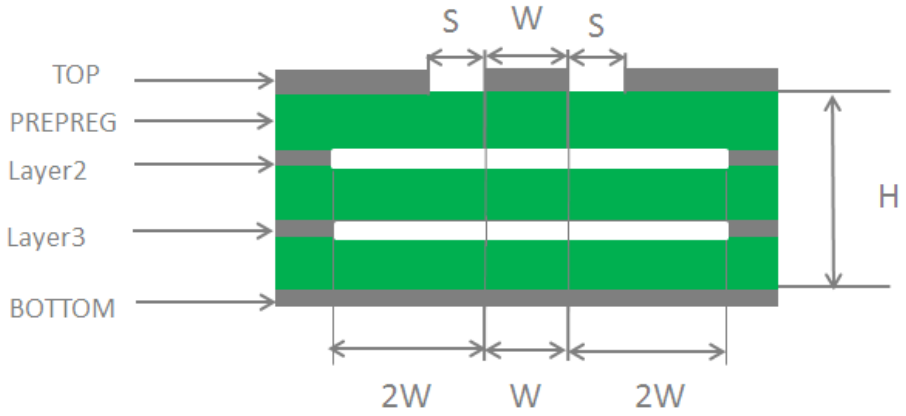


Figure 35: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use impedance simulation tool to control the characteristic impedanceof RF tracesas 50ohm.
- The GND pins adjacent to RF pins should not be hot welded, and should be fully connected to ground.
- The distance between the RF pinsand the RFconnector should be as short as possible, and all the right angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground viasaround RF traces and the reference ground could help to improve RF performance. The distance between the ground viasand RF traces should be no less than two times the width of RF signal traces (2*W).

For more details about RF layout, please refer to ***document [6]***.

5.2. GNSS Antenna Interface

The following tables show pin definition and frequency specification of GNSS antenna interface.

Table 27: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	47	AI	GNSS antenna	50ohmimpedance

Table 28: GNSS Frequency

Type	Frequency	Unit
GPS/Galileo/QZSS	1575.42±1.023	MHz
GLONASS	1597.5~1605.8	MHz
BeiDou	1561.098±2.046	MHz

A reference design of GNSS antenna is shown as below.

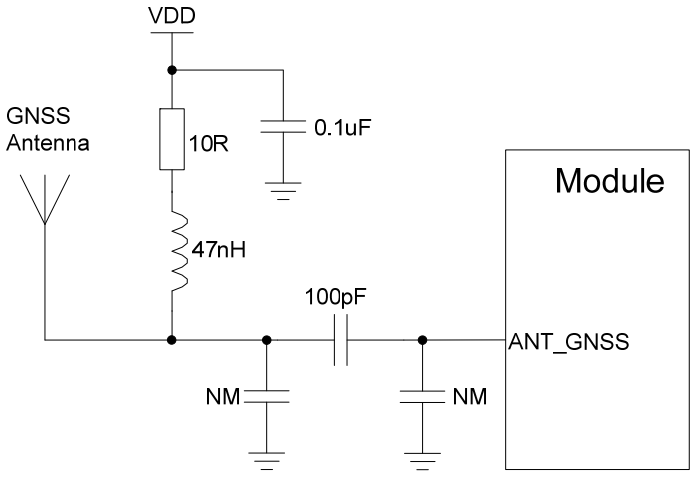


Figure 36: Reference Circuit of GNSS Antenna

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. Antenna Installation

5.3.1. Antenna Requirement

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 29: Antenna Requirements

Type	Requirements
GNSS	Frequency range: 1561~1615MHz Polarization: RHCP or linear VSWR: <2 (Typ.) Passive antenna gain: >0dBi Active antenna noise figure: <1.5dB Active antenna gain: >-2dBi Active antenna embedded LNA gain: 20dB (Typ.) Active antenna total gain: >18dBi (Typ.)
GSM/WCDMA/LTE	VSWR:≤2 Gain (dBi): 1 Max input power (W): 50 Input impedance (ohm): 50 Polarization type: Vertical Cable insertion loss: <1dB (GSM900, WCDMA B5/B6/B8/B19, LTE B5/B8/B12/B13/B18/B20/B26/B28) Cable insertion loss: <1.5dB (GSM1800, WCDMA B1/B2/B4,LTE B1/B2/B3/B4) Cable insertion loss <2dB (LTE B7/B38/B40/B41)

5.3.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use UF.L-R-SMT connector provided by HIROSE.

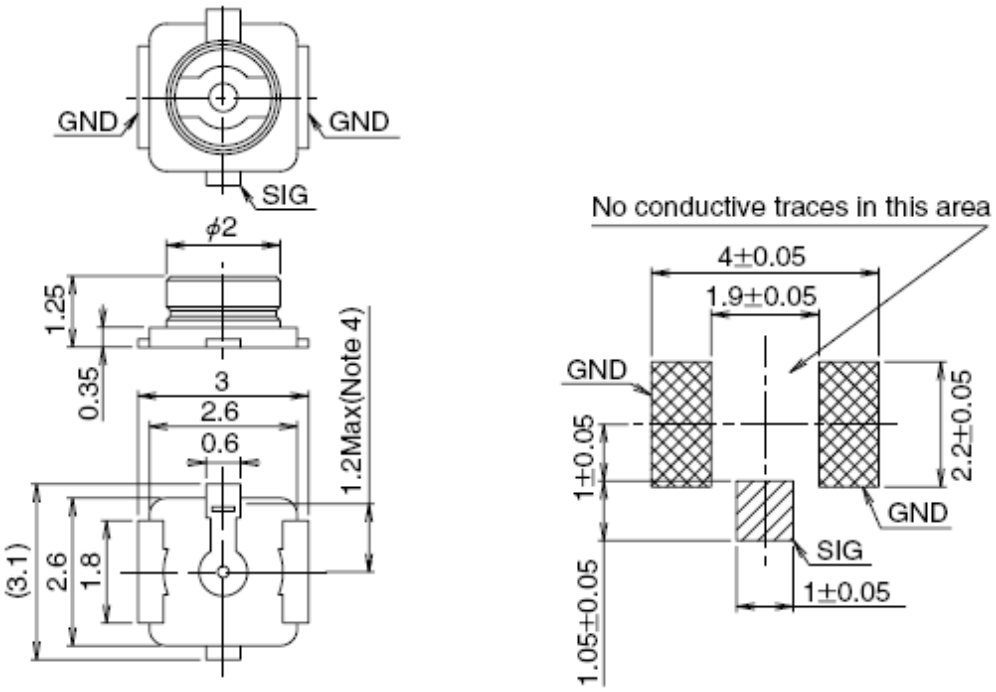


Figure 37: Dimensions of the UF.L-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the UF.L-R-SMT.

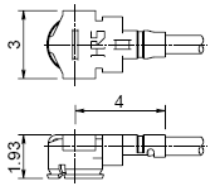
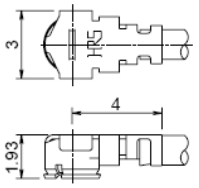
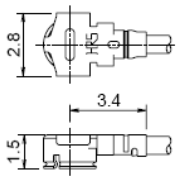
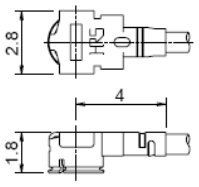
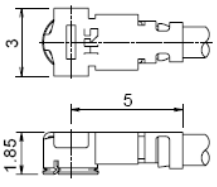
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 38:Mechanicals of UF.L-LP Connectors

The following figure describes the space factor of mated connector.

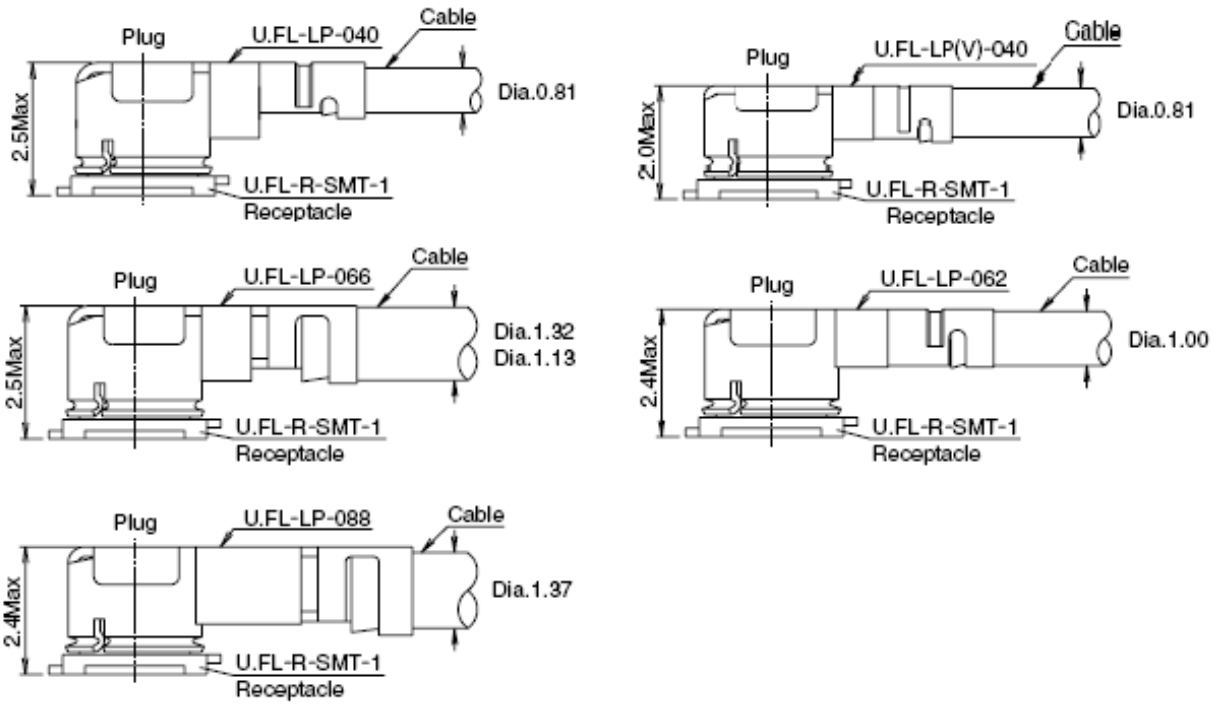


Figure 39:Space Factor of Mated Connector (Unit: mm)

For more details, please visithttp://hirose.com.

6 Electrical, Reliability and RadioCharacteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 30: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	0.8	A
Peak Current of VBAT_RF	0	1.8	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V
Voltage at ADC1	0	VBAT_BB	V

6.2. Power Supply Ratings

Table 31: The Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	Voltage must stay within the min/max values, including voltage drop, ripple and spikes.	3.3	3.8	4.3	V
	Voltage drop during burst transmission	Maximum power control level on GSM900.			400	mV
I_{VBAT}	Peak supply current (during transmissionslot)	Maximum power control level on GSM900.		1.8	2.0	A
USB_VBUS	USB detection		3.0	5.0	5.25	V

6.3. Operating Temperature

The operating temperature is listed in the following table.

Table 32: Operating Temperature

Parameter	Min.	Typ.	Max.	Unit
OperationTemperature Range[1)]	-35	+25	+75	ºC
Extended Operation Range[2)]	-40		+85	ºC

NOTES

1. [1)]Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP compliant again.

6.4. Current Consumption

Table 33: EC25-E Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	20	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.4	mA
		GSM DRX=2 (USB disconnected)	2.74	mA
		GSM DRX=9 (USB disconnected)	2.0	mA
		WCDMA PF=64 (USB disconnected)	2.7	mA
		WCDMA PF=128 (USB disconnected)	2.3	mA
		LTE-FDD PF=64 (USB disconnected)	2.0	mA
		LTE-FDD PF=128 (USB disconnected)	1.9	mA
		LTE-TDD PF=64 (USB disconnected)	4.2	mA
		LTE-TDD PF=128 (USB disconnected)	4.2	mA
	Idle state	GSM DRX=5 (USB disconnected)	22.0	mA
		GSM DRX=5 (USB connected)	31.0	mA
		WCDMA PF=64 (USB disconnected)	31.0	mA
		WCDMA PF=64 (USB connected)	36.0	mA
		LTE-FDDPF=64 (USB disconnected)	22.0	mA
		LTE-FDDPF=64 (USB connected)	32.0	mA
		LTE-TDDPF=64 (USB disconnected)	22.0	mA
		LTE-TDDPF=64 (USB connected)	32.0	mA
	GPRS data transfer (GNSS OFF)	GSM900 4DL/1UL @32.18dBm	236.0	mA
		GSM900 3DL/2UL @32dBm	392.9	mA
		GSM900 2DL/3UL @30.2dBm	466.1	mA
		GSM900 1DL/4UL @29.3dBm	554.2	mA

		DCS1800 4DL/1UL @28.9dBm	181.3	mA
		DCS1800 3DL/2UL @28.9dBm	305.3	mA
		DCS1800 2DL/3UL @28.8dBm	420.1	mA
		DCS1800 1DL/4UL @28.6dBm	531.6	mA
	EDGE data transfer (GNSS OFF)	GSM900 4DL/1UL PCL=8 @26.5dBm	156.4	mA
		GSM900 3DL/2UL PCL=8 @26.5dBm	248.1	mA
		GSM900 2DL/3UL PCL=8 @26.4dBm	340.1	mA
		GSM900 1DL/4UL PCL=8 @26.3dBm	438.8	mA
		DCS1800 4DL/1UL PCL=2 @24.9dBm	158.1	mA
		DCS1800 3DL/2UL PCL=2 @24.8dBm	251.4	mA
		DCS1800 2DL/3UL PCL=2 @24.7dBm	340.4	mA
		DCS1800 1DL/4UL PCL=2 @24.5dBm	432.8	mA
	WCDMA datatransfer(GNSS OFF)	WCDMA B1 HSDPA@22.1dBm	663.7	mA
		WCDMA B1 HSUPA@23.85dBm	662.6	mA
		WCDMA B5 HSDPA@22.5dBm	708.6	mA
		WCDMA B5 HSUPA@22.3dBm	696.6	mA
		WCDMA B8 HSDPA@21.95dBm	595.5	mA
		WCDMA B8 HSUPA@21.92dBm	593.5	mA
	LTE datatransfer(GNSS OFF)	LTE-FDD B1 @23.25dBm	783.6	mA
		LTE-FDD B3 @23.35dBm	845.8	mA
		LTE-FDD B5 @23.04dBm	795.3	mA
		LTE-FDD B7 @23.37dBm	843	mA
		LTE-FDD B8 @23.45dBm	759.9	mA
		LTE-FDD B20 @23.35dBm	755.8	mA
		LTE-TDD B38 @23.41dBm	449.5	mA
		LTE-TDD B40 @23.17dBm	431.8	mA
		LTE-TDD B41 @23.37dBm	447.2	mA

	GSM voice call	GSM900 PCL=5 @32.2dBm	231.7	mA
		DCS1800PCL=0 @23.35dBm	188.8	mA
	WCDMA voice call	WCDMA B1 @22.89dBm	724.7	mA
		WCDMA B5 @22.92dBm	698.2	mA
		WCDMA B8 @22.82dBm	628.2	mA

Table 34: EC25-A Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	20	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	0.99	mA
		WCDMA PF=64 (USB disconnected)	2.0	mA
		WCDMA PF=128 (USB disconnected)	1.6	mA
		LTE-FDD PF=64 (USB disconnected)	2.4	mA
		LTE-FDD PF=128 (USB disconnected)	1.9	mA
	Idle state	WCDMA PF=64 (USB disconnected)	22.0	mA
		WCDMA PF=64 (USB connected)	32.0	mA
		LTE-FDDPF=64 (USB disconnected)	22.0	mA
		LTE-FDDPF=64 (USB connected)	33.0	mA
	WCDMA datatransfer(GNSS OFF)	WCDMA B2 HSDPA@22.86dBm	600.0	mA
		WCDMA B2 HSUPA@22.51dBm	584.6	mA
		WCDMA B4 HSDPA@22.46dBm	578.7	mA
		WCDMA B4 HSUPA@22.27dBm	576.4	mA
		WCDMA B5 HSDPA@22.38dBm	492.0	mA
		WCDMA B5 HSUPA@21.07dBm	483.2	mA
	LTE datatransfer(GNSS OFF)	LTE-FDD B2 @23.17dBm	781.0	mA
		LTE-FDD B4 @23.05dBm	785.7	mA
		LTE-FDD B12 @23.3dBm	667.3	mA

	WCDMA voice call	WCDMA B2 @23.61dBm	670.2	mA
		WCDMA B4 @23.21dBm	630.3	mA
		WCDMA B5 @23.34dBm	536.7	mA

Table 35: GNSS Current Consumption of EC25 Series Module

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT} (GNSS)	Searching (**AT+CFUN=0**)	Cold start @Passive Antenna	54.0	mA
		Lost state @Passive Antenna	53.9	mA
	Tracking (**AT+CFUN=0**)	Instrument Environment	30.5	mA
		Open Sky @Passive Antenna	33.2	mA
		Open Sky @Active Antenna	40.8	mA

6.5. RF Output Power

The following table shows the RF output power of EC25 module.

Table 36: RF Output Power

Frequency	Max.	Min.
GSM900	33dBm±2dB	5dBm±5dB
DCS1800	30dBm±2dB	0dBm±5dB
GSM900(8-PSK)	27dBm±3dB	5dBm±5dB
DCS1800	26dBm±3dB	0dBm±5dB
WCDMA bands	23dBm+1/-3dB	<-50dBm
LTE-FDD band5	23dBm+1/-3dB	<-44dBm
LTE-FDD band7	22.5dBm+1/-3dB	<-44dBm
LTE-TDD bands	23dBm+1/-3dB	<-44dBm

NOTE

In GPRS 4 slots TX mode, the maximum output power is reduced by 3.0dB. The design conforms to the GSM specification as described in ***Chapter 13.16***of *3GPP TS 51.010-1*.

6.6. RF Receiving Sensitivity

The following tables show conducted RF receiving sensitivity of EC25 series module.

Table 37: EC25-E Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO[1)]	3GPP (SIMO)
GSM900	-109.0dBm	/	/	-102.0dBm
DCS1800	-109.0dBm	/	/	-102.0dbm
WCDMA B1	-110.5dBm	/	/	-106.7dBm
WCDMA B5	-110.5dBm	/	/	-104.7dBm
WCDMA B8	-110.5dBm	/	/	-103.7dBm
LTE-FDD B1(10M)	-98.0dBm	-98.0dBm	-101.5dBm	-96.3dBm
LTE-FDD B3(10M)	-96.5dBm	-98.5dBm	-101.5dBm	-93.3dBm
LTE-FDD B5(10M)	-98.0dBm	-98.5dBm	-101.0dBm	-94.3dBm
LTE-FDD B7(10M)	-97.0dBm	-94.5dBm	-99.5dBm	-94.3dBm
LTE-FDD B8(10M)	-97.0dBm	-97.0dBm	-101.0dBm	-93.3dBm
LTE-FDD B20(10M)	-97.5dBm	-99.0dBm	-102.5dBm	-93.3dBm
LTE-TDD B38 (10M)	-96.7dBm	-97.0dBm	-100.0dBm	-96.3dBm
LTE-TDD B40 (10M)	-96.3dBm	-98.0dBm	-101.0dBm	-96.3dBm
LTE-TDD B41 (10M)	-95.2dBm	-95.7dBm	-99.0dBm	-94.3dBm

Table 38: EC25-A Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO	3GPP (SIMO)

WCDMA B2	-110.0dBm	/	/	-104.7dBm
WCDMA B4	-110.0dBm	/	/	-106.7dBm
WCDMA B5	-110.5dBm	/	/	-104.7dBm
LTE-FDD B2 (10M)	-98.0dBm	-98.0dBm	-101.0dBm	-94.3dBm
LTE-FDD B4 (10M)	-97.5dBm	-99.0dBm	-101.0dBm	-96.3dBm
LTE-FDD B12 (10M)	-96.5dBm	-98.0dBm	-101.0dBm	-93.3dBm

Table 39: EC25-V Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO	3GPP (SIMO)
LTE-FDD B4 (10M)	-97.5dBm	-99.0dBm	-101.0dBm	-96.3dBm
LTE-FDD B13 (10M)	-95.0dBm	-97.0dBm	-100.0dBm	-93.3dBm

Table 40: EC25-J Conducted RF Receiving Sensitivity

Frequency	Primary	Diversity	SIMO	3GPP (SIMO)
WCDMA B1	-110.0dBm	/	/	-106.7dBm
WCDMA B6	-110.5dBm	/	/	-106.7dBm
WCDMA B8	-110.5dBm	/	/	-106.7dBm
WCDMA B19	-110.5dBm	/	/	-106.7dBm
LTE-FDD B1 (10M)	-97.5dBm	-98.7dBm	-100.2dBm	-96.3dBm
LTE-FDD B3 (10M)	-96.5dBm	-97.1dBm	-100.5dBm	-93.3dBm
LTE-FDD B8 (10M)	-98.4dBm	-99.0dBm	-101.2dBm	-93.3dBm
LTE-FDD B18 (10M)	-99.5dBm	-99.0dBm	-101.7dBm	-96.3dBm
LTE-FDD B19 (10M)	-99.2dBm	-99.0dBm	-101.4dBm	-96.3dBm
LTE-FDD B26 (10M)	-99.5dBm	-99.0dBm	-101.5dBm	-93.8dBm
LTE-TDD B41 (10M)	-95.0dBm	-95.7dBm	-99.0dBm	-94.3dBm

NOTE

[1)]SIMO is a smart antenna technology that uses a single antenna at the transmitter side and two antennas at the receiver side, which can improve RX performance.

6.7. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module electrostatics discharge characteristics.

Table 41: Electrostatics Discharge Characteristics

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module.All dimensions are measured in mm.

7.1. Mechanical Dimensions of the Module

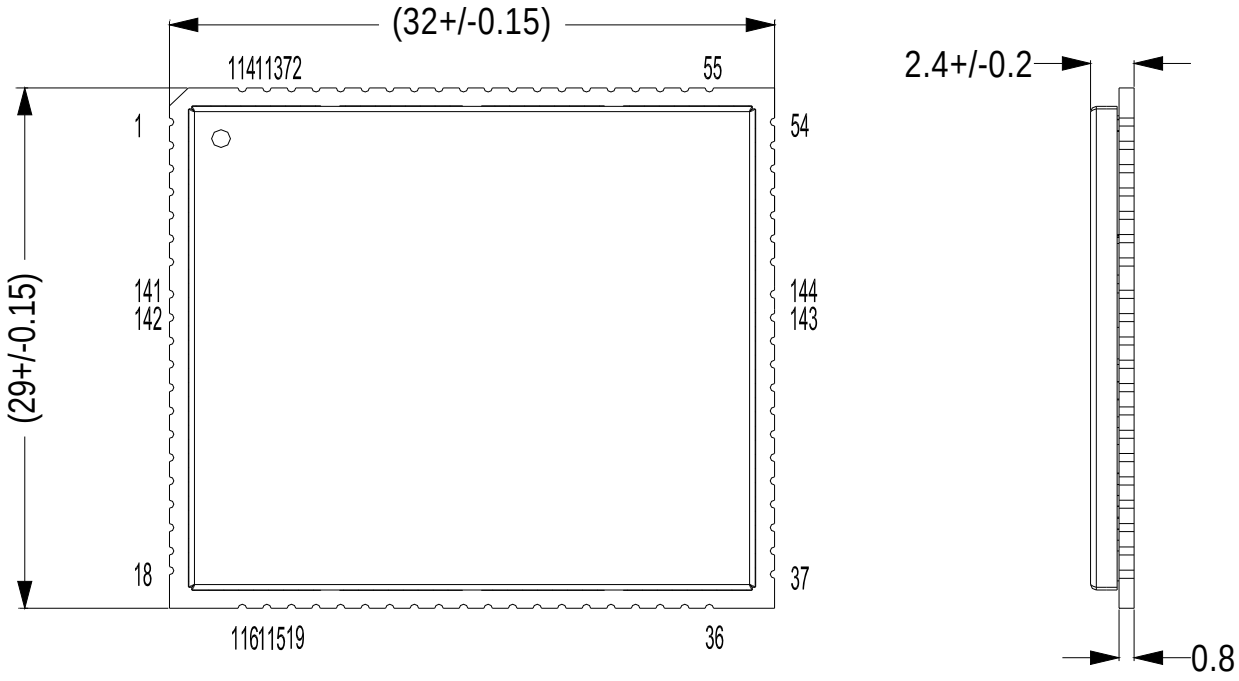


Figure 40: Module Top and Side Dimensions

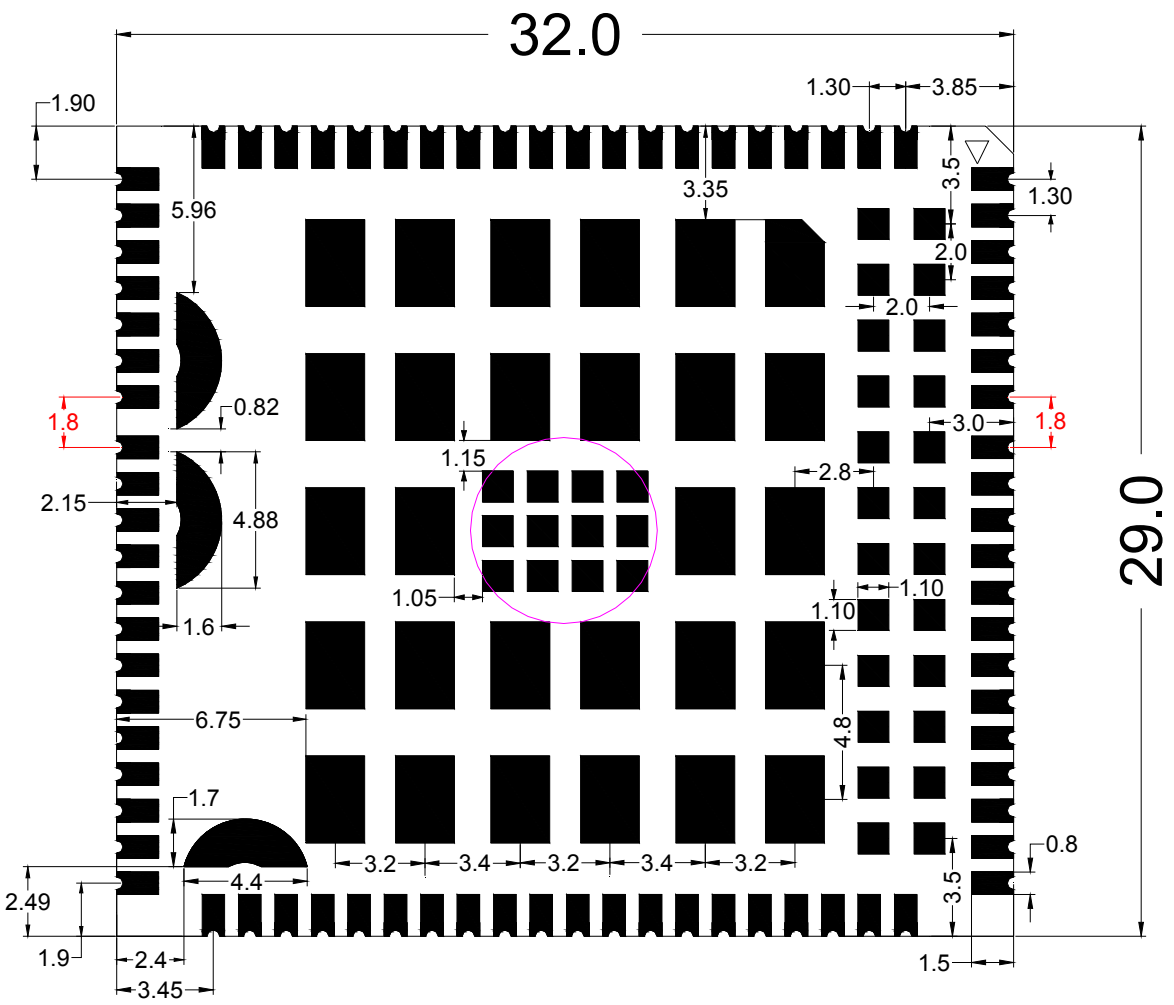


Figure 41: Module Bottom Dimensions (Bottom View)

7.2. Recommended Footprint

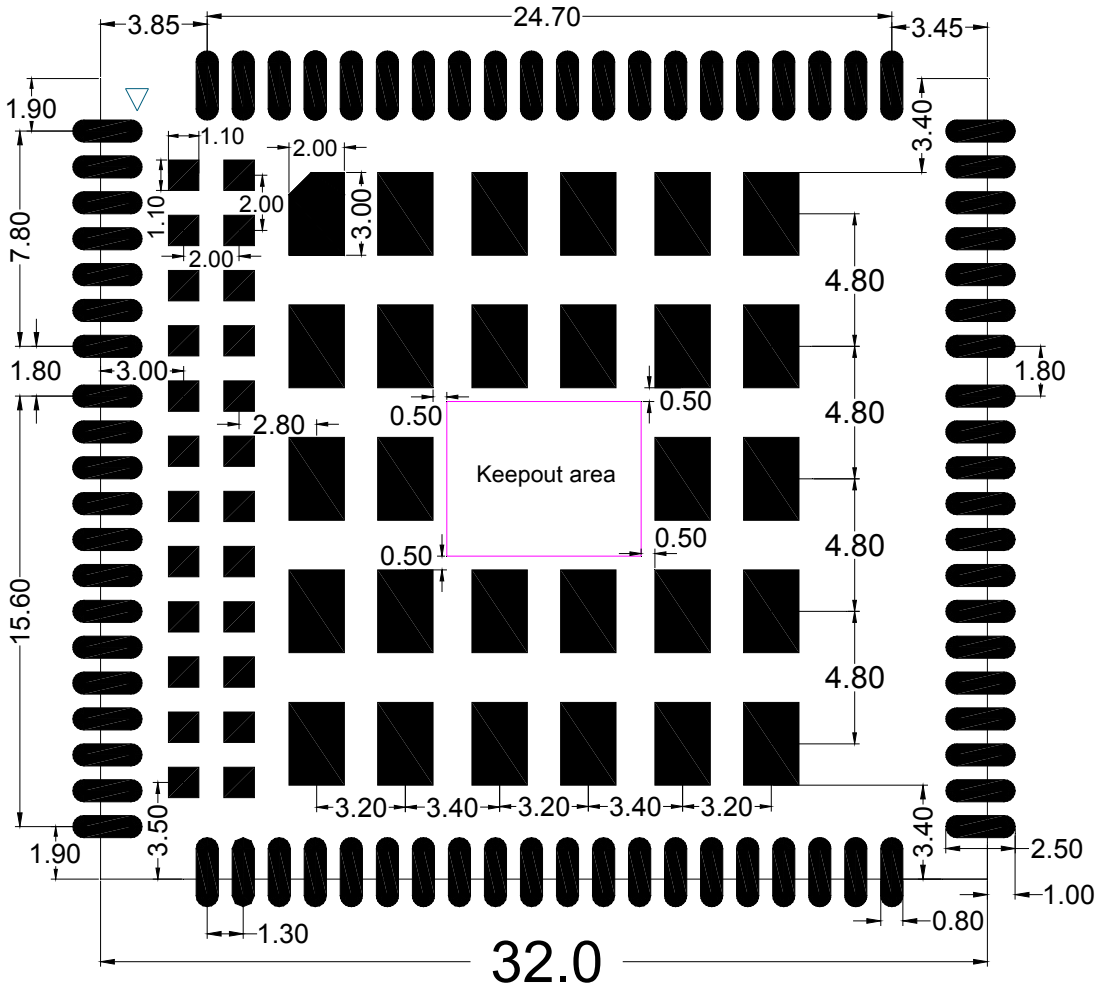


Figure 42: Recommended Footprint (Top View)

NOTES

1. The keepout area should not be designed.
2. For easy maintenance of the module, please keep about 3mm between the module and other components in thehost PCB.

7.3. Design Effect Drawings of the Module

Figure 43: Top View of the Module

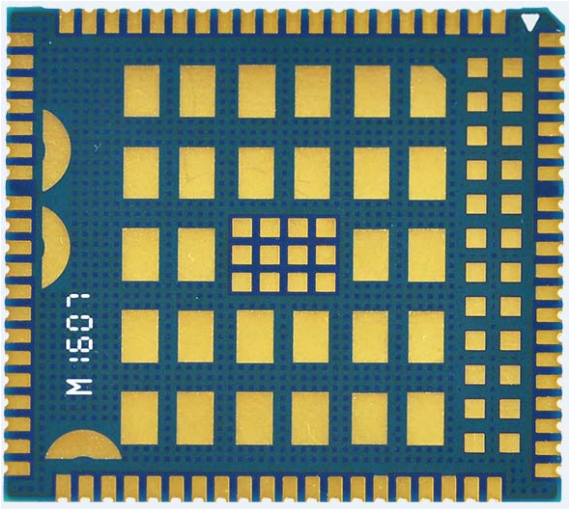


Figure 44: Bottom View of the Module

NOTE

These are design effect drawings of EC25 module. For more accurate pictures, please refer to the module that you get from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage

EC25 is stored in a vacuum-sealed bag. The storage restrictionsare shown as below.

1. Shelf life in vacuum-sealed bag: 12 months at <40ºC/90%RH.

2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:
   - Mounted within 72 hours at the factory environment of ≤30ºC/60%RH.
   - Stored at <10% RH.

3. Devices require bake before mounting, if any circumstances below occurs:
   - When the ambient temperature is 23ºC±5ºC and the humidity indicator card shows the humidity is >10% before opening the vacuum-sealed bag.
   - Device mounting cannot be finished within 72 hours at factory conditions of ≤30ºC/60%RH.

4. If baking is required, devices may be baked for 48 hours at 125ºC±5ºC.

NOTE

As the plastic packagecannot be subjected to high temperature, it should be removed from devices before high temperature (125ºC) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for baking procedure.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properlyso as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, thethickness of stencil for the module is recommended to be 0.18mm. For more details, please refer to***document [4]***.

It is suggested that the peak reflow temperature is 235 ~ 245ºC (for SnAg3.0Cu0.5 alloy). The absolute max reflow temperature is 260ºC. To avoid damage to the module caused by repeated heating, it is suggested that the module should be mounted after reflow soldering for the other side of PCB has been completed. Recommended reflow soldering thermal profile is shown below:

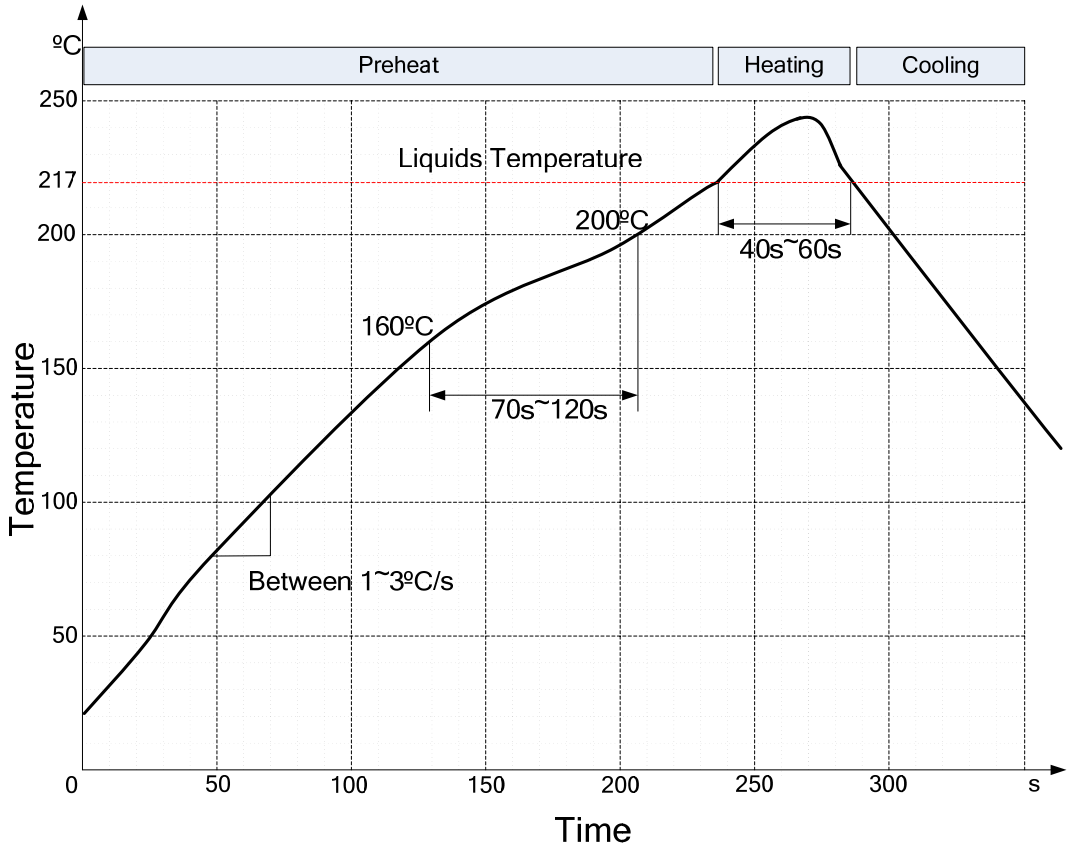


Figure 45: Reflow Soldering Thermal Profile

8.3. Packaging

EC25 is packaged in tap andreel carriers. One reel is 11.53m long and contains 250pcs modules. The figure below shows the package details, measured in mm.

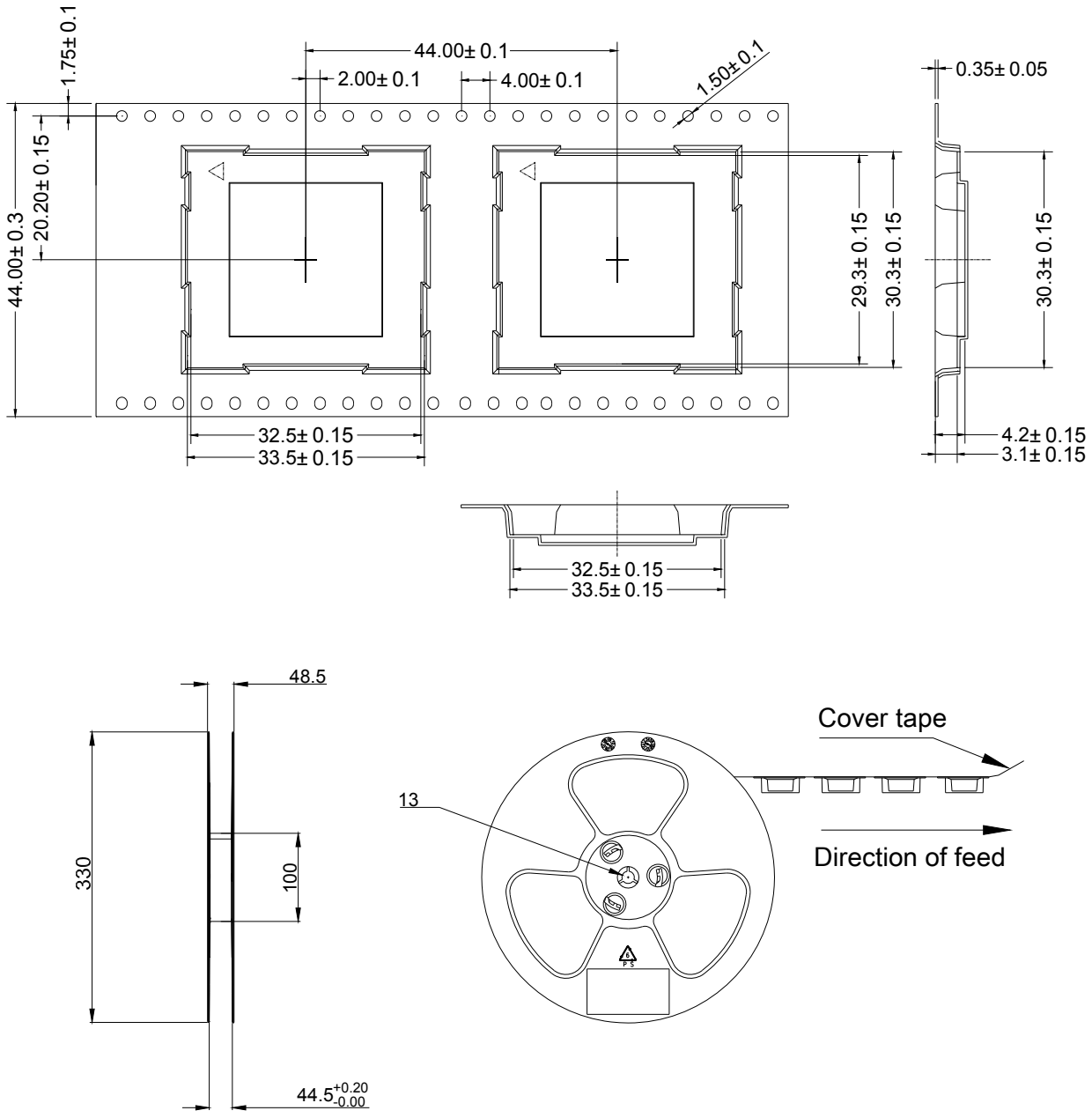


Figure 46: Tape and Reel Specifications

9 Appendix A References

Table 42: Related Documents

SN	Document Name	Remark
[1]	Quectel_EC25_Power_Management_Application_Note	EC25 Power Management Application Note
[2]	Quectel_EC25&EC21_AT_Commands_Manual	EC25 and EC21 AT Commands Manual
[3]	Quectel_EC25&EC21_GNSS_AT_Commands_Manual	EC25 and EC21 GNSS AT Commands Manual
[4]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide
[5]	Quectel_EC25_Reference_Design	EC25 Reference Design
[6]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[7]	Quectel_SGMII_Design_Application_Note	SGMII Desgin Application Note

Table 43: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear To Send
DC-HSPA+	Dual-carrier High Speed Packet Access
DFOTA	Delta Firmware Upgrade Over The Air

DL	Downlink
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
GLONASS	GLObalnaya NAvigatsionnaya Sputnikovaya Sistema, the Russian Global Navigation Satellite System
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
Inorm	Normal Current
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MS	Mobile Station (GSM engine)
MT	Mobile Terminated

PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SGMII	Serial Gigabit Media IndependentInterface
SIM	Subscriber Identification Module
SIMO	Single Input Multiple Output
SMS	Short Message Service
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TX	Transmitting Direction
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USIM	Universal Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value

V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
V_{I}max	Absolute Maximum Input Voltage Value
V_{I}min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

10 Appendix B GPRS Coding Schemes

Table 44: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

11 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 45: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5

12 Appendix D EDGE Modulationand Coding Schemes

Table 46: EDGE Modulation and Coding Schemes

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1:	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2:	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3:	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4:	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.60kbps	35.20kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps