

UG95 Hardware Design

UMTS/HSPA Module Series

Rev. UG95_Hardware_Design_FCC

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Quectel Wireless Solutions Co., Ltd.

Office 501, Building 13, No.99, Tianzhou Road, Shanghai, China, 200233

Tel: +86 21 5108 6236 Mail: <u>info@quectel.com</u>

Or our local office, for more information, please visit:

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About the Document

History

Revision	Date	Author	Description
1.0	2014-06-20	Yeoman CHEN	Initial
1.1	2014-08-21	Yeoman CHEN	 Updated transmitting power information. Added reference design for power supply in Chapter 3.6.3. Updated timing of turning on module in Figure 9. Added definition for the backup capacitor value in Chapter 3.9. Added reference design of 5V level match circuit in Figure 18. Updated RS232 level match circuit in Figure 19. Updated frequency range in Table 23. Updated reference circuit of USB interface in Figure 24. Added diagram for USB upgrade test points. Updated RF output power in Table 28. Updated recommended footprint in Figure 36.



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1 Introduction

This document defines the UG95 module and describes its hardware interface which are connected with your application and the air interface.

This document can help you quickly understand module interface specifications, electrical and mechanical details. Associated with application notes and user guide, you can use UG95 module to design and set up mobile applications easily.



1.1. Safety Information

The following safety precautions must be observed during all phases of the operation, such as usage, service or repair of any cellular terminal or mobile incorporating UG95 module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel and to incorporate these guidelines into all manuals supplied with the product. If not so, Quectel does not take on any liability for customer failure to comply with these precautions.



Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) cause distraction and can lead to an accident. You must comply with laws and regulations restricting the use of wireless devices while driving.



Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it switched off. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. Consult the airline staff about the use of wireless devices on boarding the aircraft, if your device offers a Airplane Mode which must be enabled prior to boarding an aircraft.



Switch off your wireless device when in hospitals or clinics or other health care facilities. These requests are desinged to prevent possible interference with sentitive medical equipment.



UMTS cellular terminals or mobiles operate over radio frequency signal and cellular network and cannot be guaranteed to connect in all conditions, for example no mobile fee or an invalid SIM card. While you are in this condition and need emergent help, please remember using emergency call. In order to make or receive call, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength.



Your cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency energy. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.



In locations with potencially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potencially exposive atmospheres including fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders.



2 Product Concept

2.1. General Description

UG95 serials are embedded 3G wireless communication modules, support UTMS/HSDPA/HSUPA networks. It can also provide voice functionality¹⁾ for your specific application. UG95 offers a maximum data rate of 7.2Mbps on downlink and 5.76Mbps on uplink in HSPA mode.

Table 1: UG95 Series Frequency Bands

Module	GSM	EGSM	DCS	PCS	UMTS	UMTS	UMTS	UMTS
	850	900	1800	1900	850	900	1900	2100
UG95					✓		✓	

NOTE

More details about GPRS/EDGE multi-slot configuration and coding schemes, please refer to *Appendix B*, *C* and *D*.

With a tiny profile of 23.6mm × 19.9mm × 2.2mm, UG95 can meet almost all requirements for M2M application such as automotive, metering, tracking system, security solutions, routers, wireless POS, mobile computing devices, PDA phone and tablet PC, etc..

UG95 is an SMD type module, which can be embedded in application through its 102 LGA pads.

UG95 is integrated with internet service protocols like TCP/UDP and PPP. Extended AT commands have been developed for you to use these internet service protocols easily.

2.2. Directives and Standards

The UG95 module is designed to comply with the FCC statements. FCC ID: XMR201408UG95

¹⁾ UG95 indicates Data-only and Telematics versions. Data-only version does not support voice function, Telematics version supports it.



The Host system using UG95 should have label "contains FCC ID: XMR201408UG95".

2.2.1. FCC Statement

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

2.2.2. FCC Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator and your body as well as kept minimum 20cm from radio antenna depending on the Mobile status of this module usage. This module should NOT be installed and operating simultaneously with other radio.

The manual of the host system, which uses UG95, must include RF exposure warning statement to advice user should keep minimum 20cm from the radio antenna of UG95 module depending on the Mobile status.

Note: If a portable device (such as PDA) uses UG95 module, the device needs to do permissive change and SAR testing.

The following list indicates the performance of antenna gain in certificate testing.

Part Number	Frequency Range (MHz)	Peak Gain (XZ-V)	Average Gain (XZ-V)	VSWR	Impedance
3R007	UMTS850: 824~894MHz UMTS1900: 1850~1990MHz	1 dBi typ.	1 dBi typ.	2 max	50Ω

2.3. Key Features

The following table describes the detailed features of UG95 module.

Table 2: UG95 Key Features

Feature	Details
Power Supply	Supply voltage: 3.4V~4.3V. Typical supply voltage: 3.8V.
Frequency Bands	UG95 UMTS Dual-band: 850/1900MHz.
Transmission Data	HSPA R6: Max 7.2Mbps (DL)/Max 5.76Mbps (UL). UMTS R4: Max 384kbps (DL)/Max 384kbps (UL).



Transmitting Power	Class 3 (22.25Bm+1/-1dB) for UMTS 850/1900.			
HSPA/UMTS Features	HSPA data rate is corresponded with 3GPP release 6 7.2Mbps on downlink and 5.76Mbps on uplink. WCDMA data rate is corresponded with 3GPP R4. 384kbps on downlink and 384kbps on uplink. Support both QPSK and 16-QAM modulations.			
Internet Protocol Features	Support TCP/UDP/PPP protocols. Support the protocols PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) usually used for PPP connections.			
SMS	Text and PDU mode. Point to point MO and MT. SMS cell broadcast. SMS storage: SM by default.			
USIM Interface	Support USIM card: 1.8V, 3.0V. Support USIM and SIM.			
PCM Interface	Used for audio function with external codec. Supports 8, 16, 32 bit mode with short frame synchronization. Support master mode.			
UART Interface	 Support one UART interface. 7-wire on UART interface, without DSR. Support RTS and CTS hardware flow control. Baud rate can reach up to 921600bps, auto baud rate by default. Used for AT command, data transmission or firmware upgrade. Multiplexing function. 			
USB Interface	Compliant with USB 2.0 specification (slave only), the data transfer rate can reach up to 480Mbps. Used for AT command communication, data transmission, software debug and firmware upgrade. USB Driver: Support Windows XP, Windows Vista, Windows 7 Windows 8, Windows CE5.0/6.0*, Linux 2.6/3.0, Android 2.3/4.0/4.2.			
AT Commands	Compliant with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands.			
Real Time Clock	Implemented.			
Network Indication	One pin NETLIGHT to indicate network connectivity status.			
Antenna Interface	UMTS antenna, 50Ω.			
Physical Characteristics	Size: 19.9±0.15 × 23.6±0.15 × 2.2±0.2mm. Interface: LGA. Weight: 2.5g.			
Temperature Range	Normal operation: -35°C ~ +70°C.			



	Restricted operation: -40°C ~ -35°C and +70°C ~ +85°C ¹⁾ .
	Storage temperature: -45°C ~ +90°C.
Firmware Upgrade	USB interface or UART interface.
RoHS	All hardware components are fully compliant with EU RoHS directive.

NOTES

- 1. ¹⁾ means when the module works within this temperature range, RF performance might degrade. For example, the frequency error or the phase error would increase.
- 2. * means this feature is under development.

2.4. Functional Diagram

The following figure shows a block diagram of UG95 and illustrates the major functional parts.

- RF transceiver
- Baseband
- DDR+NAND flash
- Radio frequency
- Peripheral interface
 - -- UART interface
 - --USIM card interface
 - --USB interface
 - --PCM interface
 - --I2C interface
 - --Status indication
 - --Control interface



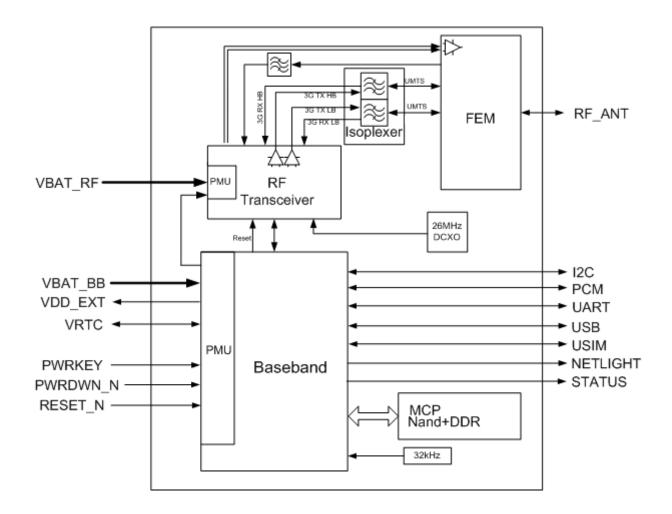


Figure 1: Functional Diagram

2.5. Evaluation Board

In order to help you to develop applications with UG95, Quectel supplies an evaluation board (UC20-EVB), RS-232 to USB cable, USB data cable, power adapter, earphone, antenna and other peripherals to control or test the module. For details, please refer to **document [2]**.



3 Application Interface

3.1. General Description

UG95 is equipped with a 62-pin 1.1mm pitch SMT pads plus 40-pin ground pads and reserved pads that connect to customer's cellular application platform. Sub-interfaces included in these pads are described in detail in the following chapters:

- Power supply
- RTC interface
- UART interface
- USIM interface
- USB interface
- PCM interface
- Status indication



3.2. Pin Assignment

The following figure shows the pin assignment of the UG95 module.

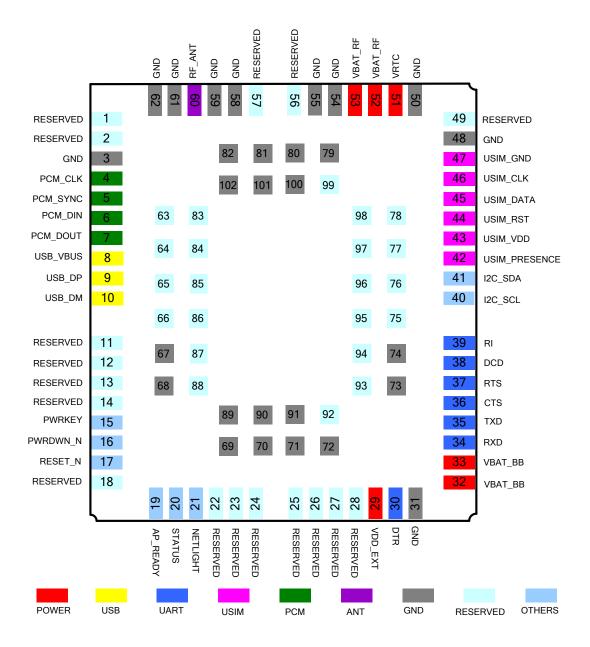


Figure 2: Pin Assignment (Top View)

NOTES

- 1. Keep all RESERVED pins and unused pins unconnected.
- 2. GND pads should be connected to ground in the design.



3.3. Pin Description

The following tables show the UG95's pin definition.

Table 3: IO Parameters Definition

Description
Bidirectional input/output
Digital input
Digital output
Power input
Power output
Analog input
Analog output
Open drain

Table 4: Pin Description

Power Supply						
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment	
VBAT_BB	32,33	PI	Power supply for module baseband part.	Vmax = 4.3V Vmin = 3.4V Vnorm = 3.8V	It must be able to provide sufficient current up to 0.8A.	
VBAT_RF	52,53	PI	Power supply for module RF part.	Vmax = 4.3V Vmin = 3.4V Vnorm = 3.8V	It must be able to provide sufficient current in a transmitting burst which typically rises to 2.0A.	
VRTC	51	PI/ PO	Power supply for internal RTC circuit.	V_{O} max = 1.9V when VBAT \geq 3.4V. V_{I} = 1V~1.9V at I_{IN} max = 2uA when VBAT is not applied.	Keep this pin unconnected if unused.	



VDD_EXT	29	РО	Provide 1.8V for external circuit.	Vnorm = 1.8V I _O max = 20mA	Power supply for external GPIO's pull up circuits.
GND	3,31,48, 50,54,55, 58,59,61, 62,67~74, 79~82, 89~91, 100~102		Ground.		
Turn On/Off					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	15	DI	Turn on the module.	$R_{PU} \approx 200 k\Omega$ $V_{IH} max = 2.1 V$ $V_{IH} min = 1.3 V$ $V_{IL} max = 0.5 V$	Pull-up to 1.8V internally. Active low.
PWRDWN_N	16	DI	Turn off the module.	$R_{PU} \approx 4.7 k\Omega$ $V_{IH} max = 2.1 V$ $V_{IH} min = 1.3 V$ $V_{IL} max = 0.5 V$	Pull-up to 1.8V internally. Active low.
RESET_N	17	DI	Reset the module.	$R_{PU} \approx 200 k\Omega$ $V_{IH} max = 2.1 V$ $V_{IH} min = 1.3 V$ $V_{IL} max = 0.5 V$	Pull-up to 1.8V internally. Active low.
Status Indicat	ion				
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
STATUS	20	DO	Indicate the module operating status.	$V_{OH}min = 1.3V$ $V_{OL}max = 0.5V$	1.8V power domain.
NETLIGHT	21	DO	Indicate the module network status.	$V_{OH}min = 1.3V$ $V_{OL}max = 0.5V$	1.8V power domain.
USB Interface					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	8	PI	USB insert detection.	Vmax = 5.25V Vmin = 2.5V Vnorm = 5.0V	USB insert detection.
USB_DP	9	Ю	USB differential data bus.	Compliant with USB 2.0 standard	Require differential impedance of 90Ω .



USB_DM	10	Ю	USB differential data bus.	Compliant with USB 2.0 standard specification.	Require differential impedance of 90Ω .
USIM Interface	•				
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USIM_GND	47		Specified ground for USIM card.		
USIM_VDD	43	РО	Power supply for USIM card.	For 1.8V USIM: Vmax = 1.85V Vmin = 1.75V For 3.0V USIM: Vmax = 2.9V Vmin = 2.8V	Either 1.8V or 3.0V is supported by the module automatically.
USIM_DATA	45	Ю	Data signal of USIM card.	For 1.8V USIM: $V_{IL}max = 0.35V$ $V_{IH}min = 1.25V$ $V_{OL}max = 0.25V$ $V_{OH}min = 1.25V$ For 3.0V USIM: $V_{IL}max = 0.5V$ $V_{IH}min = 2.05V$ $V_{OH}min = 2.05V$	Pull-up to USIM_VDD with 4.7k resistor internally.
USIM_CLK	46	DO	Clock signal of USIM card.	For 1.8V USIM: $V_{OL}max = 0.25V$ $V_{OH}min = 1.25V$ For 3.0V USIM: $V_{OL}max = 0.25V$ $V_{OH}min = 2.05V$	
USIM_RST	44	DO	Reset signal of USIM card.	For 1.8V USIM: V_{OL} max = 0.25V V_{OH} min = 1.25V For 3.0V USIM: V_{OL} max = 0.3V V_{OH} min = 2.05V	
USIM_PRES ENCE	42	DI	USIM card input detection.	V_{IL} max = 0.35V V_{IH} min = 1.3V V_{IH} max = 1.85V	1.8V power domain. External pull-up resistor is required.



Main UART Interface						
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment	
RI	39	DO	Ring indicator.	V_{OL} max = 0.25 V V_{OH} min = 1.55 V	1.8V power domain.	
DCD	38	DO	Data carrier detection.	V_{OL} max = 0.25 V V_{OH} min = 1.55 V	1.8V power domain.	
CTS	36	DO	Clear to send.	V_{OL} max = 0.25V V_{OH} min = 1.55V	1.8V power domain.	
RTS	37	DI	Request to send.	V_{IL} max = 0.35V V_{IH} min = 1.3V V_{IH} max = 1.85V	1.8V power domain.	
DTR	30	DI	Data terminal ready.	V_{IL} max = 0.35V V_{IH} min = 1.3V V_{IH} max = 1.85V	1.8V power domain.	
TXD	35	DO	Transmit data.	V_{OL} max = 0.25V V_{OH} min = 1.55V	1.8V power domain.	
RXD	34	DI	Receive data.	V_{IL} max = 0.35V V_{IH} min = 1.3V V_{IH} max = 1.85V	1.8V power domain.	
RF Interface						
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment	
RF_ANT	60	Ю	RF antenna.	50Ω impedance		
PCM Interface	•					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment	
PCM_IN	6	DI	PCM data input.	V_{IL} min = -0.3V V_{IL} max = 0.35V V_{IH} min = 1.3V V_{IH} max = 1.85V	1.8V power domain.	
PCM_OUT	7	DO	PCM data output.	V_{OL} max = 0.25 V V_{OH} min = 1.55 V	1.8V power domain.	
PCM_SYNC	5	Ю	PCM data frame sync signal.	V_{OL} max = 0.25V V_{OH} min = 1.55V V_{IL} min = -0.3V V_{IL} max = 0.35V V_{IH} min = 1.3V V_{IH} max = 1.85V	1.8V power domain. In master mode, it is an output signal.	



PCM_CLK	4	Ю	PCM data bit clock.	V_{OL} max = 0.25V V_{OH} min = 1.55V V_{IL} min = -0.3V V_{IL} max = 0.35V V_{IH} min = 1.3V V_{IH} max = 1.85V	1.8V power domain. In master mode, it's an output signal.
I2C Interface	•				
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
I2C_SCL	40	DO	I2C serial clock.	V_{OL} max = 0.25V V_{OH} min = 1.55V	1.8V power domain. External pull-up resistor is required.
I2C_SDA	41	Ю	I2C serial data.	V_{OL} max = 0.25V V_{OH} min = 1.55V V_{IL} min = -0.3V V_{IL} max = 0.35V V_{IH} min = 1.3V V_{IH} max = 1.85V	1.8V power domain. External pull-up resistor is required.
Other Pins					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
AP_READY	19	DI	Application processor sleep state detection.	V_{IL} min = -0.3V V_{IL} max = 0.35V V_{IH} min = 1.3V V_{IH} max = 1.85V	1.8V power domain.
RESERVED	Pins				
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RESERV ED	1,2, 11~14,18 22~28, 49,56,57, 63~66, 75~78, 83~88, 92~99.		Reserved		Keep these pins unconnected.

NOTE

AP_READY is under development.



3.4. Operating Modes

The table below briefly summarizes the various operating modes referred in the following chapters.

Table 5: Overview of Operating Modes

Mode	Details			
Normal Operation	UMTS Idle	Software is active. The module has registered to the UMTS network and the module is ready to send and receive data.		
	UMTS Talk/Data	UMTS connection is ongoing. In this mode, the power consumption is decided by network setting (e.g. TPC pattern) and data transfer rate.		
	HSPA Idle	Software is active. The module has registered to the HSPA network and the module is ready to send and receive data.		
	HSPA Data	HSPA data transfer is ongoing. In this mode, the power consumption is decided by network setting (e.g. TPC pattern) and data transfer rate.		
Minimum Functionality Mode		nand can set the module entering into a minimum functionality mode g the power supply. In this case, both RF function and USIM card will		
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level. During this mode, the module can still receive paging message, SMS and voice call from the network normally.			
Power Down Mode	In this mode, the power management unit shuts down the power supply for the baseband part and RF part. Only the power supply for RTC remains. Software is not active. The serial interface is not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.			

3.5. Power Saving

3.5.1. Sleep Mode

UG95 is able to reduce its current consumption to a minimum value during the sleep mode. The following section describes power saving procedure of UG95.

3.5.1.1. UART Application

If application processor communicates with module via UART interface, the following preconditions can



let the module enter into the sleep mode.

- Execute AT command AT+QSCLK=1 to enable the sleep mode.
- Drive DTR to high level.

The following figure shows the connection between the module and application processor.

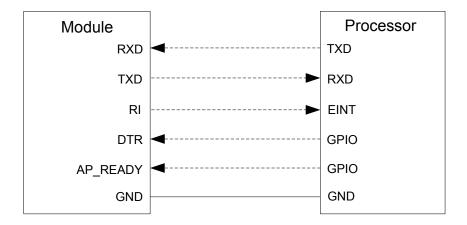


Figure 3: UART Sleep Application

The RI of module is used to wake up the processor, and AP_READY will detect the sleep state of processor (can be configured to high level or low level detection). You should pay attention to the level match shown in dotted line between module and processor. Drive DTR to low level will wake up the module.

In sleep mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally, but the UART port is not accessible

3.5.1.2. USB Application with Suspend Function

TBD

3.5.1.3. USB Application without Suspend Function

If application processor communicates with module via USB interface, and processor does not support USB suspend function, you should disconnect USB_VBUS with additional control circuit to let the module enter into sleep mode.

- Execute AT command AT+QSCLK=1 to enable the sleep mode.
- Disconnect USB_VBUS.



Supply power to USB_VBUS will wake up the module.

The following figure shows the connection between the module and application processor.

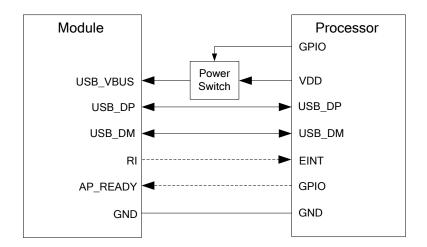


Figure 4: USB Sleep Application without Suspend Function

In sleep mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.

NOTE

AP_READY is under development.

3.5.2. Minimum Functionality Mode

Minimum functionality mode reduces the functionality of the module to minimum level, thus minimizes the current consumption at the same time. This mode can be set as below:

Command AT+CFUN provides the choice of the functionality levels: <fun>=0, 1, 4.

- AT+CFUN=0: Minimum functionality, RF part and USIM card will be closed.
- AT+CFUN=1: Full functionality (by default).
- AT+CFUN=4: Disable RF function (airplane mode). All AT commands related to RF function are not accessible.

For detailed information about command AT+CFUN, please refer to document [1].



3.6. Power Supply

3.6.1. Power Supply Pins

UG95 provides four VBAT pins dedicated to connect with the external power supply. There are two separate voltage domains for VBAT.

- VBAT RF with two pads for module RF.
- VBAT_BB with two pads for module baseband.

The following table shows the VBAT pins and ground pins.

Table 6: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Тур.	Max.	Unit
VBAT_RF	52,53	Power supply for module RF part.	3.4	3.8	4.3	V
VBAT_BB	32,33	Power supply for module baseband part.	3.4	3.8	4.3	V
GND	3,31,48,50 54,55,58, 59,61,62, 67~74, 79~82, 89~91,	Ground	-	-	-	-
	100~102					

3.6.2. Decrease Voltage Drop

The power supply range of the module is $3.4V \sim 4.3V$. Because of the voltage drop during the transmitting time, a bypass capacitor of about $100\mu\text{F}$ with low ESR should be used. Multi-layer ceramic chip (MLCC) capacitor can provide the best combination of low ESR. Three ceramic capacitors (100nF, 33pF, 10pF) are recommended to be applied to the VBAT pins. The capacitors should be placed close to the UG95's VBAT pins. The following figure shows star structure of the power supply.

The main power supply from an external application has to be a single voltage source and has to be expanded to two sub paths with star structure. In addition, in order to get a stable power source, it is suggested to use a zener diode of whose reverse zener voltage is 5.1V and dissipation power is more than 0.5W.

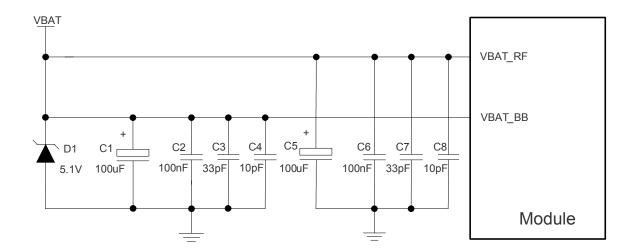


Figure 5: Star Structure of the Power Supply

Please pay special attention to the power supply design for applications. Make sure the input voltage will never drop below 3.4V. If the voltage drops below 3.4V, the module will turn off automatically. The PCB traces from the VBAT pins to the power source must be wide enough to ensure that there isn't too much voltage drop occurs in the transmitting procedure. The width of VBAT_BB trace should be no less than 1mm, and the width of VBAT_RF trace should be no less than 2mm, and the principle of the VBAT trace is the longer, the wider.

3.6.3. Reference Design for Power Supply

The power design for the module is very important, since the performance of power supply for the module largely depends on the power source. The power supply is capable of providing the sufficient current up to 2A at least. If the voltage drop between the input and output is not too high, it is suggested to use a LDO to supply power for module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as a power supply.

The following figure shows a reference design for +5V input power source. The designed output for the power supply is 3.88V and the maximum load current is 3A.



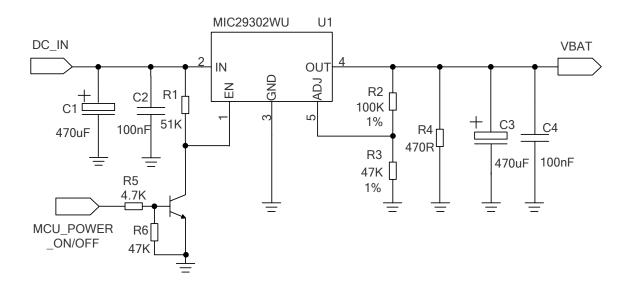


Figure 6: Reference Circuit of Power Supply

NOTE

It is suggested to disconnect power supply to turn off the module when the module is in abnormal state.

3.6.4. Monitor the Power Supply

You can use the **AT+CBC** command to monitor the VBAT_BB voltage value. For more details, please refer to **document [1]**.

3.7. Turn on and off Scenarios

3.7.1. Turn on Module

Turn on the module using the PWRKEY. The following table shows the pin definition of PWRKEY.

Table 7: PWRKEY Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRKEY	15	Turn on the module.	V_{IH} max = 2.1V V_{IH} min = 1.3V V_{IL} max = 0.5V	Pull-up to 1.8V internally with $200k\Omega$ resistor.



When UG95 is in power down mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level at least 100ms. It is recommended to use an open drain/collector driver to control the PWRKEY. You can monitor the level of the STATUS pin to judge whether the module is turned on or not. The STATUS pin output a high level, after UG95 is turned on. A simple reference circuit is illustrated in the following figure.

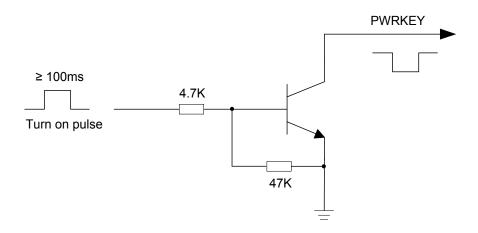


Figure 7: Turn on the Module Using Driving Circuit

The other way to control the PWRKEY is using a button directly. A TVS component is indispensable to be placed nearby the button for ESD protection. When pressing the key, electrostatic strike may generate from finger. A reference circuit is showed in the following figure.

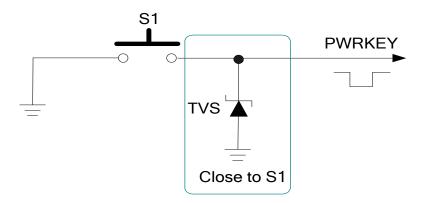


Figure 8: Turn on the Module Using Keystroke

The turn on scenarios is illustrated as the following figure.



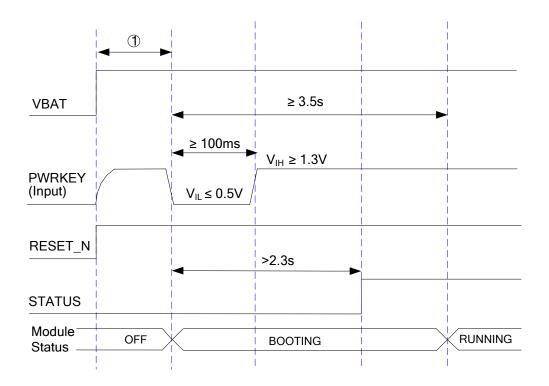


Figure 9: Timing of Turning on Module

NOTE

① Make sure that VBAT is stable before pulling down PWRKEY pin. It is suggested to pull down PWRKEY pin after VBAT is stable 30ms at a voltage of 3.8V. It is not suggested to pull down PWRKEY pin always.

3.7.2. Turn off Module

The following procedures can be used to turn off the module:

- Normal power down procedure: Turn off the module using the PWRDWN N pin.
- Normal power down procedure: Turn off the module using command AT+QPOWD.
- Automatic shutdown: Turn off the module automatically if under-voltage or over-voltage is detected.

3.7.2.1. Turn off Module Using the PWRDWN_N Pin

The following table shows the pin definition of PWRDWN N.



Table 8: PWRDWN_N Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRDWN_N	16	Turn off the module.	V_{IH} max = 2.1V V_{IH} min = 1.3V V_{IL} max = 0.5V	Pull-up to 1.8V internally with $4.7k\Omega$ resistor.

Driving the PWRDWN_N to a low level voltage at least 100ms, the module will execute power-down procedure after PWRDWN_N is released. It is recommended to use an open drain/collector driver to control the PWRDWN_N. You can monitor the level of the STATUS pin to judge whether the module is turned off or not. The level of STATUS pin is low, after UG95 is turned off. A simple reference circuit is illustrated in the following figure.

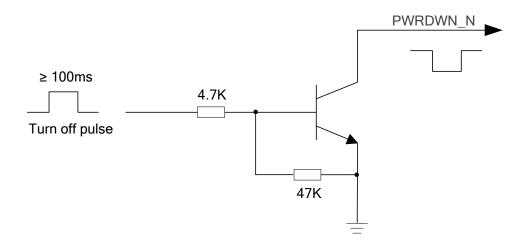


Figure 10: Turn off the Module Using Driving Circuit

The other way to control the PWRDWN_N is using a button directly. A TVS component is indispensable to be placed nearby the button for ESD protection. When pressing the key, electrostatic strike may generate from finger. A reference circuit is showed in the following figure.

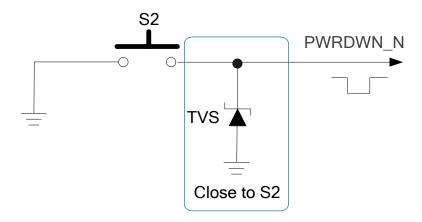


Figure 11: Turn off the Module Using Keystroke



The power-down scenario is illustrated as the following figure.

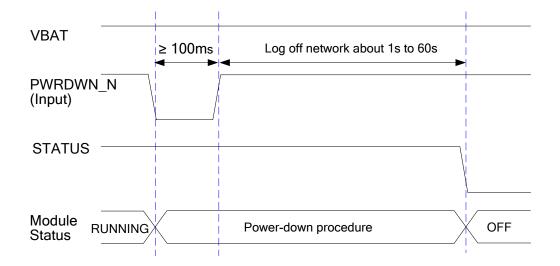


Figure 12: Timing of Turning off Module

During power-down procedure, module will log off network and save important data. After logging off, module sends out "OK", and then sends out "POWERED DOWN" and shut down the internal power supply. The power on VBAT pins is not allowed to turn off before the URC "POWERED DOWN" is output to avoid data loss. If logging off is not done within 60s, module will shut down internal power supply forcibly.

After that moment, the module enters the power down mode, no other AT commands can be executed and only the RTC is still active. The power down mode can also be indicated by the STATUS pin.

3.7.2.2. Turn off Module Using AT Command

It is also a safe way to use AT command **AT+QPOWD** to turn off the module, which is similar to turning off the module via PWRDWN N Pin.

Please refer to *document* [1] for details about the AT command of AT+QPOWD.

3.7.2.3. Automatic Shutdown

The module will constantly monitor the voltage applied on the VBAT, if the voltage \leq 3.5V, the following URC will be presented:

+QIND: "vbatt",-1



If the voltage ≥ 4.21V, the following URC will be presented:

+QIND: "vbatt",1

The uncritical voltage is 3.4V to 4.3V, If the voltage > 4.3V or < 3.4V the module would automatically shut down itself.

If the voltage < 3.4V, the following URC will be presented:

+QIND: "vbatt",-2

If the voltage > 4.3V, the following URC will be presented:

+QIND: "vbatt",2

NOTES

- 1. The value of voltage threshold can be revised by AT command, refer to **document [1]** for details.
- 2. Automatic shutdown is under development.

3.8. Reset the Module

The RESET N can be used to reset the module.

Table 9: RESET_N Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET_N	17	Reset the module.	V_{IH} max = 2.1V V_{IH} min = 1.3V V_{IL} max = 0.5V	Pull-up to 1.8V internally with 200k Ω resistor. Active low.

You can reset the module by driving the RESET_N to a low level voltage for more than 100ms and then releasing.

The recommended circuit is similar to the PWRKEY control circuit. You can use open drain/collector driver or button to control the RESET_N.

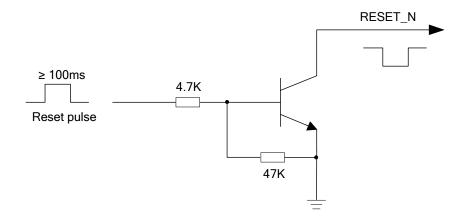


Figure 13: Reference Circuit of RESET_N by Using Driving Circuit

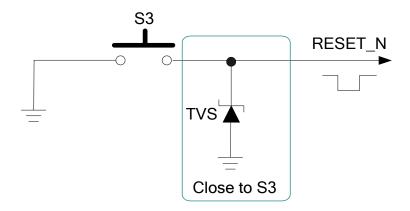


Figure 14: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated as the following figure.

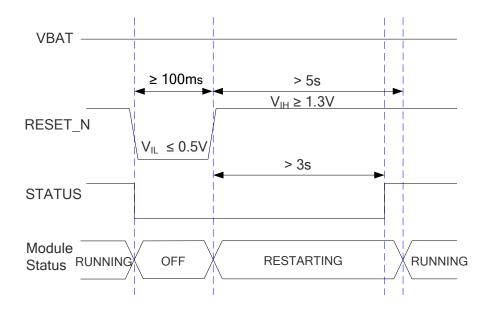


Figure 15: Timing of Resetting Module



NOTE

Use the RESET_N only when turning off the module by the command **AT+QPOWD** and the PWRDWN_N pin failed.

3.9. RTC Interface

The RTC (Real Time Clock) can be powered by an external capacitor through the pin VRTC when the module is powered down and there is no power supply for the VBAT. If the voltage supply at VBAT is disconnected, the RTC can be powered by the capacitor. The capacitance determines the duration of buffering when no voltage is applied to UG95.

The capacitor is charged from the internal LDO of UG95 when there is power supply for the VBAT. A serial $1K\Omega$ resistor had been placed on the application inside the module. It limits the input current of the capacitor.

The following figure shows the reference circuit for VRTC backup.

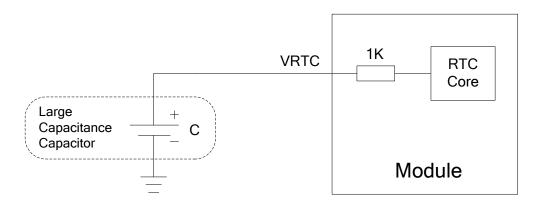


Figure 16: RTC Supply from Capacitor

In order to evaluate the capacitance of capacitor according to the backup time, we have to consider the following parameters:

- VRTC The starting voltage of the capacitor. (Volt)
- VRTC_{MIN} The minimum voltage acceptable for the RTC circuit.(Volt)
- I The current consumption of the RTC circuitry when VBAT = 0.(Ampere)
- B _{Time} Backup Time.(Second)
- C The backup capacitance. (Farad)



When the power is off and only VRTC is running, the way of calculating the backup capacitor as follows:

C= B _{Time} *I/(VRTC-VRTC_{MIN})

For example, when the capacitor is 1000uF:

- VRTC = 1.8V
- VRTC_{MIN} = 1.0V
- I = 2uA
- C = 1000uF

The backup time is about 400s.

3.10. UART Interface

The module provides 7 lines UART interface.

UART interface supports 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800 and 921600bps baud rate, and the default is auto-baud rate. This interface can be used for data transmission, AT communication or firmware upgrade.

The module is designed as the DCE (Data Communication Equipment), following the traditional DCE-DTE (Data Terminal Equipment) connection. The following tables show the pin definition of UART interface.

Table 10: Pin Definition of the Main UART Interface

-			5	
Pin Name	Pin No.	I/O	Description	Comment
DTR	30	DI	Data terminal ready.	1.8V power domain.
RXD	34	DI	Receive data.	1.8V power domain.
TXD	35	DO	Transmit data.	1.8V power domain.
CTS	36	DO	Clear to send.	1.8V power domain.
RTS	37	DI	Request to send.	1.8V power domain.
DCD	38	DO	Data carrier detection.	1.8V power domain.
RI	39	DO	Ring indicator.	1.8V power domain.



The logic levels are described in the following table.

Table 11: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V _{IL}	-0.3	0.35	V
V _{IH}	1.3	1.85	V
V _{OL}	0	0.25	V
V _{OH}	1.55	1.8	V

UG95 provides one 1.8V UART interface. A level shifter should be used if your application is equipped with a 3.3V UART interface. A level shifter TXS0108EPWR provided by **Texas Instruments** is recommended. The following figure shows the reference design of the TXS0108EPWR.

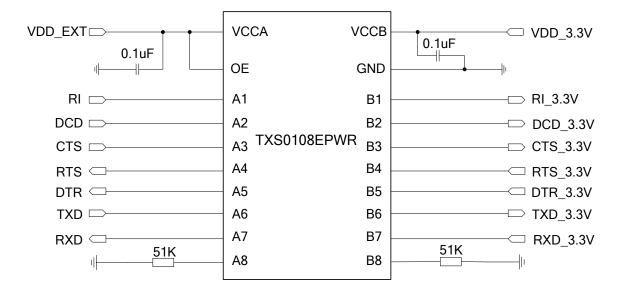


Figure 17: Reference Circuit of Logic Level Translator

The reference design of 5V level match is shown as below. The construction of dotted line can refer to the construction of solid line. Please pay attention to direction of connection. Input dotted line of module should refer to input solid line of the module. Output dotted line of module should refer to output solid line of the module.



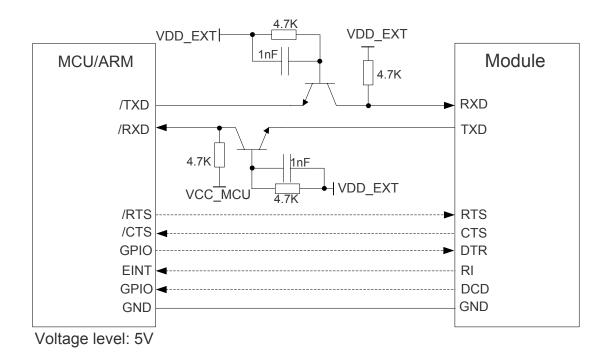


Figure 18: Reference Circuit with Transistor Circuit

The following figure is an example of connection between UG95 and PC. A voltage level translator and a RS-232 level translator chip must be inserted between module and PC, since the UART interface does not support the RS-232 level, while support the 1.8V CMOS level only.

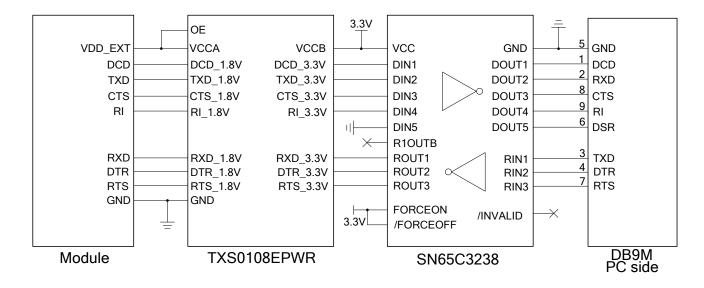


Figure 19: RS232 Level Match Circuit

Please visit http://www.ti.com for more information.



NOTES

- The module disables the hardware flow control by default. When hardware flow control is required, RTS and CTS should be connected to the host. AT command AT+IFC=2,2 is used to enable hardware flow control. AT command AT+IFC=0,0 is used to disable the hardware flow control. For more details, please refer to document [1].
- 2. Rising edge on DTR will let the module exit from the data mode by default. It can be disabled by AT commands. Refer to *document* [1] for details.
- 3. DCD is used as data mode indication. Refer to **document [1]** for details.
- 4. It is suggested to set USB_DP, USB_DM and USB_VBUS pins as test points and then place these test points on the DTE for debug.

3.11. USIM Card Interface

3.11.1. USIM Card Application

The USIM card interface circuitry meets ETSI and IMT-2000 SIM interface requirements. Both 1.8V and 3.0V USIM cards are supported.

Table 12: Pin Definition of the USIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_PRES ENCE	42	DI	USIM card detection input.	1.8V power domain.
USIM_VDD	43	РО	Power supply for USIM card.	Either 1.8V or 3.0V is supported by the module automatically.
USIM_RST	44	DO	Reset signal of USIM card.	
USIM_DATA	45	Ю	Data signal of USIM card.	Pull-up to USIM_VDD with 4.7k resistor internally.
USIM_CLK	46	DO	Clock signal of USIM card.	
USIM_GND	47		Specified ground for USIM card.	



The following figure shows the reference design of the 8-pin USIM card.

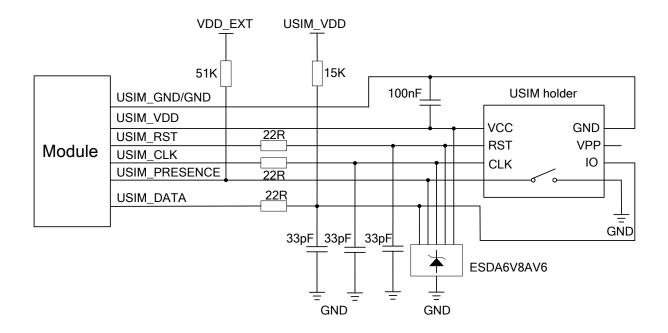


Figure 20: Reference Circuit of the 8-Pin USIM Card

UG95 supports USIM card hot-plugging via the USIM_PRESENCE pin. If you do not need the USIM card detection function, keep USIM_PRESENCE unconnected. The reference circuit for using a 6-pin USIM card socket is illustrated as the following figure.

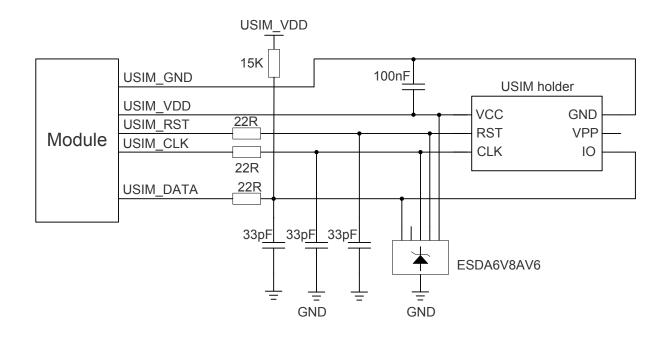


Figure 21: Reference Circuit of the 6-Pin USIM Card



In order to enhance the reliability and availability of the USIM card in customer's application, please follow the following criterion in the USIM circuit design:

- Keep layout of USIM card as close as possible to the module. Assure the possibility of the length of the trace is less than 200mm.
- Keep USIM card signal away from RF and VBAT alignment.
- Assure the ground between module and USIM holder short and wide. Keep the width of ground and USIM_VDD no less than 0.5mm to maintain the same electric potential. The decouple capacitor of USIM VDD should be less than 1uF and must be near to USIM holder.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away with each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add TVS such as WILL (http://www.willsemi.com) ESDA6V8AV6. The 22Ω resistors should be added in series between the module and the USIM card so as to suppress the EMI spurious transmission and enhance the ESD protection.

3.11.2. Design Considerations for USIM Card Holder

For 8-pin USIM card holder, it is recommended to use Molex 91228. Please visit http://www.molex.com for more information.

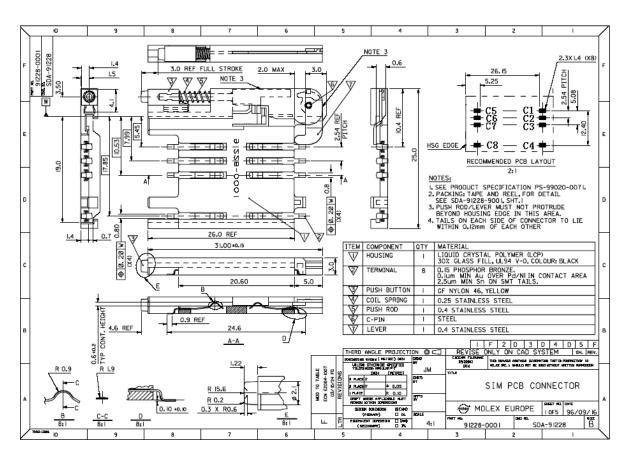


Figure 22: Molex 91228 USIM Card Holder



Table 13: Pin Description of Molex USIM Card Holder

Name	Pin	Function
VDD	C1	USIM card power supply.
RST	C2	USIM card reset.
CLK	C3	USIM card clock.
1	C4	Not defined.
GND	C5	Ground.
VPP	C6	Not connected.
DATA I/O	C7	USIM card data.
1	C8	Pull-down GND with external circuit. When the tray is present, C4 is connected to C8.

For 6-pin USIM card holder, it is recommended to use Amphenol C707 10M006 512 2. Please visit http://www.amphenol.com for more information.

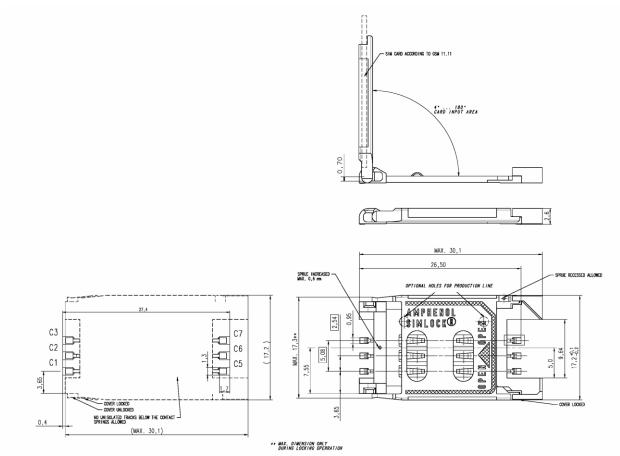


Figure 23: Amphenol C707 10M006 512 2 USIM Card Holder



Table 14: Pin Description of Amphenol USIM Card Holder

Name	Pin	Function
VDD	C1	USIM card power supply.
RST	C2	USIM card reset.
CLK	C3	USIM card clock.
GND	C5	Ground.
VPP	C6	Not connected.
DATA I/O	C7	USIM card data.

3.12. USB Interface

UG95 contains one integrated Universal Serial Bus (USB) transceiver which complies with the USB 2.0 specification and supports high speed (480 Mbps), full speed (12 Mbps) and low speed (1.5 Mbps) mode. The USB interface is primarily used for AT command, data transmission, software debug and firmware upgrade. The following table shows the pin definition of USB interface.

Table 15: USB Pin Description

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	9	Ю	USB differential data bus (positive).	Require differential impedance of 90Ω .
USB_DM	10	Ю	USB differential data bus (minus).	Require differential impedance of 90Ω .
USB_VBUS	8	PI	Used for detecting the USB interface connected.	2.5~5.25V. Typical 5.0V.

More details about the USB 2.0 specifications, please visit http://www.usb.org/home.



The following figure shows the reference circuit of USB interface.

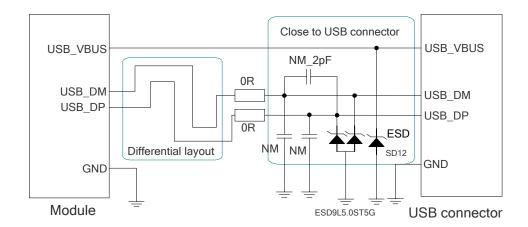


Figure 24: Reference Circuit of USB Application

In order to ensure the USB interface design corresponding with the USB 2.0 specification, please comply with the following principles:

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90ohm.
- Pay attention to the influence of junction capacitance of ESD component on USB data lines. Typically, the capacitance value should be less than 2pF such as ESD9L5.0ST5G.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is
 important to route the USB differential traces in inner-layer with ground shielding not only upper and
 lower layer but also right and left side.
- Keep the ESD components as closer to the USB connector as possible.
- It is suggested to reserve RC circuit near USB connector for debug.

The USB interface is recommended to be reserved for firmware upgrade in your design. The following figure shows the recommended test points.

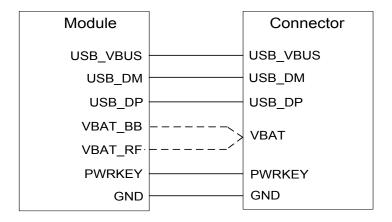


Figure 25: Test Points of Firmware Upgrade



NOTE

- 1. UG95 module can only be used as a slave device.
- 2. It is suggested to set USB_DP, USB_DM and USB_VBUS pins as test points and then place these test points on the DTE for debug.
- 3. USB interface supports software debug and firmware upgrade by default.

3.13. PCM and I2C Interface

UG95 provides one Pulse Code Modulation (PCM) digital interface for audio design, which supports the following features:

- Supports 8, 16, 32 bit mode with short frame synchronization, the PCM support 8 bit mode by default since the PCM codec default configuration is AT+QDAI=1. Refer to document [1] for more details.
- Supports master mode.
- Supports audio sample rate 8 kHz.

The following table shows the pin definition of PCM and I2C interface which can be applied on audio codec design.

Table 16: Pin Definition of PCM and I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_CLK	4	Ю	PCM data bit clock.	1.8V power domain.
PCM_SYNC	5	Ю	PCM data frame sync signal.	1.8V power domain.
PCM_IN	6	DI	PCM data input.	1.8V power domain.
PCM_OUT	7	DO	PCM data output.	1.8V power domain.
I2C_SCL	40	DO	I2C serial clock.	Require external pull-up resistor.
I2C_SDA	41	Ю	I2C serial data.	Require external pull-up resistor.

In PCM audio format the MSB of the channel included in the frame (PCM_SYNC) is clocked on the second CLK falling edge after the PCM_SYNC pulse rising edge. The period of the PCM_SYNC signal (frame) lasts for Data word bit +1 clock pulses.

UG95's firmware has integrated the configuration on ALC5616 application with I2C interface. You can execute command AT+QDAI=3 to configure the ALC5616 codec, and refer to *document* [1] for more



details. Data bit is 32 bit and the sampling rate is 8 KHz. The following figure shows the timing of the application with ALC5616 codec.

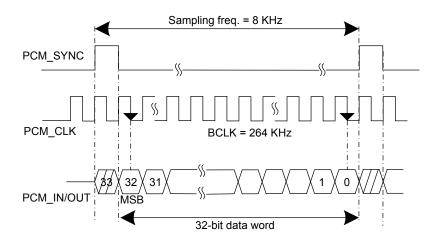


Figure 26: PCM Master Mode Timing

In general, the BitClockFrequency (CLK) is furnished by the following expression:

BitClockFrequency = (DataWordBit +1) × SamplingFrequency

The following figure shows the reference design of PCM interface with external codec IC.

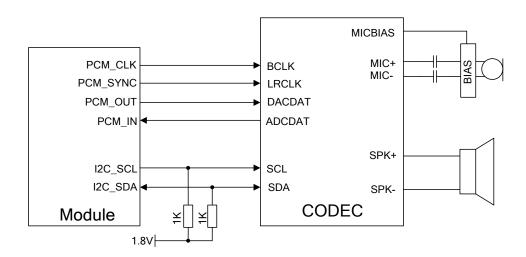


Figure 27: Reference Circuit of PCM Application with Audio Codec

NOTE

It is recommended to reserved RC (R=22Ω, C=22pF) circuit on the PCM lines, especially for PCM_CLK.



3.14. Network Status Indication

The NETLIGHT signal can be used to drive a network status indication LED. The following tables describe pin definition and logic level changes in different network status.

Table 17: Pin Definition of Network Indicator

Pin Name	Pin N	o. I/O	Description	Comment
NETLIGHT	21	DO	Indicate the module network activity status.	1.8V power domain.

Table 18: Working State of the Network Indicator

Pin Name	Status	Description
	Flicker slowly (200ms High/1800ms Low)	Networks searching.
NETLIGHT	Flicker slowly (1800ms High/200ms Low)	ldle.
	Always High	Voice&CSD calling.

A reference circuit is shown in the following figure.

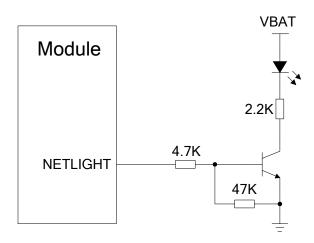


Figure 28: Reference Circuit of the NETLIGHT



3.15. Operating Status Indication

The STATUS pin is set as an output pin and can be used to judge whether module is power-on. In customer's design, this pin can be used to drive an LED in order to judge the module's operation status.

The following table describes pin definition of STATUS.

Table 19: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module operation status.	1.8V power domain.

A reference circuit is shown as below.

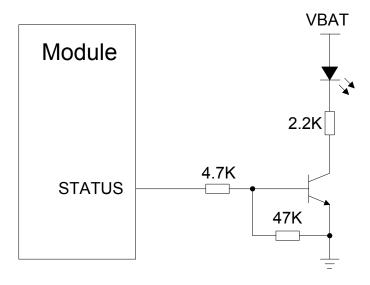


Figure 29: Reference Circuit of the STATUS



4 Antenna Interface

The Pin 60 is the RF antenna pad. The RF interface has an impedance of 50Ω .

4.1. UMTS Antenna Interface

4.1.1. Pin Definition

Table 20: Pin Definition of the RF Antenna

Pin Name	Pin No.	I/O	Description	Comment
GND	58		ground	
GND	59		ground	
RF_ANT	60	Ю	RF antenna pad	50Ω impedance
GND	61		ground	
GND	62		ground	

4.1.2. Operating Frequency

Table 21: The Module Operating Frequencies

Band	Receive	Transmit	Unit
UMTS1900	1930 ~ 1990	1850 ~ 1910	MHz
UMTS850	869 ~ 894	824 ~ 849	MHz

4.1.3. Reference Design

The RF external circuit is recommended as below. It should reserve a π -type matching circuit for better RF performance. The capacitors are not mounted by default.



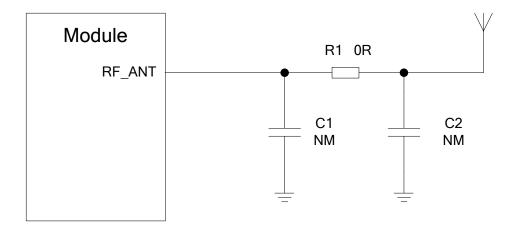


Figure 30: Reference Circuit of Antenna Interface

UG95 provides an RF antenna PAD for customer's antenna connection. The RF trace in host PCB connected to the module RF antenna pad should be micro-strip line or other types of RF trace, whose characteristic impendence should be close to 50Ω . UG95 comes with grounding pads which are next to the antenna pad in order to give a better grounding.

4.2. Antenna Installation

4.2.1. Antenna Requirement

The following table shows the requirement on UMTS antenna.

Table 22: Antenna Cable Requirements

Туре	Requirements
UMTS 850	Cable insertion loss <1dB
UMTS 1900/2100	Cable insertion loss <1.5dB

Table 23: Antenna Requirements

Туре	Requirements
Frequency Range	UG95 UMTS Dual-band: 850/1900MHz.
VSWR	≤ 2



Gain (dBi)	1
Max Input Power (W)	50
Input Impedance (Ω)	50
Polarization Type	Vertical

4.2.2. Install the Antenna with RF Connector

The following is the antenna installation with RF connector provided by HIROSE. The recommended RF connector is UF.L-R-SMT.

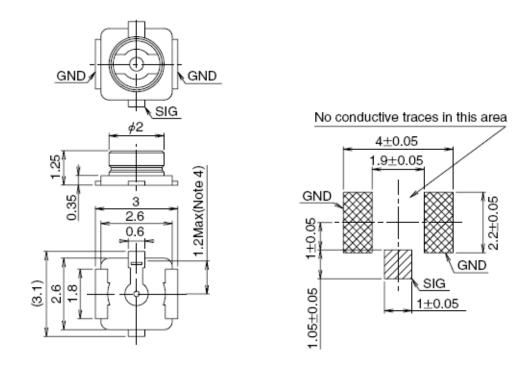


Figure 31: Dimensions of the UF.L-R-SMT Connector (Unit: mm)

You can use U.FL-LP serial connector listed in the following figure to match the UF.L-R-SMT.



	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Part No.	4	25 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	3.4	87	38. 5. 5. 5. 5. 5. 5. 7. 7. 7. 7. 7. 7. 7. 7. 7. 7. 7. 7. 7.
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5 71.7	
RoHS			YES		

Figure 32: Mechanicals of UF.L-LP Connectors (Unit: mm)

The following figure describes the space factor of mated connector

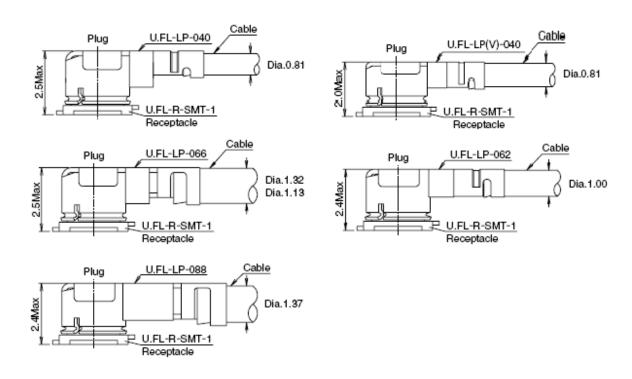


Figure 33: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://www.hirose.com.



5 Electrical, Reliability and Radio Characteristics

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of module are listed in the following table.

Table 24: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	0.8	A
Peak Current of VBAT_RF	0	2	A
Voltage at Digital Pins	-0.3	2.3	V

5.2. Power Supply Ratings

Table 25: The Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Тур.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	Voltage must stay within the min/max values, including voltage drop, ripple, and spikes.	3.4	3.8	4.3	V
USB_VBUS	USB insert detection		2.5	5.0	5.25	V



5.3. Operating Temperature

The operating temperature is listed in the following table.

Table 26: Operating Temperature

Parameter	Min.	Тур.	Max.	Unit
Normal Temperature	-35	25	70	°C
Restricted Operation ¹⁾	-40~ -35		70 ~ 85	°C
Storage Temperature	-45		90	°C

NOTE

5.4. Current Consumption

The values of current consumption are shown below.

Table 27: The Module Current Consumption

Parameter	Description	Conditions	Min.	Тур.	Max.	Unit
OFF state supply current I _{VBAT} WCDMA supply current		Power down		70		uA
		Sleep (USB disconnected) @DRX=6		1.98		mA
		Sleep (USB disconnected) @DRX=7		1.46		mA
		Sleep (USB disconnected) @DRX=8		1.24		mA
	Sleep (USB disconnected) @DRX=9		1.15		mA	
		Idle (USB disconnected) @DRX=6		12		mA

¹⁾ When the module works within the temperature range, the deviations from the RF specification may occur. For example, the frequency error or the phase error would increase.



Parameter	Description	on	Conditions	Min.	Тур.	Max.	Unit
			Idle (USB connected) @DRX=6		31.7		mA
			UMTS2100 HSDPA @max power		524		mA
			UMTS2100 HSUPA @max power		536		mA
			UMTS1900 HSDPA @max power		522		mA
	WCDMA	data	UMTS1900 HSUPA @max power		563		mA
	transfer		UMTS850 HSDPA @max power		490		mA
			UMTS850 HSUPA @max power		520		mA
			UMTS900 HSDPA @max power		510		mA
			UMTS900 HSUPA @max power		512		mA

5.5. RF Output Power

The following table shows the RF output power of UG95 module.

Table 28: Conducted RF Output Power

Frequency	Max.	Min.
UMTS1900	22.25dBm+1/-1dB	<-50dBm
UMTS850	22.25dBm+1/-1dB	<-50dBm

5.6. RF Receiving Sensitivity

The following table shows the conducted RF receiving sensitivity of UG95 module.

Table 29: Conducted RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.)
UMTS1900	-110.5dBm



UMTS850 -110.5dBm

5.7. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.



6 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm.

6.1. Mechanical Dimensions of the Module

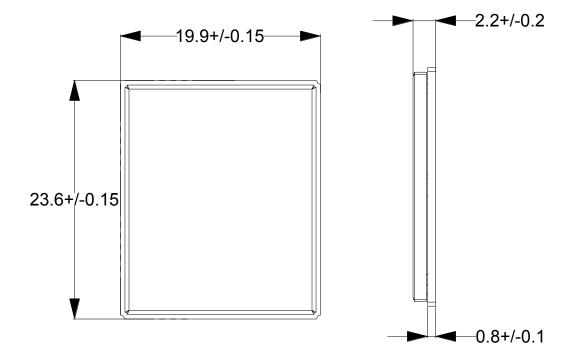


Figure 34: UG95 Top and Side Dimensions

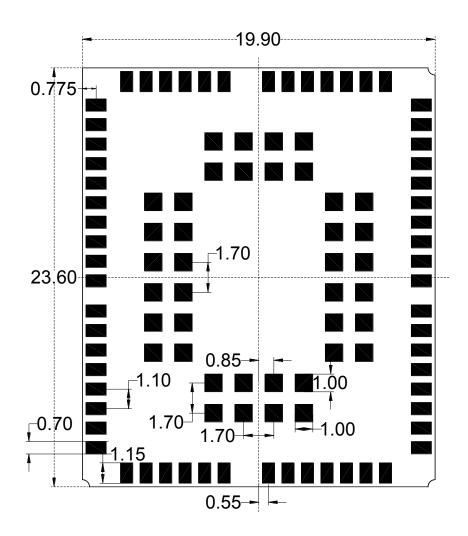


Figure 35: UG95 Bottom Dimension (Top View)



6.2. Footprint of Recommendation

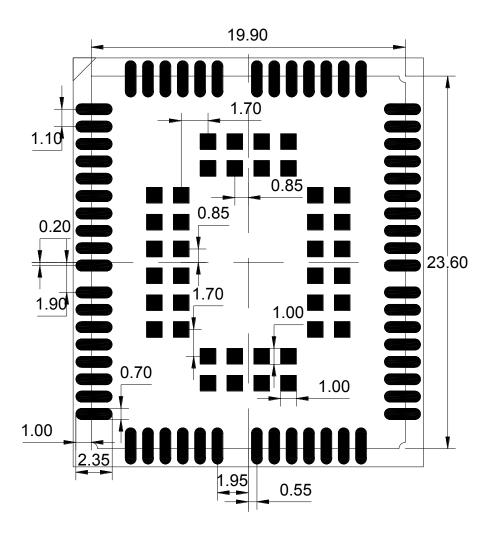


Figure 36: Recommended Footprint (Top View)

NOTES

- 1. In order to maintain the module, keep about 3mm between the module and other components in the host PCB.
- 2. All RESERVED pins must not be connected to GND.



6.3. Top View of the Module



Figure 37: Top View of the Module

6.4. Bottom View of the Module

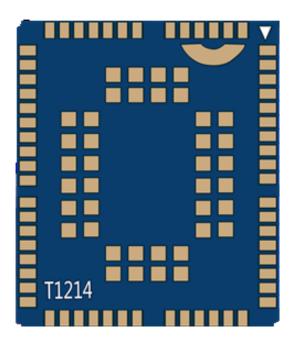


Figure 38: Bottom View of the Module



7 Storage and Manufacturing

7.1. Storage

UG95 is stored in the vacuum-sealed bag. The restriction of storage condition is shown as below.

Shelf life in sealed bag is 12 months at < 40°C/90%RH.

After this bag is opened, devices that will be subjected to reflow solder or other high temperature process must be:

- Mounted within 72 hours at factory conditions of ≤ 30°C/60%RH.
- Stored at <10% RH.

Devices require bake, before mounting, if:

- Humidity indicator card is >10% when read 23°C±5°C.
- Mounted for more than 72 hours at factory conditions of ≤ 30°C/60% RH.

If baking is required, devices may be baked for 48 hours at 125°C±5°C.

NOTE

As plastic container cannot be subjected to high temperature, module needs to be taken out from container to high temperature (125°C) bake. If shorter bake times are desired, please refer to IPC/JEDECJ-STD-033 for bake procedure.

7.2. Manufacturing and Welding

The squeegee should push the paste on the surface of the stencil that makes the paste fill the stencil openings and penetrate to the PCB. The force on the squeegee should be adjusted so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil at the hole of the module pads should be 0.13mm. For details, please refer to **document [6]**.



It is suggested that peak reflow temperature is $235 \sim 245^{\circ}$ C (for SnAg3.0Cu0.5 alloy). Absolute max reflow temperature is 260° C. To avoid damage to the module when it was repeatedly heated, it is suggested that the module should be mounted after the first panel has been reflowed. The following picture is the actual diagram which we have operated.

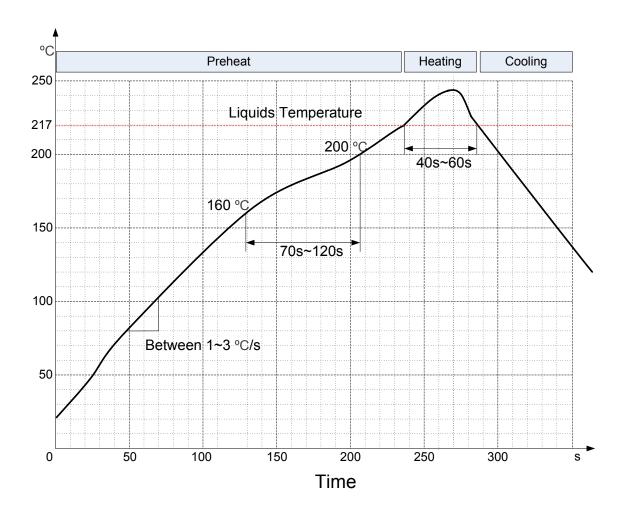


Figure 39: Reflow Soldering Profile

7.3. Packaging

TBD



8 Appendix A Reference

Table 30: Related Documents

SN	Document Name	Remark
[1]	Quectel_UG95_AT_Commands_Manual	UG95 AT Commands Manual
[2]	Quectel_UC20_EVB_User_Guide	UC20 EVB User Guide
[3]	Quectel_UG95_Reference_Design	UG95 Reference Design
[4]	Quectel_UG95&M95_Reference_Design	UG95 and M95 Compatible Reference Design
[5]	Quectel_UG95&M95_Compatible_Design	UG95 and M95 Compatibility Design Specification
[6]	Quectel_Module_Secondary_SMT_User_ Guide	Module Secondary SMT User Guide

Table 31: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
ARP	Antenna Reference Point
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear To Send
DRX	Discontinuous Reception
DCE	Data Communications Equipment (typically module)
DTE	Data Terminal Equipment (typically computer, external controller)



DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Extended GSM900 band (includes standard GSM900 band)
ESD	Electrostatic Discharge
FR	Full Rate
GMSK	Gaussian Minimum Shift Keying
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
I/O	Input/Output
IMEI	International Mobile Equipment Identity
lmax	Maximum Load Current
Inorm	Normal Current
LED	Light Emitting Diode
LNA	Low Noise Amplifier
MO	Mobile Originated
MS	Mobile Station (GSM engine)
MT	Mobile Terminated
PAP	Password Authentication Protocol
PBCCH	Packet Broadcast Control Channel
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol



PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
RMS	Root Mean Square (value)
RTC	Real Time Clock
Rx	Receive
SIM	Subscriber Identification Module
SMS	Short Message Service
TDMA	Time Division Multiple Access
TE	Terminal Equipment
TX	Transmitting Direction
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USIM	Universal Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V _{IH} max	Maximum Input High Level Voltage Value
V _{IH} min	Minimum Input High Level Voltage Value
V _{IL} max	Maximum Input Low Level Voltage Value
V _{IL} min	Minimum Input Low Level Voltage Value



V _I max	Absolute Maximum Input Voltage Value
V _I min	Absolute Minimum Input Voltage Value
V _{OH} max	Maximum Output High Level Voltage Value
V _{OH} min	Minimum Output High Level Voltage Value
V _{OL} max	Maximum Output Low Level Voltage Value
V _{OL} min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access



9 Appendix B GPRS Coding Scheme

Table 32: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	C4-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4



10 Appendix C GPRS Multi-slot Class

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependant, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications. The description of different multi-slot classes is shown in the following table.

Table 33: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5



11 Appendix D EDGE Modulation and Coding Scheme

Table 34: EDGE Modulation and Coding Scheme

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1:	GMSK	1	9.05kbps	18.1kbps	36.2kbps
CS-2:	GMSK	1	13.4kbps	26.8kbps	53.6kbps
CS-3:	GMSK	1	15.6kbps	31.2kbps	62.4kbps
CS-4:	GMSK	1	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	С	8.80kbps	17.60kbps	35.20kbps
MCS-2	GMSK	В	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	С	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	В	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	В	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps