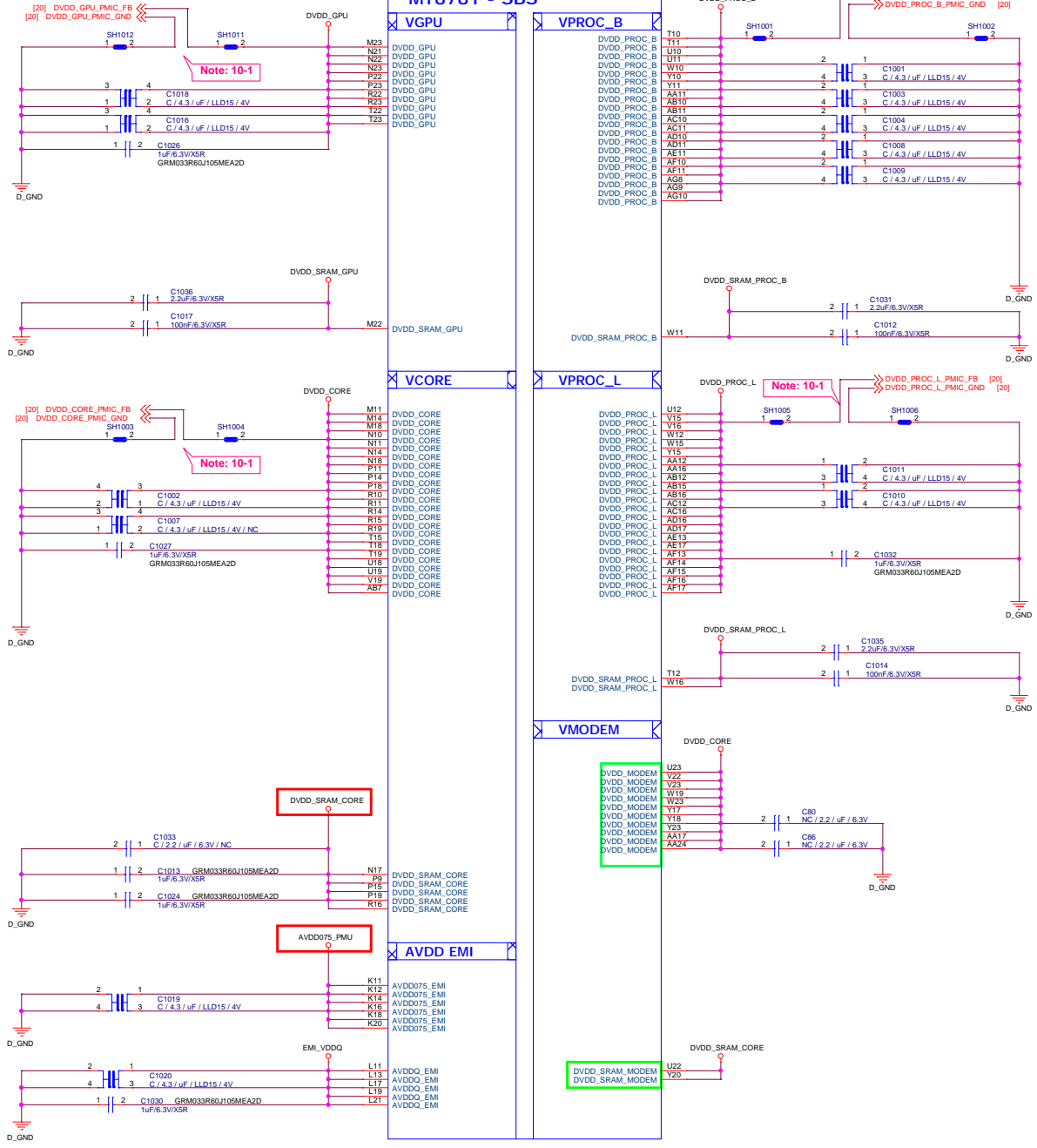


U1001-2  
U / MT8781\_DSC

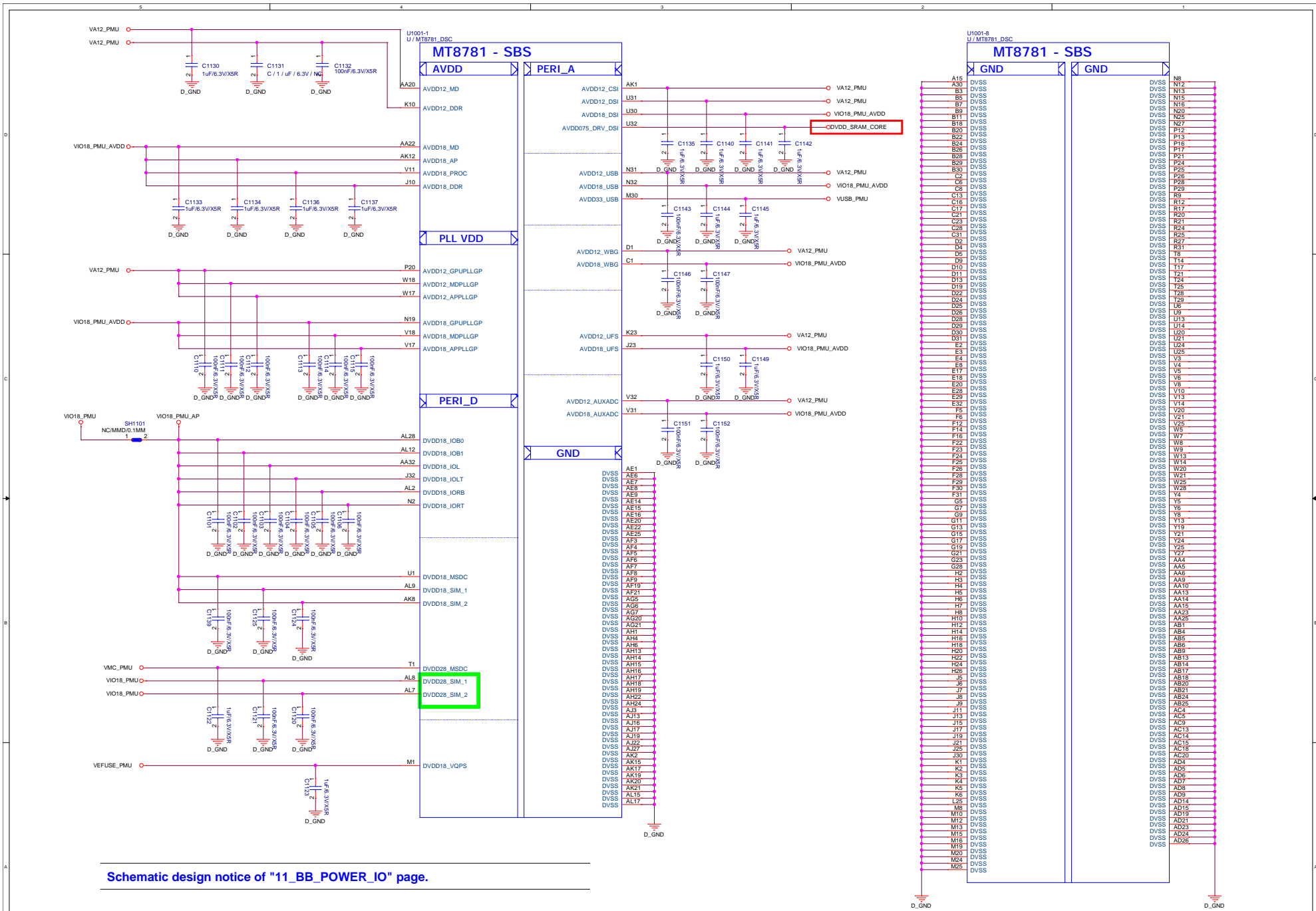
**MT8781 - SBS**



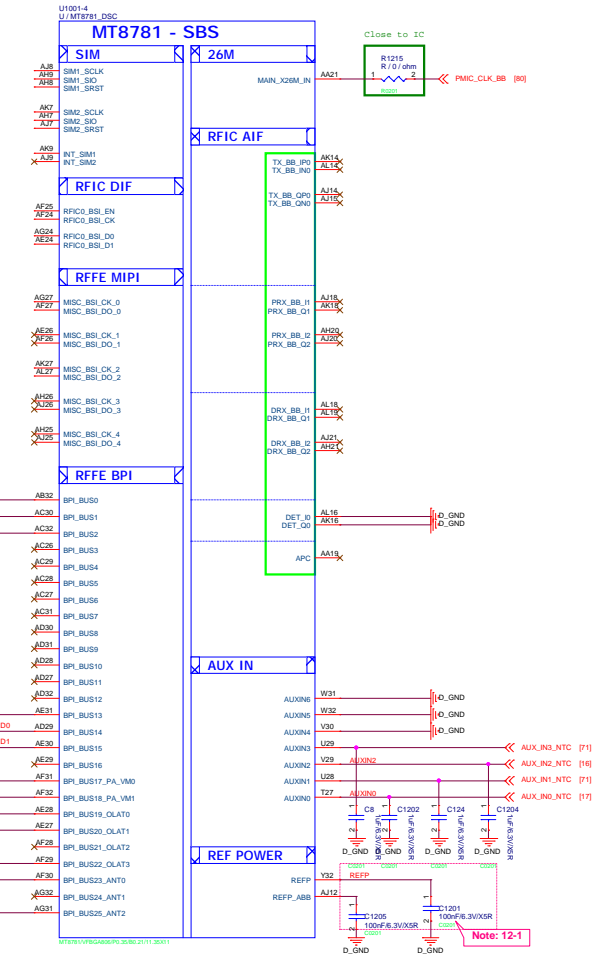
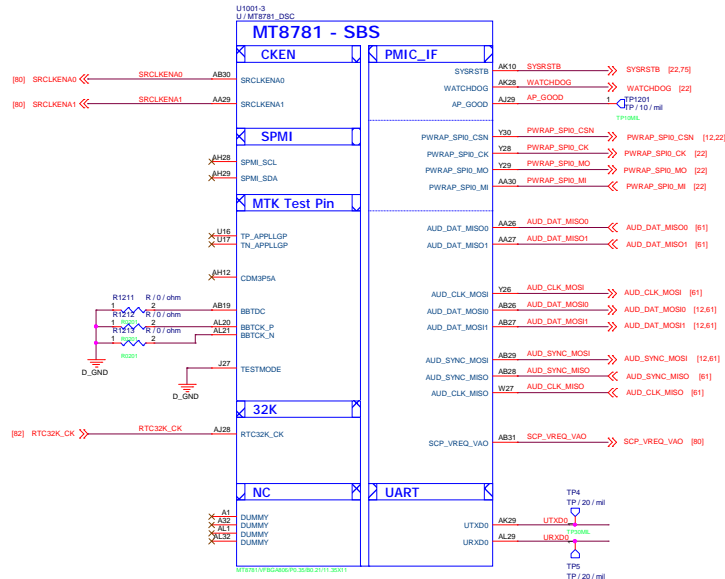
**Schematic design notice of "10\_BB\_POWER\_PDN" page.**

Note 10-1: Differential pair of PMIC remote sense must be close to BB's ball.  
Remote sense trace with GND shielding to PMIC (Differential)

<b>SECRET</b>	
Title	10_BB_PDN1
Size	MTK Confidential
Date	Saturday, October 08, 2022
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Schematic design notice of "11\_BB\_POWER\_IO" page.



**Schematic design notice of "12\_BB\_1" page:**

Note 12-1: The de-coupling cap. for REFP have to be placed as close to BB as possible.

Note 12-2: "PWRAP\_SPIO\_CSN" and "AUD\_DAT\_MOSI0" pin features in trapping pin to enable JTAG.

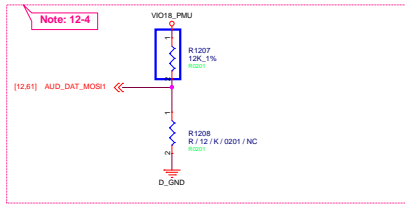
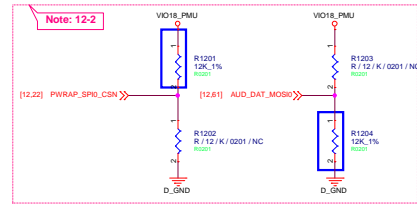
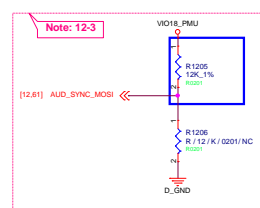
PWRAP_SPIO_CSN	AUD_DAT_MOSI0	AP JTAG Mode	IO JTAG Mode
H (Default)	L (Default)	N/A	N/A
H	H (by external PU)	SPI5_CSB, SPI5_CLK, SPI5_MO, SPI5_MI, EINT13	N/A
L (by external PD)	L	SPI1_CSB, SPI1_CLK, SPI1_MO, SPI1_MI, EINT13	N/A
L (by external PD)	H (by external PU)	N/A	N/A

Note 12-3: "AUD\_SYNC\_MOSI" pin features in trapping pin to booting (UFS/eMMC).

AUD_SYNC_MOSI	Storage Booting Mode
L (Default)	Only UFS boot
H (by external PU)	Only eMMC boot

Note 12-4 "AUD\_DAT\_MOSI1" pin features in trapping pin for SW co-load.

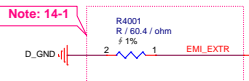
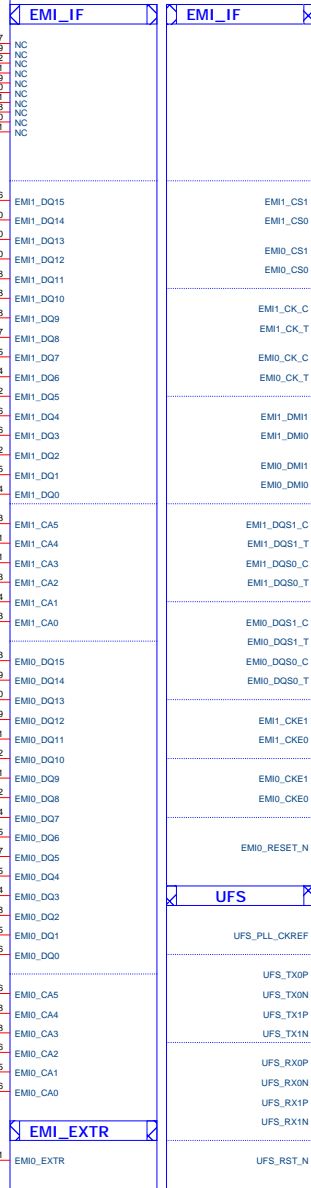
AUD_DAT_MOSI1	Mode
L (Default)	LP4x-MCP
H (by external PU)	LP4x-Discrete





U1001-5  
U/MT8781\_DSC

**MT8781 - SBS**



**Schematic design notice of "14\_BB\_3\_Interface" page:**

Note 14-1: R4001 please select 60.4 ohm (1%) resistor

Note 14-2: Make sure TX/RX connection (T to in, R to out and P to t, N to c)

<b>RECALCULATED</b>	
Title	14_BB_3
Size	C
<b>MTK Confidential</b>	
Date	Saturday, October 08, 2022
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**Schematic design notice of "16\_BB\_AUXADC" page.**

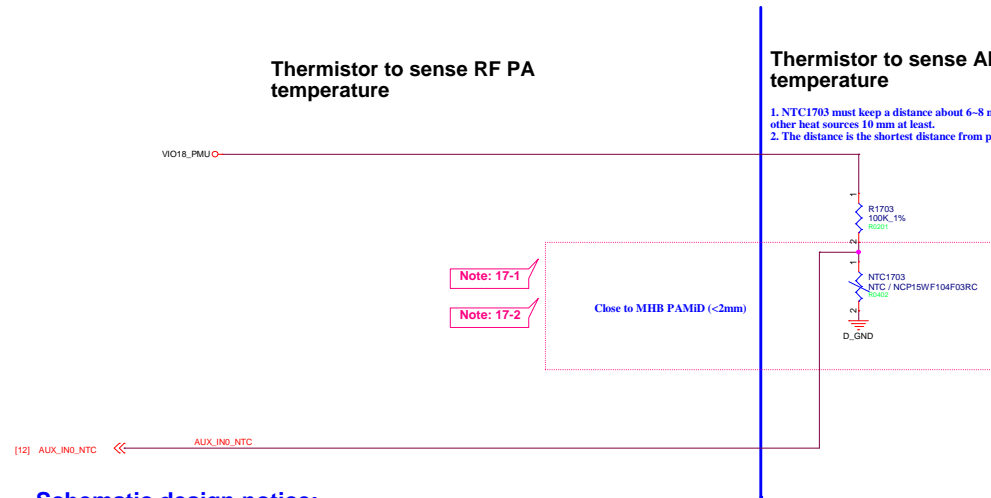
	AUX_IN2 (RF SKU/PCB ID) (ADC range is 0.05~1.45V)
SKU1 EU+CHN+JPN	0.05V 0V(R1604=NC, R1606=100K)
SKU2 NA	0.21V 0.21V(R1604=750K, R1606=100K)
Reserved	0.42V 0.41V(R1604=330K, R1606=100K)
Reserved	0.62V 0.62V(R1604=191K, R1606=100K)
Reserved	0.82V 0.82V(R1604=120K, R1606=100K)
Reserved	1.04V 0.99V(R1604=100K, R1606=137K)
Reserved	1.24V 1.24V(R1604=100K, R1606=220K)
Reserved	1.45V 1.45V(R1604=100K, R1606=422K)

<b>SECRET</b>	
Title	16_BB_AUXADC
Size	MTK Confidential
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**Thermistor to sense RF PA temperature**

**Thermistor to sense AP temperature**

1. NTC1703 must keep a distance about 6-8 mm away from AP and far from other heat sources 10 mm at least.
2. The distance is the shortest distance from package edge to edge.

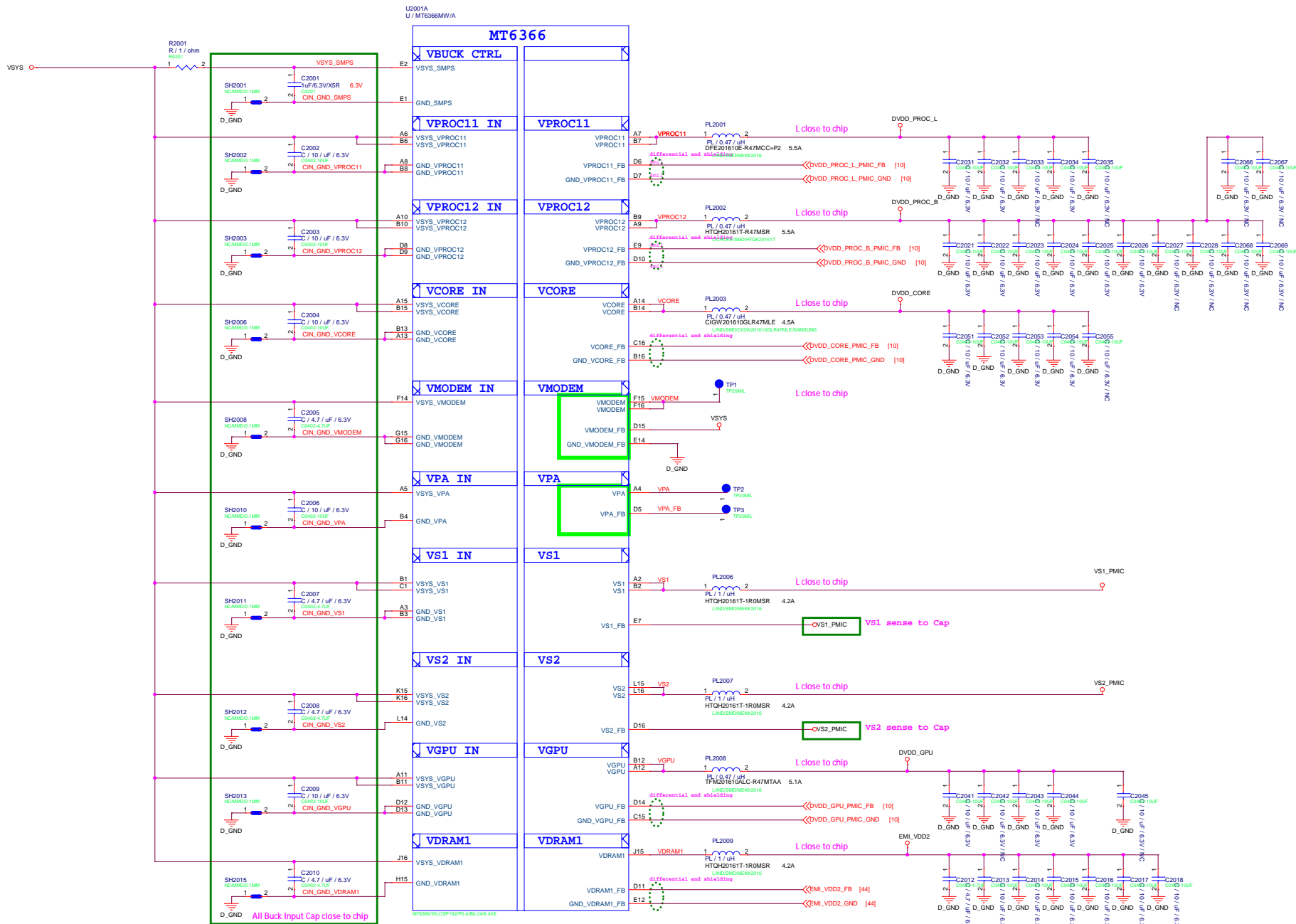


**Schematic design notice:**

Note 17-1: SW Default Configuration is as followings  
 AUX\_IN0\_NTC is for AP Temp.  
 AUX\_IN1\_NTC is for MHB PAMiD Temp.

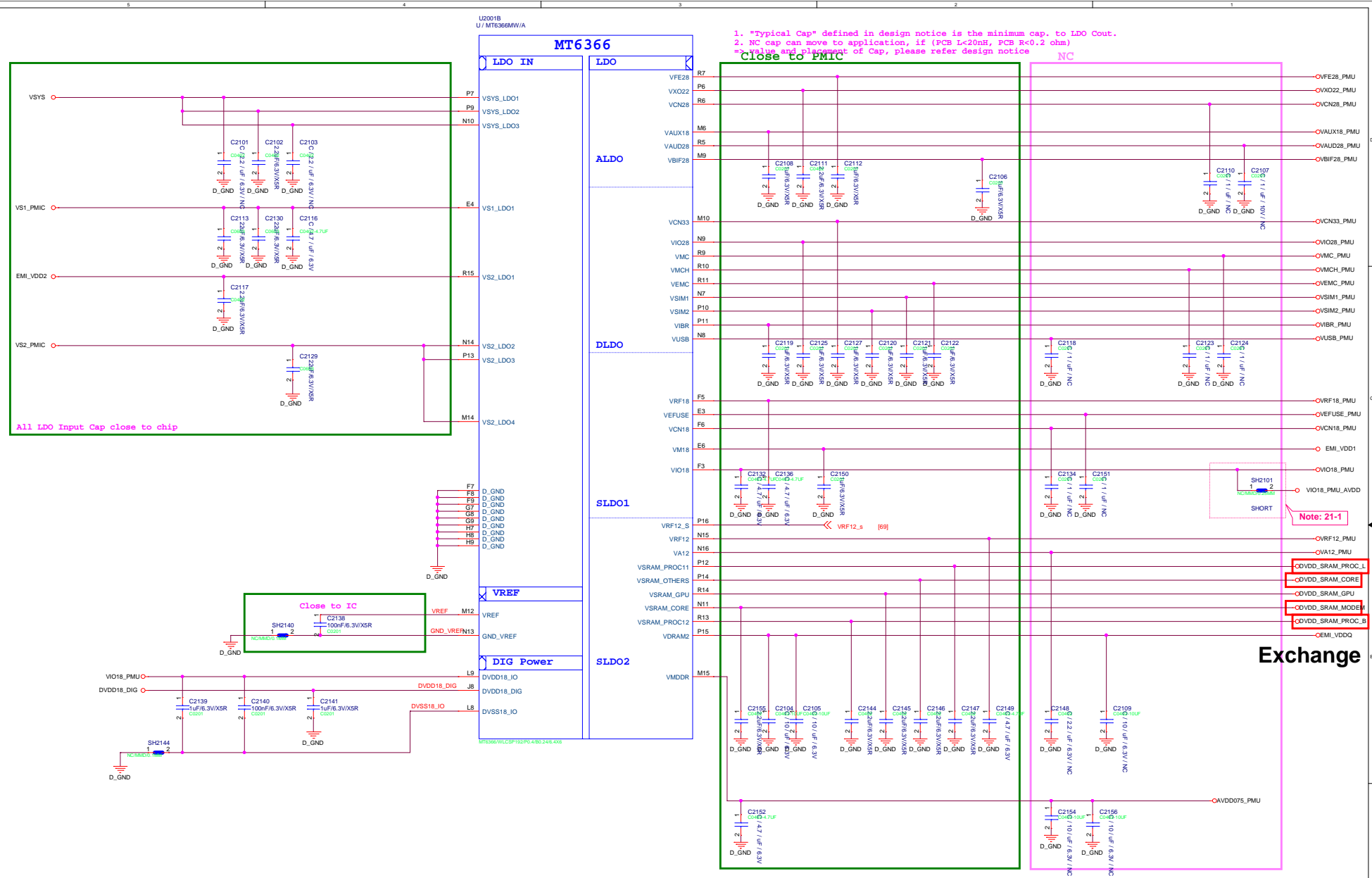
Note 17-2: If your design or placement is different with SW Default Config.  
 Please refer to "MTXXXX Thermal User Manuel.docx" and modify SW setting.

<b>SECRET</b>	
Title	17_BB_AUXADC_Thermal
Size	MTK Confidential
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<b>REVISION</b>	
Title	20_POWER_MT6366-Buck
Size	MTK Confidential
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1. "Typical Cap" defined in design notice is the minimum cap. to LDO Cout.  
 2. NC cap can move to application, if (PCB L<20nH, PCB R<0.2 ohm)  
 = value and placement of Cap, please refer design notice

All LDO Input Cap close to chip

Close to IC

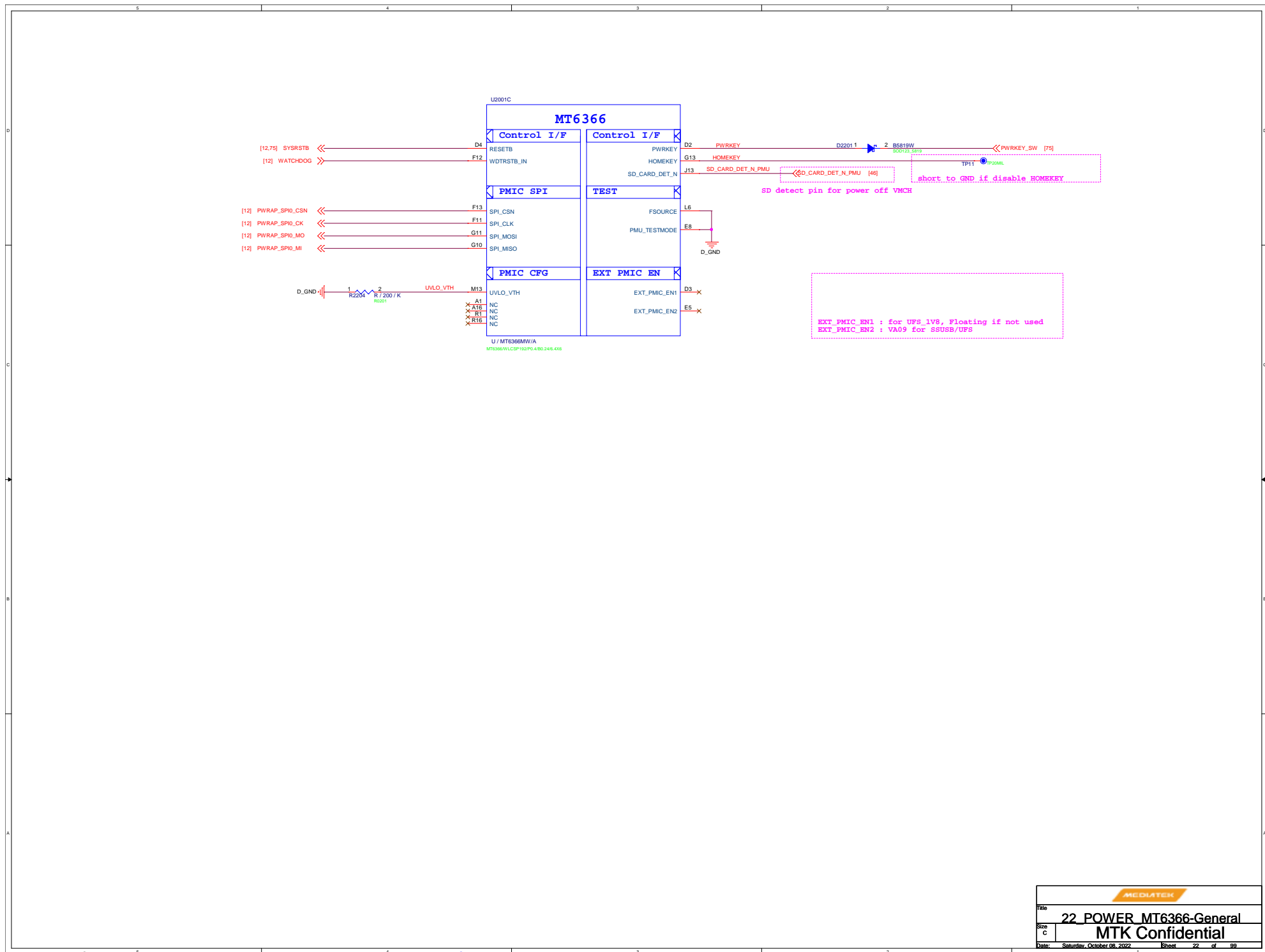
Note: 21-1

Exchange

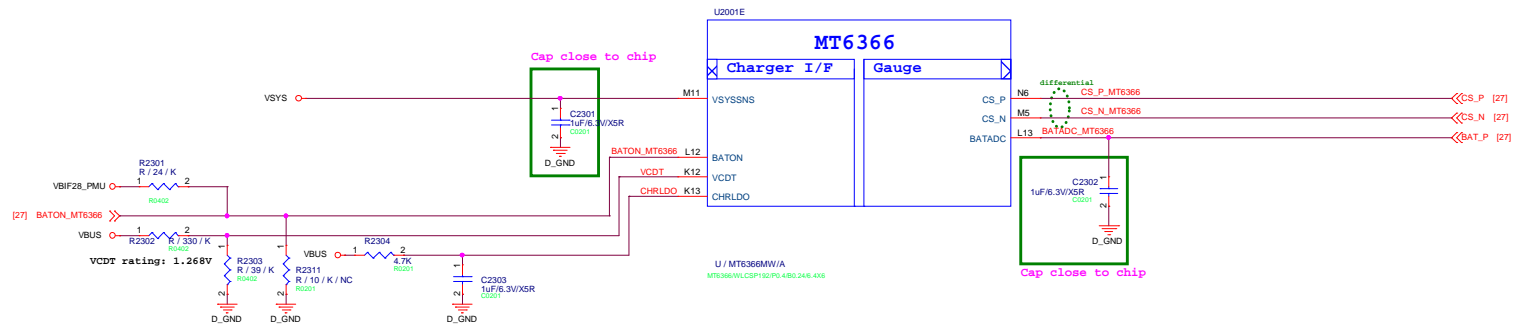
Schematic design notice of "21\_POWER\_MT6366-LDO" page.

Note 21-1: Please set SH2101 close to C2132, making star connection between VIO18\_PMU and VIO18\_PMU\_AVDD near to LDO cap. C2132  
 Please also refer to MT6366 design notice for further detail design information

<b>SECRET</b>	
Title	21_POWER_MT6366-LDO
Size	C
<b>MTK Confidential</b>	
Date	Saturday, October 08, 2022
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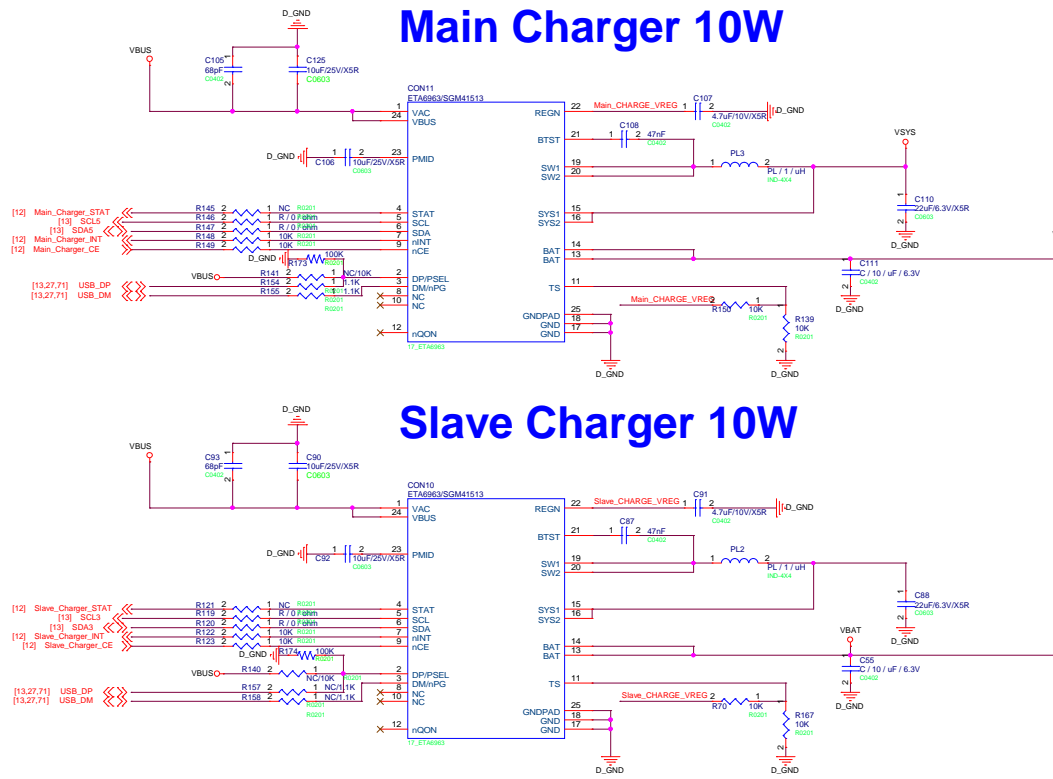
EXT\_PMIC\_EN1 : for UFS\_V18, Floating if not used  
EXT\_PMIC\_EN2 : VA09 for SSUSB/UFS



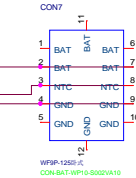
Schematic design notice of "23\_POWER\_MainPMIC-Charger" page:

<b>SECRET</b>	
Title	23_POWER_MainPMIC-Charger
Size	MTK Confidential
Date	Saturday, October 08, 2022
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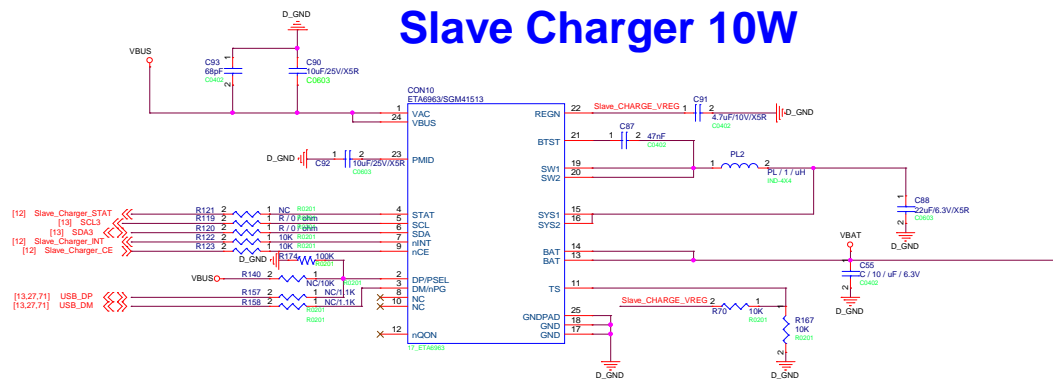
# Main Charger 10W



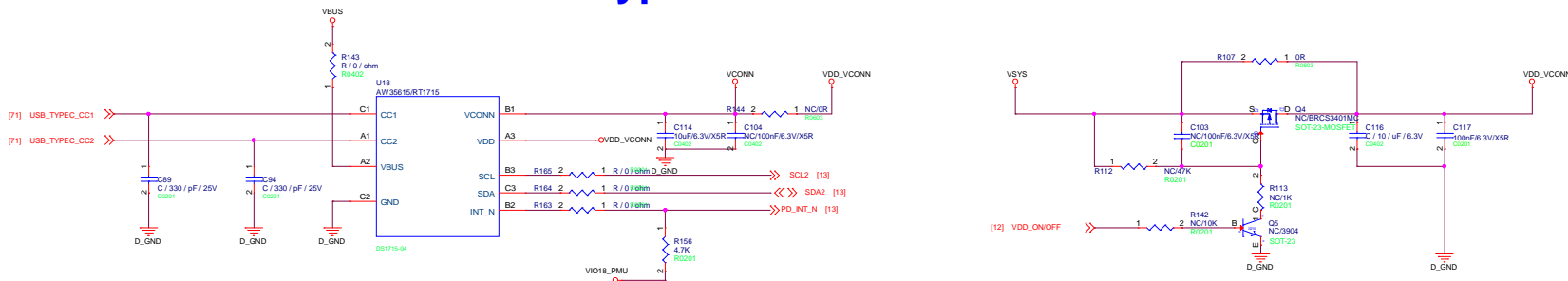
# BATTERY CONNECTOR



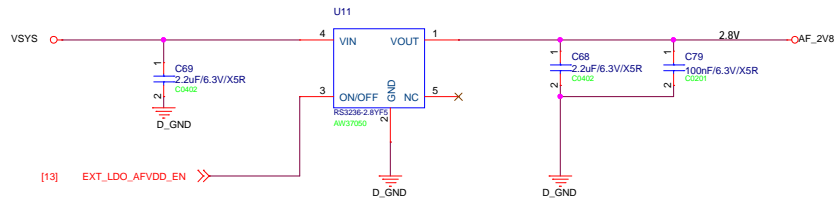
# Slave Charger 10W



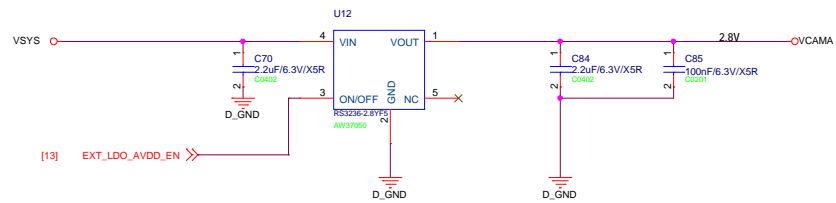
# USB Type-C PD Controller



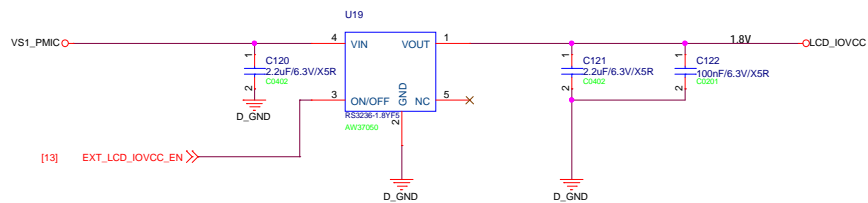
### LDO for Rear Camera AF\_2.8V 500mA



### LDO for Camera VCAMA 2.8V 500mA



### LDO for Pannel LCD\_IOVDD 1.8V 500mA



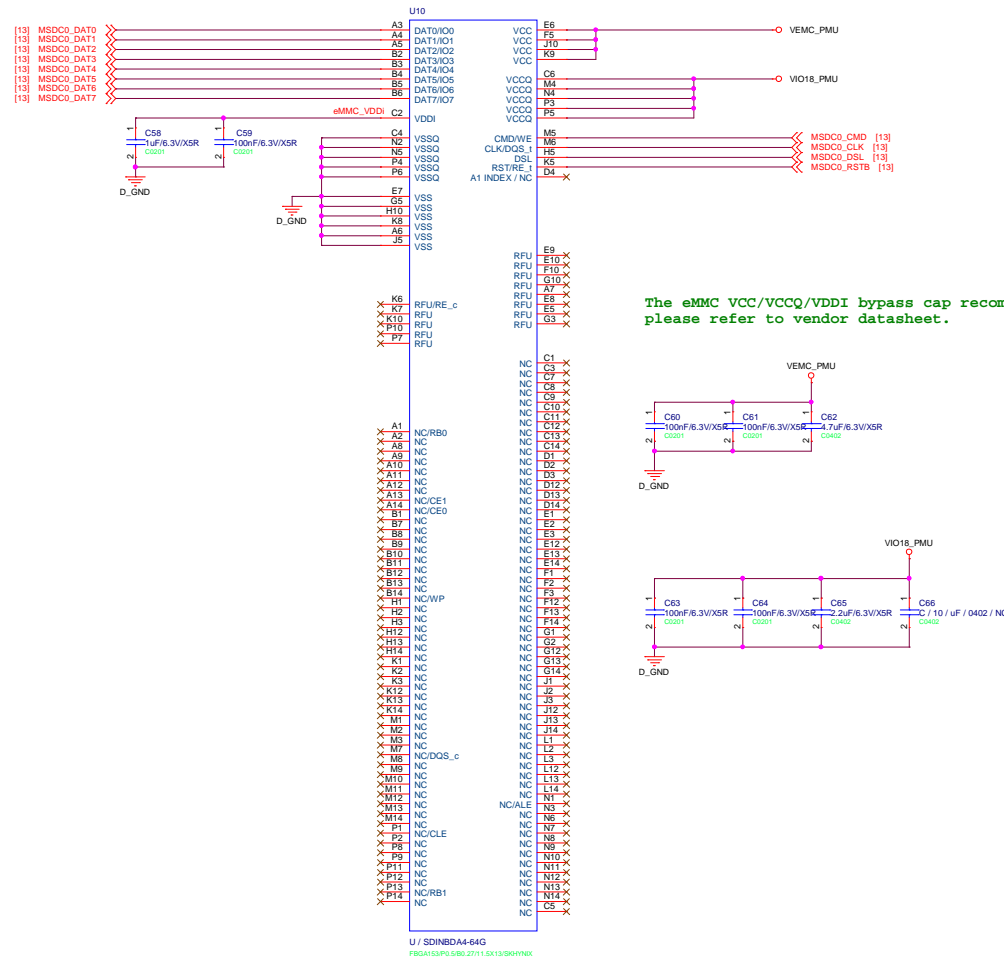
Schematic design notice of "28\_POWER\_EXT\_LDO" page:

XXX  
XXX  
XXX

Title: 29_POWER_EXT	
Size: Custom	MTK Confidential
Date: Saturday, October 08, 2022	Sheet: 29 of 99

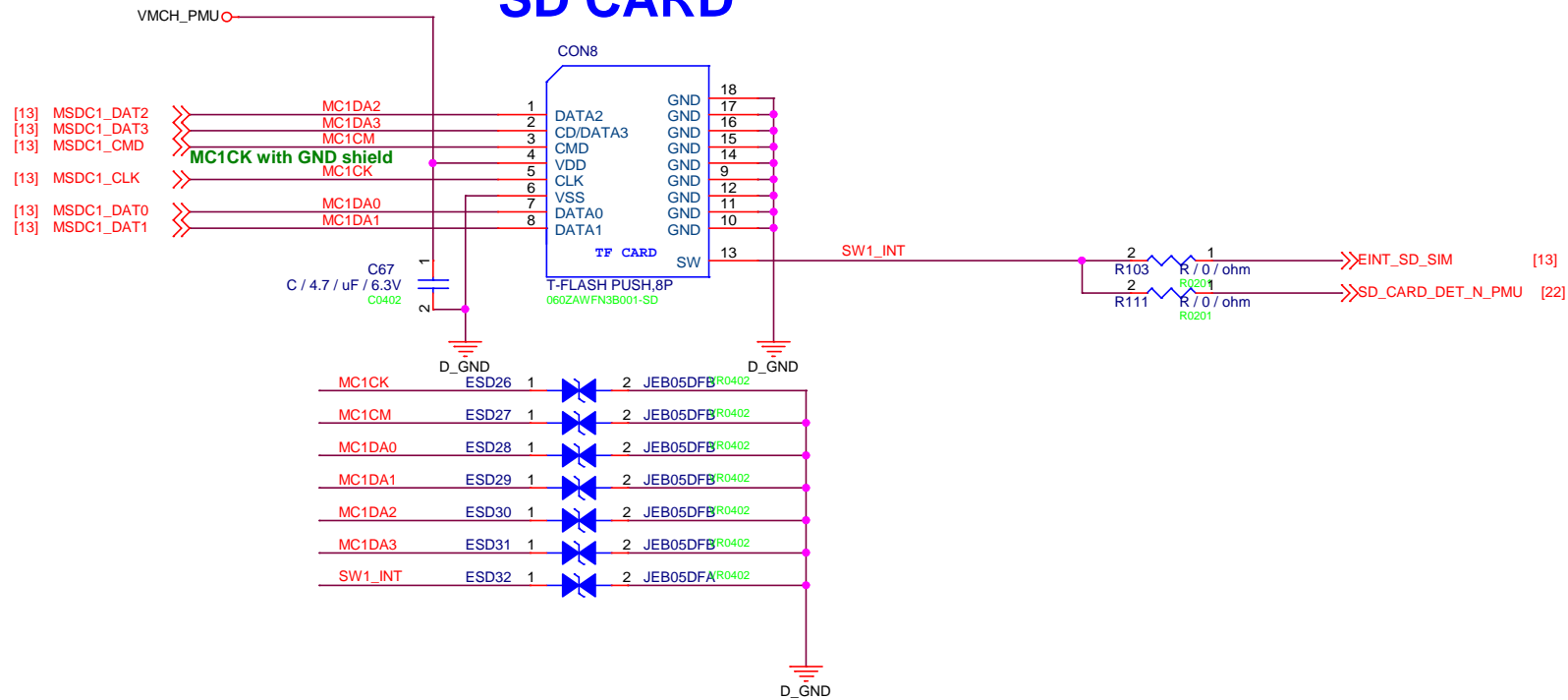


# eMMC



The eMMC VCC/VCCQ/VDDI bypass cap recommend value, please refer to vendor datasheet.

# SD CARD



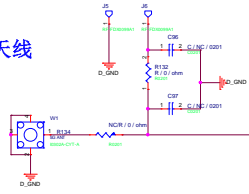
Schematic design notice of "46\_MEMORY\_SD Card" page.

Note 46-1:

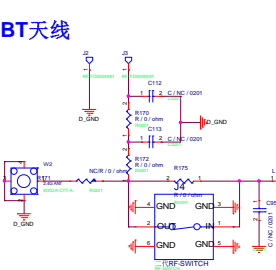
Title	
46_Memory_SD Card	
Size	Custom
MTK Confidential	
Date:	Saturday, October 08, 2022
Sheet	46 of 99



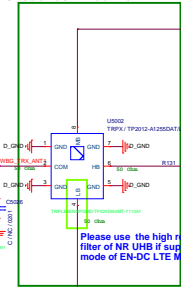
5G WIFI天线



2.4G WIFI+BT天线



Close to Antenna



Please use the high rejection filter of NR UHB if support two Tx mode of EN-DC LTE MB+NR UHB

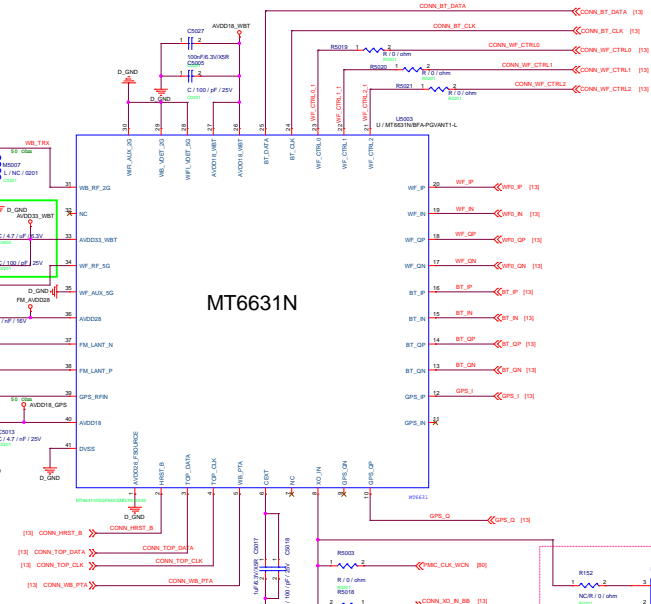
if need to pass 2G 2nd harmonic FCC spec, need add BPF @ 5G RF port. Details and FM refer to the document < MT6631 2G Tx 2nd harmonic improvement for specific customers have more strict 2nd harmonic spec >

<Additional> 5G PCB loss is higher and trace must kept short and 5G-ohm No layer transition

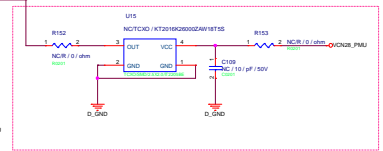
\*GPIO\_GPS\_LNA\_EN\* has to use GPIO with \*O:GPS\_L1\_ELNA\_EN\* function. Please refer to \*MT6781\_GPIO\_Application\_Spec\* to select suitable GPIO with \*O:GPS\_L1\_ELNA\_EN\* function.

Please reserve this notch for GPS and cellular co-existence if support LTE B13/14

MT6631N



TCXO

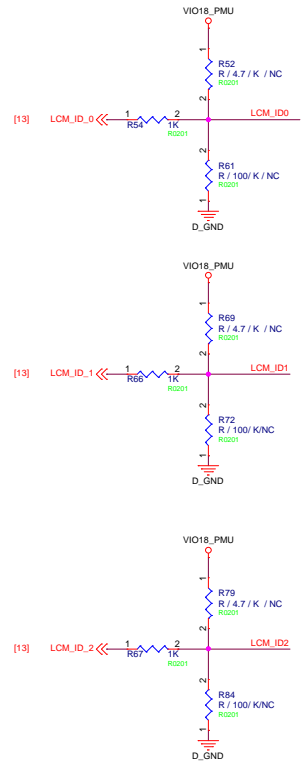




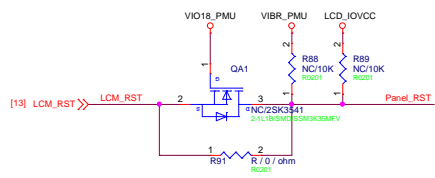




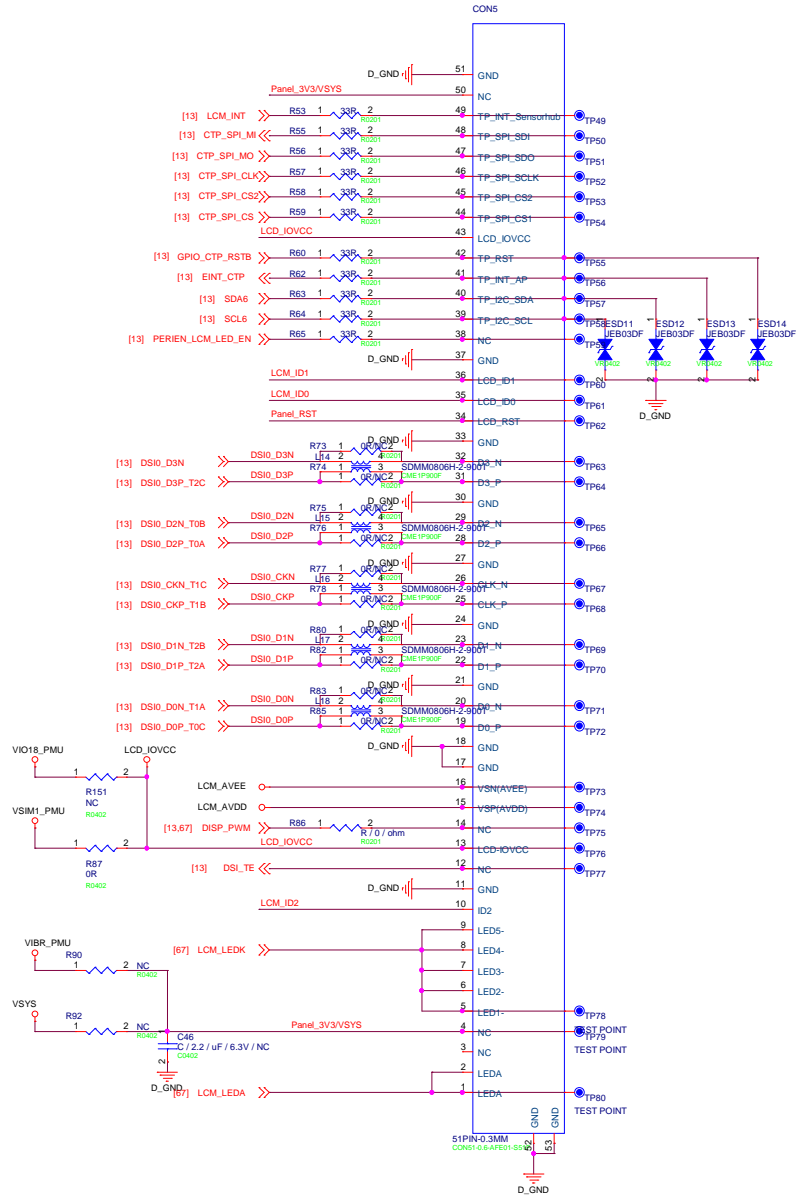
# Panel\_ID



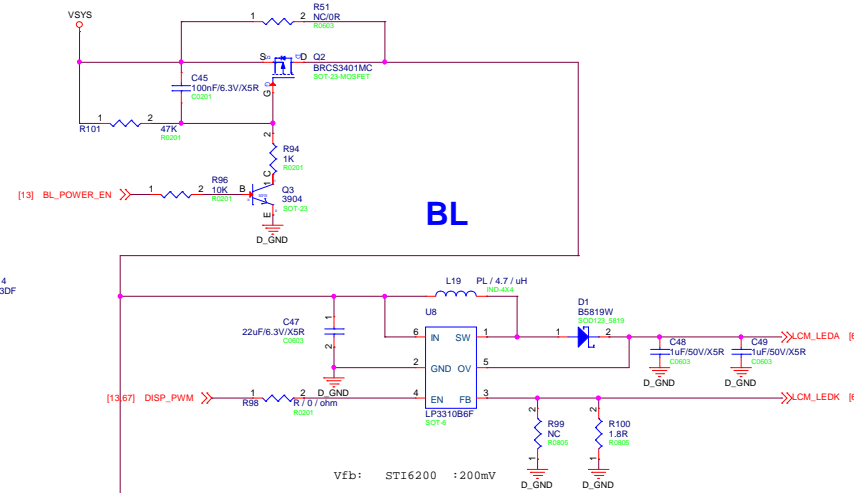
# Panel\_RESET



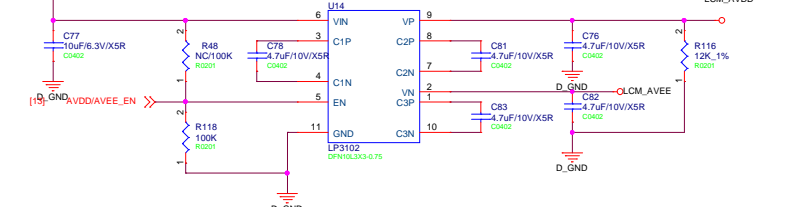
# 10.1"、10.4"Panel LCM Connector



# BL

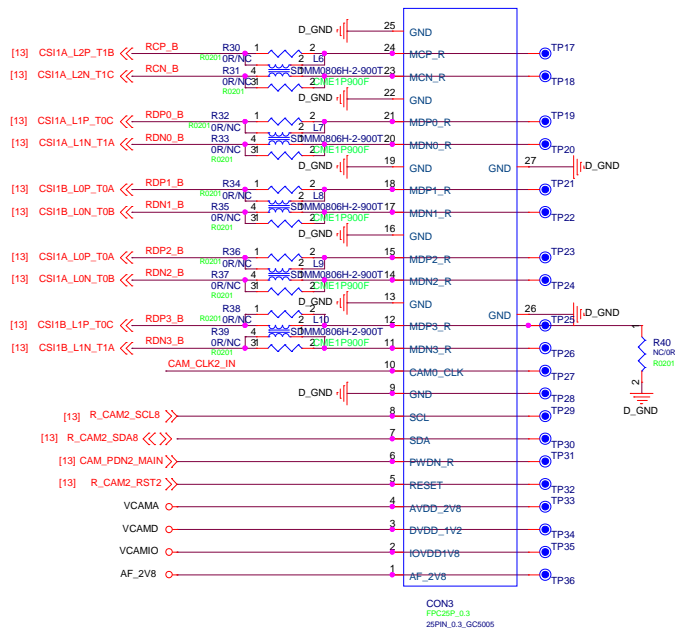


# AVDD/AVEE

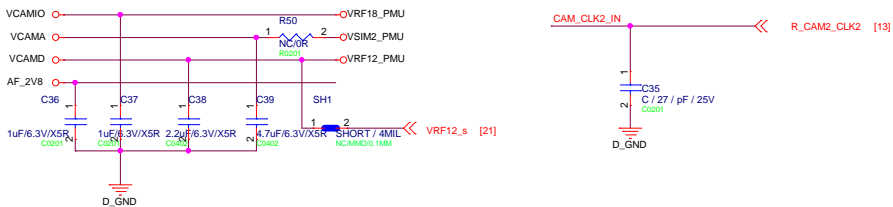


<b>MEDIATEK</b>	
File	67_PERI_LCD
Size	MTK Confidential
Date	Saturday, October 08, 2022
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# Rear Camera



CSI #	Pad name	4-lane DPHY mode		
		4-lane	2-lane	1-lane
CSI-1	CSI1A_L0P_T0A	RDP2	N/A	N/A
	CSI1A_L0N_T0B	RDN2	N/A	N/A
	CSI1A_L1P_T0C	RDP0	RDP0	RDP0
	CSI1A_L1N_T1A	RDN0	RDN0	RDN0
	CSI1A_L2P_T1B	RCP	RCP	RCP
	CSI1A_L2N_T1C	RCN	RCN	RCN
	CSI1B_L0P_T0A	RDP1	RDP1	N/A
	CSI1B_L0N_T0B	RDN1	RDN1	N/A
	CSI1B_L1P_T0C	RDP3	N/A	N/A
	CSI1B_L1N_T1A	RDN3	N/A	N/A



Name	Output Voltage (V)	I <sub>OUT-MAX</sub> (mA)	Expected Use
VSIM1	1.7/1.8/1.86/2.76/3.0/3.1	200	SIM
VSIM2	1.7/1.8/1.86/2.76/3.0/3.1	200	SIM
VIBR	1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3	200	Vibrator
Name	Output Voltage (V)	I <sub>OUT-MAX</sub> (mA)	Expected Use
VFE28	2.8	50	RFFE
VXO22	2.24	50	DCXO
VRF18	1.81	450	RF
VRF12	1.2	800	RF

## 2.5 Power Consumption

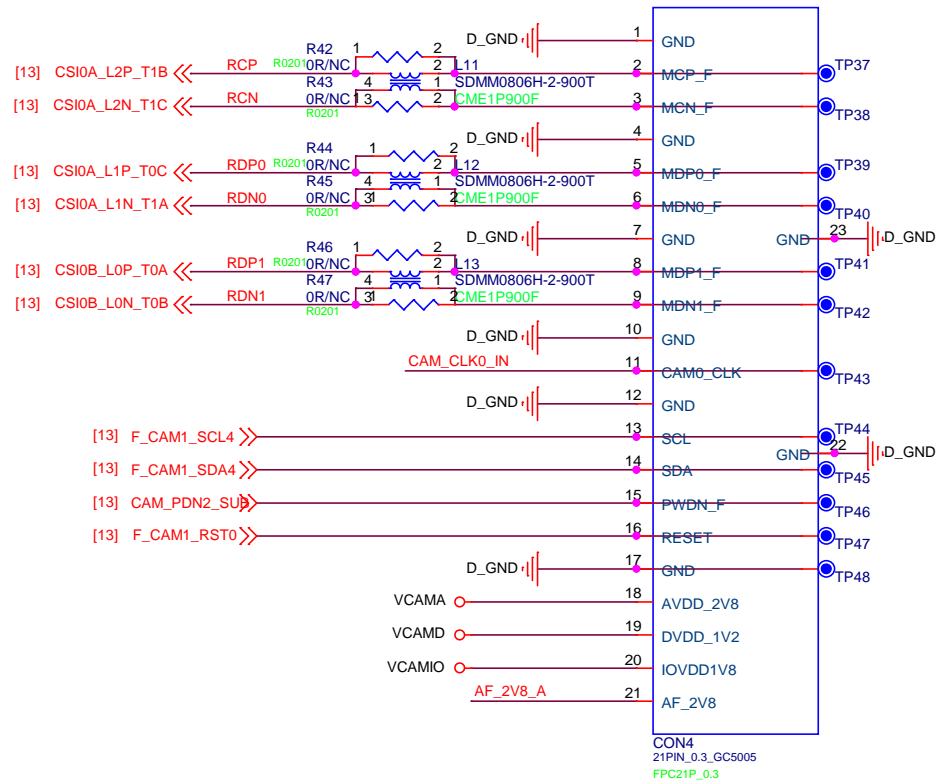
Table 3: Power Consumption

Item	Symbol	Min	Typ	Max	Unit
Full size @30fps 2-lane	l <sub>mode</sub>	-	30	60	mA
	l <sub>idle</sub>	-	75	150	mA
	l <sub>standby</sub>	-	1	10	mA
Full size @30fps 4-lane	l <sub>mode</sub>	-	30	60	mA
	l <sub>idle</sub>	-	75	150	mA
	l <sub>standby</sub>	-	1	10	mA
1032x1224 @60fps	l <sub>mode</sub>	-	30	60	mA
	l <sub>idle</sub>	-	60	110	mA
	l <sub>standby</sub>	-	1	10	mA
1080P@60fps	l <sub>mode</sub>	-	30	60	mA
	l <sub>idle</sub>	-	50	100	mA
	l <sub>standby</sub>	-	1	10	mA
720P@60fps	l <sub>mode</sub>	-	30	60	mA
	l <sub>idle</sub>	-	50	100	mA
	l <sub>standby</sub>	-	1	10	mA
Standby current	l <sub>mode</sub>	-	5	90	µA
	l <sub>idle</sub>	-	120	2500	µA
	l <sub>standby</sub>	-	50	190	µA
Power off current	l <sub>low</sub>	-	-	9	µA

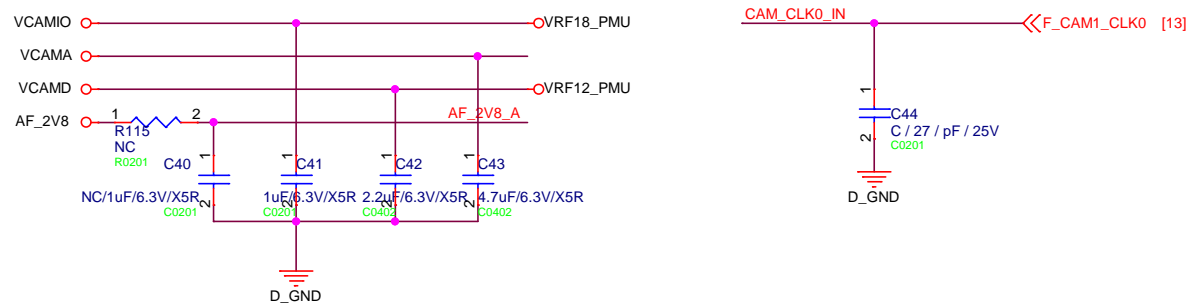


File: 69\_PERI\_CAMERA Rear  
 Size: Custom  
 MTK Confidential  
 Date: Saturday, October 08, 2022 Sheet: 69 of 99

# Front Camera



CSI #	Pad name	4-lane DPHY mode		
		4-lane	2-lane	1-lane
CSI-0	CSI0A_L0P_T0A	RDP2	N/A	N/A
	CSI0A_L0N_T0B	RDN2	N/A	N/A
	CSI0A_L1P_T0C	RDP0	RDP0	RDP0
	CSI0A_L1N_T1A	RDN0	RDN0	RDN0
	CSI0A_L2P_T1B	RCP	RCP	RCP
	CSI0A_L2N_T1C	RCN	RCN	RCN
	CSI0B_L0P_T0A	RDP1	RDP1	N/A
	CSI0B_L0N_T0B	RDN1	RDN1	N/A
	CSI0B_L1P_T0C	RDP3	N/A	N/A
	CSI0B_L1N_T1A	RDN3	N/A	N/A



**MEDIATEK**

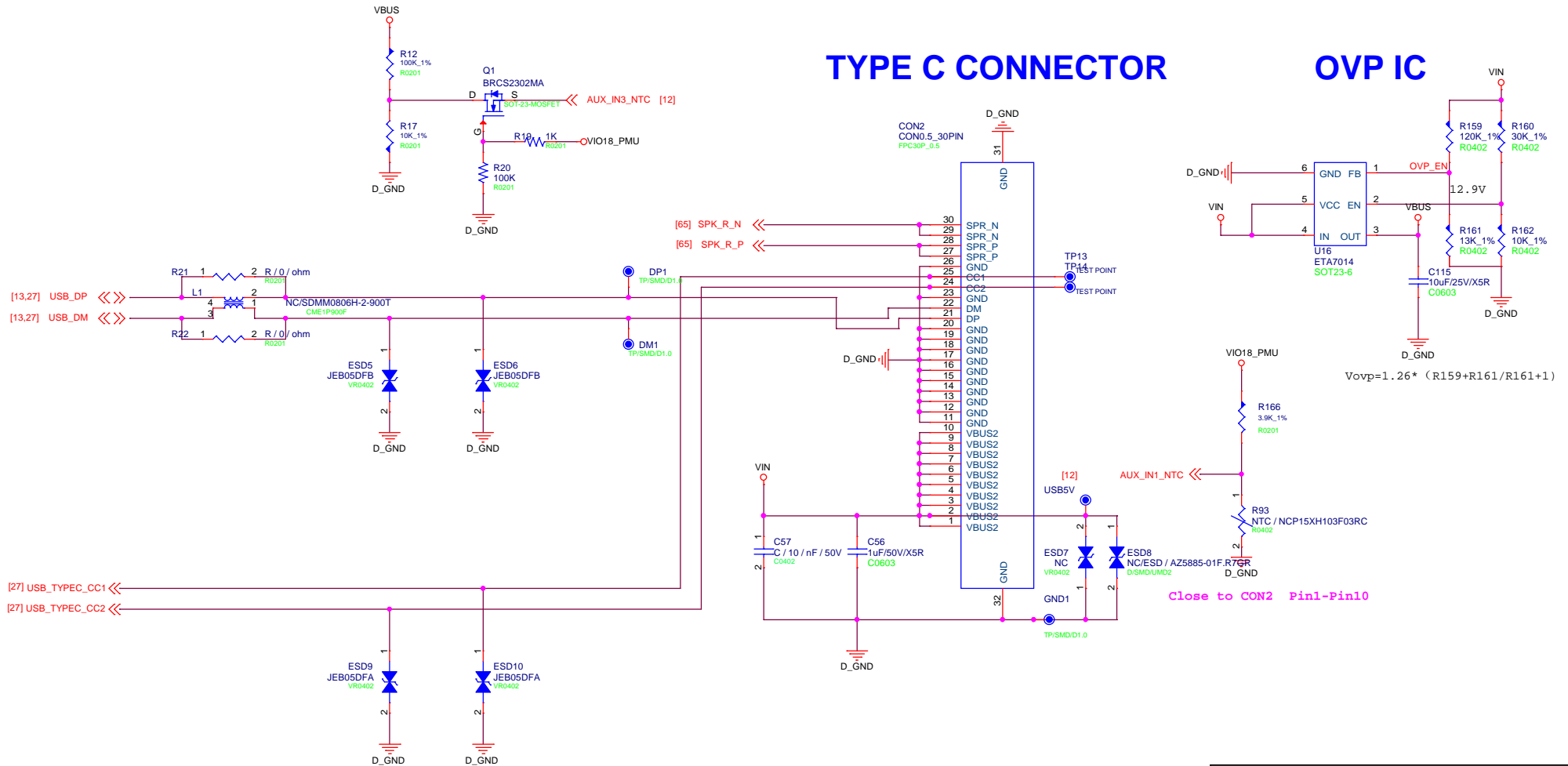
Title: **70\_PERI\_CAMERA\_Front**

Size: Custom

Date: Saturday, October 08, 2022 Sheet 70 of 99

# TYPE C CONNECTOR

# OVP IC

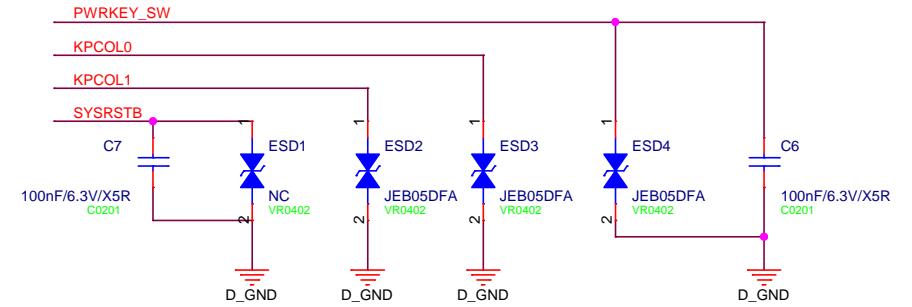
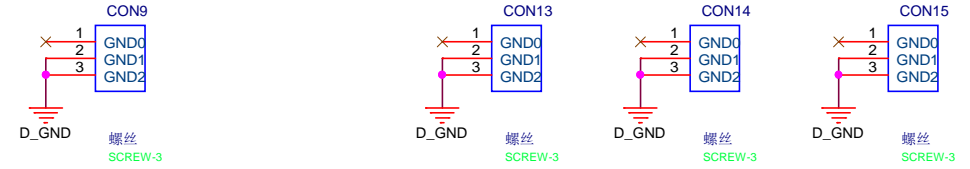
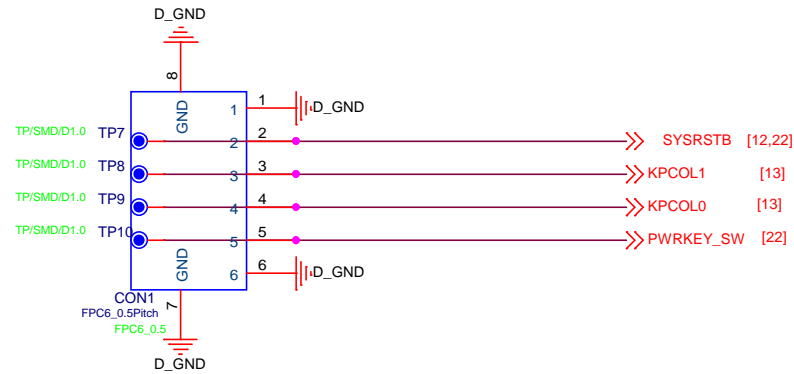


<b>MEDIATEK</b>	
Title	71_PERI_USB_DTB
Size	Custom
<b>MTK Confidential</b>	
Date:	Saturday, October 08, 2022
Sheet	71 of 99

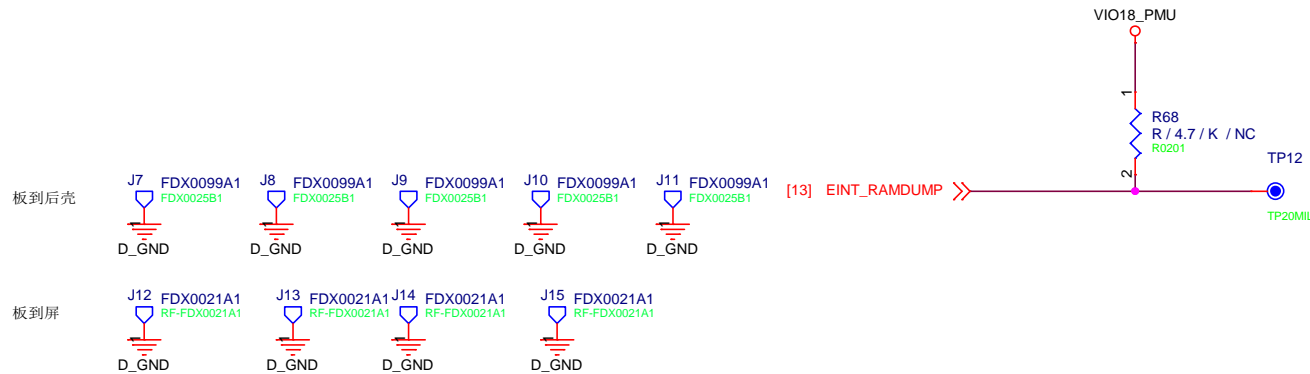


# Power Key / Key Pad

DO NOT put pull-up resistor on PWRKEY

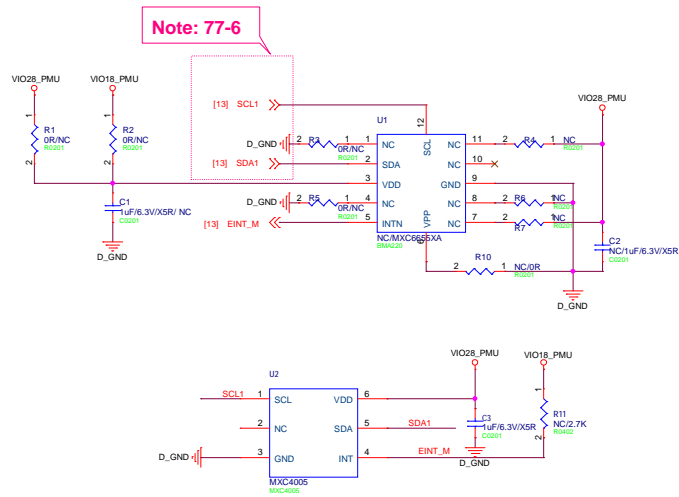


# RAMDUMP debug key

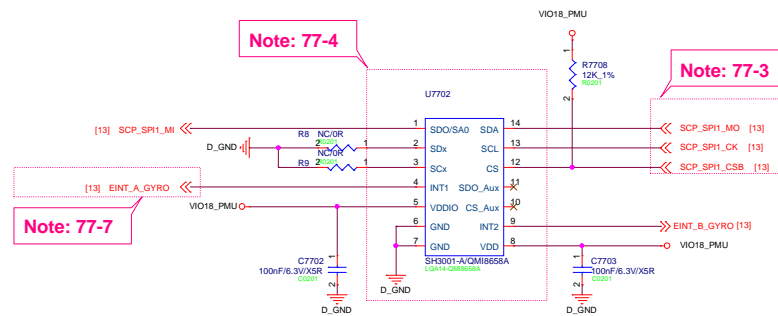


Title	75_PERI_KEYPAD
Size	Custom
<b>MTK Confidential</b>	
Date:	Saturday, October 08, 2022
Sheet	75 of 99

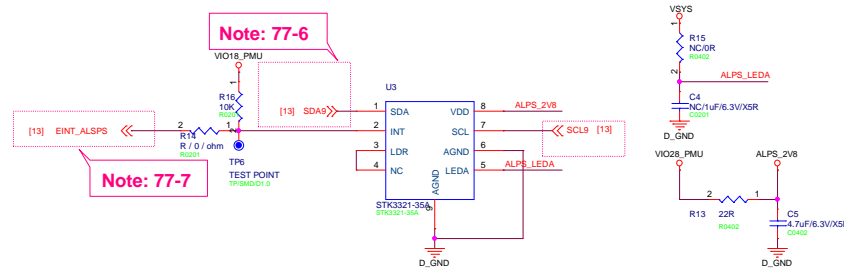
## G-Sensor



## Accerometer + Gyro Sensor (Reserve)



## ALS + Proximity Sensor



### Schematic design notice of "77\_PERI\_SENSORS\_MEMs\_ALS/PS" page.

Note 77-1: [M sensor] Keep a minimum distance of 15mm from power ICs / PCB traces of more than 100mA / magnet component. Check HW design notice for more detail

Note 77-2: [A+G] For optimized GPS performance, please check HW design notice for Sensor selection guide

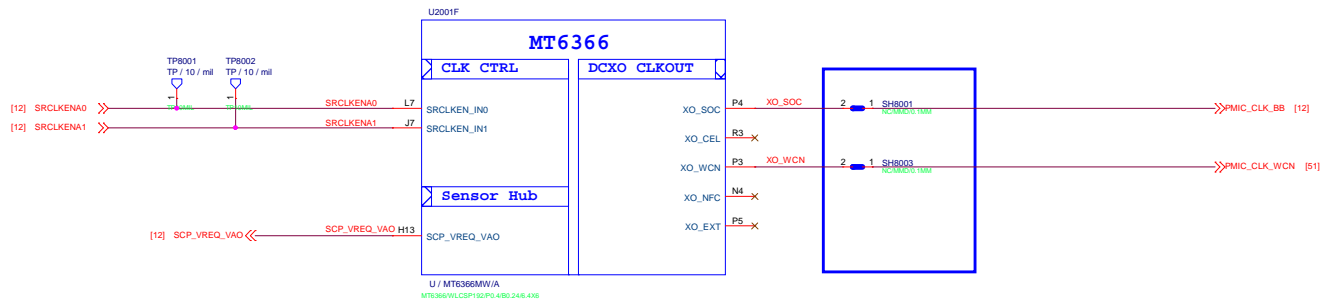
Note 77-3: [A+G] MUST use SPI for optimized sensor hub performance **DO NOT USE I2C**

Note 77-4: [A+G] Suggest choose sensor support **FIFO watermark interrupt** otherwise we cannot support Hifi-sensor, daydream VR. And Sensor-location accuracy will become worse.

Note 77-5: [Baro] Reserve Baro sensor for LPPe feautre (Must for North America Operator / NA SKU)

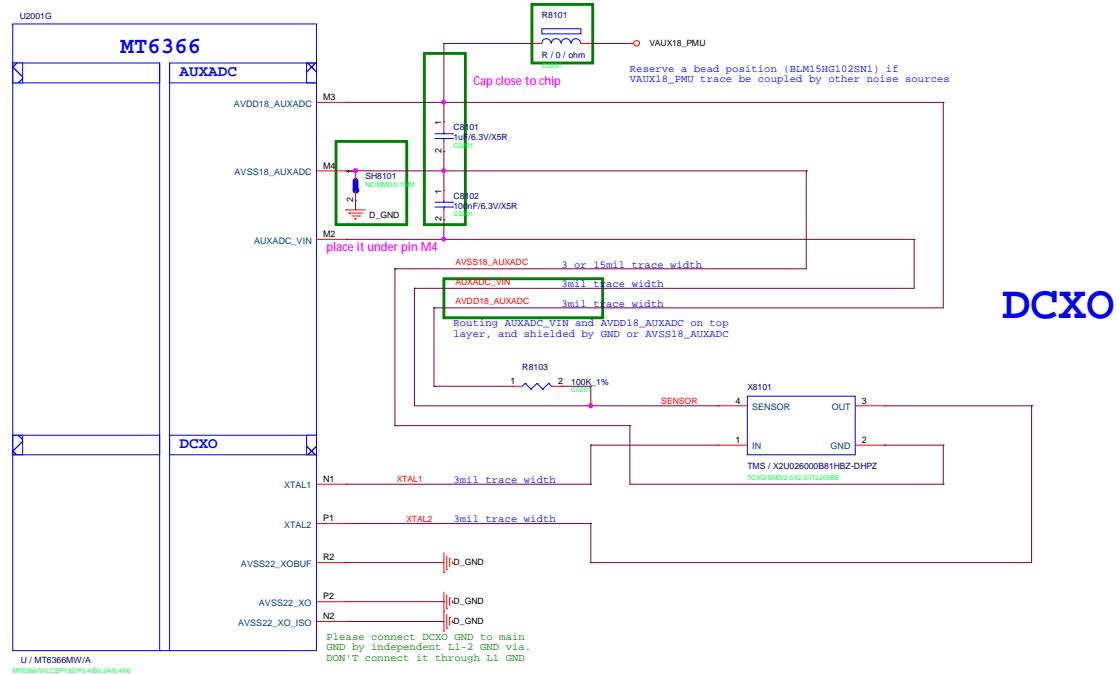
Note 77-6: **DO NOT** share Sensor hub i2C to other non-SCP device

Note 77-7: Interrupt pin of MEMS sensor must be assign to SCP\_EINT



Schematic design notice of "80\_SYSCLK\_CoClock-26MHz" page:

<b>SECRET</b>	
Title	80_SYSCLK_CoClock-26MHz
Size	C
<b>MTK Confidential</b>	
Date	Saturday, October 08, 2022
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### Schematic design notice of "81\_SYCLK\_Clock-26MHz-TSX" page:

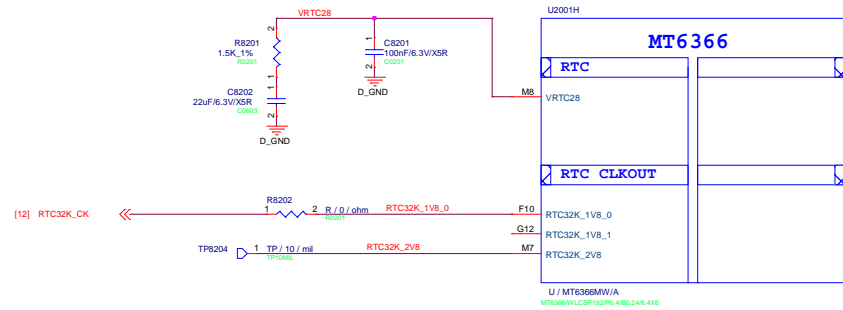
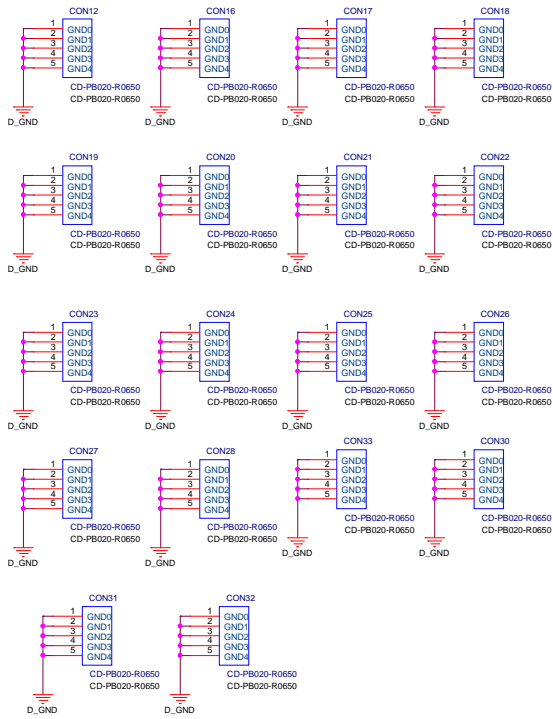
Route AVDD18\_AUXADC/AUXADC\_VIN as differential trace (3 mil each) with well GND shielding and route AVSS18\_AUXADC with 15mil trace width under AVDD18\_AUXADC/AUXADC\_VIN trace to provide return current path.

#### TMS and TCXO Selection:

TMS: R8103=R8106=R8104=R8105=0ohm, R8101=C8103=R8107=NC

TCXO: R8103=R8106=R8104=NC, R8101=C8103=R8107=0ohm, R8105= 10nF, TCXO pin1=TMS pin3

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Schematic design notice of "82\_SYSClk\_RTC32K" page:

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