| DATE | REVISION | ISSUE | DESCRIPTION |
|---|---|---|---|
| 06/20/06 | 0A | Willy Yang | Initial Design based on usb35pn_q_1 |
| 06/26/06 | 1A | Willy Yang | 1. Remove TP1, TP2, TP3, TP4, TP5, TP6, TP11, TP12, TP13, TP14, TP15, and TP23.<br>2. Add JTAG Interface.<br>3. D1, D2, R111, R112 is marked as NL.<br>4. U18 is AS179-92; C41 is 3.0 pF; L1 is 3.9nH; L2 is NL.<br>5. Add GPIO00 and C1 as well as C10 is marked as 2.7pF.<br>6. U15: 88W8338 -> 88W8388.<br>7. L31: 0 -> BEAD32 OHMS<br>8. L32 and L33: 0 -> BEAD60 OHMS<br>9. L34, and L35: 0 -> NL<br>10. C74: 68uF -> NL<br>11. U5: OSC_SMD_5x3 -> NL OSC_SMD_5x3<br>12. R1122: 0 -> 16K; R33: NL -> 100K<br>13. U1: 88W8010/ 88W8015 -> 88W8015<br>14. BA1: WPSMLBLN001C -> RFBLN2012090A0T<br>15. U17: MASWSS0136 -> AS179-92<br>16. ANT1 and ANT2: Hirose U.FL-R-SMT -> U.FL-R-SMT |
| 08/10/06 | 0B | Willy Yang | 1.Remove GPIO03, GPIO04 and GPIO05; Add GPIO12, GPIO13, GPIO14 and GPIO15.<br>2.LED D2 controlled by GPIO12 |
| 06/07/007 | R2.0.1 | Willy Yang | 1. R1122=0 ohm; R33=NL. |

# US101-MV  802.11b/g USB Module Schematics

### Main Chipsets: Marvell 88W8388 + 88W8015

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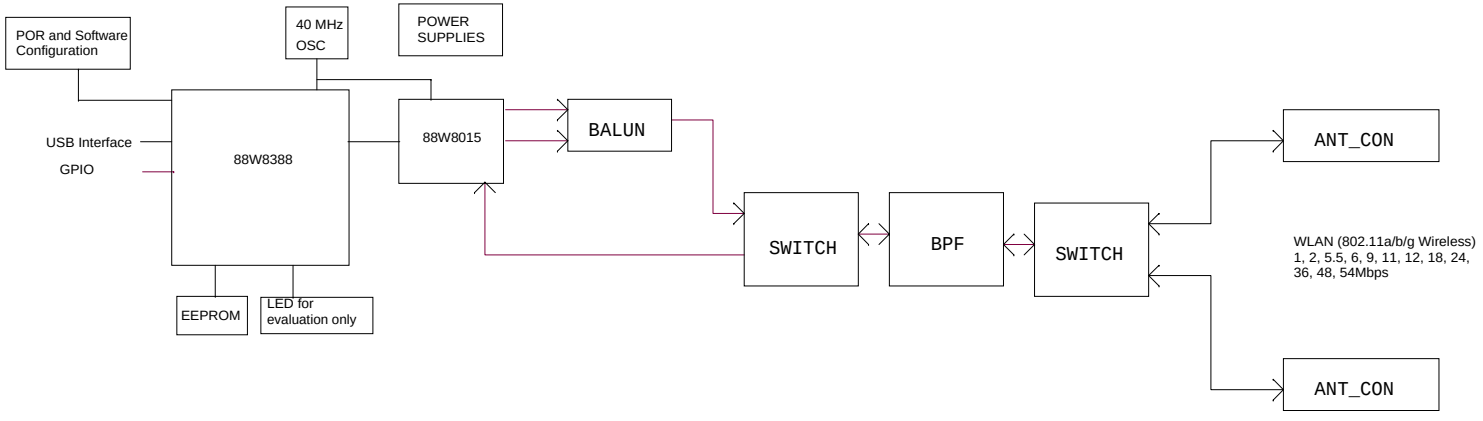
| Model | US101-MV  802.11b/g USB Module Schematics | | |
| Title | | Drawn | Willy Yang |
| DWG No. | <Doc> | Rev | R2.0.1 |
| Size C | Date Friday, July 24, 2009 | Sheet 1 | of 4 |

# Block Diagram




ANT_CON : ANTENNA CONNECTOR
BPF : BAND PASS FILTER



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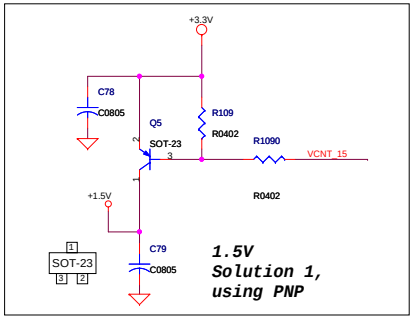
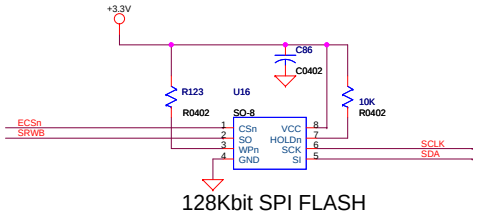
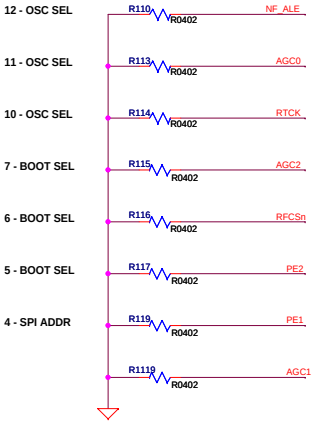



128Kbit SPI FLASH

**INITIALIZATION CONFIGURATION**




8338 RESET CONFIGURATION

**MOUNT THESE RESISTORS CLOSE TO THE CHIP**

**14 NF_CLE**
**13 NF_WPn**
---
**0 0 External MAC mode (need 35 pins)**
**0 1 External USB2.0 Phy mode (need 31 pins)**
**1 0 Reserved**
**1 1 Normal Operation (default)**

**12 NF_ALE**
**11 AGC0**
**10 RTCK**
---
**0 0 0 20 MHz**
**0 0 1 20 MHz**
**0 1 0 40 MHz (default)**
**0 1 1 38.4 MHz**
**1 0 0 19.2 MHz**
**1 0 1 26 MHz**
**1 1 0 44 MHz**
**1 1 1 44 MHz**

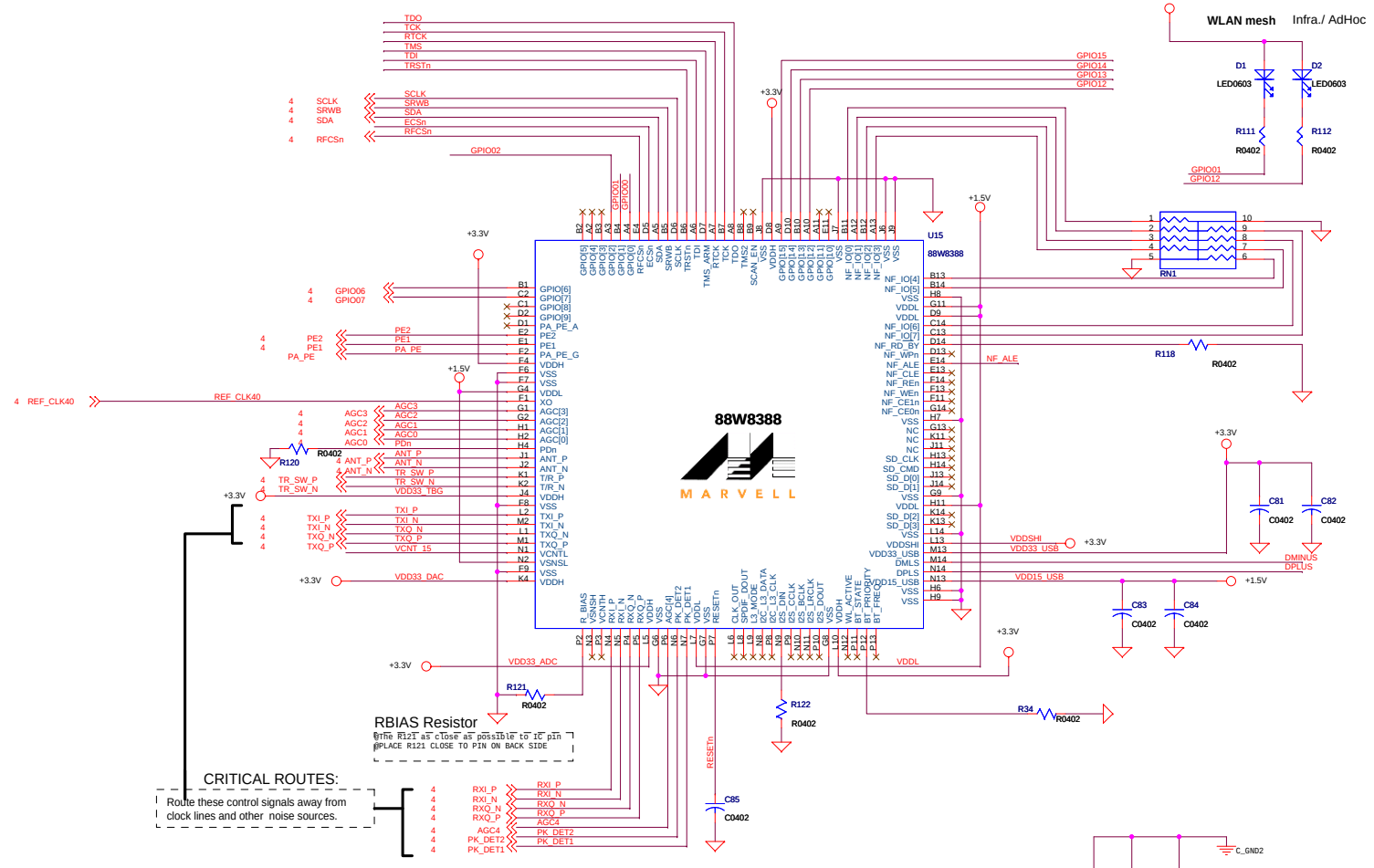
**9 SCLK**
---
**0 ABU Test bus enable**
**1 ABU Test disable (default)**

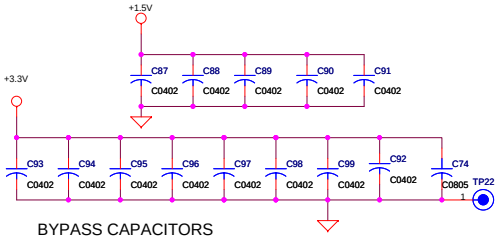
**8 ECSn**
---
**0 Short reset for test purpose**
**1 Long Reset (default)**

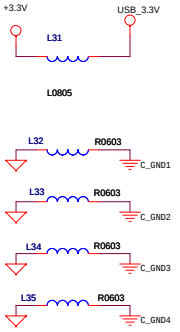
**7 AGC2**
**6 RFCSn**
**5 PE2**
---
**0 0 0 Boot from UART**
**0 0 1 Boot from uWire EEPROM**
**0 1 0 Boot from memory test**
**0 1 1 Reserved**
**1 0 0 Boot from 2-wire EEPROM**
**1 0 1 Boot from host interface bus-no SPI (default)**
**1 1 0 Boot from SPI EEPROM**
**1 1 1 Boot from host interface bus**

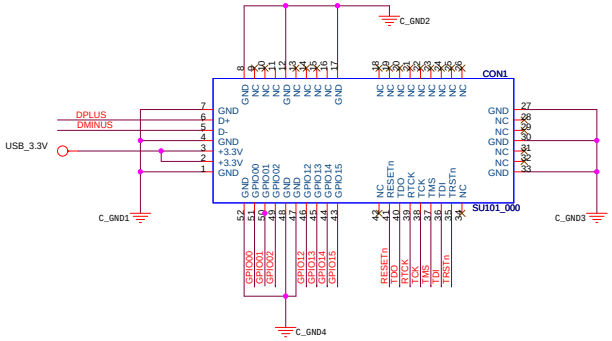
**4 PE1**
---
**0 3Byte SPI EEPROM or 16-bit Flash**
**1 2Byte SPI EEPROM or 8-bit Flash (default)**

**3 AGC3**
---
**0 Reserved**
**1 Boot from BootROM (default)**

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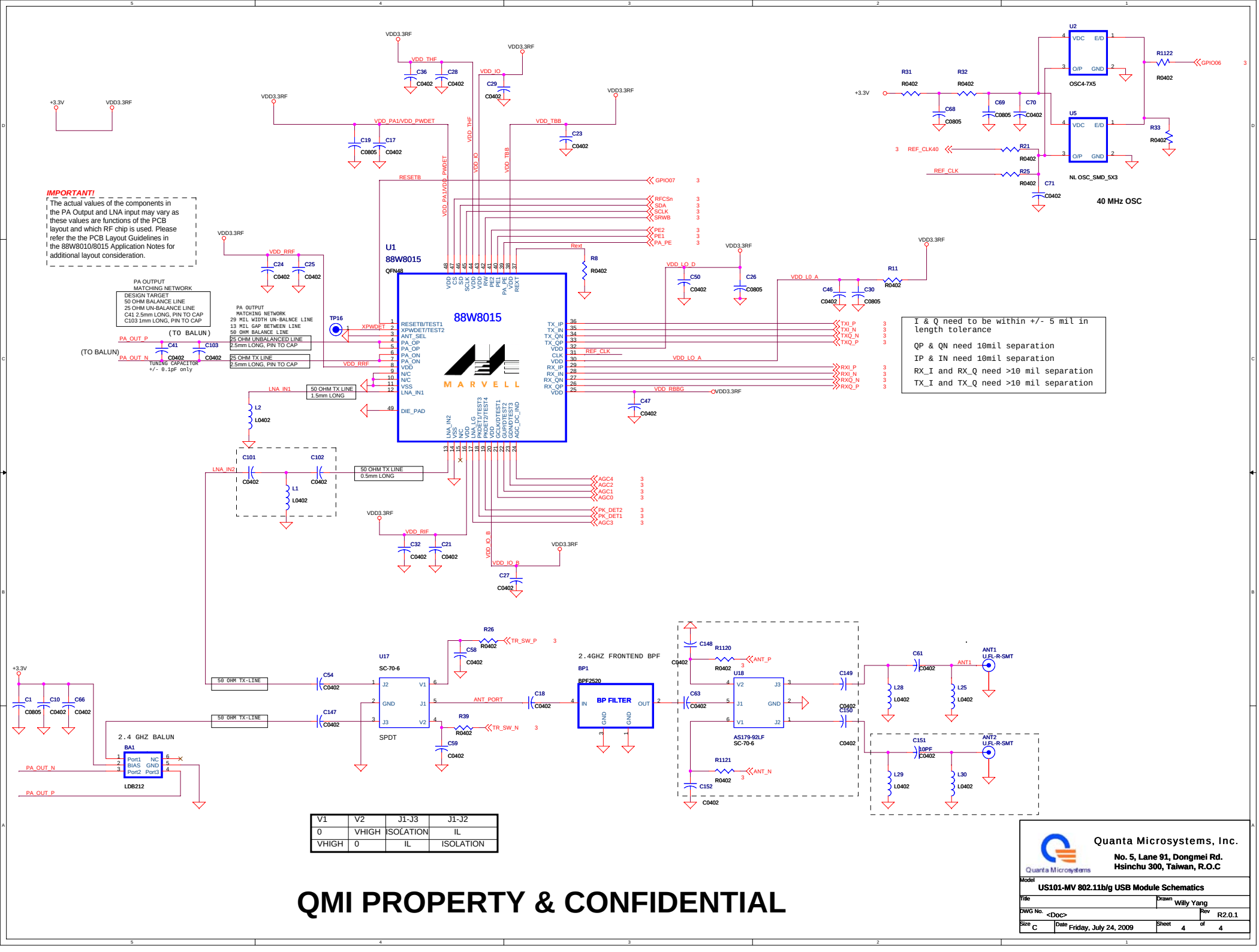
IMPORTANT!
The actual values of the components in the PA Output and LNA input may vary as these values are functions of the PCB layout and which RF chip is used. Please refer the the PCB Layout Guidelines in the 88W8010/8015 Application Notes for additional layout consideration.
U1
88W8015
QFN48
88W8015
MARVELL
PA OUTPUT MATCHING NETWORK
DESIGN TARGET
50 OHM BALANCE LINE
25 OHM UN-BALANCE LINE
C41 2.5mm LONG, PIN TO CAP
C103 1mm LONG, PIN TO CAP
(TO BALUN)
PA OUTPUT MATCHING NETWORK
29 MIL WIDTH UN-BALNCE LINE
13 MIL GAP BETWEEN LINE
50 OHM BALANCE LINE
25 OHM UNBALANCED LINE
2.5mm LONG, PIN TO CAP
25 OHM TX LINE
2.5mm LONG, PIN TO CAP
TUNING CAPACITOR
+/- 0.1pF only
I & Q need to be within +/- 5 mil in length tolerance
QP & QN need 10mil separation
IP & IN need 10mil separation
RX_I and RX_Q need >10 mil separation
TX_I and TX_Q need >10 mil separation
40 MHz OSC
OSC4-7X5
NL OSC_SMD_5X3
2.4GHZ FRONTEND BPF
BP FILTER
2.4 GHZ BALUN
LDB212
SPDT
SC-70-6
AS179-92LF
50 OHM TX-LINE
50 OHM TX LINE
1.5mm LONG
0.5mm LONG
V1 V2 J1-J3 J1-J2
0 VHIGH ISOLATION IL
VHIGH 0 IL ISOLATION
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