FCC ID: XJO8970006

Technical Description:

This Power Sensor is a transceiver operating at a single frequency: 2.457GHz. It operates in conjunction with the Bike Console and the Bike Speed Sensor. It reads the angle data from the angle sensor and receives speed data from the Bike Speed sensor. It computes the power and transmits the data to the Bike console.

The brief circuit description is listed as follows:

- U1 and associated circuit act as Voltage Regulator.
- U4 and associated circuit act as 3D Sensor.
- U2 and associated circuit act as Microprocessor.
- Module ANT11TS33M4IB act as 2.4GHz Transmitter, Receiver, Antenna, Modulator and Demodulator.

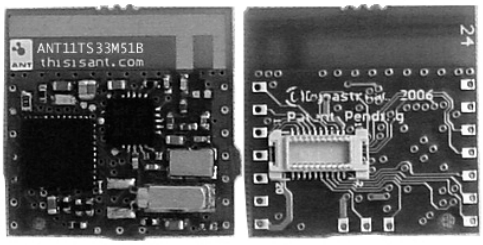
Antenna Used:

Internal, Integral on board antenna

ANT11Txx3MxIB
RF Transceiver Module

FEATURES

- 2.4GHz worldwide ISM band
- 20mm x 20mm drop-in module
- SensRcore™ development platform
- Ultra-low-power operation
- Simple sync/async serial interface
- Integrated F antenna
- Broadcast, acknowledged, or burst data transmissions
- Message rates 0.5Hz - 200Hz (8byte data payload)
- Burst transfer rates up to 20Kbps (true data throughput)
- 1 Mbit/sec RF data rate
- Up to 1/4/8 ANT channels
- 125 selectable RF channels
- Up to 3 public, managed and/or private networks
- 1.8V to 3.6V supply voltage range
- -40°C to +85°C operating temperature
- FCC test ready
- RoHS Compliant



FAMILY MEMBERS

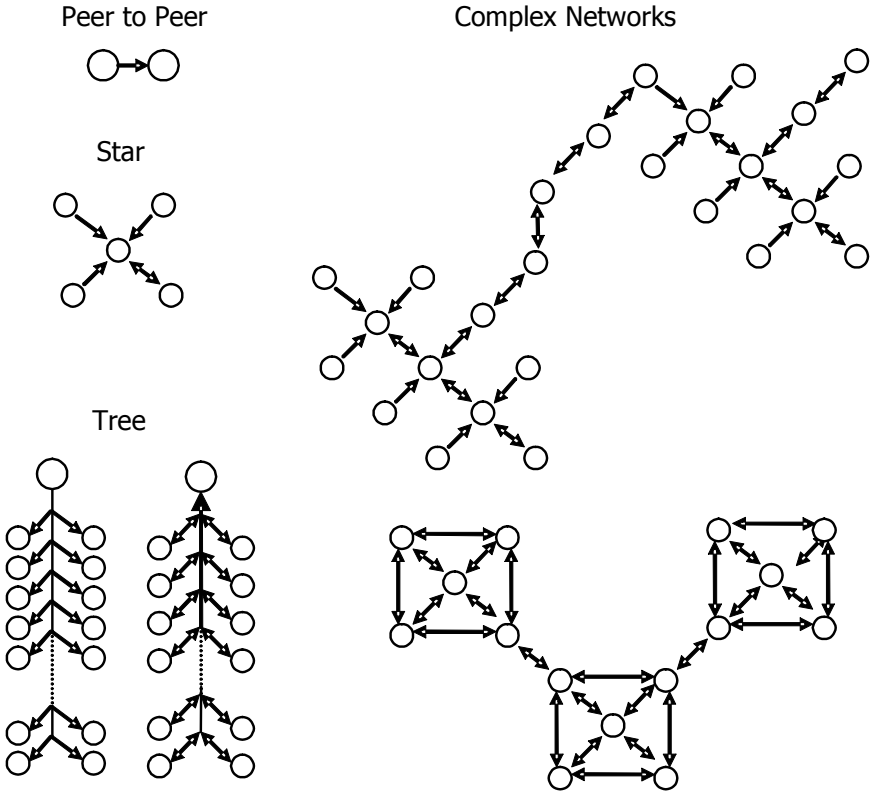
ANT11TS33M4IB / ANT11TS33M5IB
8 ANT ch, SensRcore™ with 8 data ch

ANT11TS53M4IB / ANT11TS53M5IB
4 ANT ch, SensRcore™ with 6 data ch

ANT11TS63M4IB / ANT11TS63M5IB
1 ANT ch, SensRcore™ with 4 data ch

ANT11TR13M4IB / ANT11TR13M5IB
8 channel

ANT NETWORK CONFIGURATIONS



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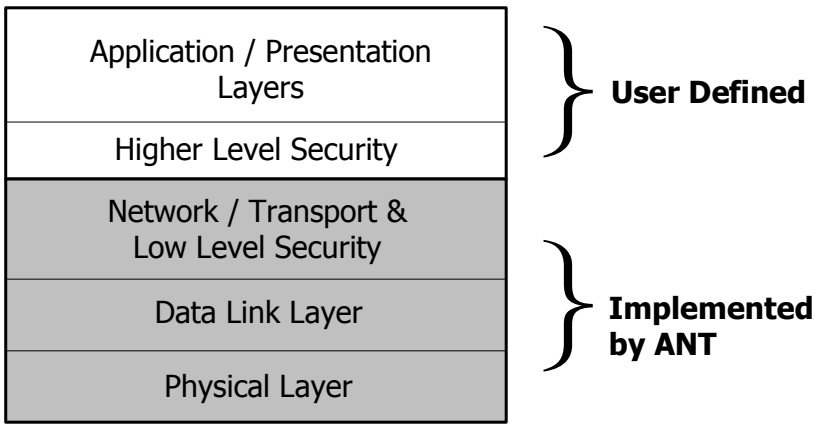
ANT Overview

Dynastream's ANT technology provides a low-latency, wireless communications protocol solution between multiple devices in a Personal Area Network configuration. ANT's benefits of low power, low cost, and small physical size provide an ideal platform for a wide range of sensor, monitoring, and control applications.

A low-overhead protocol, ANT provides wireless protocol capability with a very low component cost, enabling the growth of wireless in low-cost application environments. ANT supports private and public network architectures with 2^{32} uniquely addressable devices possible, ensuring that each device can be uniquely identified from another in the same network or from devices of other wireless PAN providers. Moreover, ANT incorporates several built-in features that provide the host application with transmission options and immunity from cross-talk to ensure reliable communication of data.

ANT provides carefree handling of the Physical, Network, and Transport OSI layers. In addition, it incorporates key low-level security features that form the foundation for user-defined, sophisticated, network-security implementations. ANT ensures adequate user control while considerably lightening computational burden in providing a simple yet effective wireless networking solution.



The Dynastream ANT RF modules encompass the complete protocol stack coupled with a 2.4GHz radio transceiver to provide a drop-in wireless solution for a host application processor. The modules are 100% RF tested by Dynastream for compliance with FCC regulations.

Dynastream's ANT product technology is available in a number of formats to suit a wide variety of application needs. In addition to the Dynastream ANT dual-chip chipsets, RF modules, Development Kits, and USB dongles, it is available in single-chip integrated form as the nRF24AP1 from Nordic Semiconductor.

A complete description of the ANT message protocol is found in the ANT Message Protocol and Usage document. The serial interface details are provided in the Interfacing with ANT General Purpose Chipsets and Modules document.

1 SensRcore™ Platform

Both analog and digital sensors can be directly connected to the ANT microcontroller (MCU) when configured to operate in SensRcore mode. The channel configuration parameters are stored in non-volatile memory and are enabled upon power-up. A full wireless sensor device can be created with its major components comprised of the sensor, the ANT protocol MCU, and the ANT radio. This application eliminates the need for a host MCU to transfer sensor inputs to the wireless system; the component cost, size, and power of the target sensor device are reduced.

When I/O pins are configured as digital inputs or outputs, the electrical requirements are the same as all other signaling pins. When I/O pins are configured as analog inputs, different signal ranges can be selected with different reference voltages. The reference voltages available are V_{DD}, 2.5V, and 1.5V. Signals that exceed the specified reference level will be read by the A/D as a maximum value. Signal levels should not exceed V_{DD}. Each AIOx pin can be used as an analog input or a digital I/O pin; each IOx pin can be used only as a digital I/O pin.

I/O pins that are not being used in a specific SensRcore mode configuration should be left configured as digital inputs, which is the default setting.

2 Pin Assignment

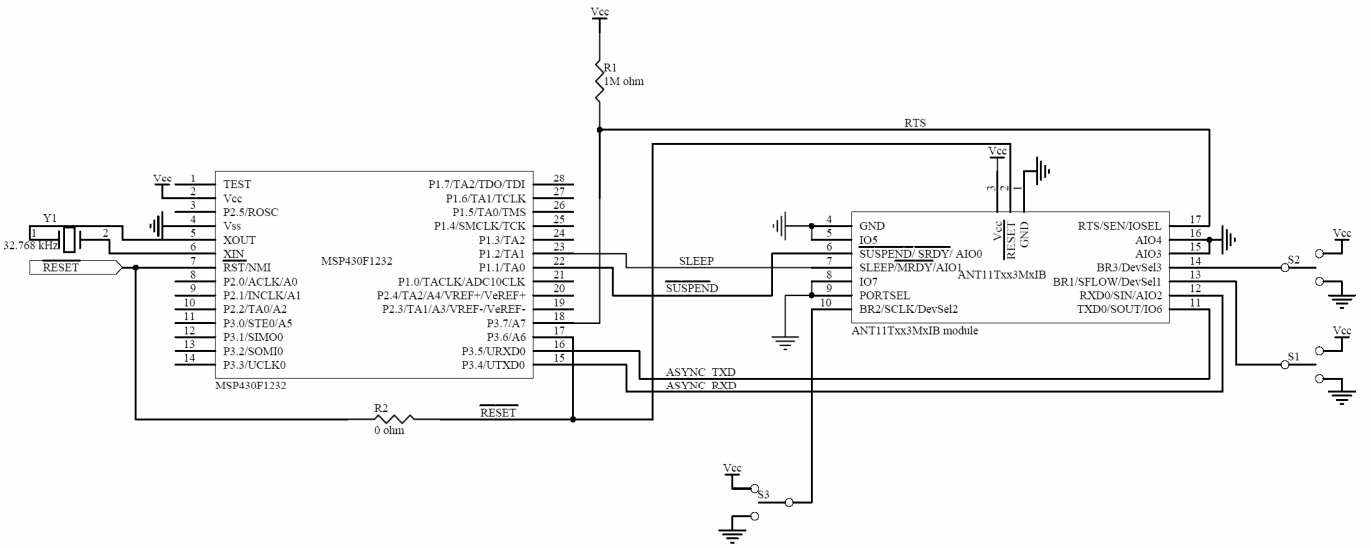
The ANT11Txx3MxIB module contains a dual-chip ANT implementation. The ANT MCU contains the ANT protocol stack along with the ANT serial interface. The radio chip is Nordic Semiconductor's nRF24L01. The module may be connected to the user's host controller using the 17 pin-out assignment (surface mount) style or the 20-pin Molex header connection style provided below:

Surface Mount Pin #s	Molex- 20-pin header	Pin Name	Async Mode	Sync Mode	SensRcore Mode	Description
1	6	TIE_GND1	GND	GND	GND	Not used, must be tied to ground
2	10	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	Active low Reset pin
3	1	Vcc	Vcc	Vcc	Vcc	Power Supply Source
4	19	TIE_GND2	Tie to GND	Tie to GND	Tie to GND	
5	8	IO5	Tie to GND	Tie to GND	IO5	SensRcore Mode ->Digital Input/Output
6	17	$\overline{\text{SUSPEND}}$ / $\overline{\text{SRDY}}$ /AIO0	$\overline{\text{SUSPEND}}$	$\overline{\text{SRDY}}$	AIO0	ASync -> Suspend control Sync -> Serial Port Ready Mode ->Analog/Digital Input Output
7	15	SLEEP/ $\overline{\text{MRDY}}$ /AIO1	SLEEP	$\overline{\text{MRDY}}$	AIO1	Async -> Sleep Mode Enable Sync -> Message Ready indication SensRcore Mode ->Analog/Digital Input Output
8	13	IO7	Tie to GND	Tie to GND	IO7	SensRcore Mode ->Digital Input/Output
9	11	PORTSEL	PORTSEL (Tie to GND)	PORTSEL (Tie to Vcc)	Tie to GND	Asynchronous or Synchronous port select
10	7	BR2/SCLK/ DevSel2	BR2	SCLK	DevSel2	Async->Baud Rate Selection Sync->Clock Output Signal SensRcore Mode ->Configuration selection
11	4	TXD0/SOUT/ IO6	TXD0	SOUT	IO6	Async->Transmit Data Signal Sync ->Data Output SensRcore Mode -> Digital Input/Output
12	3	RXD0/SIN/AIO2	RXD0	SIN	AIO2	Async -> Receive Data Signal Sync-> Data Input SensRcore Mode ->Analog/Digital Input Output
13	5	BR1/SFLOW/ DevSel1	BR1	SFLOW	DevSel1	Async->Baud Rate Selection Sync->Bit or Byte flow control select SensRcore Mode ->Configuration selection
14	9	BR3/DevSel3	BR3	Tie to GND	DevSel3	Async->Baud Rate Selection Sync-> Tie low SensRcore Mode ->Configuration selection
15	14	AIO3	Tie to GND	Tie to GND	AIO3	SensRcore Mode ->Analog/Digital Input Output
16	12	AIO4	Tie to GND	Tie to GND	AIO4	SensRcore Mode ->Analog/ Digital Input Output
17	2	RTS/SEN/IOSEL	RTS	SEN	IOSEL (Tie to GND)	Async->Request to Send Sync-> Serial Enable Signal SensRcore Mode ->IOSEL Tie low
	16, 18, 20	NC	NC	NC	NC	No Connection

3 Sample Designs

Samples 3.1, 3.2, and 3.3 show the proper electrical connectivity of an ANT11TxxxMxIB module to an application's host microcontroller. The three reference designs use the 17 pin-out assignment connection style.

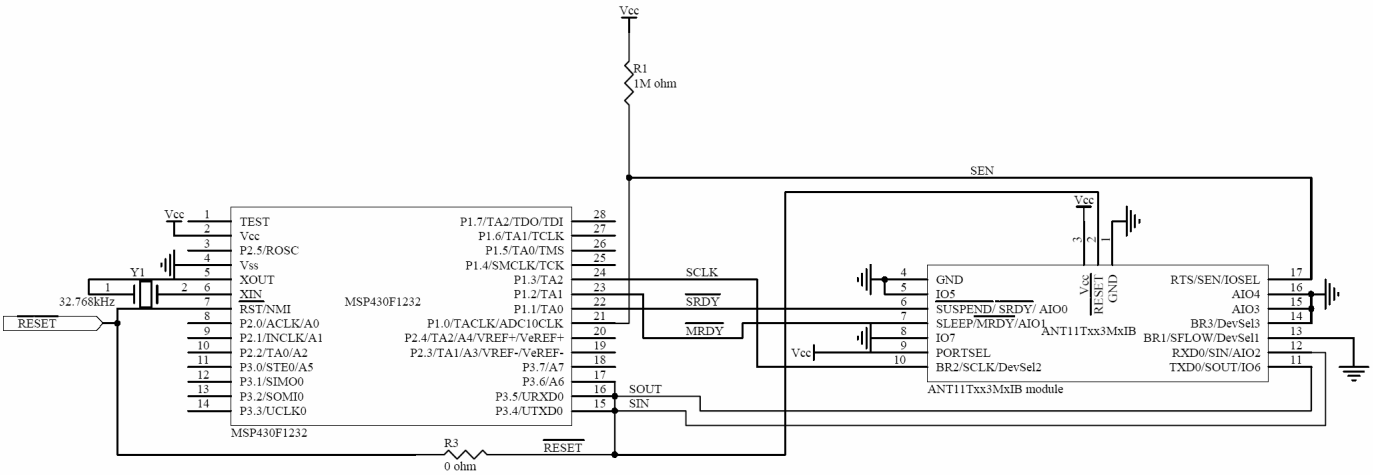
3.1 **Async Mode**



Notes:

- Module RXD and TXD connected directly to hardware USART of microcontroller.
- The illustrated switches on the baud rate selection pins (BR1, BR2, and BR3) are for ease of use only. The Baud rate selection pins may be connected directly to the logic level of interest.
- R2 allows optional control of the module $\overline{\text{RESET}}$ signal by a microcontroller I/O pin.

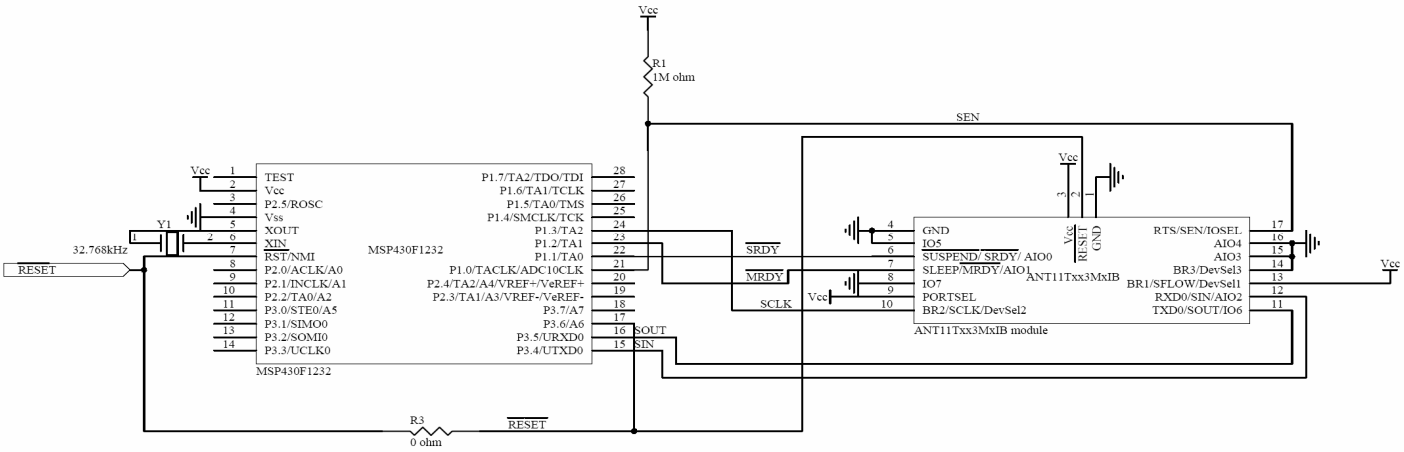
3.2 **Byte Sync Mode**



Notes:

- Module SOUT and SIN connected directly to hardware USART of microcontroller.
- SCLK and SEN need to be on interrupt-capable I/O pins on the microcontroller.
- R3 allows optional control of the module $\overline{\text{RESET}}$ signal by a microcontroller I/O pin.

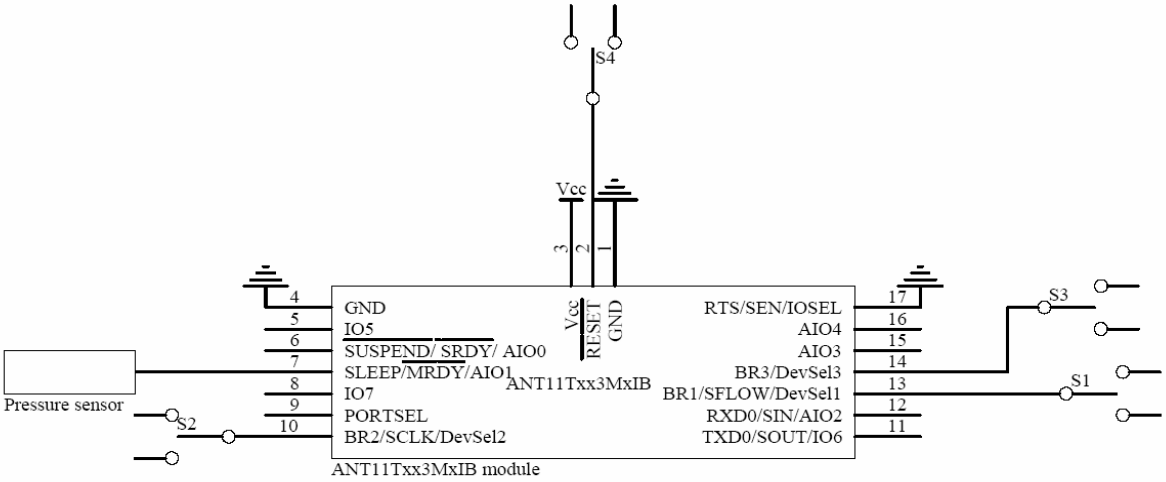
3.3 Bit Sync Mode



Notes:

- All interface signals are connected directly to I/O pins on the microcontroller.
- SCLK and SEN need to be on interrupt-capable I/O pins on the microcontroller.
- R3 allows optional control of the module $\overline{\text{RESET}}$ signal by a microcontroller I/O pin.

3.4 SensRcore™ Mode (pressure sensor configuration)



4 Electrical Specifications

Absolute Maximum Ratings	
Voltage applied at Vcc to Vss	-0.3V to +3.6V
Input Voltage at any pin	-0.3V to Vcc +0.3V
Diode Current at any pin	±2mA
Operating Temperature	-40°C to +85°C
Storage Temperature	-40°C to +105°C

Note: Stress exceeding one or more of the absolute maximum ratings may cause permanent damage to the chipsets.

Conditions: VDD = +2.0V, VSS = 0V, T_A = - 40°C to +85°C

Symbol	Parameter (condition)	Notes	Min	Typ	Max	Units
	Operating conditions					
VDD	Supply voltage		2.2	3.0	3.6	V
TEMP	Operating temperature		-40	25	+85	ºC
	Digital input pin					
V_{IH}	HIGH level input voltage		1.9		VDD	V
V_{IL}	LOW level input voltage		Vss			V
	Digital output pin					
V_{OH}	HIGH level output voltage (I_{OH}=-0.5mA)		VDD-0.25		VDD	V
V_{OL}	LOW level output voltage (I_{OL}=0.5mA)		Vss		0.25	V
	Analog input pin					
V_{Analog}	Input voltage range	4)	Vss		VDD	V
F_{Sample}	Sample rate	5)	0.002		500	Sample/s
	Counter input pin					
$F_{Counter}$	Input frequency				1000	Hz
	Synchronous serial timing					
sclk freq.	Synchronous clock frequency (byte mode)		285	300	315	kHz
$t_{ReadValid}$	Data is valid on read before low-to-high transition on the clock (byte mode)		0.5			µs
$t_{WriteValid}$	Data must be valid on write within this time after a high-to-low transition on the clock (byte mode)				2	µs
$t_{SRDY\ MinLow}$	Minimum $\overline{SRDY}$ low time		2.5			µs
t_{Reset}	Synchronous Reset. $\overline{SRDY}$ falling edge to $\overline{MRDY}$ falling edge		250			µs
	General RF conditions					
f_{OP}	Operating frequency	1)	2400		2524	MHz
$F_{CHANNEL}$	Channel spacing			1		MHz
Δf	Frequency deviation			±156		kHz

Symbol	Parameter (condition)	Notes	Min	Typ	Max	Units
	Current consumption					
I_{Idle}	No active channels – no communications			1.1		µA
$I_{Suspend}$	Asynchronous suspend activated			1.1		µA
I_{Base}	Base active current			2.6		µA
I_{sample}	Average current/analog sample			0.5		µA
I_{SC_RF}	Average current/ ANT message in sensRcore mode			13		µA
$I_{Msg\ Rx\ Byte\ Sync}$	Average current / Rx message in byte sync mode			10.5		µA
$I_{Msg\ Rx\ BitSync}$	Average current / Rx message in bit sync mode			13.1		µA
$I_{Msg\ Rx\ 57600}$	Average current / Rx message in Async mode at 57 600 baud			9.1		µA
$I_{Msg\ Rx\ 19200}$	Average current / Rx message in Async mode at 19 200 baud			10.4		µA
$I_{Msg\ Rx\ 4800}$	Average RF current / Rx message in Async mode at 4800 baud			8.5		µA
$I_{Msg\ Tx\ Byte\ Sync}$	Average current / Tx-only message in byte sync mode			6.4		µA
$I_{Msg\ Tx\ BitSync}$	Average current / Tx-only message in bit sync mode			10.8		µA
$I_{Msg\ Tx\ 57600}$	Average current / Tx-only message in Async mode at 57 600 baud			5.7		µA
$I_{Msg\ Tx\ 19200}$	Average current / Tx-only message in Async mode at 19 200 baud			7.5		µA
$I_{Msg\ Tx\ 4800}$	Average current / Tx-only message in Async mode at 4800 baud			4.4		µA
$I_{Msg\ TR\ Byte\ Sync}$	Average current / Tx message in byte sync mode			14.1		µA
$I_{Msg\ TR\ BitSync}$	Average current / Tx message in bit sync mode			18.4		µA
$I_{Msg\ TR\ 57600}$	Average current / Tx message in Async mode at 57 600 baud			13.5		µA
$I_{Msg\ TR\ 19200}$	Average current / Tx message in Async mode at 19 200 baud			15.0		µA
$I_{Msg\ TR\ 4800}$	Average current / Tx message in Async mode at 4800 baud			11.7		µA
$I_{Msg\ Ack\ ByteSync}$	Average current / Acknowledged message in byte sync mode			19.6		µA
$I_{Msg\ Ack\ Bit\ Sync}$	Average current / Acknowledged message in bit sync mode			23.4		µA
$I_{Msg\ Ack\ 57600}$	Average current / Acknowledged message in Async mode at 57 600 baud			18.7		µA
$I_{Msg\ Ack\ 19200}$	Average current / Acknowledged message in Async mode at 19 200			19.9		µA

Symbol	Parameter (condition)	Notes	Min	Typ	Max	Units
	baud					
$I_{Msg\ Ack\ 4800}$	Average current / Acknowledged message in Async mode at 4800 baud			17.2		µA
I_{Peak}	Peak Current consumption			19		mA
I_{PeakTx}	Peak Current – Tx-only @ 0dBm			13		mA
I_{Ave}	Broadcast Tx-only @ 0.5Hz in byte sync mode			5.8		µA
I_{Ave}	Broadcast Tx-only @ 2Hz in byte sync mode			15.4		µA
I_{Ave}	Broadcast Rx @ 0.5Hz in byte sync mode			7.8		µA
I_{Ave}	Acknowledged @ 0.5Hz in byte sync mode			12.4		µA
I_{Ave}	Burst continuous @ 14Kbps in byte sync mode			2.24		mA
I_{Ave}	Burst continuous @ 20Kbps in byte sync mode			3.21		mA
I_{Ave}	Burst continuous @ 10Kbps in bit sync mode			3.22		mA
I_{Ave}	Burst continuous @ 14Kbps in Async mode at 57 600 baud			2.37		mA
I_{Ave}	Burst continuous @ 20Kbps in Async mode at 57 600 baud			3.31		mA
	Transmitter operation					
P_{RF}	Maximum output power	2)		0	4	dBm
ΔP	Output power variation	3)			± 4	dBm
P_{BW}	20dB bandwidth for modulated carrier				1000	kHz
P_{RF2}	2nd adjacent channel transmit power 2MHz				-20	dBm
P_{RF3}	3rd adjacent channel transmit power 3MHz				-40	dBm
I_{VDD}	Supply peak current @ 0dBm output power			11.3		mA
I_{VDD}	Supply peak current @ -20dBm output power			7		mA
	Receiver operation					
I_{VDD}	Supply peak current receive mode			12		mA
RX_{SENS}	Sensitivity at 0.1%BER (@1000kbps)			-85		dBm
C/I_{CO}	C/I co-channel			9		dB
C/I_{1ST}	1st adjacent channel selectivity C/I 1MHz			8		dB
C/I_{2ND}	2nd adjacent channel selectivity C/I 2MHz			-22		dB
C/I_{3RD}	3rd adjacent channel selectivity C/I 3MHz			-30		dB

1) Usable band is determined by local regulations.
2) Maximum output power with 0dBm output power setting.