OZMO2000

Single-chip ultra-low power Wi-Fi Direct solution

Datasheet v1.2 – June 2012

1 General Description

The OZMO2000 is a single-chip, fully integrated radio, baseband, and microcontroller System-on-Chip (SoC) bringing Wi-Fi CERTIFIED™ Wi-Fi Direct technology to cost and power sensitive peripheral devices.

Building on the ground-breaking OZMO1000, the OZMO2000 offers higher data rates, more extensive application interfaces, additional memory, hardware crypto accelerators, an integrated power amplifier, an audio PLL and a low-power RCO sleep timer.

Dual-band radio design allows seamless interoperability with Ozmo-enabled IEEE802.11a/b/g/n hosts.

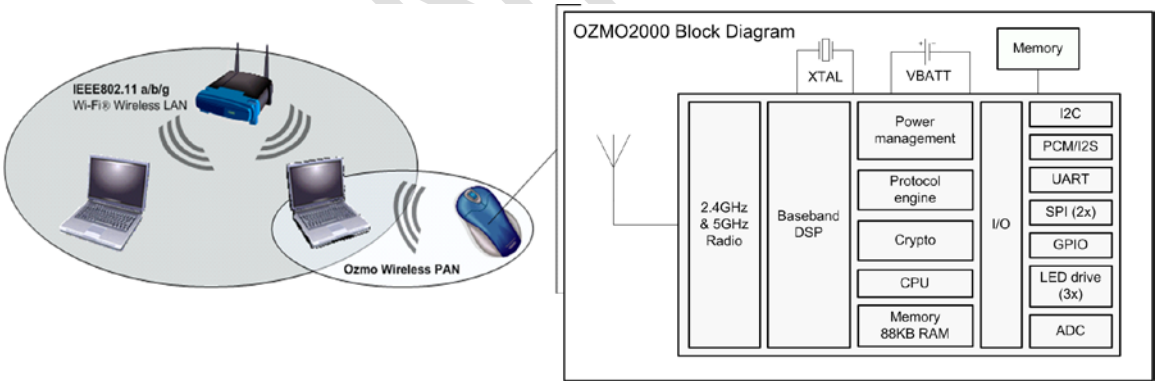
Application programmable low-power states and fast power up algorithms make the OZMO2000 ideally suited for long-lasting battery-powered peripheral applications.

The OZMO2000 connects to external controllers, sensors, buttons, LEDs and flash memory.

The OZMO2000 audio interface subsystem includes an audio PLL and a flexible digital audio interface block, making it ideally suited for interfacing to external audio codec and signal processing devices.

The provided software runs on a power-efficient R8051XC core, is compatible with Wi-Fi CERTIFIED™ Wi-Fi Direct and Windows 7 SoftAP host systems, and optionally provides application support for various peripheral devices.

2 Block diagram



3 Applications

- Cordless Human Interface Devices (HID)
  - Mouse
  - Keyboard
  - Game controller
  - Remote control
- Cordless Audio Devices
  - Stereo gaming headset
  - Stereo headphones
  - Stereo speakers
  - Mono & stereo microphones
- Smart energy/Wireless sensors
- Low power wireless bridge devices

4 Benefits

- Reduced system cost thanks to high level of integration and elimination of host dongle.
- On-chip 8051 processor eliminates need for external micro-controller in most applications.
- Flexible application interfaces, including 2 independent SPI master/slave interfaces, UART, I2C, PCM/I2S, GPIOs, 3 LED drivers with PWM support and a General-Purpose ADC.
- Long battery life thanks to low power radio and systems design.
- Low latency thanks to agile systems architecture and fast wake up algorithms.
- Available in 7x7mm 56-pin QFN package.

5 Features

- Patented and patent-pending technology
- Dual band 2.4GHz or 5GHz operation
- Supports all mandatory IEEE802.11 a/b/g rates
  - 1-11 Mbps 802.11b
  - 6-24 Mbps 802.11a/g
- Built-in support for over-the-air firmware upgrades
- Compatible with
  - Wi-Fi CERTIFIED™ Wi-Fi Direct
  - Windows7 Certified host systems leveraging SoftAP functionality
  - Intel Centrino2 MyWiFi Technology
  - Ozmo host dongle
- Support for PIN and push-button easy pairing based on Wi-Fi® Protected Setup (WPS)
- Flexible differential or single-ended antenna input
- Internal 50Ω input matching
- 1.8V – 3.6V single-supply
- On-chip LDOs and power management engine
- Integrated Power Amplifier configurable for extended battery-life or maximum Tx power
- Optionally configurable for use with external PA and LNA.
- Low power sleep timer
- Power-efficient CPU subsystem with
  - on-board R8051XC processor
  - 56 kBytes of code/data RAM
  - 32 kBytes of buffer RAM
  - 8 kBytes of ROM
- Hardware crypto accelerators
- Native 128-bit AES encryption
- Integrated audio PLL
- Flexible application interface block
  - I2C, UART, GPIO and 2 SPI master/slave
  - 3 LED drivers with PWM
  - 8-bit General Purpose ADC
  - PCM/I2S digital audio interface

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6 Functional Block Diagram

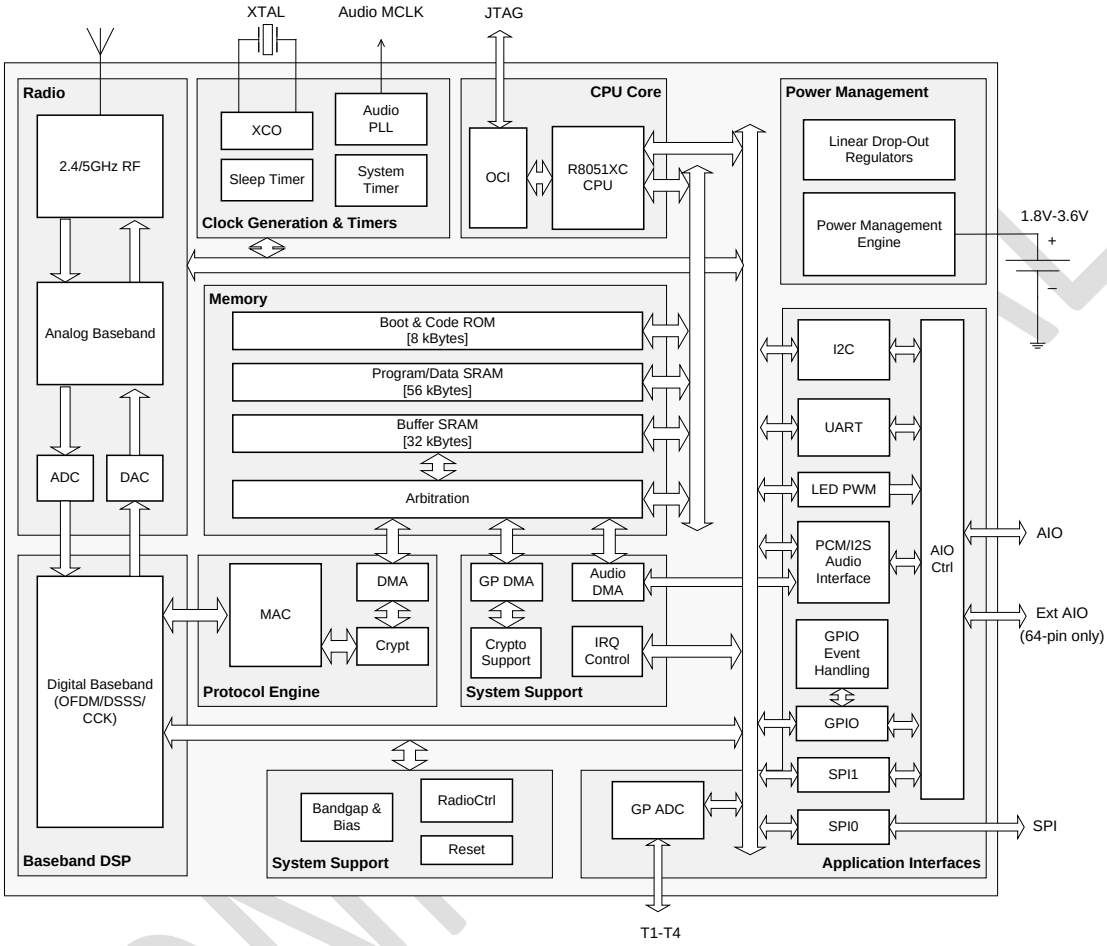


Figure 1: OZMO2000 Functional block diagram

7 Description of Functional Blocks

7.1 RF Transceiver

The OZMO2000 utilizes a dual band transceiver that is low power and has fast turn-on times. The differential input receiver includes on-chip matching, amplification, filtering, and analog to digital conversion of I and Q signals. The differential input is shared with the differential output of the transmitter. The transmitter includes the digital to analog conversion function, filtering, and power amplifier.

7.2 Baseband and Logic

7.2.1 Physical Layer Hardware Engine DSP

The OZMO2000 supports Orthogonal Frequency-Division Multiplexing (OFDM) – Binary Phase-Shift Key (BPSK) and Quadrature Phase-Shift Key (QPSK) as well as Direct Sequence Spread Spectrum (DSSS) and Complementary Code Keying (CCK) modulation schemes. These schemes ensure high transmission reliability, even in the presence of severe channel conditions like multi-path and narrowband interference. Furthermore, the support for these modulation schemes makes the OZMO2000 compatible with the modulation schemes specified for 6, 9, 12, 18, and 24Mbps data rates in IEEE802.11g and IEEE802.11a and 1, 2, 5.5, and 11Mbps data rates in IEEE802.11b.

7.2.2 Protocol Engine (MAC & Crypt)

The hardware protocol engine enables rapid frame checking/decoding and a turnaround time between reception and transmission that meets the IEEE802.11 Short Inter-Frame Space (SIFS) requirement.

For transmitted frames the following actions occur:

- The data is extracted from buffer RAM using DMA
- A timestamp may be inserted
- If encryption is enabled the MIC is computed and appended to the frame and the contents are encrypted using AES/CCM
- The FCS is computed and added
- The PLCP header is computed and pre-pended on the frame

Upon receipt of a frame the protocol engine performs the following actions:

- PLCP header checked for rate and checksum and length extracted
- Frame Check Sequence (FCS) is verified
- Target MAC address is verified
- If encryption is active for the frame, the frame is decrypted and the Message Integrity Code (MIC) computed using AES/CCM protocol as used in IEEE802.11
- Frame contents are copied to buffer RAM using DMA

The protocol engine can automatically format and transmit control frames in response to a reception observing the IEEE802.11 SIFS timing.

The MAC protocol engine is coupled to the power management states of the OZMO2000 and ensures efficient use of power only as required.

7.2.3 Power Management

There are seven hardware power states in the OZMO2000 as shown in Figure 2. There are two active states (Transmit and Receive) and five low power states (Standby, Doze, Dream, Sleep and Deep Sleep). The OZMO2000 uses a combination of clock gating, aggressive power down schemes and multiple power domains controlled by dedicated regulators to achieve low power consumption in any given power state.

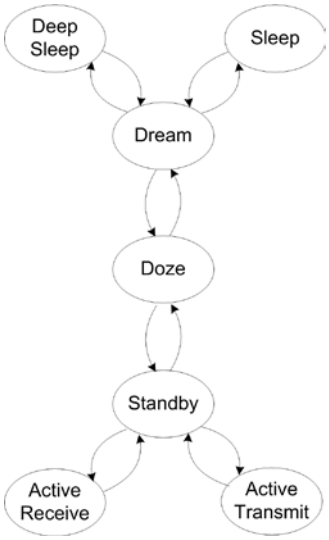


Figure 2: OZMO2000 supported power states

- The Active states are the highest power states. All power domains are active in these states, and all blocks required for either transmit (Active-transmit state) or receive (Active-receive state) are powered up.
- In the various low-power states, more and more of the on-chip circuitry is shut-down, but in a way which can be recovered quickly. In it's lowest-power state the OZMO2000 consumes only 2uA, but retains the necessary data so that a connection can be quickly resumed.

Which power states are triggered and how much time is spent in a particular power state depends on the connectivity states of the peripheral device. More details on the connectivity states and how this translates to system battery life for a particular peripheral device application can be found in the appropriate Application Notes.

7.3 Microcontroller

The OZMO2000 contains an embedded CPU core that provides the processing platform for peripheral device application and protocol software. The CPU core is an R8051XC. This is based on the Intel® MCS51 instruction set with enhanced performance and capability compared to a standard 80C51; a CPU cycle is one clock compared to twelve clocks for the 80C51. A further processor architectural enhancement is the provision of multiple auto-incrementing Data Pointer (DPTR) registers which dramatically increase the efficiency of processor-based data transfer. In addition, the OZMO2000 has a number of specialized arithmetic functions to assist in the cryptographic requirements of key generation. The R8051XC core is a Harvard architecture with separate code and data memory.

7.4 Memory

88Kbytes of on-chip RAM is provided to support the CPU. This memory space is shared between program, data and buffer memory. The buffer memory and program/data memory can be accessed simultaneously so that the processor is not delayed by DMA transfers. At reset, on-chip ROM can download code from an external serial Flash device to program memory.

7.5 Application Interfaces

The OZMO2000 IC has a flexible I/O block offering the following digital application interfaces:

- 16 I/O pins that can be configured to perform one of the following interface functions:
    - I2C
    - Synchronous/Asynchronous Serial (UART)
    - SPI master/slave
    - PCM/I2S audio interface
    - LED PWM interface
    - General Purpose I/O (GPIO) that may be configured as inputs or outputs

The I/O configuration block enables software to map the 16 application I/O pins (AIO0 – AIO15) to either general purpose I/O, to one of the serial interfaces, or to the audio interface. Software sets the I/O configuration via registers in the I/O configuration block. Each of the I/O pins can be mapped to the default function, or to one of two alternative functions to simplify application PCB layout. A high or low output current drive can be selected as well as enabling internal pull-ups or pull-downs on GPIO inputs.

Software may reconfigure AIO0 – AIO2 to drive LEDs as an alternate function. In this mode these pins act as open drain outputs.

- A dedicated SPI interface for loading of the program memory from an external memory device. This interface is in addition to the SPI interface that can be configured through the 16 I/O pins. The SPICLK, SPIMISO and SPIMOSI pins are dedicated SPI interface signals that on a hardware reset enable the program memory to be loaded from an external serial Flash device. The chip select for this device is also on a dedicated pin (SPIBOOTCS).

- An auxiliary output pin, AUXO. This can be assigned to one of four output functions:
    - General Purpose output
    - External regulator control (default at reset)
    - CLKOUT signal
    - UART TxD

- An audio master clock output, AUDIOCLK.

In addition to a flexible digital application interface block, OZMO2000 also offers access to a General-Purpose Analog-to-Digital Converter (ADC), which is accessible through any one of the analog test I/Os, T1-T4.

7.5.1 I2C

The I2C interface provides a bus controller that meets the Philips I2C™ specification.

I2C is a synchronous serial bus that uses a two-wire interface for communication: serial clock (SCL) and serial data (SDA). The bus is a multi-master bus supporting several attached devices. The I2C bus controller supports master-transmit, master-receive, slave-transmit, and slave-receive operating modes. The data transfer rate may be up to 400kbps (I2C fast mode).

7.5.2 UART

The UART interface provides a flexible full-duplex UART and baud rate generator supporting four modes of operation:

- 8-bit synchronous transmitter/receiver with a fixed baud rate related to the CPU clock.
- 8-bit asynchronous transmitter/receiver with programmable baud rate.
- 9-bit asynchronous transmitter/receiver with a fixed baud rate related to the CPU clock.
- 9-bit asynchronous transmitter/receiver with programmable baud rate.

7.5.3 SPI Master/Slave

The OZMO2000 supports two SPI interfaces. One dedicated SPI interface (“SPI0”) and one SPI interface that can be configured through the I/O block (“SPI1”).

Each SPI interface is a full duplex synchronous serial interface using four physical signals for communication: SPI clock (SPICLK), master to slave data (SPIMOSI), slave to master data (SPIMISO) and a device chip select (SPICSn).

Each block can be configured in one of two modes:

- SPI master; where the interface provides the serial clock and chip select, or
- SPI slave; where the serial clock and chip select become inputs driven by a master.

Up to four chip select signals are available when the device is operating as a master, depending on I/O block configuration. SPI chip select 0 of the dedicated SPI interface is mapped to the external SPIBOOTCS signal and is reserved for the SPI external Flash that is used for non-volatile code storage.

The SPICLOCK is set by a programmable divider based on either the crystal clock (f_{xo}) or PLL clock (f_{PLL}); selection being based on the setting of an internal configuration register. The maximum SPICLOCK frequency is $f_{xo}/2$ or $f_{PLL}/2$ when writing in master mode and $f_{xo}/4$ when reading or writing in slave mode.

7.5.4 PCM/I2S Audio Interface

The digital audio interface is a flexible PCM/I2S port suitable for connection to external audio codec devices. The interface supports:

- PCM and I2S interface formats.
- 8 or 16 bit audio word length.
- Sample clock generation for common audio sample rates, e.g. 8 kHz or 44.1kHz.
- Support of different sample rates for audio input and output.
- Long or short frame synchronization signal in PCM mode.

The digital audio interface may be configured to use either PCM or I2S formats. The PCM interface mode is intended for simple interfacing to 'voice quality' codec devices; commonly 8 kHz 8-bit μ-law or A-law, or ≤16-bit linear encoding. The I2S interface mode is intended for simple interfacing to 'music quality' stereo audio devices. The digital audio interface format for I2S follows the Philips I2S™ specification.

The interface may be configured to operate as a master where the sample and bit clock signals are generated and output to the codec or as a slave where the audio bit clock and frame synchronization frequencies are input from the external codec.

An audio PLL enables the production of accurate audio clocks regardless of the XCO frequency. The audio master clock is available on a dedicated I/O pin, AUDIOCLK, in either master, or slave mode.

A two-channel DMA engine is used to transfer data between the audio interface and buffer memory.

7.5.5 LED PWM

The LED Pulse Width Modulation (PWM) block allows up to three LEDs to be controlled on AIO0-2; these could be separate LEDs, or elements of a multi-color LED. The intensity of each LED can be set independently using a PWM scheme. A simple pulse generator provides basic LED flash patterns.

The LED PWM block is driven from the core logic supply, and timing is derived from an internal timer clock.

The intensity of each LED is programmable using a PWM scheme with an adjustable on-time within a 12.288ms period. The on-time is set via an internal register, and is divided into 4096 linear 3μs steps (3μs to 12.288ms). This PWM control in conjunction with the LED enable bit enables the LED intensity to be adjusted from fully off to fully on.

The LED PWM block contains a simple pulse generator that can be used to flash one or more of the LEDs without having to produce a timed pattern using the processor. The pulse generator is able to generate one or two pulses approximately every one to nine seconds. Each pulse may be short or long. A short pulse is two PWM periods in length (24.576ms) and a long pulse is 24 PWM periods (~295ms) in length. When there are two pulses they are always separated by 24 PWM periods (~295ms).

7.5.6 GPIO

Any of the application I/O pins may be configured as a general purpose I/O signal. All pins default to GPIO inputs at reset with internal weak pull-up or pull down resistors.

AIO0-2 are 5V tolerant pins with 16mA drive capability and CMOS inputs (not Schmitt trigger). They can be configured as LED drivers.

AIO3-15, AIO16-23, SPI0 signals (including SPIBOOTCS) and AUXO are 4/8mA drive programmable. Note that the default drive strength following a reset for all AIOs and AUXO is 4mA. The SPI outputs default to 8mA drive strength.

7.5.7 General Purpose ADC

An 8-bit General Purpose ADC is accessible through the analog test I/Os, T1-T4. The ADC has a full scale input range from 155mV to 800mV and a conversion time of less than 10us. The ADC has a Differential Nonlinearity (DNL) of less than 0.5LSB. Without special manufacturing calibrations, the ADC achieves a +/-5% accuracy.

7.6 Firmware

Reference firmware is available to implement various peripherals based on the OZMO2000. This firmware provides a co-operative multitasking operating system with a deferred procedure call (DPC) interrupt structure and inter-process communication through semaphores. The firmware is layered so that the functions of link establishment and maintenance are self-contained. The application layer functions that control the peripherals are able to receive and send data without significant knowledge of the underlying protocol. The firmware is written mostly in the 'C' language but takes full advantage of the R8051XC extended functionality through some 8051 assembler sections.

Multiple images of firmware may be stored in the flash memory so that updating in the field is practical and safe. Furthermore, one image is dedicated to the "pre-paired" mode of operation and provides the extensive functions that enable secure pairing to occur. This includes Diffie-Hellman key computation, HMAC-256, SHA-256 and AES/CBC keywrap as used in the Wi-Fi® Protected Setup approach. The use of a separate "pre-paired" image means that the code overhead of these functions is not loaded unless required.

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

This is an ESD sensitive device. Take necessary precautions when handling.

Parameter	Min	Max	Units
Storage temperature	-40	+125	°C
Supply voltage: VBATT = VBATT1 = VBATT2 = VBATT3 = VDDIO	-0.3	3.6	V
VSS	-0.3	0.3	V
Input voltage: Digital I/O pins (except AIO0, AIO1, & AIO2)	-0.3	VBATT + 0.3	V
Input voltage: AIO0, AIO1, & AIO2	-0.3	5.0	V
RF Input Power		+20	dBm

8.2 Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating temperature	0		+70	°C
Supply voltage: VBATT = VBATT1 = VBATT2 = VBATT3 = VDDIO	1.8		3.6	V
VSS		0		V

8.3 Terminal Characteristics

VBATT = VBATT1 = VBATT2 = VBATT3 = VDDIO, T_A=25C

8.3.1 Digital I/O

Parameter	Conditions	Min	Typ	Max	Units
V_{IL}, input logic low	1.8 < VBATT < 3.6	-		0.3*VBATT	V
V_{IH}, input logic high	1.8 < VBATT < 3.6	0.7*VBATT		-	V
ΔV, input hysteresis			0.4		V
I_I, input resistance	Pull-up resistor to VBATT (see section 9 for which pins)		42		KΩ
I_I, input resistance	Pull-down resistor to VSS (see section 9 for which pins)		42		KΩ
V_{OL}, output logic low (max drive selected)	I_{OL} = 8 mA (AIO[15:3], AUDIOCLK, TDO, TSTSEL1, AUXO)			0.2*VBATT	V
V_{OL}, output logic low (max drive selected)	I_{OL} =16 mA (AIO[2:0])			0.2*VBATT	V
V_{OH}, output logic high (max drive selected)	I_{OH} = 8 mA (AIO[15:3], AUDIOCLK, TDO, AUXO)	0.8*VBATT			V
V_{OH}, output logic high (max drive selected)	I_{OL} = 16 mA (AIO[2:0])	0.8*VBATT			V
I_{OZ}, output tri-state current	0.0 V < V_0 < 3.6 V	-10		10	µA
C_I, input capacitance			3		pF
C_{IO}, input / output capacitance			3		pF

Terminal characteristics are guaranteed by design.

8.3.2 Crystal Oscillator

Parameter	Conditions	Min	Typ	Max	Units
Crystal frequency			24		MHz
Crystal tolerance	Manufacturing tolerance @Ta = 25C	-10		10	ppm
Crystal tolerance	Full temperature range, 0C < Ta < 70C	-10		10	ppm
Crystal tolerance	Full temperature range and manufacturing tolerance	-20		20	ppm
Xtal resonance resistance	24 MHz, fundamental mode		50	100	Ω
Xtal load capacitance			8		pF
Xtal input level			1.1		V

8.4 Power Consumption

Typical Peak Current at 25°C, 6Mbps operation

Parameter	Conditions	Min	Typ	Max	Units
I_{cc}, Active TX, Pout = 0dBm	2.45 GHz; VBATT = 1.8v		78		mA
I_{cc}, Active TX, Pout = -3dBm	5.20 GHz; VBATT = 1.8v		90		mA
I_{cc}, Active TX, Pout = 10dBm	2.45 GHz; VBATT = 1.8v		130		mA
I_{cc}, Active TX, Pout = 6dBm	5.20 GHz; VBATT = 1.8v		220		mA
I_{cc}, Active RX, listen[(2)]	2.45 GHz; VBATT = 3.6v		60		mA
	5.20 GHz; VBATT = 3.6v		62		mA
I_{cc}, Active RX, packet[(2)]	2.45 GHz; VBATT = 3.6v		70		mA
	5.20 GHz; VBATT = 3.6v		72		mA
I_{cc}, Standby[(3)]	VBATT = 1.8v		6		mA
I_{cc}, Doze[(3)]	VBATT = 1.8v		900		µA
I_{cc}, Dream[(3)]	VBATT = 1.8v		750		µA
I_{cc}, Sleep	VBATT = 1.8v		175		µA
I_{cc}, Deep Sleep	VBATT = 1.8v		2		µA

[(2)] For maximum operating range
[(3)] Depends on CPU and peripheral activity

8.5 Radio Characteristics

VBATT = VBATT1 = VBATT2 = VBATT3 = VDDIO, 1.8v < VBATT < 3.6v (unless otherwise noted), T_A=25C

8.5.1 Operating Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Operating frequency	IEEE802.11b/g-compatibility mode	2.412		2.472	GHz
Operating frequency	IEEE802.11a-compatibility mode	4.915		5.805	GHz

8.5.2 Radio Receiver

Parameter	Conditions	Min	Typ		Max	Units
			2.4G	**5.2G**		
Sensitivity at 1% PER, 200 Bytes packet(4)	6 Mbps		-78	-82		dBm
	9 Mbps		-76	-78		dBm
	12 Mbps		-74	-77		dBm
	18 Mbps		-71	-73		dBm
Sensitivity at 10% PER, 200 Bytes packet(4)	1,2,5.5,11 Mbps		-81	n/a		dBm
	6 Mbps		-79	-83		dBm
	9 Mbps		-77	-79		dBm
	12 Mbps		-76	-78		dBm
	18 Mbps		-74	-75		dBm
	24 Mbps		-69	-70		dBm
Maximum Received signal strength at 1% PER, 200 Bytes packet(4)	6 Mbps		0			dBm
	9 Mbps		0			dBm
	12 Mbps		0			dBm
	18 Mbps		0			dBm
	24 Mbps		0			dBm
Maximum Received signal strength at 10% PER, 200 Bytes packet(4)	1,2,5.5,11 Mbps		-10			dBm
Input impedance(5)	Differential		100			Ω
Return loss (S11) (4)	2.45 GHz		-15			dB
	5.80 GHz		-12			dB
Adjacent channel blocker selectivity(5)	+/- 25MHz offset		29			dB
Alternate adjacent channel blocker selectivity(5)	+/- 50MHz offset		34			dB

(4) Sensitivity and return loss guaranteed by characterization; typical values are based on default firmware settings

8.5.3 Radio Transmitter

Parameter	Conditions	Min	Typ	Max	Units
Output impedance[5]	Differential		100		Ω
RF output power – "0dBm mode"[6]	2.45GHz; VBATT = 1.8v-3.6V		0		dBm
RF output power – "0dBm mode"[6]	5.2GHz; VBATT = 1.8v-3.6V		-3		dBm
RF output power – "Turbo mode"[6]	2.45GHz; VBATT = 1.8v-3.6V		10		dBm
RF output power – "Turbo mode"[6]	5.2GHz; VBATT = 1.8v-3.6V		6		dBm
RF power control range[6]			10		dB
Carrier leakage[6]	2.45 GHz		-27		dBr
	5.20 GHz		-32		dBr
Relative constellation error (EVM) @ 6Mbps data rate	2.45 GHz		-15		dB
	5.20 GHz		-10		dB
Adjacent channel transmit power ($f=f_0+25$ MHz)			-35		dBr

[5] Guaranteed by design simulation data

[6] RF output power and carrier leakage are adjustable by firmware; the numbers in the table are default values referred to as "0dBm mode", and "Turbo mode" respectively.

8.6 ESD Caution Notice

ESD (Electrostatic Discharge) can damage this device. Ozmo, Inc. recommends that all integrated circuits be handled and stored using appropriate ESD precautions. Failure to observe proper procedures can cause ESD damage ranging from performance degradation to complete device failure.

9 Pin Description

The following table provides a brief description of each pin.

9.1 56-pin QFN Pinout

Pin Name	56 Pin QFN Number	Type	Description	Notes
TDO	1	O	JTAG test data output. Connected to the OCI debug interface.	
TMS	2	I	JTAG test mode select signal. Connected to the OCI debug interface.	Weak internal pull-up.
T4	3	A	Analog test I/O.	Used during testing; Access to General-Purpose ADC.
T3	4	A	Analog test I/O.	Used during testing; Access to General-Purpose ADC
T2	5	A	Analog test I/O.	Used during testing; Access to General-Purpose ADC.
T1	6	A	Analog test I/O.	Used during testing; Access to General-Purpose ADC.
RF5P	7	RF	Differential 5GHz RF input/output.	Needs AC coupling
RF5N	8	RF	Differential 5GHz RF input/output.	Needs AC coupling
VDDA_PA	9	Pout	PA regulator output voltage.	Output of the internal VDDA_PA LDO.
VBATT3	10	P	Unregulated battery input, operational range 1.8 – 3.6V.	
VBATT1	11	P	Unregulated battery input, operational range 1.8 – 3.6V.	
VDDA_RF	12	Pout	Analog / RF regulator output voltage.	Output of the internal VDDA_RF LDO.
RF2P4N	13	RF	Differential 2.4GHz RF input/output.	Needs AC coupling
RF2P4P	14	RF	Differential 2.4GHz RF input/output.	Needs AC coupling
VDDA_LO	15	Pout	Analog / LO regulator output voltage.	Output of the internal VDDA_LO LDO.
EXTR	16	A	Connect to external 140Kohm resistor for reference circuit.	
VDDA_AN	17	Pout	Analog / baseband regulator output voltage.	Output of the internal VDDA_AN LDO.
VBATT2	18	P	Unregulated battery input, operational range 1.8 – 3.6V.	
XOIN	19	A	Crystal input (24 MHz).	
XOCAP	20	A	Crystal capacitors.	
TSTMODE	21	I	Test mode.	Set to logic low for normal operation, weak internal pull-down.
AUDIOCLK	22	O	Audio clock output.	Output of audio PLL.
TSTSEL0	23	I	Test mode.	Set to logic high for normal operation, weak internal pull-up.
TSTSEL1	24	I/O	Test mode, JTAG POD reset_n.	Set to logic high for normal operation, weak internal pull-up.
TSTCLK	25	I	Test clock input.	Set to logic low for normal operation, weak internal pull-down.

Pin Name	56 Pin QFN Number	Type	Description	Notes
VDDIO	26	P	I/O power supply voltage; Unregulated battery input, operational range 1.8 – 3.6V.	
AIO2	27	I/O	Application I/O pin 2. May be configured as GPIO or allocated to one of the supported standard interfaces.	16mA LED drive capability; weak internal pull-up; 5v tolerant pin.
AIO1	28	I/O	Application I/O pin 1. May be configured as GPIO or allocated to one of the supported standard interfaces.	16mA LED drive capability; weak internal pull-up; 5v tolerant pin.
AIO0	29	I/O	Application I/O pin 0. May be configured as GPIO or allocated to one of the supported standard interfaces.	16mA LED drive capability; weak internal pull-up; 5v tolerant pin.
AIO15	30	I/O	Application I/O pin 15. May be configured as GPIO or allocated to one of the supported standard interfaces.	8mA source / sink capability, weak internal pull-up.
AIO14	31	I/O	Application I/O pin 14. May be configured as GPIO or allocated to one of the supported standard interfaces.	8mA source / sink capability, weak internal pull-down.
VDDIO	32	P	I/O power supply voltage; Unregulated battery input, operational range 1.8 – 3.6V.	
AIO13	33	I/O	Application I/O pin 13. May be configured as GPIO or allocated to one of the supported standard interfaces.	8mA source / sink capability, weak internal pull-down.
AIO12	34	I/O	Application I/O pin 12. May be configured as GPIO or allocated to one of the supported standard interfaces.	8mA source / sink capability, weak internal pull-up.
AIO11	35	I/O	Application I/O pin 11. May be configured as GPIO or allocated to one of the supported standard interfaces.	8mA source / sink capability, weak internal pull-up.
AIO10	36	I/O	Application I/O pin 10. May be configured as GPIO or allocated to one of the supported standard interfaces.	8mA source / sink capability, weak internal pull-up.
VDDIO	37	P	I/O power supply voltage; Unregulated battery input, operational range 1.8 – 3.6V.	
AIO9	38	I/O	Application I/O pin 9. May be configured as GPIO or allocated to one of the supported standard interfaces.	8mA source / sink capability, weak internal pull-up.
AIO8	39	I/O	Application I/O pin 8. May be configured as GPIO or allocated to one of the supported standard interfaces.	8mA source / sink capability, weak internal pull-up.

Pin Name	56 Pin QFN Number	Type	Description	Notes
AIO7	40	I/O	Application I/O pin 7. May be configured as GPIO or allocated to one of the supported standard interfaces.	8mA source / sink capability, weak internal pull-up.
AIO6	41	I/O	Application I/O pin 6. May be configured as GPIO or allocated to one of the supported standard interfaces.	8mA source / sink capability, weak internal pull-down.
AIO5	42	I/O	Application I/O pin 5. May be configured as GPIO or allocated to one of the supported standard interfaces.	8mA source / sink capability, weak internal pull-down.
AIO4	43	I/O	Application I/O pin 4. May be configured as GPIO or allocated to one of the supported standard interfaces.	8mA source / sink capability, weak internal pull-up.
VDDRET	44	Pout	Digital retention regulator output voltage.	Output of the internal VDD_RET LDO.
VDDIO	45	P	I/O power supply voltage; Unregulated battery input, operational range 1.8 – 3.6V.	
VDDD	46	Pout	Digital regulator output voltage.	Output of the internal VDDD LDO.
AIO3	47	I/O	Application I/O pin 3. May be configured as GPIO or allocated to one of the supported standard interfaces.	8mA source / sink capability, weak internal pull-up.
SPIMOSI	48	I/O	SPI Master-Out-Slave-In serial data signal.	8mA source / sink capability, weak internal pull-up.
SPIMISO	49	I/O	SPI Master-In-Slave-Out serial data signal.	8mA source / sink capability, weak internal pull-up.
SPICLK	50	I/O	SPI clock signal.	8mA source / sink capability, weak internal pull-up.
SPIBOOTCS	51	I/O	Chip select for external serial SPI Flash.	8mA source / sink capability, weak internal pull-up.
VDDIO	52	P	I/O power supply voltage; Unregulated battery input, operational range 1.8 – 3.6V.	
AUXO	53	O	Auxiliary output. May be configured as GPIO or allocated to one of the supported standard interfaces.	8mA source / sink capability, weak internal pull-up.
RST_N	54	I	System reset, active low.	No internal pull-up or pull-down.
TCK	55	I	JTAG test clock signal. Connected to the OCI debug interface.	Must be high at reset for normal operation, weak internal pull-up.
TDI	56	I	JTAG test data input. Connected to the OCI debug interface.	Weak internal pull-up.
VSS[7]	Exposed DAP	GND	Device ground.	Must be connected to ground for normal operation.

[7] The QFN package has an exposed die attach pad (DAP) that must be connected to ground.

Pin types are as follows:

- I Digital input
- O Digital output
- I/O Digital input/output

RF	RF
A	Analog
P	Power
Pout	Output of on-chip LDO
GND	Ground
NC	No connect

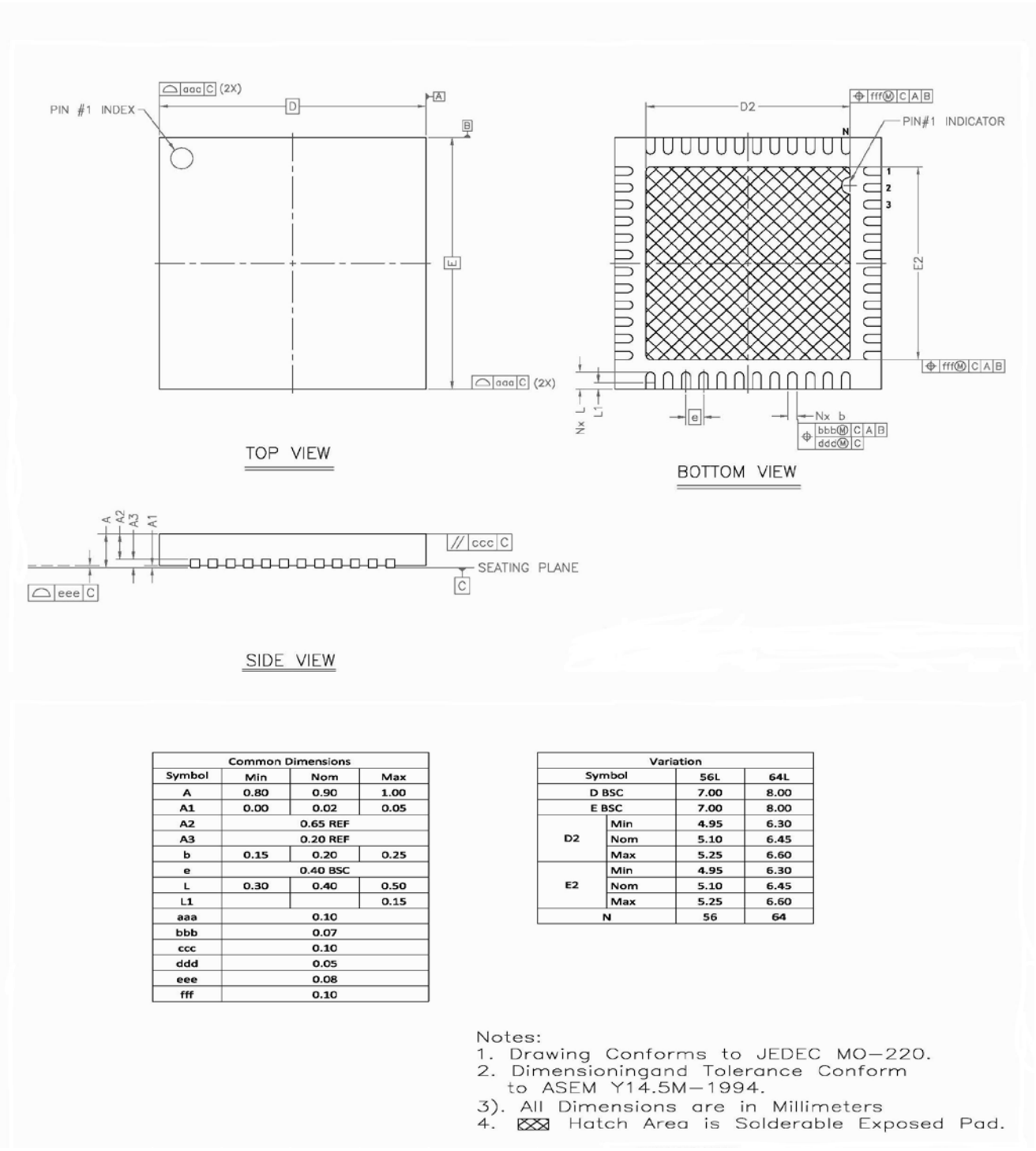
9.2 IO Pin functions

IO Pin Configurations (controlled by Ozmo Firmware)

PIN	CONFIG 0	CONFIG 1	CONFIG 2	CONFIG 3
AIO0	**GPIO0**	LED0	reserved	UART TXD
AIO1	**GPIO1**	LED1	reserved	UART TXD
AIO2	**GPIO2**	LED2	reserved	MODEGSEL
AIO3	**GPIO3**	I2C SCL	SPI0CS1/SPI0SS	SPI1MISO
AIO4	**GPIO4**	I2C SDA	reserved	SPI1MOSI
AIO5	**GPIO5**	UART TXD	I2C SCL	PAEN
AIO6	**GPIO6**	UART RXD	I2C SDA	LNAEN
AIO7	**GPIO7**	SPI1CS0/SPI1SS	reserved	reserved
AIO8	**GPIO8**	AUDIO BITCLK	reserved	SPI0CS2/SPI1CS2
AIO9	**GPIO9**	AUDIO_OUT FS	reserved	SPI0CS3/SPI1CS3
AIO10	**GPIO10**	AUDIO_OUT	reserved	SPICS1
AIO11	**GPIO11**	AUDIO_IN	reserved	reserved
AIO12	**GPIO12**	AUDIO_IN FS	reserved	reserved
AIO13	**GPIO13**	SPI1MISO	reserved	TXSW
AIO14	**GPIO14**	SPI1MOSI	reserved	RXSW
AIO15	**GPIO15**	SPI1CLK	reserved	UART TXD/RXD
AUXO	**AUX_GPO**	EXTREGEN	CLKOUT	UART TXD

10 Package Information

10.1 Package Outline Drawing



Common Dimensions			
Symbol	Min	Nom	Max
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.65 REF	
A3		0.20 REF	
b	0.15	0.20	0.25
e		0.40 BSC	
L	0.30	0.40	0.50
L1			0.15
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Variation			
Symbol		56L	64L
D BSC		7.00	8.00
E BSC		7.00	8.00
D2	Min	4.95	6.30
	Nom	5.10	6.45
	Max	5.25	6.60
E2	Min	4.95	6.30
	Nom	5.10	6.45
	Max	5.25	6.60
N		56	64

Notes:
1. Drawing Conforms to JEDEC MO-220.
2. Dimensioningand Tolerance Conform to ASEM Y14.5M-1994.
3). All Dimensions are in Millimeters
4. Hatch Area is Solderable Exposed Pad.

Figure 3 OZMO2000 package outline drawing

10.2 Marking Information

The following markings will appear on the package. All markings are in white laser.

Line 1: OZMO Logo
Line 2: OZMO product number
Line 3: YWW-RR - date code
Line 4: TTTT – lot ID

11 Ordering Information

Use the following table to select the correct ordering number for the version of the Ozmo2000 that is required.

Order Number	Package Type	Shipping Option
OZMO2000A-Q56-1	Q56 - 56 QFN	1 - Tray
OZMO2000A-Q56-2	Q56 - 56 QFN	2 – Tape and Reel

12 Revision history:

1.1	April 2011	Minor edits
1.2	June 2012	Added IO map & Turbo mode specs. Removed: RTC ref, xtal freq's other than 24MHz, ref's to 64pin pkg.

OZMO DEVICES
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