Circuit Description

	Location	Part Name	Value	Function
1	X400	RESONATOR,LAP 25.000MHz	25.000MHz	Crystal supply to Ethernet Controller(U403)
2	U403	IC,ENC28J60T-C/SS		Ethernet Controller MAC/PHY
3	U500,U501	IC,IRS2092STRPBF	≒380KHz	Digital Amp
4	Q501,Q502,Q507,Q508	FET,1RF6645	≒380KHz	Switching device
5	X100	RESONATOR,SEG55 16.9344	16.9344MHz	Crystal supply to CPU(U101)
6	U101	IC,UPD78F1146AGB-GAH-AX		CPU

Remark: The module FS2026 and RF chip-set information, please refer to the following pages.

Venice 6 FS2026

Internet radio/network audio/DAB/FM-RDS module

General description

The Venice 6 FS2026 module is a complete hardware and software solution for Internet radio, network audio and DAB/FM-RDS products. It provides the simplest and lowest-cost solution for high-quality audio streaming from live Internet radio stations or network-based music collections.

Several configurations are available, with different combinations of integrated RF receivers for WiFi networks, DAB Band 3, L-Band and FM reception.

Based around Frontier Silicon's powerful Chorus 2i processor, Venice 6 streams radio stations and music files in a variety of formats and protocols including MP3, Windows® Media Audio (WMA) and REAL, and enables a new generation of stand-alone network-based audio products.

Frontier Silicon provides a complete set of evaluation and reference platforms, which can be used to enable rapid development of Venice 6-based systems. Applications include a wide range of audio products, from kitchen and alarm clock radios to CD micro systems, boomboxes and HiFi tuners.

Modes

- Live Internet radio broadcasts
- Internet radio "listen again" on-demand content
- Network audio playback
- DAB Digital Audio Broadcast radio
- FM radio reception with RDS
- Audio playback from USB

Audio Decoders

- MP3, WMA, Real Audio

Playlist Support

- M3U, ASX, PLS, PLY

Connectivity

- USB 2.0 device/host
- 802.11b/g – WEP, TKIP, WPA, WPA2 security
- On-board audio DAC with stereo analogue line output
- Digital output for HiFi applications
- LCD interface supports range of display types
- Infrared remote control
- Keyboard presets, rotary encoder

Features

- Software upgradeable in the field
- Simple registration and configuration via
  - remote control
  - front panel
  - vTuner web portal
- Clock/alarms
- uPnP support
- On-board WiFi antenna for easy integration in final products

Ordering information

Part	Description
FS2026-W	WiFi
FS2026-WB	WiFi, DAB Band 3, FM
FS2026-WD	WiFi, DAB L-Band and Band 3, FM
FS2026-B	DAB Band 3, FM
FS2026-D	DAB L-Band and Band 3, FM
Please contact Frontier Silicon for evaluation board.	

Legal and precautionary notices

This document supersedes all previous versions. In line with its policy of continuous improvement, Frontier Silicon reserves the right to make changes to products and documentation without notice.

Frontier Silicon accepts no liability for any losses alleged to have arisen from use of this document or associated products.

The Frontier Silicon logo is a trademark of Frontier Silicon. Windows is a registered trademark of Microsoft Corporation.

DAB and MP3 technologies are subject to end-user patent licences: please contact Frontier Silicon for more details.

Frontier Silicon Limited

Gleneagles Ground Floor
The Belfry
Colonial Way
Watford
Herts
WD24 4WH
United Kingdom

Tel: +44 (0)1923 474200

Fax: +44 (0)1923 202251

E-mail: info@frontier-silicon.com

Web: www.frontier-silicon.com

CAUTION: **The product(s) described in this document contain static-sensitive parts and must be handled in a static-controlled environment.**

Contents

List of figures

List of tables

Revision history

Revision number	Date	Document maturity	Description
1	February 2007	Initial	First release

Table 1: Revision history

Document maturity key

Initial Initial data, all subject to change.

Preliminary Preliminary data; minor details may be missing or subject to change.

Complete All sections complete.

Revised Additions/corrections incorporated.

Obsolete Document refers to a discontinued or soon-to-be-discontinued product. Withdrawn from external distribution.

1 Introduction

1.1 Features

Figure 1 shows a block diagram of the Venice 6 module. The main components are the WiFi receiver, the Apollo FS1110 tri-band RF front end, the Chorus 2i FS1020 processor, a serial boot FLASH and an audio DAC.

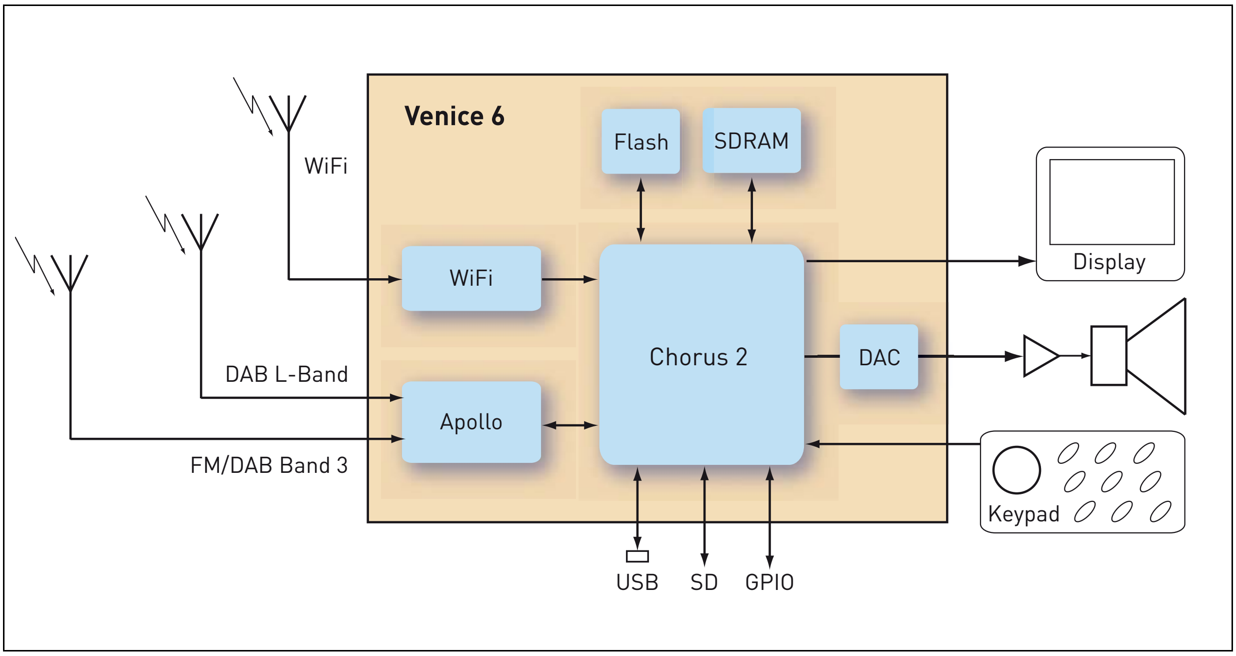


Figure 1: Venice block diagram

The Chorus 2i processor is an extremely flexible baseband receiver covering a number of physical layer standards, particularly those utilising COFDM modulation. The baseband signal processing is achieved using a blend of hardware and software to optimise trade-offs between power, cost and flexibility.

Venice 6 measures 40 x 112 mm (with on-board antenna) or 40 x 107 mm (without on-board antenna). The underside of the module has a 'solid copper' ground plane and all components are on the top of the module. With the exception of the connectors and screw holes, all components are fitted inside the two-chamber screen can. The RF and baseband sections are screened from each other.

1.2 Feedback

To contribute feedback on this document, please e-mail technical-publications@frontier-silicon.com.

Include the following information:

- document title, number and date:
  Venice 6 FS2026 Datasheet, FSQ 0000 1474 Rev 1, February 2007,
- section number and heading if referring to a specific part of the document.

2 Applications

Venice 6 is designed to work in different applications in either master or slave mode. The 64-way pin connector available on the module provides a range of functionalities which can be interfaced to drive different peripherals to form a full system.

This chapter presents some common applications using Venice 6.

2.1 Venice 6 pin assignments

Figure 2 shows possible signals that can exist on the Venice 6 pins.

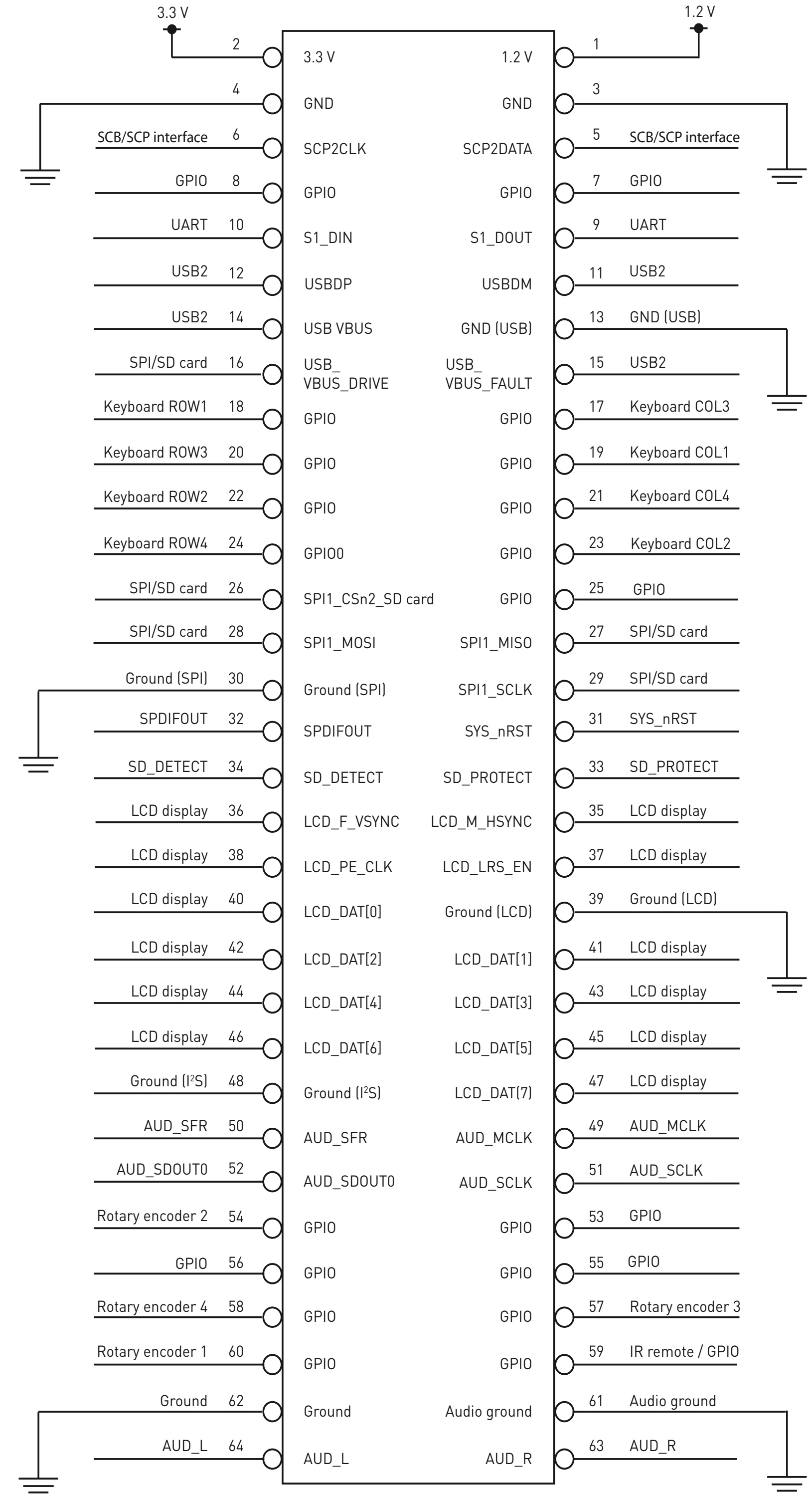


Figure 2: Venice pin assignments

2.2 Master mode application

Figure 3 shows Venice 6 in master mode implementation, functioning as the main system controller in the radio.

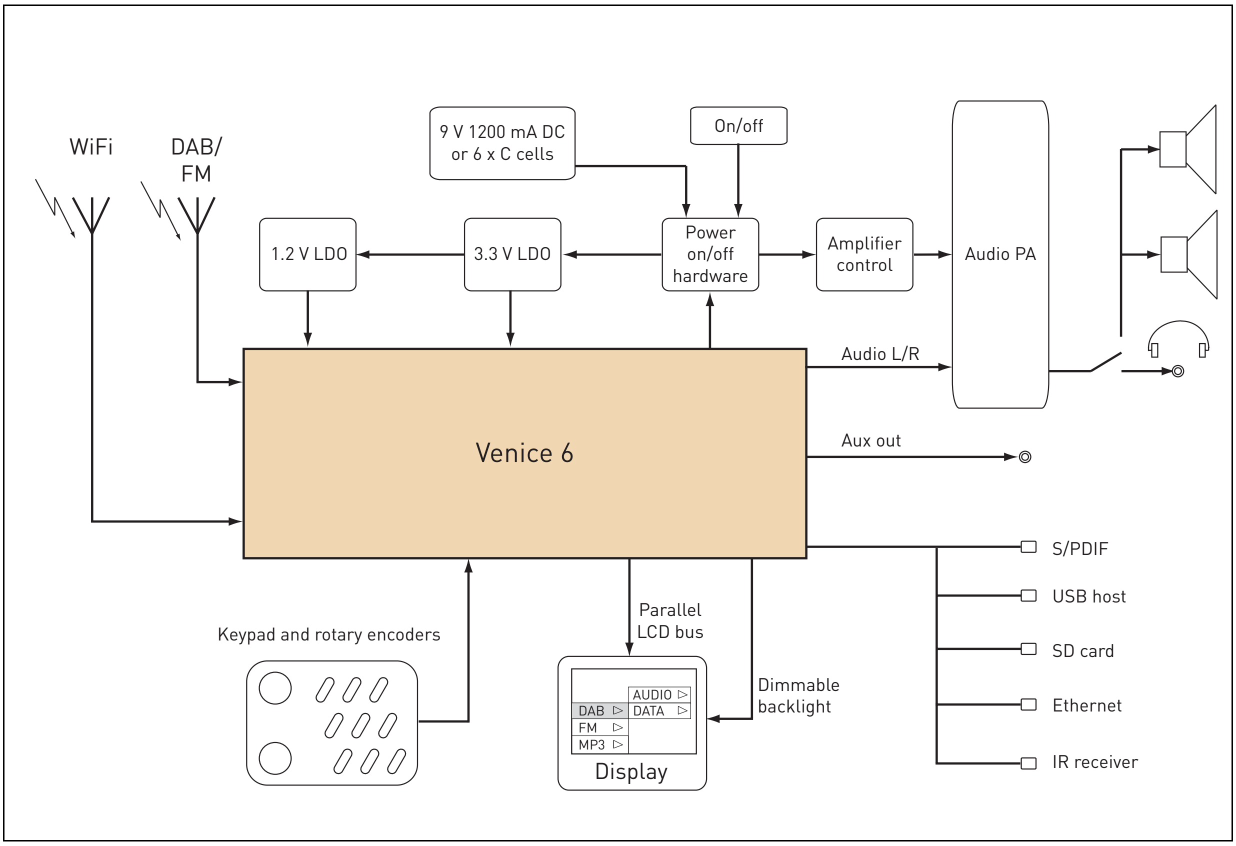


Figure 3: Master mode application

2.3 Slave mode application

Figure 4 shows Venice 6 in a slave mode implementation.

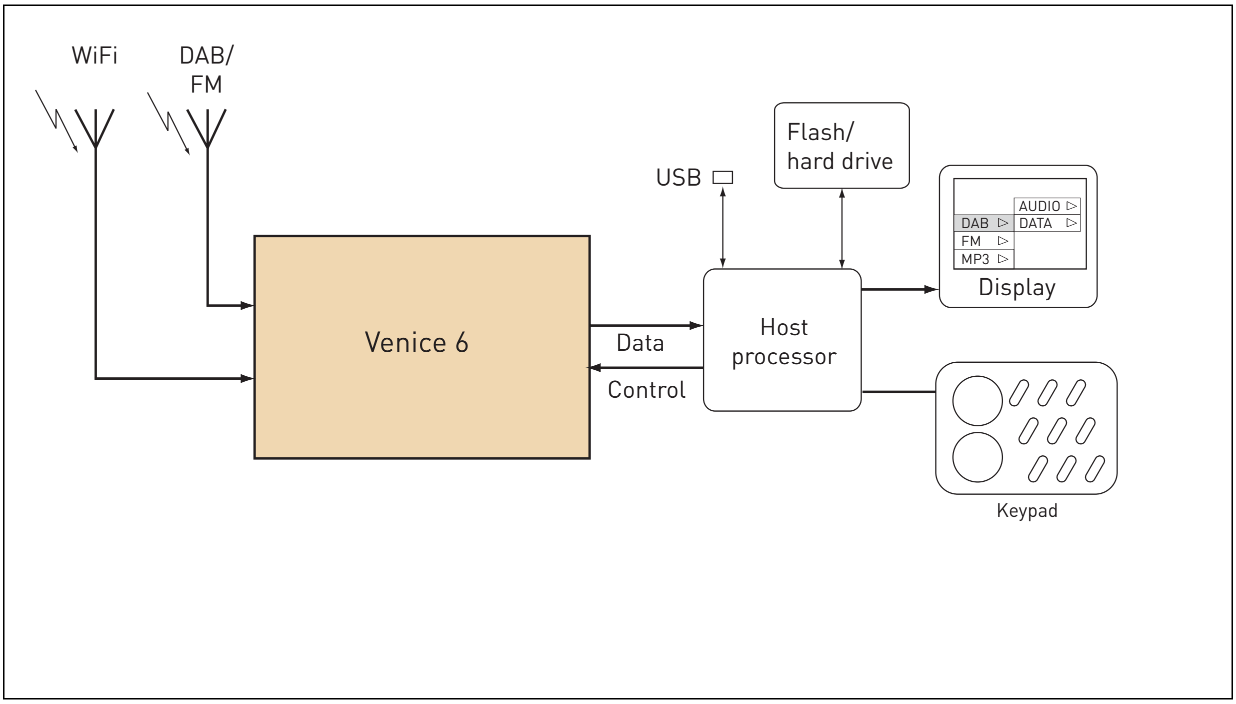


Figure 4: Slave mode application

3 Hardware interfaces

Venice 6 supports a number of hardware interfaces. The characteristics of these interfaces are detailed below. *Figure 2* shows the pin assignments on the main connector, J1.

Note: Some of these interfaces may be mutually exclusive.

3.1 DAB/FM broadcast input

Two RF inputs are provided and can support any combination of Band 2 (FM), Band 3 (DAB) and L-Band (DAB). The RF input connector site can accept one of the following connectors:

- 2.6 mm UMP
- SMA
- SMB
- F-type
- coaxial flying lead (pig-tail).

3.2 WiFi connection

The WiFi connection is both a transmitter and a receiver. WiFi can be connected as an option by a connector, or the product can be shipped with an integral, board-mounted, antenna with a link connecting it to the WiFi radio block. The link and antenna can be removed to allow the fitement of an RF connector, or cable if required.

The WiFi connection can support either of the following connectors:

- 2.6 mm UMP
- SMA

3.3 Analogue audio output

A stereo line level output is provided by the on-PCB stereo audio DAC.

Parameter	Min	Typ	Max	Units	Comments
Load resistance	3.0			kΩ	To mid-rail or AC coupled
Signal level		0.6		V_{RMS}	into 10 kΩ
THD (full scale)		0.01	0.02	%	THD full scale
SNR	95	97	102	dB	3.3 V supply
3 dB audio bandwidth (referenced to 1 kHz level)	TBD		20,000	Hz	In DAB mode
	TBD		12,500	Hz	In FM mode

Table 2: Audio analogue output

3.4 Digital audio output (I^2S)

An I^2S bus is provided comprising master clock, bit clock, sample frame, stereo in, and stereo out for basic stereo operation with an external DAC or CODEC.

- LR clock - 1 x f_S clock from either 256f_S or 384f_S clock.
- Bit clock - generated with appropriate extra clocks for 16 bit data in 32 bit frame, etc.
- Frame - 32/48/64 bits (2 channels).
- Serial data - MSB first; left justified or right justified 16/18/20/22/24/28/30/32 bits.

Pin number	Pin description	Alternate usage	Driver capability
49	AUD_MCLK	-	2 mA
50	AUD_SFR		
51	AUD_SCLK		
52	AUD_SDOUT0		

Table 3: Digital audio output

Note: If S/PDIF is the main audio output and the I^2S bus is not used, pins 49-52 may be used as GPIOs.

3.5 Asynchronous serial port (UART)

Venice 6 provides a UART channel at the 2 x 32-way connector. The maximum baud rate available on this UART is 115200 baud.

Pin number	Pin description	Alternate usage	Driver capability
9	S1_DOUT	Spare GPIO	2 mA
10	S1_DIN		

Table 4: Asynchronous serial port (UART)

3.6 Serial control bus (SCB)

The serial control bus is a bi-directional, two-wire, open collector SCP-style bus and is used to control Venice 6 by the host processor.

The functionality of the SCB is master/slave transmitter/receiver in standard or fast mode (100/400 kHz). Multi-master operation is not supported by this port. These pins are 5 V tolerant.

Pin number	Pin description	Alternate usage	Driver capability
5	SCP2DATA	Display control	4 mA
6	SCP2CLK	Display control	

Table 5: Serial control bus (SCB)

3.7 Serial peripheral interface (SPI)

The serial peripheral interface (SPI) pins can be used to interface the Venice 6 module to an SD card or an Ethernet chip to provide wired connectivity.

The SPI pins are shown in *Table 6*.

Pin number	SPI mode	Alternate usage	Driver capability
5	SPI2_CSn		4 mA
6	SPI2_SCLK		
7	SPI2_SO	GPIO	2 mA
7	SPI2_SI	GPIO	
26	SPI1_CSn2_SD card	GPIO	8 mA
27	SPI1_MISO	GPIO	
28	SPI1_MOSI	GPIO	
29	SPI1_SCLK	GPIO	2 mA

Table 6: Serial peripheral interface (SPI)

3.8 SD card interface

The SPI port can be used to interface with an SD card. The connectivity between Venice 6 and an SD card is shown in *Table 7*.

<table>
<tr><th>Pin number</th><th>SD card interface</th><th>Venice 6</th></tr>
<tr><td>1</td><td>Card detect DAT3</td><td>SPICS1</td></tr>
<tr><td>2</td><td>Command/response</td><td>SPISO</td></tr>
<tr><td>3</td><td>Ground</td><td></td></tr>
<tr><td>4</td><td>Supply voltage</td><td></td></tr>
<tr><td>5</td><td>Clock</td><td>SPICSLK</td></tr>
<tr><td>6</td><td>Ground</td><td></td></tr>
<tr><td>7</td><td>Data bit 0</td><td>SPISI</td></tr>
<tr><td>8</td><td>Data bit 1</td><td rowspan="3">GPIO</td></tr>
<tr><td>9</td><td>Data bit 2</td></tr>
<tr><td>10</td><td>Detect</td></tr>
<tr><td>11</td><td>Protect/detect</td><td>Ground</td></tr>
<tr><td>12</td><td>Protect</td><td>GPIO</td></tr>
</table>

Table 7: SD card interface

3.9 Ethernet interface

For information about the Ethernet interface, see the Application Note.

3.10 LCD port

TBD

3.11 General Purpose I/O

When the hardware is suitably configured some of the following lines may be used as GPIO signals. The state of each GPIO signal can be read by software. The logic level and tri-state drive of each GPIO signal can also be controlled by software.

Pin number	Pin description	Driver capability
7	GPIO	2 mA
8	GPIO	
9	GPIO	
10	GPIO	
17	GPIO	8 mA
18	GPIO	
19	GPIO	
20	GPIO	
21	GPIO	
22	GPIO	
23	GPIO	
24	GPIO	
25	GPIO	
26	GPIO	
27	GPIO	
28	GPIO	
29	GPIO	
32	GPIO	2 mA

Table 8: GPIO

Pin number	Pin description	Driver capability
33	GPIO	8 mA
34	GPIO	
35	GPIO	
36	GPIO	
37	GPIO	
38	GPIO	
40	GPIO	
41	GPIO	
42	GPIO	
43	GPIO	
44	GPIO	
45	GPIO	
46	GPIO	
47	GPIO	
49	GPIO	2 mA
50	GPIO	
51	GPIO	
52	GPIO	
53	GPIO	8 mA
54	GPIO	
55	GPIO	
56	GPIO	
57	GPIO	
58	GPIO	
59	GPIO	
60	GPIO	

Table 8: GPIO

3.12 S/PDIF audio output

The S/PDIF audio output carries a stereo digital audio output on a single wire using the signal format defined in IEC60958 *[reference 13]*.

Pin number	Pin description	Alternate usage	Driver capability
32	S/PIDIF OUT	-	4 mA

Table 9: S/PDIF audio output

3.13 Infrared remote

An Infrared Remote (IR) interface is present on the main connector, J1.The Philips RC5 IR protocol is supported.

Pin number	Pin description	Alternate usage	Driver capability
59	IR remote	GPIO	

Table 10: Infrared remote

3.14 USB 2 interface

A USB 2.0 interface is available on the module, which supports both device and host operation.

Pin number	Pin description	Alternate usage	Driver capability
11	USBDM	USB2	
12	USBDP	USB2	
13	Gnd (USB)	Gnd (USB)	
14	USB VBUS	USB2	
15	USB_VBUS_FAULT	USB2	
16	USB_VBUS_DRIVE		

Table 11: USB 2 interface

The USB parameters are shown in *Table 12*.

Parameter	Min	Typ	Max	Units
High level output voltage			3.6	V
Low level output voltage	0.6			
Pin current		0.45		mA

Table 12: USB parameters

3.15 Debug connector

An optional debug connector can be fitted.

Pin number	Function	Chorus 2i pads	ATMEL FLASH	Pad function description
1	TMS	JTAG_TMS		JTAG Test Port Test Mode Select
2	TDO	JTAG_TDO		JTAG Test Port Data Out
3	TCK	JTAG_TCK		JTAG Test Port Clock
4	TDI	JTAG_TDI		JTAG Test Port Data In
5	-	-		
6	Ground	Ground		
7	Ground	Ground		
8	SYS_RST	SYSA_RSTn		
9	Ground	Ground		
10	FCS		CS#	
11	FSI		SI	
12	FSCK		SCLK	
13	Ground		Ground	
14	FSO		SO	
15	3V3		Supply	

Table 13: DASH connector

4 Power supplies

Venice 6 requires a 1.2 V ± 10% supply, (optionally 1.0 V ± 5%), for the digital baseband circuits and 3.3 V + 5% / - 10% for the RF circuits and other baseband devices such as the audio DAC. Both supplies should be clean with low ripple. Any noise on these supplies will affect performance.

Voltage, V	**Supply level**, mA		**Condition**
	Typ	**Max**	
3.3	160	350	DAB only
	160	350	Soft FM
	300	600	Internet radio
	400	900	Internet radio and DAB/FM
1.2	180	350	DAB only
	180	350	Soft FM
	250	350	Internet radio
	400	5050	Internet radio and DAB/FM

Table 14: Power supply requirements

There is some supply filtering on the Venice 6 DC supply lines. This takes the form of a Pi network with a ferrite bead inductor in the supply line and with one or more capacitors to ground on either side.

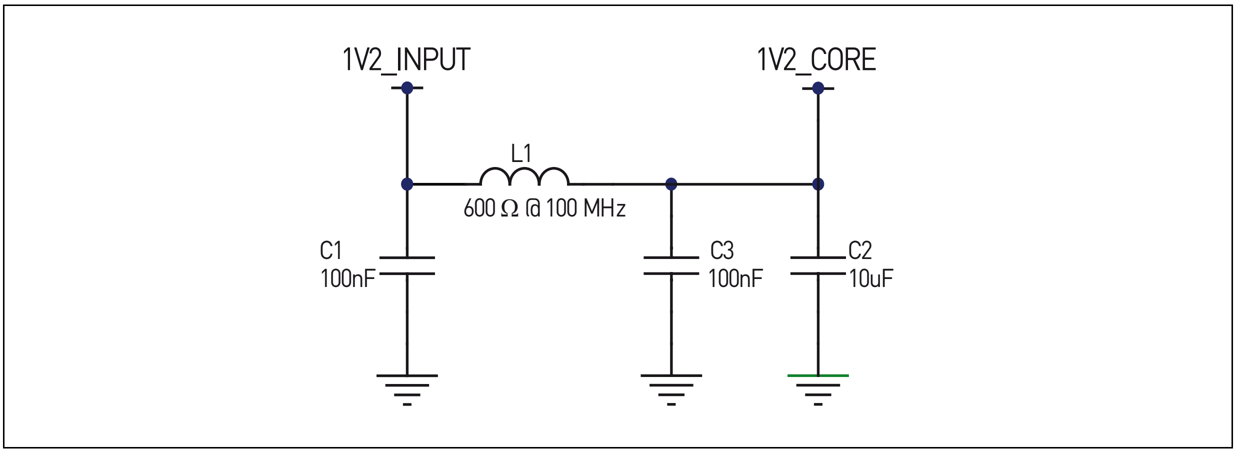


Figure 5: DC supply filtering

Venice 6 must have its voltage rails regulated. Choose regulators that will cope with power requirements in excess of those required, due to the burst requirements of the DAB receiver.

Incorporate suitable bulk de-coupling to provide for the burst nature of the module's power requirements and to reduce the noise and ripple applied to the module. The capacitors should be mounted as close as possible to the 2 x 32-way connector.

Locate the regulators as close as possible to the module connector. Use a solid ground plane if possible. If this is not possible, use large tracks with the ground connections from each regulator joining close to the module.

4.1 Power-on timing

The 3.3 V supply must always be at a higher voltage than the 1.2 V supply. Thus, the 3.3 V should come on first. This can be arranged via ordering of the linear regulators, scaling of decoupling capacitors, or by use of reset management chips (where the 1.2 V regulator has an enable).

When in slave mode, the time at which commands can be accepted is identified by the issuance of a 'Command Reset' message over the serial interface. This indicates that the module has concluded its boot process.

4.2 Power-off timing

Venice 6 is designed so that the power can be removed in any order at any time without affecting the module. However, when in slave mode the power to the digital section should be removed not less than 400 ms after the previous command was issued. This ensures that the command is processed.

5 Build options

5.1 Introduction

Venice 6 has been designed for flexibility in application and use. This section describes the different build options available on the module.

5.2 DAB/FM antenna connectivity

The main DAB/FM antenna connector may be any one of the following:

- 2.6 mm UMP,
- SMA,
- SMB,
- F-Type,
- coaxial flying lead (pig-tail) 75 Ω.

These connectors can support operation in Bands 2/3 and L-Band.

5.3 WiFi antenna connectivity

The module supports the following WiFi antenna options:

- on-board printed F-antenna,
- SMA,
- 2.6 mm UMP.

5.4 Flash memory

Venice 6 supports an on-board Flash memory with an SPI compatible interface. Memories of 4, 8, 16 and 32 Mb capacities are supported.

Note: Size of Flash used will depend on software features required by customers.

Flash memory, Mb	**Example Atmel parts**
4	AT45DB041D-SU
8	AT45DB081D-SU
16	AT45DB161D-SU
32	AT45DB321D-SU

Table 15: Flash memory support

5.5 F-type antenna

TBD

6 Performance characteristics

6.1 Introduction

Venice 6 supports 802.11 b/g WiFi connectivity.

Venice 6 is a Eureka 147 DAB receiver to EN61000-4-2 supporting:

- Band 3 (174.928 MHz to 239.20 MHz)
  - Korean Band 3 (175.280 MHz to 214.736 MHz)
- L-Band (1452.960 MHz to 1490.624 MHz)
  - Canadian L-Band (1452.816 MHz to 1491.184 MHz)

with typical performance equal to or better than EN50248:2001 *[reference 10]*.

Venice 6 supports Band 2 Soft FM (87.5 MHz to 108 MHz) and meets parts of the BS 5942-2:1987 Hi-Fidelity minimum performance when tested to BS 60315-4 *[reference 11]*.

6.2 WiFi performance

Venice 6 supports the mandatory modes required by 802.11b and 802.11g plus some optional modes to provide those listed in *Table 16*. The maximum transmit power of the WiFi module is limited to 20 dBm Effective Isotropic Radiated Power (EIRP). The WiFi module's transmit power and the antenna gain added together must not exceed 20 dBm EIRP.

Mode	Bit Rate	Modulation	Sensitivity		Transmit EVM	Max Power (EIRP)
			Minimum	**Typical**		
DSSS	1 Mbs	DBPSK	-83dBm 8% FER	-94dBm 8% FER	<35% peak	20 dBm
DSSS	2 Mbs	DQPSK	-83dBm 8% FER	-94dBm 8% FER	<35% peak	
HR/DSSS	5.5 Mbs	DQPSK	-83dBm 8% FER	-93dBm 8% FER	<35% peak	
HR/DSSS	11 Mbs	DQPSK	-83dBm 8% FER	-91dBm 8% FER	<35% peak	
ERP-OFDM	6 Mbps	BPSK 1/2 rate	-82dBm 10% PER	-89dBm 10% PER	-5 dB RMS	
	9 Mbps	BPSK 3/4 rate	-81dBm 10% PER	-89dBm 10% PER	-8 dB RMS	
	12 Mbps	QPSK 1/2 rate	-79dBm 10% PER	-89dBm 10% PER	-10 dB RMS	
	18 Mbps	QPSK 3/4 rate	-77dBm 10% PER	-87dBm 10% PER	-13 dB RMS	
	24 Mbps	16QAM 1/2 rate	-74 dBm 10% PER	-85 dBm 10% PER	-16 dB RMS	
	36 Mbps	16QAM 3/4 rate	-70 dBm 10% PER	-81 dBm 10% PER	-19 dB RMS	
	48 Mbps	64QAM 2/3 rate	-66 dBm 10% PER	-75 dBm 10% PER	-22 dB RMS	
	54 Mbps	64QAM 3/4 rate	-65 dBm 10% PER	-74 dBm 10% PER	-25 dB RMS	

Table 16: WiFi performance

6.3 RF performance

6.3.1 DAB Band 3

(Unless otherwise specified Ta = 25°C, Vcc = 3.3 V,

Operating mode = decoding one DAB stereo audio channel at 192 kbit/s)

Parameters	Min	Typ	Max	Units
Band 3 tuning range	174.928		239.200	MHz
Band 3 large signal	-5	0		dBm
Band 3 sensitivity	-95	-97		
Band 3 far off selectivity	40			dB
Band 3 adjacent channel	30	32		

Table 17: Band 3 performance

6.3.2 DAB L-Band

(Unless otherwise specified Ta = 25°C, Vcc = 3.3 V,

Operating mode = decoding one DAB stereo audio channel at 192 kbit/s)

<table>
<tr><th>Parameters</th><th>Min</th><th>Typ</th><th>Max</th><th>Units</th></tr>
<tr><td>L-Band tuning range</td><td>TBD</td><td>TBD</td><td>TBD</td><td rowspan="2">MHz</td></tr>
<tr><td>Canadian L-Band</td><td>TBD</td><td>TBD</td><td>TBD</td></tr>
<tr><td>L-Band large signal</td><td>TBD</td><td>TBD</td><td>TBD</td><td rowspan="4">dBm</td></tr>
<tr><td>L-Band sensitivity</td><td>TBD</td><td>TBD</td><td>TBD</td></tr>
<tr><td>L-Band far off selectivity</td><td>TBD</td><td>TBD</td><td>TBD</td></tr>
<tr><td>L-Band adjacent channel</td><td>TBD</td><td>TBD</td><td>TBD</td></tr>
</table>

Table 18: L-Band performance

6.3.3 FM performance

(Unless otherwise specified Ta = 25°C, Vcc = 3.3 V,

Operating mode = decoding one FM stereo audio channel at +/- 75 kHz with 1 kHz tone)

<table>
<tr><th>Parameters</th><th>Min</th><th>Typ</th><th>Max</th><th>Units</th></tr>
<tr><td>FM band tuning range</td><td>89.5</td><td>-</td><td>108</td><td>MHz</td></tr>
<tr><td>FM sensitivity (S+N)/ N=26dB</td><td>-106</td><td>-108</td><td>-</td><td rowspan="2">dBm</td></tr>
<tr><td>Large signal handling capacity</td><td>-</td><td>0</td><td>-</td></tr>
<tr><td>(S+N)/N ultimate signal-to-noise ratio</td><td>-</td><td>63</td><td>-</td><td>dB</td></tr>
<tr><td>THD</td><td>-</td><td>0.15</td><td>-</td><td>%</td></tr>
<tr><td>Tuning step size</td><td>-</td><td>50</td><td>-</td><td>KHz</td></tr>
<tr><td rowspan="2">FM selectivity (+200 kHz)
(-200 kHz)</td><td>30</td><td>40</td><td>-</td><td rowspan="3">dB</td></tr>
<tr><td>25</td><td>40</td><td>-</td></tr>
<tr><td>Stereo separation</td><td>25</td><td>40</td><td>-</td></tr>
</table>

Table 19: FM performance

6.4 Audio specification

(Unless otherwise specified, Ta = 25°C, Vcc = 3.3 V).

Mode of Operation	**Lower 3 dB frequency limit** (with respect to 1 kHz)	**Higher 3 dB frequency limit** (with respect to 1 kHz)
FM	20 Hz	12.5 kHz
DAB	20 Hz	20 kHz

Table 20: Audio bandwidth

A typical SNR of 99 dBA is achieved, worst case 97 dBA, in DAB mode. This is dependant on the load applied.

7 Electrical specification

7.1 Absolute maximum ratings

Parameter	Min	Typ	Max	Unit	Comments
3V3 power terminal	-0.3	3.3	4.0	V	
1V2 power terminal	-0.3	1.2	1.32		
V_{IN}	-0.3		5.5	V	Other than supply pins
Storage temperature	-40		+85	°C	
I_{OUT}	10		100	mA[a]	
Humidity	0		90	%	Non-condensing
RF input			0	dBm	
Other inputs	-0.3		3.6	V	
Outputs	-20		+20	mA	

Table 21: Absolute maximum ratings

a. Total for all I/O

7.2 Typical values

7.2.1 Operating conditions

Parameter	Min	Typ	Max	Comments	Units
Operating temperature	-10		+70		°C
3V3 input current		350 - 500		WiFi	mA
1V2		160		DAB and FM	

Table 22: Typical operating conditions

7.2.2 Main signal levels

Parameter	Min	Typ	Max	Units
LOW level input voltage	-0.3		0.8	V
HIGH level input voltage	2		5.5	
Threshold point	1.33	1.42	1.52	
Schmitt trigger low-to-high threshold	1.67	1.73	1.79	
Schmitt trigger high-to-low threshold	1.01	1.07	1.15	
Input leakage current	-10		+10	μA

Table 23: Main signal levels

8 Mechanical specification

8.1 Physical specification

Venice 6 is a single-sided assembly built on to a 6-layer printed circuit board. The RF and baseband circuitry are shielded to meet EMC and RF performance specifications. The shielding separates the RF and baseband sections.

The module has a 64-way (2 x 32-way) 2.54 mm pitch, main connector mounted along one edge. This allows the use of either vertical or right angle mount connectors.

8.2 Physical layout

The following diagrams show the placement of the major components when viewed from the top and the dimensions in mm.

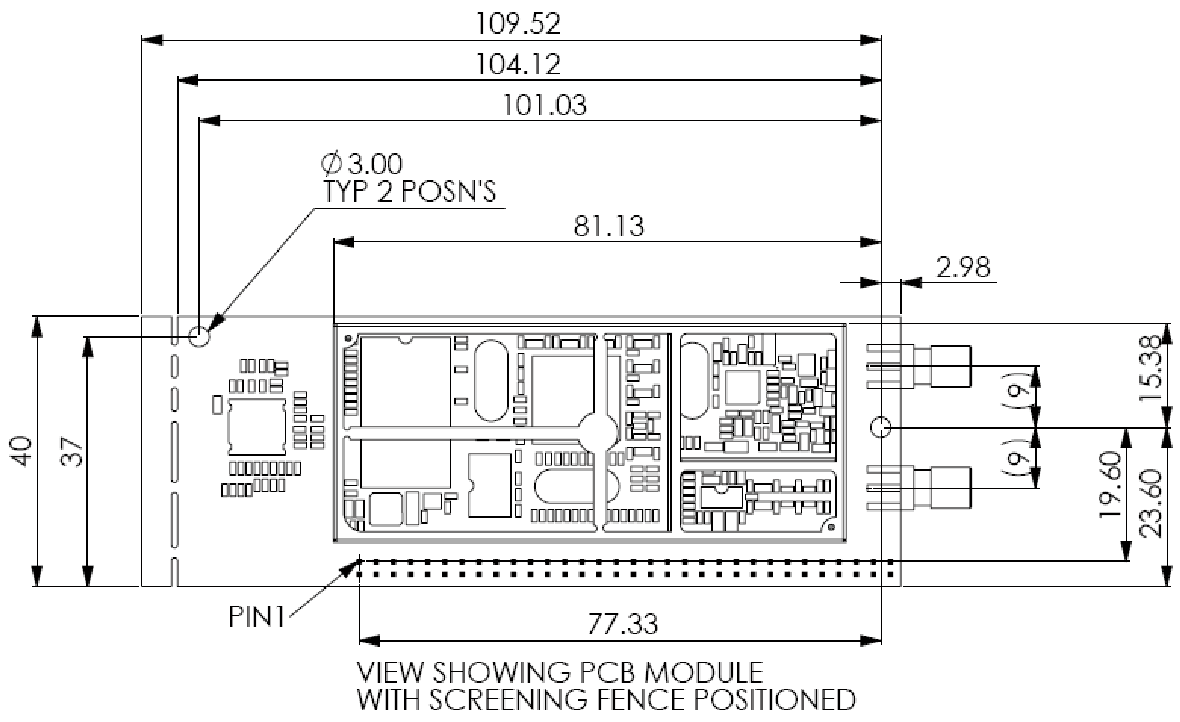


Figure 6: Board dimensions, top view

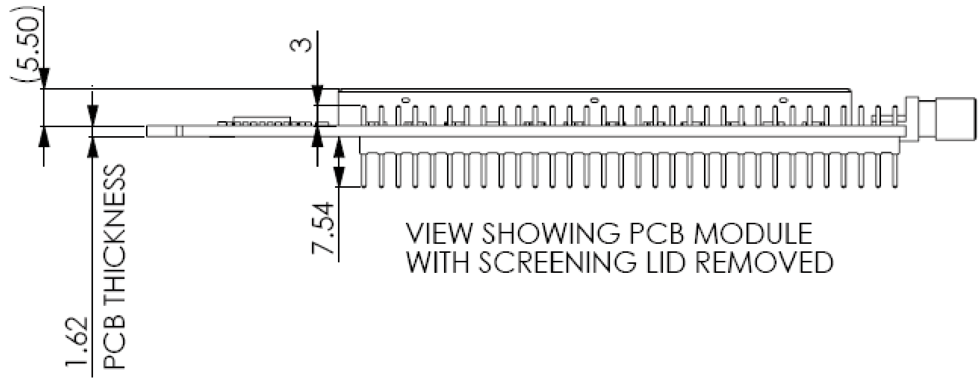


Figure 7: Board dimensions, side view

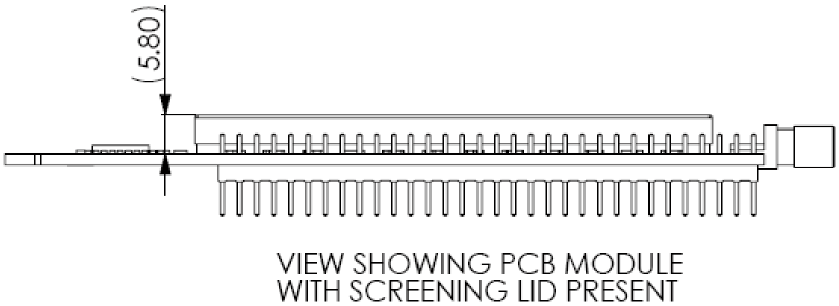


Figure 8: Overall height with screen can lid fitted

8.3 Connectors

The module supports three connectors.

- J4/J6/J7 are the RF input connectors
  - J4 and J6 support 2.6 mm UMP, SMB, SMA and F-type connectors
  - J7 supports 2.6 mm UMP and SMA connectors
- J2 (DASH debug connector) is offered as an optional extra on production units.
- J1 is the main connection to Venice 6 and carries all logic and power connections.

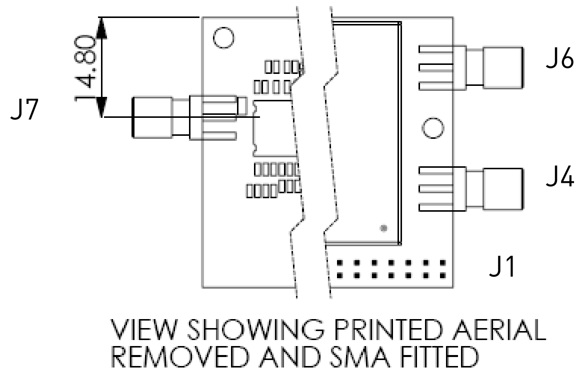


Figure 9: Module connector locations, top view

8.3.1 J1 - main connector

J1 is a 2 x 32-way dual row and 2.54 mm pitch, through PCB part.

8.4 Mating connectors

The following items are the female connectors that we recommend for placement on a customer application.

Manufacturer	Part number	Type
Imperial	J4A-301S-320-B	64-way Through-hole mount female connector
Imperial	G7P-645-G	64-way Surface mount female connector

Table 24: Mating connectors

The mating connectors are shown in *Figure 10* and *Figure 11*. They have a limited number of cycles of operation before they wear out. We recommend that they are connected/disconnected no more than xx times. They are not Frontier Silicon parts and may be subject to change.

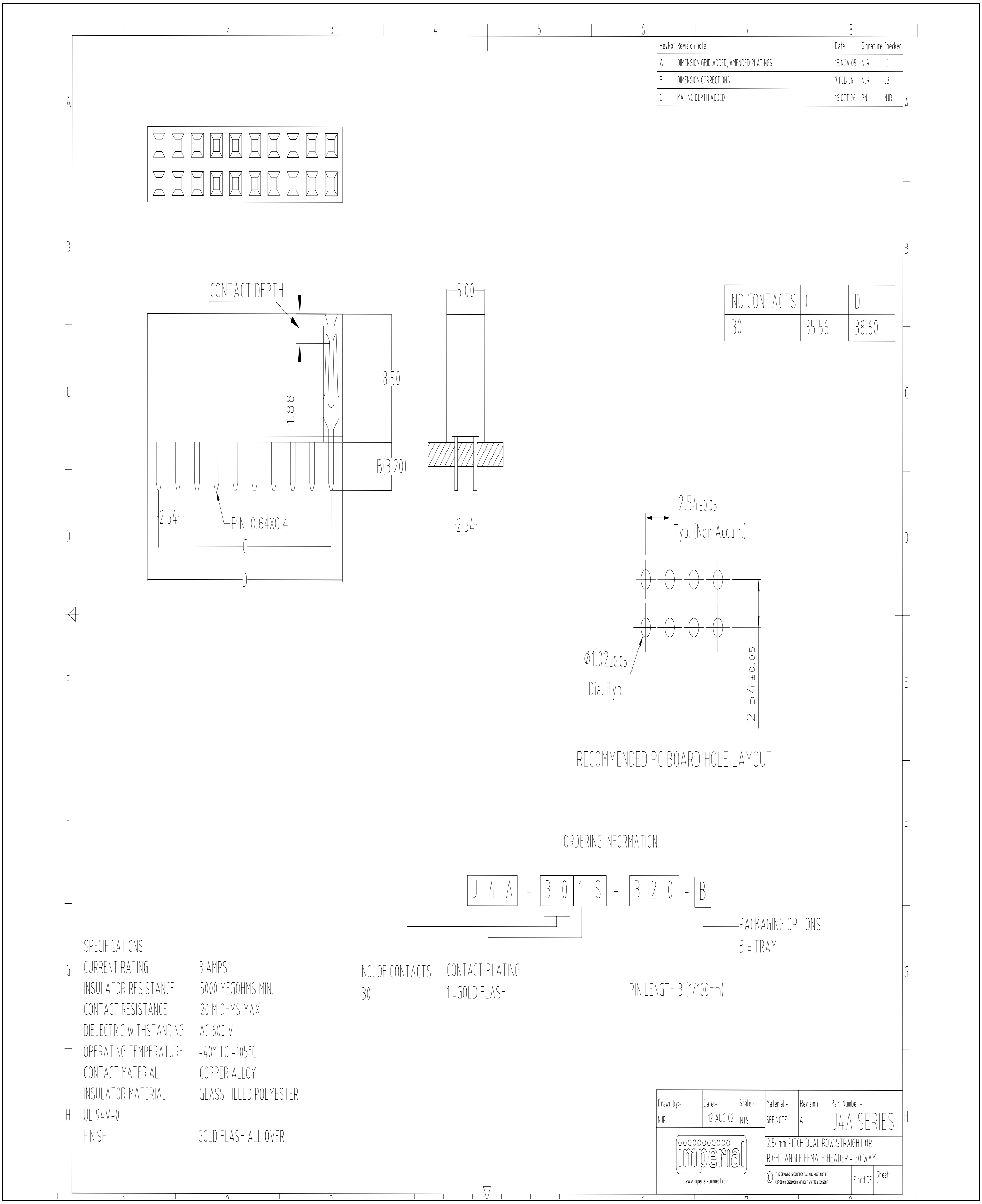


Figure 10: Mating connector J4A-301S-320-B

The G7P-645-G mating connector is shown in *Figure 11*.

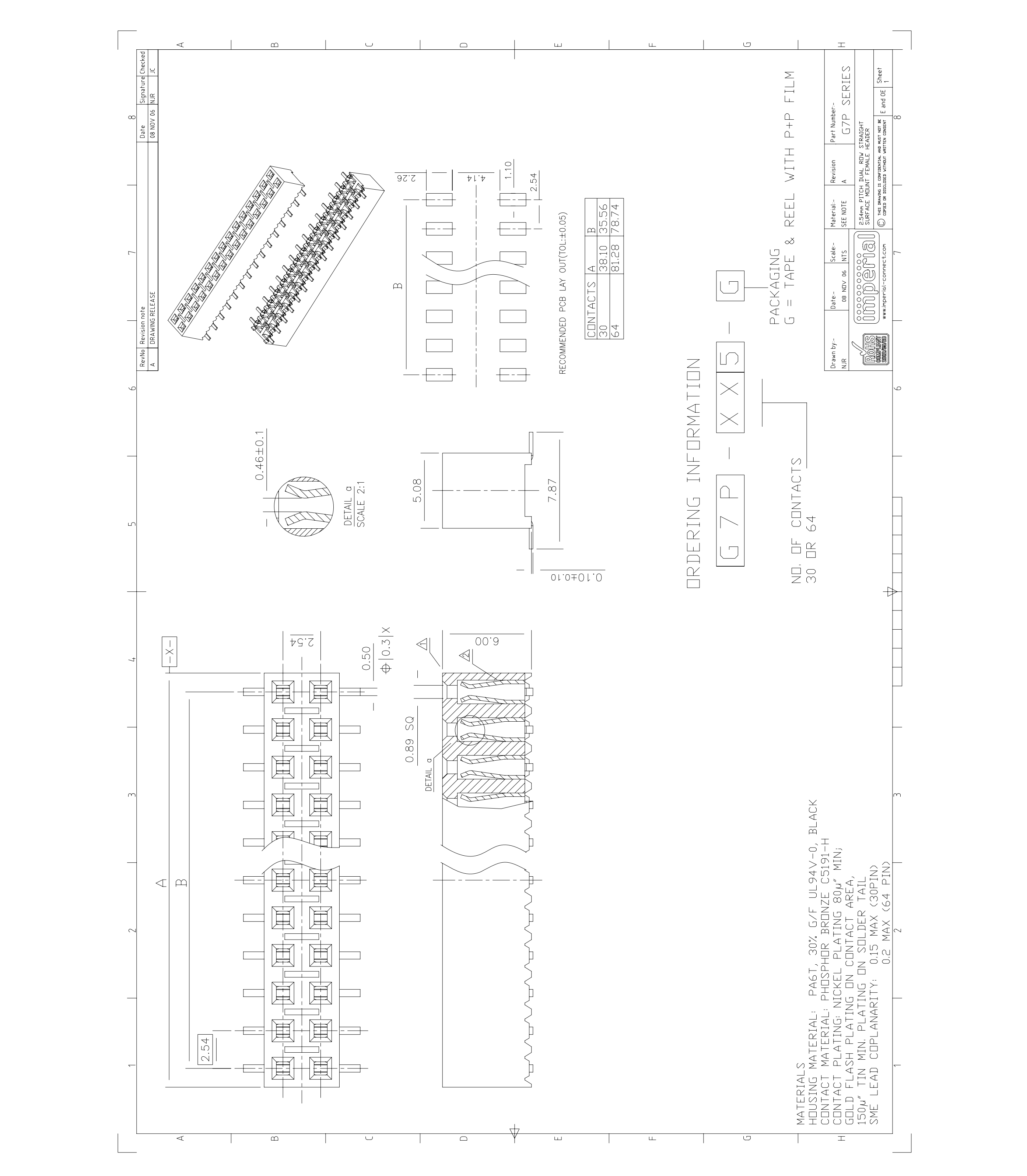


Figure 11: Mating connector G7P-645-G

Compliance standards

Electromagnetic compatibility (EMC)

Venice 6 is tested in configurations representative of typical DAB consumer products to the following standard:

BS EN 55022:1998

BS EN 55013: 2001

The electromagnetic compatibility of a particular product is dependent upon the use and installation of the module within the product. Care should be taken to integrate the module with due regard to the effects of conducted and radiated signals.

Electrostatic discharge (ESD) protection

Venice 6 is an ESD-sensitive device. It is tested to EN300.401. Special handling precautions should be used during manufacturing and testing. For example, use electrostatic controls compliant with *ANSI/ESD S20.20* *[reference 18]* or *JEDEC Standard JESD-625* *[reference 17]*.

Restriction of hazardous substances (RoHS)

All Frontier Silicon products use RoHS certified components and are assembled using lead-free processes; see the *Frontier Silicon Declaration of Materials Compliance* *[reference 2]*.

‘Green’ compliance

Frontier Silicon adheres to best industry practice regarding the avoidance of environmentally harmful substances in products, above and beyond legal requirements such as RoHS.

Bibliography

The following documents provide background, peripheral or more detailed information for Venice 6. They are not all specifically referenced within the text of this datasheet.

Domain		Document	
		Title	No
Frontier Silicon		1 Environmental Policy	FSQ 0000 0329
		2 Declaration of Materials Compliance	FSQ 0000 1008
	Venice 6 FS2026 Product description	3 Product Brief	FSQ 0000 1019
		4 Software Product Specification	-
	Chorus 2i FS1020 Highly Integrated DAB System-on-Chip	5 Product Brief	FSQ 0000 0604
		6 Overview Datasheet	FSQ 0000 1161
		7 Hardware Datasheet	FSQ 0000 1346
	Apollo FS1110 Tri-Band Dual-Mode T-DMB Radio Receiver IC	8 Product Brief	FSQ 0000 0626
		9 Datasheet	FSQ 0000 0612
British Standards		10 Characteristics of DAB Receivers	BS EN 50248:2001
		11 Methods of measurement on radio receivers for various classes of emission	BS 60315-4
		12 High fidelity audio equipment and systems; minimum performance requirements.	BS 5942-2:1987
		13 Digital Audio Interface, parts 1 and 3	IEC 60958
		14 Information technology equipment. Radio disturbance characteristics. Limits and methods of measurement	BS EN 55022:1998
		15 (Incorporating Corrigendum No 1). Sound and Television Broadcast Receivers and associated equipment - Radio disturbance characteristics - Limits and methods of measurement.	BS EN 55013: 2001
JEDEC		16 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)	JESD22-A114
		17 Requirements For Handling Electrostatic-discharge-sensitive (ESDS) Devices	JESD625
EDA (Electrostatic Discharge Association)		18 ESD Association Standard for the Development of an Electrostatic Discharge Control Program for – Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)	ANSI/ESD S20.20

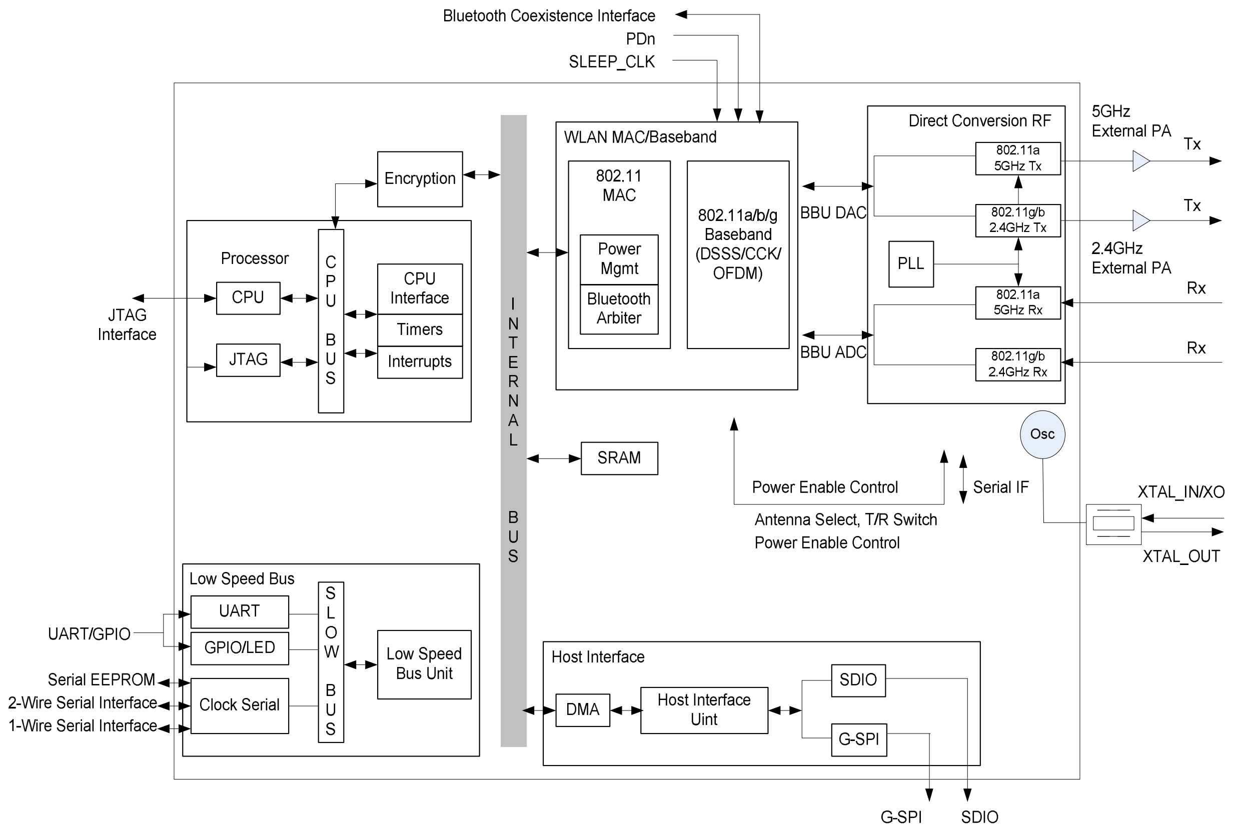
Table 25: References

Glossary

CPU	Central Processing Unit
DAB	Digital Audio Broadcasting
DMB	Digital Multimedia Broadcasting
FMI	(NAND) Flash Memory Interface
GPIO	General Purpose Input/Output
IC	Integrated Circuit
NAND	NOT AND (Boolean logic)
PC	[Wintel-compatible] Personal Computer
SCP	Serial Control Protocol
SPI	Serial Peripheral Interface
SPI master	Provides SPI clock and initiates data transactions and requests
SPI slave	Receives SPI clock and responds to data transactions and requests
SRAM	Static Random Access Memory
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus

RF Chipset Descriptions

The Marvel 88W8686 RF chipset provides the combined functions of the IEEE Standard 802.11/802.11b Direct Sequence Spread Spectrum (DSSS), 802.11a/g (802.11a is not used in this product) Orthogonal Frequency Division Multiplexing (OFDM) baseband modulation, Medium Access Controller (MAC), CPU, memory, host interfaces, and direct conversion WLAN RF radio on a single integrated chip. The block diagram of the RF chipset is shown in Fig. 3.



Block diagram of 88W8686

Main Features

General Features

- 802.11b/g wireless RF and baseband, MAC, CPU, memory, and host interfaces
- Integrates all RF to baseband transmit and receive operations, with support for external PAs

Payload Data Rates

- IEEE 802.11 data rates of 1 and 2 Mbps
- IEEE 802.11b data rates of 5.5 and 11Mbps
- IEEE 802.11g data rates of 6, 9, 12, 18, 24, 36, 48, and 54 Mbps

Network

MAC

- Supports Ad-Hoc and Infrastructure modes
- Hardware filtering of 64 multicast and 96 unicast addresses and additional firmware options
- Supports long and short preamble generation on a frame-by-frame basis
- Supports IEEE Power Save mode

Security

- WEP 64- and 128-bit encryption with hardware TKIP processing
- WPA (Wi-Fi Protected Access)
- CCMP hardware implementation as part of 802.11i security standard

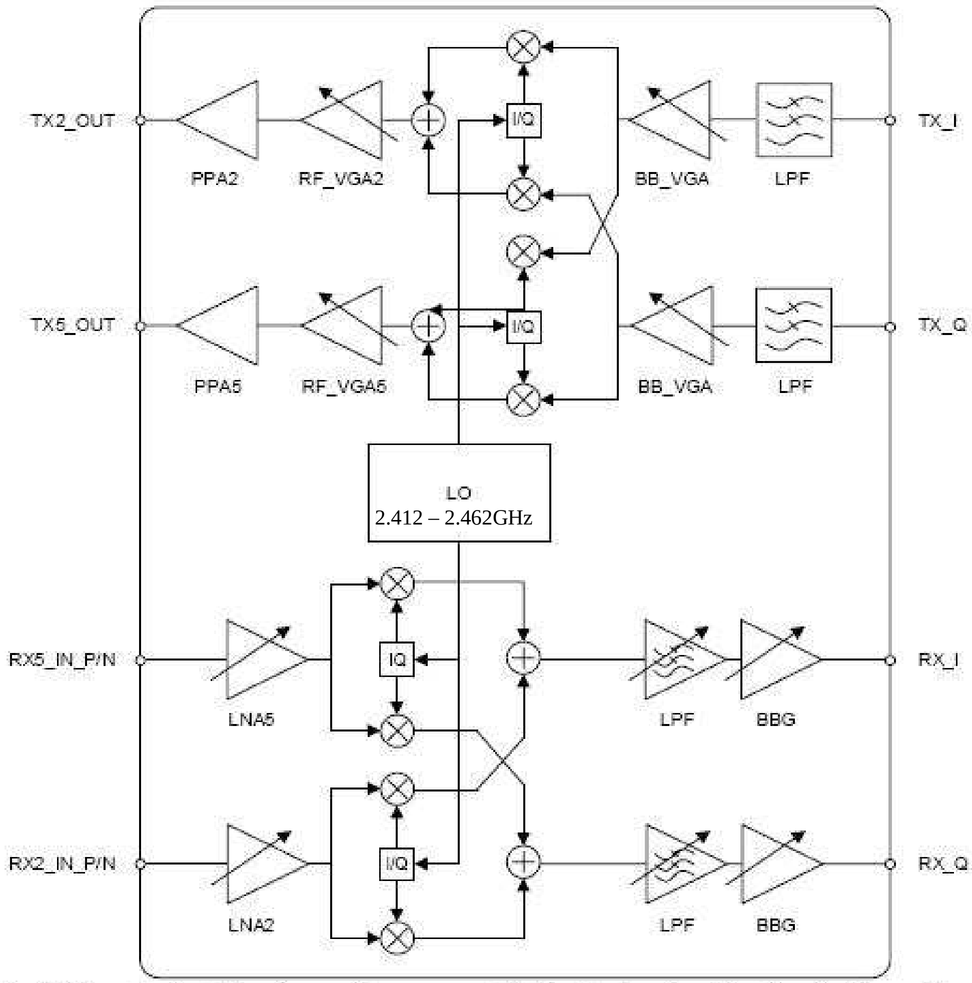
Physical Layer

Baseband

- DSSS and OFDM modulation
- Advanced Equalizer for Complementary Code Keying (CCK) modes

CPU

- Integrated S3C2440A (ARM9) -Compliant Marvell Feroceon CPU
- 400 MHz operating frequency



The LNAs and adjustable gain amplifiers are controlled by the baseband functionality. Channel frequencies are controlled through an internal serial bus, programmed through software.

Simplified Radio Block Diagram

Radio Architecture

The 88W8686 direct conversion WLAN RF radio integrates all necessary functions for receive and transmit, including LNAs, up and down converters, adjustable gain amplifier, filter, and pre-drivers.

The supported frequency channels for operation in the 2.4 GHz ISM radio bands are shown in below table.

Channel	Frequency (GHz)	North America
1	2.412	X
2	2.417	X
3	2.422	X
4	2.427	X
5	2.432	X
6	2.437	X
7	2.442	X
8	2.447	X
9	2.452	X
10	2.457	X
11	2.462	X

Receive Path

The 88W8686 receiver consists of:

- 2.4 GHz LNA/quadrature down conversion mixers
- Variable gain amplifiers
- Pair of baseband LPFs
- Programmable gain amplifiers (analogue signal processing on the quadrature demodulated signals)

Receive Automatic Gain Control

The 88W8686 supports a proprietary AGC interface between the radio and baseband processor. To manage overall gain distribution, the total gain is distributed among the RF and baseband stages. The total gain is realized through variable gain stages within each of the RF, and baseband sections.

The gain adjustment of the integrated LNA and AGC is seamlessly controlled by the baseband processor functions integrated into the 88W8686. The entire receive path has over 90 dB of voltage gain and 90 dB of gain control range.

Baseband Circuits

The quadrature demodulator down converts and I/Q splits the signal received to in-phase and quadrature phase. Signals are then passed through a pair of LPFs to reject the adjacent channel energy, and a pair of variable gain stages amplifies the signal to the full scale of the analog to digital converters.

Both the corner frequency of the LPF and the offset of the baseband stages are calibrated automatically. These calibrations occur frequently enough to adjust for changes in environmental conditions.

Transmit Path

The transmit path includes:

- Pair of LPFs
- Pair of baseband variable gain amplifiers
- Quadrature up-converter
- RF variable gain amplifier
- 2.4 GHz preamplifier

Tx Radio Band Operation

The variable gain amplifier is used for power control. The preamplifier is designed to support a wide range of external power amplifiers. The embedded power control loop is also flexible enough to accept a wide range of power detector characteristics.

Tx Power Control

The transmitter signal path is affected by changes in environmental conditions and the accuracy of external components. Therefore, proper gain control is required to account for gain variations in the transmit signal path due to temperature and process variations.

Gain control is accomplished with a power control loop circuit. The loop consists of a power detector that monitors the actual PA output during every Tx packet and compares that level with a power detect threshold. That gain is then adjusted on the next Tx packet.

The power of each WiFi module is calibrated to the value in module specification and the gain setting is stored in EEPROM. This gain setting limits the maximum power transmission that is guaranteed to be lower than the test mode samples.