580MHz MIPS® Core
IEEE 802.11 b/g/n 2x2 MIMO Wi-Fi
20MHz, 130Mbps
Network Media Module

Product Data Sheet
Module : LS6-N22S

Rev: 3.7

1. Introduction

Libre LS6-N22S is a complete network media module. It includes an 802.11n MAC and baseband, a 2.4 GHz 2x2 MIMI radio and FEM, a 580MHz MIPS® 24K™ CPU core, with supporting FLASH and DRAM memory. The module also includes all the necessary I/O and control interfaces required to build feature rich networked media products, yet cost effective with very little additional electronic design.

The embedded high performance CPU can process many advanced applications, such as network media streaming, rendering, routing, security and special advanced Libre technology features. The LS6-N22S also includes a selection of interfaces to support a variety of applications, such as I2S audio interface, a USB port and SD port for accessing external storage, SPI and UART for data and control.

Combined with the extensive LibreSync software, this small form factor and low cost design provide excellent Wi-Fi and processing performance for the wireless connectivity required in today CE products.

2. Module Feature Summary

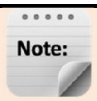
Key Features

- Embedded MIPS24KEc (580 MHz) with 64 KB I-Cache and 32 KB D-Cache
- 2T2R 2.4 GHz with 130 Mbps PHY data rate
- Legacy 802.11b/g and HT 802.11n modes
- 20 MHz channel bandwidth
- Libre's advanced multi-zone audio streaming technology
- Reverse Data Grant (RDG)
- Maximal Ratio Combining (MRC)
- Space Time Block Coding (STBC)
- 16-bit DDR2 64Mbytes
- Serial Flash 16Mbytes
- SPI, SD-XC
- 1x USB 2.0
- An optimized PMU

- Green AP
- Intelligent Clock Scaling (exclusive)
- DDR2: ODT off, Self-refresh mode
- I2C, I2S, SPI, UART, JTAG, GPIO
- I2S interface supports 16-bit/96kHz (slave mode)
- Hardware NAT with IPv6
- WEP64/128, TKIP, AES, WPA, WPA2, WAPI
- QoS: WMM, WMM-PS
- WPS: PBC, PIN

3. LibreSync Features

LibreSync modules have extensive software features for connected media streaming and control applications. These include system level control and interface features as well as networking features.
Please refer to the full "LibreSync Feature List" for details of supported features.



Platform features can vary based on module configuration/derivatives and commercial engagement details.

4. Block Diagram

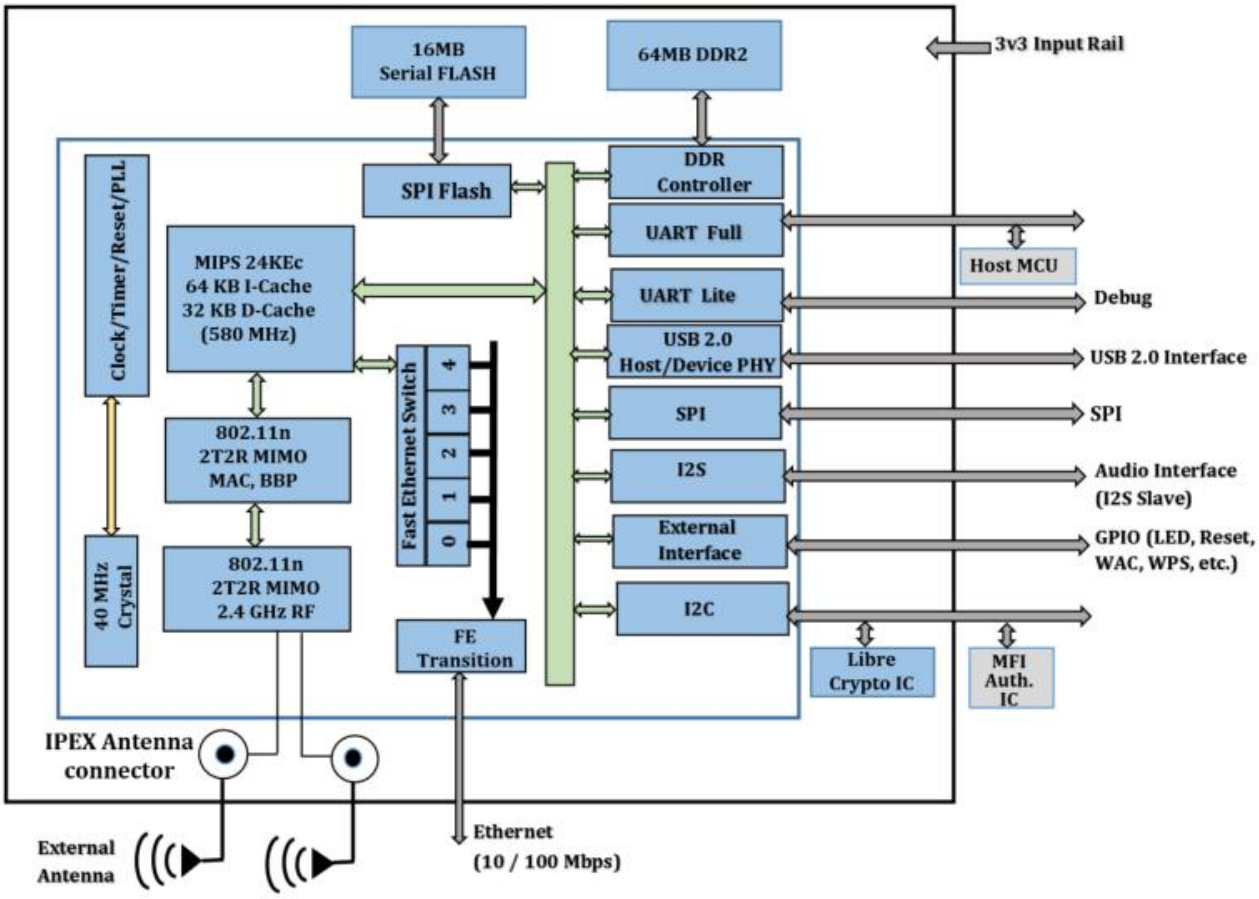


Figure 4-1: LS6-N22S Block Diagram

5. Specifications

5.1. General Specification

Parameter	Description / Values
Model	LS6-N22S
Product Name	LibreSync LS6 Network Media Module
Chipset	MT7620A
Standard	Wi-Fi – IEEE802.11b, IEEE802.11g, IEEE802.11n, standards

Data Transfer Rate	1,2,5.5,6,11,12,18,22,24,30,36,48,54,60,90,120, and maximum of physical layer rate of 130Mbps
Frequency Band	2.4 GHz
Input Voltage	3.3 V ± 5 %
Operating Temperature	-20˚C to + 55˚C
Dimensions	40mm X 26mm X 5.1mm (L x W x H) ± 0.2mm

5.2. Wi-Fi Specification

Parameter	Description / Values
Standard	IEEE802.11b, IEEE802.11g, IEEE802.11n standards
Data Rate	• 802.11b : 11, 5.5, 2, 1 Mbps • 802.11g : 54, 48, 36, 24, 18, 12, 9, 6 Mbps • 802.11n : MCS 0 to 7 for HT20MHz
Modulation	• 802.11b : CCK, DQPSK, DBPSK • 802.11g : 64QAM, 16QAM, QPSK, BPSK • 802.11n : 64QAM, 16QAM, QPSK, BPSK
Network Architecture	• Ad-hoc mode (Peer-to-Peer) • Infrastructure Mode
Operation Channel	2.4GHz • 11: (Ch. 1-11) – United States • 13: (Ch. 1-13) – Europe
Frequency Range	2.412 ~ 2.483 GHz

Transmit Output Power	• 802.11b : < 19.5 dBm at 11Mbps • 802.11g : < 16.5 dBm at 54Mbps • 802.11n : < 15.5 dBm at MCS7
Receiver Sensitivity	• 802.11b : -84 dBm at 11Mbps • 802.11g : -73 dBm at 54 Mbps • 802.11n : -64 dBm at 130 Mbps (MCS7)
Security	WEP 64&128 bit, WPA, WPA-PSK, WPA2, WPA2-PSK, WPS, IEEE 802.1x, IEEE 802.11i
Current Consumption	• TX Mode : 420 mA • RX Mode : 220 mA

6. Mechanical, Connectors and Interfaces

6.1. Physical Module

Estimated at 40mm x 26mm x 5.1mm (L x W x H) ± 0.2mm

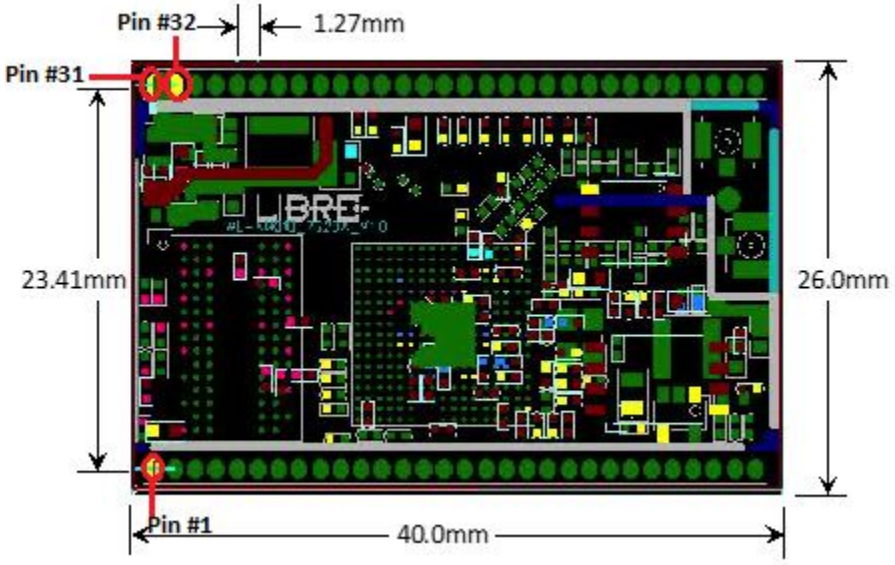


Figure 6-1: LS6-N22S Physical Dimensions

Note:

- Dimensions are in millimetres
- Dimensional tolerance is +/- 0.2mm
- PCB thickness is 1mm
- Design for 5.1mm physical Z height clearance (space for shields/clearance)

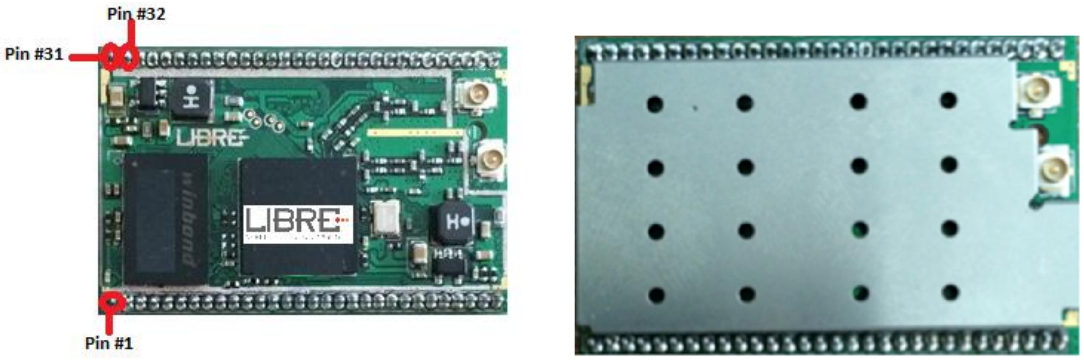
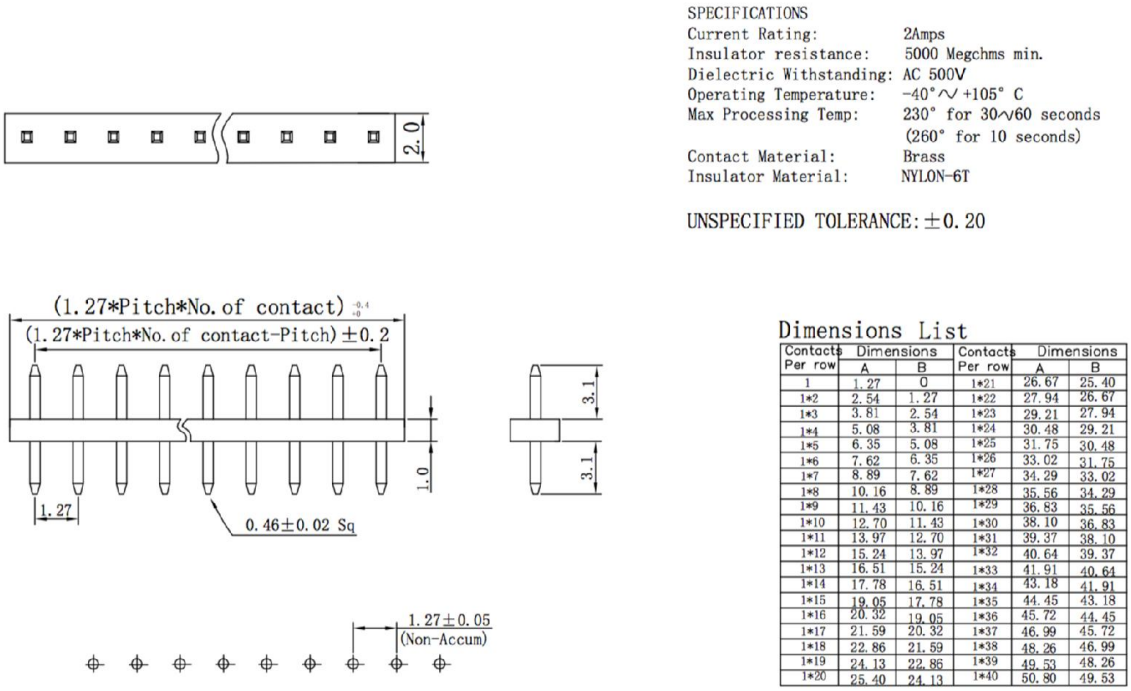


Figure 6-2: LS6-N22S Top View With and Without Shield

6.2. Connector Specification



Contacts Per row	Dimensions A	Dimensions B	Contacts Per row	Dimensions A	Dimensions B
1	1.27	0	1*21	26.67	25.40
1*2	2.54	1.27	1*22	27.94	26.67
1*3	3.81	2.54	1*23	29.21	27.94
1*4	5.08	3.81	1*24	30.48	29.21
1*5	6.35	5.08	1*25	31.75	30.48
1*6	7.62	6.35	1*26	33.02	31.75
1*7	8.89	7.62	1*27	34.29	33.02
1*8	10.16	8.89	1*28	35.56	34.29
1*9	11.43	10.16	1*29	36.83	35.56
1*10	12.70	11.43	1*30	38.10	36.83
1*11	13.97	12.70	1*31	39.37	38.10
1*12	15.24	13.97	1*32	40.64	39.37
1*13	16.51	15.24	1*33	41.91	40.64
1*14	17.78	16.51	1*34	43.18	41.91
1*15	19.05	17.78	1*35	44.45	43.18
1*16	20.32	19.05	1*36	45.72	44.45
1*17	21.59	20.32	1*37	46.99	45.72
1*18	22.86	21.59	1*38	48.26	46.99
1*19	24.13	22.86	1*39	49.53	48.26
1*20	25.40	24.13	1*40	50.80	49.53

Figure 6-3: LS6-N2SS Connector Specification

6.3. Pin Descriptions

6.3.1. Connector 1

Description	Function	MT7620A BALL	Pin
3.3VD	3.3VD		**1**
Ground	GND		**2**
I2C_Clock	I2C_SCK	U14	**3**
I2C_Data	I2C_SDA	T14	**4**
GPIO0/WPS	GPIO0	D7	**5**
POWER ON RESET I/P	PORST_N	C6	**6**
UART_TXD	UART_TXD1	T12	**7**
UART_RXD	UART_RXD1	T13	**8**
UART CTS	UART_CTS1	P11	**9**
UART RTS	UART_RTS1	U12	**10**
DEBUG-UART Lite TXD	UART_TXD2	P13	**11**
DEBUG-UART Lite RXD	UART_RXD2	R14	**12**
Ground	GND		**13**
12MHz_REFCLK_OUT	I2S_REFLCK	K14	**14**
I2S_RXD	I2SDI	P12	**15**
I2S_TXD	I2SWDO	U13	**16**
I2S_LRCLK	I2SWS	R12	**17**
I2S BIT CLOCK	I2SCLK	R13	**18**
Ground	GND		**19**
GPIO	GPIO24	H17	**20**

WLAN Activity LED	WLAN_ACT_LED	G4	**21**
GPIO	GPIO25	H16	**22**
GPIO	GPIO26	J17	**23**
Ground	GND		**24**
USB_DM	USB_D-	C16	**25**
USB_DP	USB_D+	C17	**26**
Ground	GND		**27**
WLAN ACTIVE(WLAN GRANT)	BT_WACT/GPIO58	T8	**28**
BT Auxiliary / FREQ	BT_AUX/GPIO57	U9	**29**
Bluetooth TX/RX	BT_STAT/GPIO56	T9	**30**

I2C_SCK & I2C_SDA requires 2.2K ohm resistor to be added to I2C interface.

6.3.2. Connector 2

Description	Function	MT7620A BALL	Pin
3.3VD	3.3VD		**31**
3.3VD	3.3VD		**32**
GND	Ground		**33**
SPCK	SPI_SPCK/GPIO4	D8	**34**
MOSI	SPI_MOSI/GPIO5	A8	**35**
MISO	SPI_MISO/GPIO6	C8	**36**
SPI-CS1	SPI_CS1/GPIO37	C9	**37**

GPIO/SPI_REQ	GPIO27	J16	**38**
Ground	GND		**39**
Port4 RX+	EPHY_RXP_P4	N16	**40**
Port4 RX+-	EPHY_RXN_P4	N17	**41**
Port4 TX+	EPHY_TXP_P4	M16	**42**
Port4 TX-	EPHY_TXN_P4	M17	**43**
Ground	GND		**44**
SD_WP	SD_WP/GPIO48	P10	**45**
SD_CD	SD_CD/GPIO50	P9	**46**
SD_D3	SD_D3/GPIO55	U10	**47**
SD_D2	SD_D2/GPIO54	T10	**48**
SD_D1	SD_D1/GPIO53	U11	**49**
SD_D0	SD_D0/GPIO52	T11	**50**
SD_CMD	SD_CMD/GPIO51	R10	**51**
SD_CLK	SD_CLK/GPIO49	R8	**52**
Ground	GND		**53**
WAC / factory default reset	GPIO28	G16	**54**
ETH_ACT_LED	EPHY_LED4	J4	**55**
GPIO	GPIO23	K15	**56**
IR INPUT	GPIO29	G17	**57**
BT ACTIVE (BT_REQ)	BT_ACT/GPIO47	R9	**58**

Ground	GND		**59**
BT Antenna SELECT	BT_ANT/GPIO59	U8	**60**

7. Design Recommendations

Boot strap signals as mentioned in the Table 7-1, should not be driven by external devices until the module (SoC) comes out of reset.

Typically 150 ms is the time taken to come out of the reset after power on of the module (SoC).

This mandates implementation of appropriate power sequencing mechanism on base-board. That is, there has to be 30ms delay between Supplying powers to LS module (SoC) and power to any other device on the base-board.

Boot Strap Signal	Description
WLAN_ACT_LED	Do not drive the pin LOW but this pin can be driven HIGH.
SPI_MOSI	Do not connect the pin to logic HIGH, but can be driven LOW.
SPI_CLK	Do not connect the pin to logic HIGH, but can be driven LOW.
UART_TXD2	Do not drive the pin LOW but this pin can be driven HIGH.

Table 7-1: Boot Strap Signal Requirement

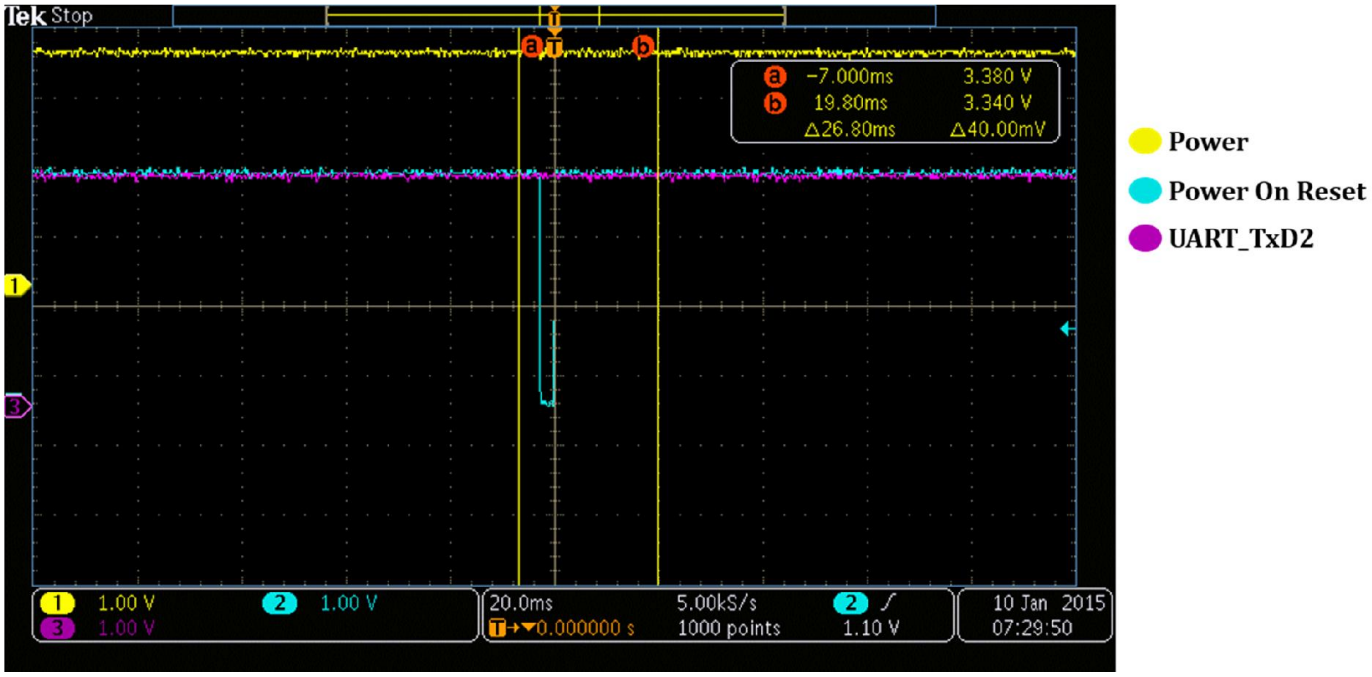


Figure 7-1: External Reset

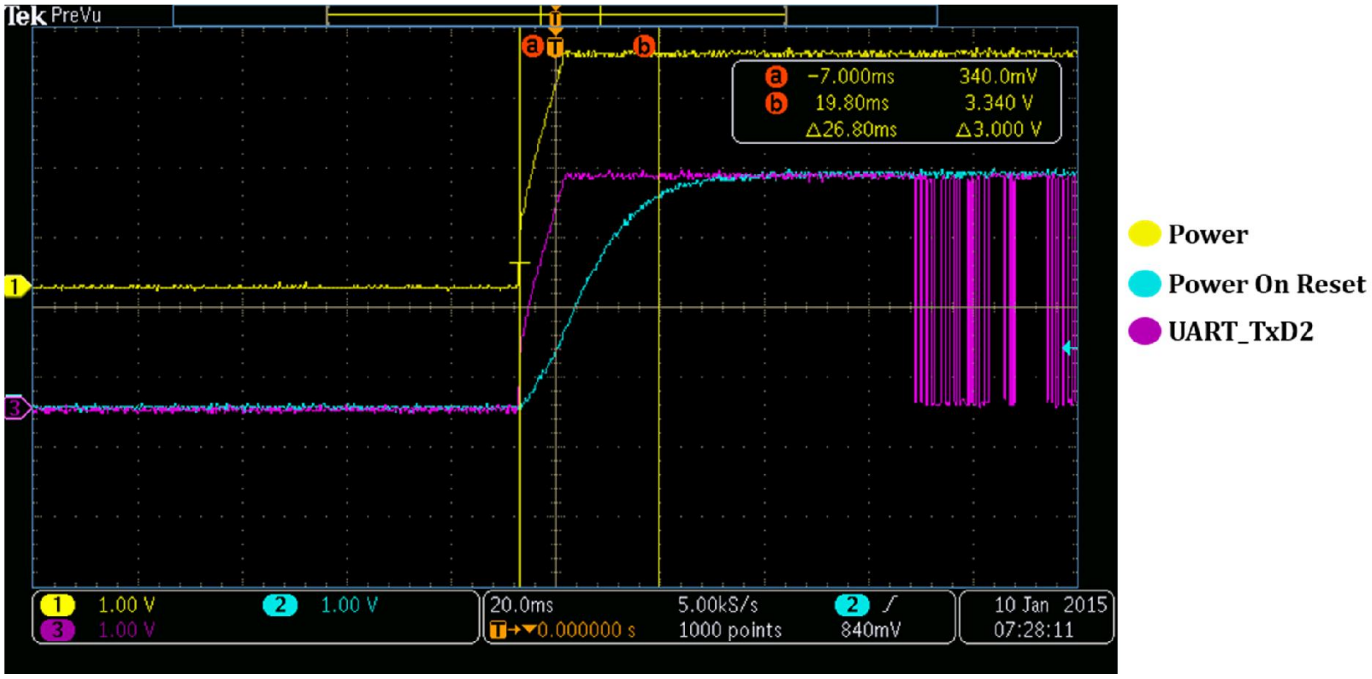


Figure 7-1: Power On Sequence

8. Environmental

8.1. Storage Conditions

The calculated shelf life in a sealed bag is 12 months if stored between 0°C and 40˚C at less than 90% relative humidity (RH).

After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

- Mounted within 168 hours in factory conditions, i.e. <30°C at 60% RH.
- Storage humidity needs to maintained at <10%RH.
- Baking is necessary if the customer exposes the component to air for over 168 hrs.
  - Baking conditions: 125°C for 8hrs.

9. Reference Schematics

9.1. SD Interface

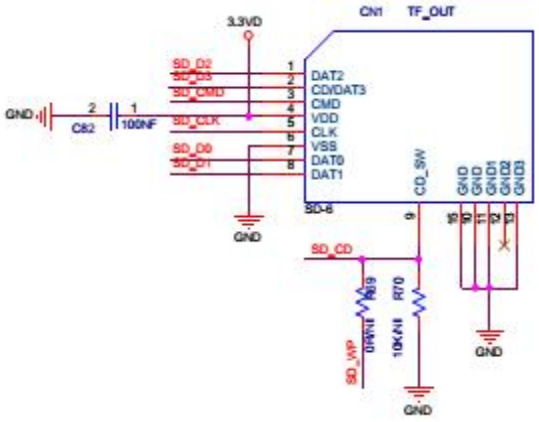


Figure9-1: SD Card

9.2. Reset and WPS

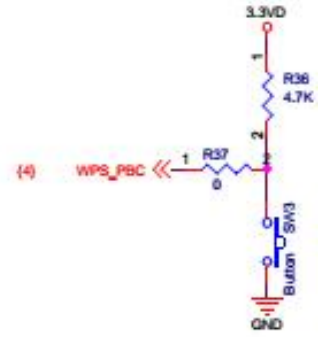


Figure 9-2: WPS

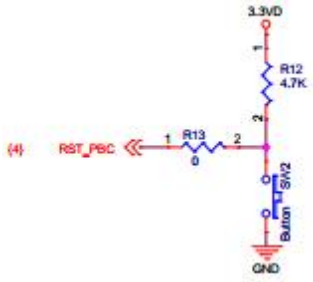


Figure 9-3: Reset

9.3. UART Interface

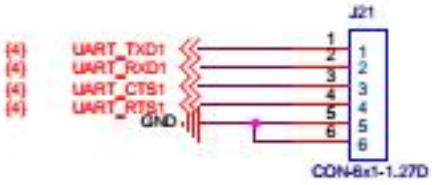


Figure 9-4: UART 1

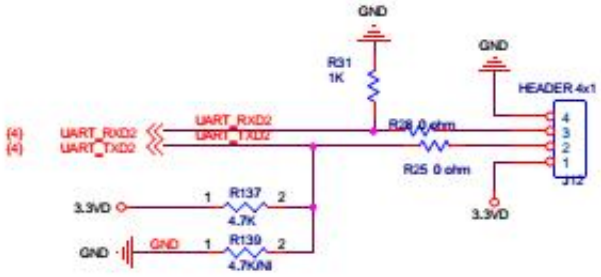


Figure 9-5: UART 2

9.4. USB Interface

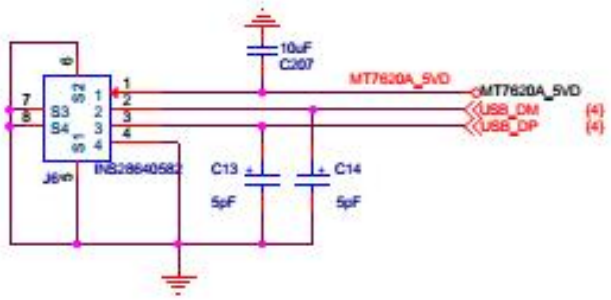


Figure 9-6: USB

9.5. Ethernet Interface

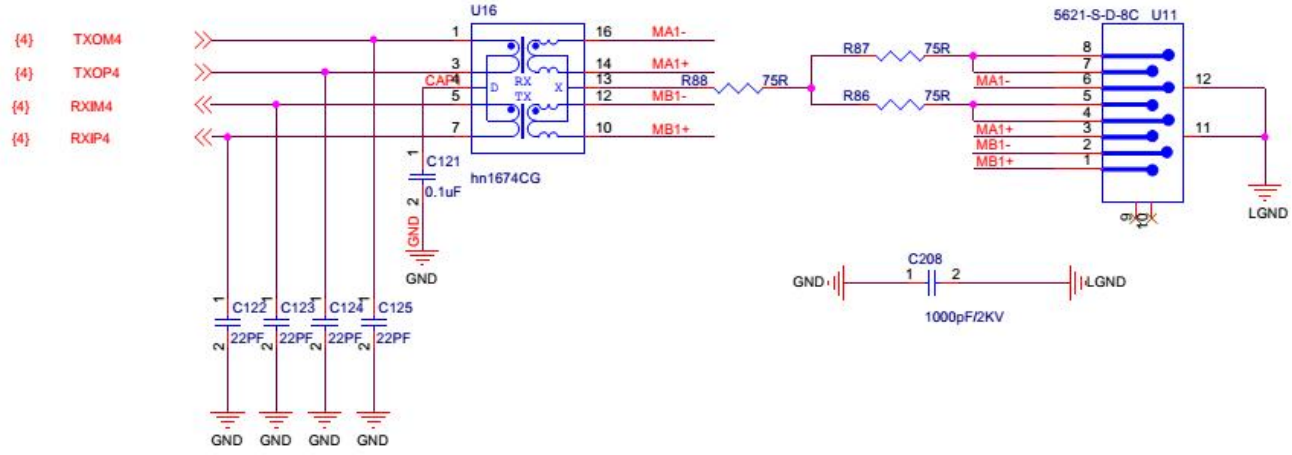


Figure 9-7: Ethernet

9.6. Power Supply

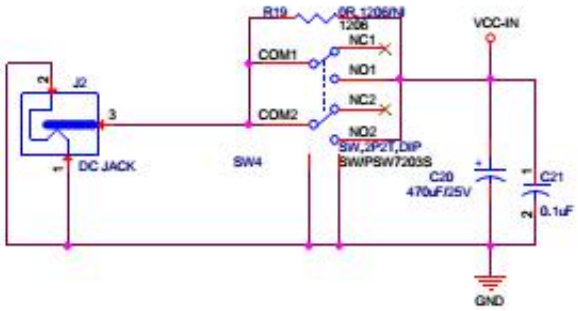


Figure 9-8: 9V DC Input

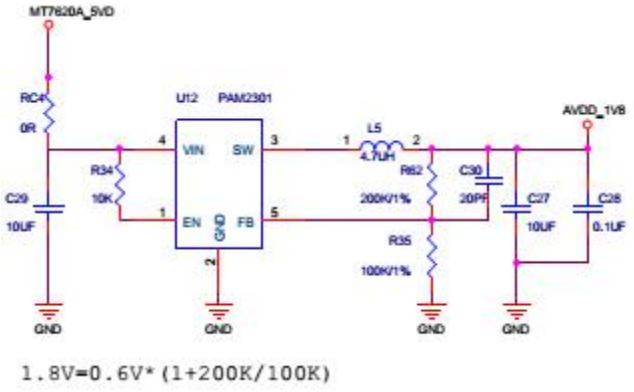


Figure 9-9: 1.8V DC Converter

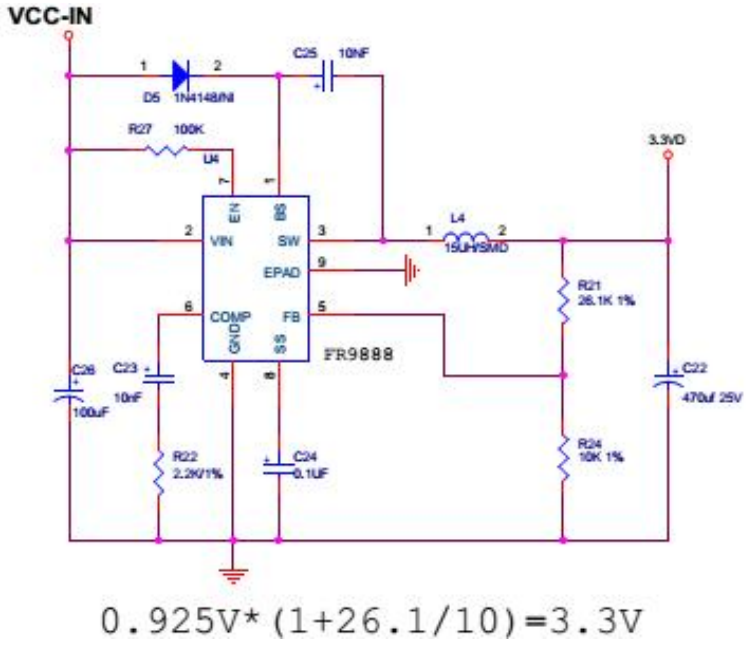


Figure 9-10: 3.3V DC Converter

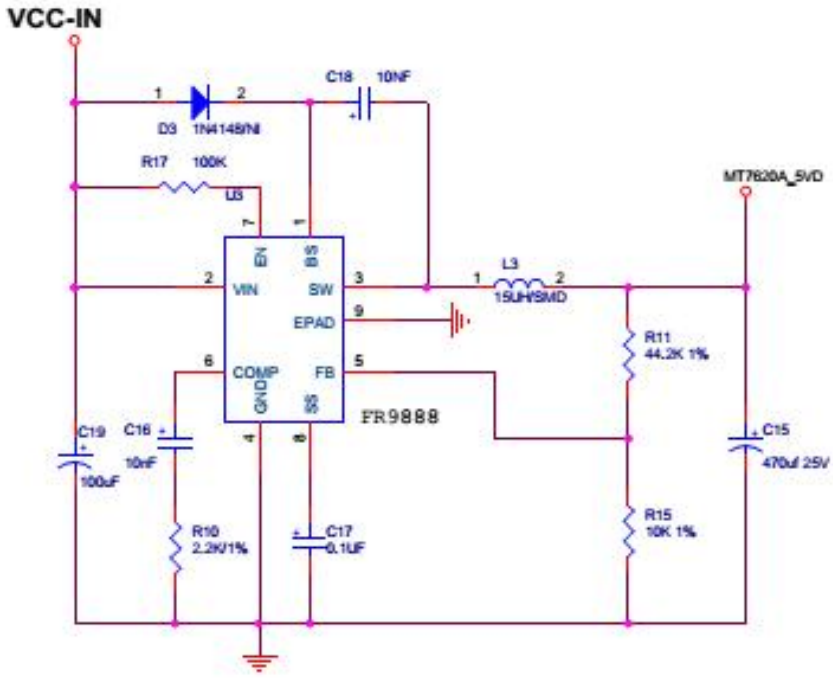


Figure 9-11: 5V DC Converter

9.7. MFI 2.0C Authentication Circuit

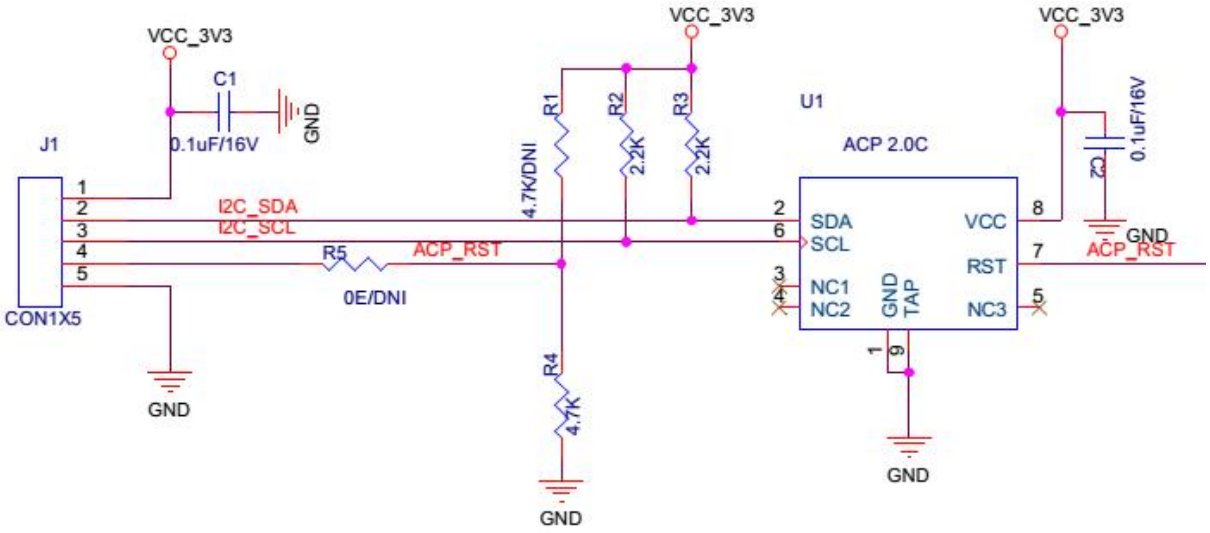


Figure 9-12: MFI 2.0C Authentication

10. Disclaimer

THE MATERIALS AND INFORMATION ARE PROVIDED “AS IS” WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A Pas RTICULAR PURPOSE OR NON-INFRINGEMENT.

We use reasonable efforts to include accurate and up-to-date information in this document. It does not however, make any representations as its accuracy or completeness of information. Use of this document is at your own risk. Libre Wireless Technologies, its suppliers, and other parties involved in creating and delivering this document’s contents shall not be liable for any special, indirect, incidental, or consequential damages, including without limitation, lost revenues or lost profits.