AW-GH381

IEEE 802.11 b/g Wireless LAN & Bluetooth Module IC

For Mobile Phones, DSCs, PMPs and Gaming Devices

Datasheet

Version 0.3

Document release	Date	Modification	Initials	Approved
Version0.1	2007/11/14	Initial Version	Ivan Chen	CE Huang
Version0.2	2008/2/29	New Function Block Base on 8688 B0	Ivan Chen	CE Huang
Version0.3	2008/3/4	Add Pin 63 SDIO multi-function selection	Ivan Chen	CE Huang

1. General Description

1-1. Product Overview and Functional Description

AzureWave Technologies, Inc. introduces the first IEEE 802.11b/g WLAN &Bluetooth combo module IC---**AW-GH381**. The module IC is targeted to mobile devices including **Mobile Phones, Digital Still Cameras (DSCs), Portable Media Players (PMPs), Personal Digital Assistants (PDAs), and Gaming Devices** which need small footprint package, low power consumption, multiple interfaces and OS support. By using AW-GH381, the customers can easily enable the Wi-Fi and BT embedded applications with the benefits of **high design flexibility, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11b/g standard, the AW-GH381 uses Direct Sequence Spread Spectrum (**DSSS**), Orthogonal Frequency Division Multiplexing (**OFDM**), **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-GH381. In addition to the support of **WPA/WPA2** and **WEP** 64-bit and 128-bit encryption, the AW-GH381 also supports the **IEEE 802.11i** security standard through the implementation of **Advanced Encryption Standard** (**AES)/Counter Mode CBC-MAC Protocol (CCMP),** and **WEP** with **TKIP** security mechanisms. The AW-GH381 also supports **IPSec** with **DES/3DES/ASE** encryption and **MD5/SHA-1** authentication.

For the video, voice and multimedia applications the AW-GH381 support **802.11e Quality of Service** (**QoS).**

For Bluetooth operation, the AW-GH381 is **Bluetooth 2.1+Enhanced Data Rate (EDR)** compliant.**. Bluetooth 2.1+Enhanced Data Rate (EDR)** can make it **easier to connect devices, lower power consumption and improved security**. The customer can base on different system to select WLAN/BT single antenna or WLAN/BT use different antennas.

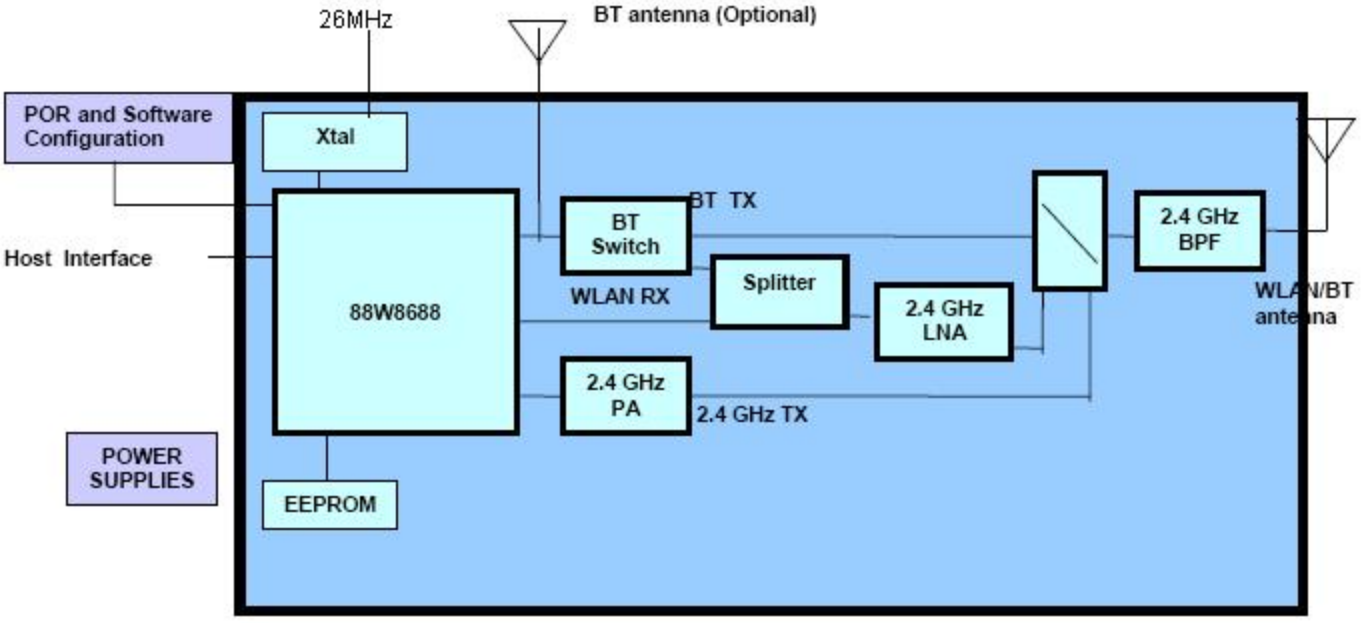
The AW-GH381 supports **SDIO** and **G-SPI** for WLAN to the host processor. **High speed UART, PCM/Inter-IC Sound(I^2S)** interface are available to connect the BT core the host processor**.** AW-GH381 is suitable for multiple mobile processors for different applications. With the support **cellular phone co-existence**, the AW-GH381 is also the best solution for mobile phones and PDA phones applications.

AW-GH381 module adopts Marvell's latest highly-integrated WLAN & Bluetooth SoC---**88W8688**. All the other components are implemented by all means to reach the mechanical specification required. AW-GH381 uses **IC module integration package** technology that provides customers mounting mechanism to secure the AW-GH381 module against vibration and shock on the host system. AW-GH381 uses module IC integration package technology can provide more **reliable** and **strong** electrical and mechanical performance.

1-2. Key Features

- Small footprint: 9.6mm(L) x 9.6mm(W) x 1.3 mm(H)
- SDIO, G-SPI interfaces support for WLAN
- High speed UART,PCM/Inter-IC Sound(I^2S) for Bluetooth
- Audio Codec interface support
- Cellular phone co-existence support
- Multiple power saving modes for low power consumption
- IEEE 802.11i for advanced security
- Quality of Service (QoS) support for multimedia applications
- WLAN drivers for Vista, WinXP, WinCE, Linux 2.6, WinMobile 5.0/6.0
- BT Profile Stacks:iAnywher(ESI) stacks for Linux and Windows Mobile,,Linux BlueZ stack, Win Mobile Native stack, Vista Natvie stack
- Lead-free design

A simplified block diagram of the AW-GH381 module is depicted in the figure below.



Power Consumption	**TBD**
Operating Range	**Open Space: ~300m ; Indoor: ~100m for WLAN Minimum 10 m indoor for Bluetooth The transmission speed may vary according to the environment)**
Security	**◆ WEP 64-bit and 128-bit encryption with H/W TKIP processing ◆ WPA/WPA2 (Wi-Fi Protected Access) ◆ AES-CCMP hardware implementation as part of 802.11i security standard**
Operating System Compatibility	**Win CE 4.2/.NET, Win CE 5.0, Linux, Pocket PC 2004/2005**
Co-Existence	**Bluetooth and cell phone(GSM/DCS/WCDMA/UMTS/3G) co-existence**

2. Electrical Characteristics

2-1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Units
3.3V_PA	PA power supply			3.3	4.6	V
3V_IO	Digital I/O power supply			3.0	4.2	V
VIO_X1	Host I/O power supply			1.8	2.3	V
				3.3	4.2	
VIO_X2	Digital power supply			1.8	2.3	V
				3.3	4.2	
VDD18_X3	Internal voltage power supply			1.8	2.3	V
VDD18A	Analog I/O power supply			1.8	2.3	V
1.2_EXT	Digital power supply			1.2	1.35	V

2-2. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
3.3V_PA	PA power supply		3	3.3	3.6	V
3V_IO	Digital I/O power supply		2.7	3	3.3	V
VIO_X1	Host I/O power supply		1.62	1.8	1.98	V
			2.97	3.3	3.63	
VIO_X2	Digital power supply		1.62	1.8	1.98	V
			2.97	3.3	3.63	
VDD18_X3	Internal voltage power supply		1.62	1.8	1.98	V
VDD18A	Analog I/O power supply		1.7	1.8	1.9	V
1.2_EXT	Digital power supply		1.14	1.2	1.32	V

2-3. Clock Specifications

AW-GH381 has internal reference clock source. The frequency is 38.4MHz. When you first time samples run the product. Please keep OSC signal outside the module.

38.4 MHz Clock Timing

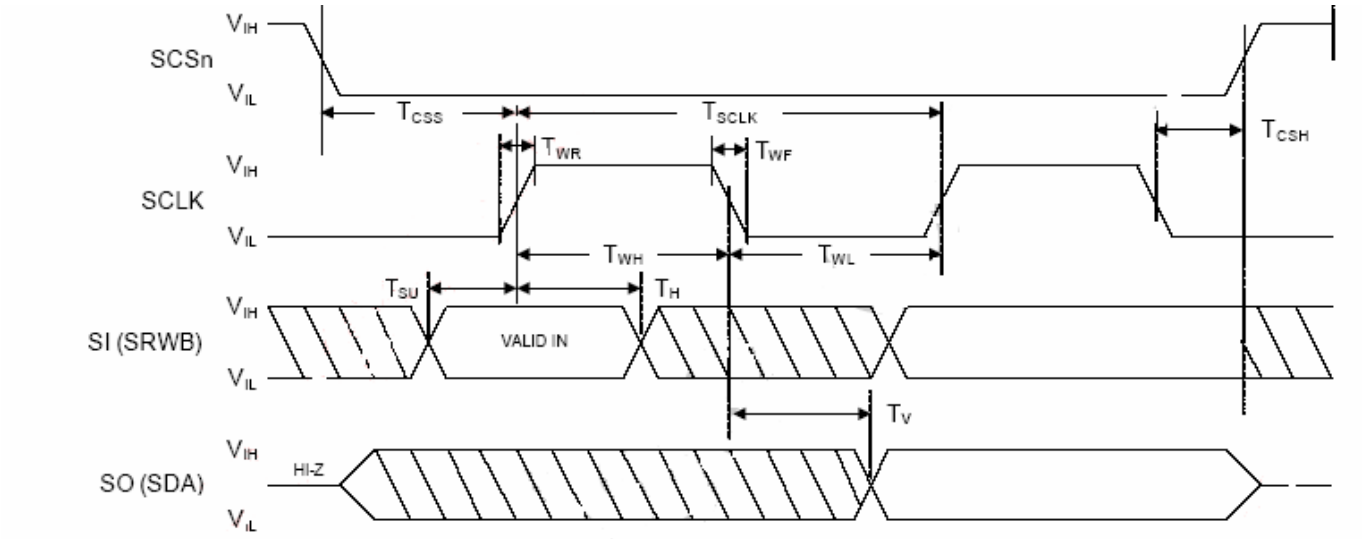
Note: Over full range of values specified in the Recommended operating conditions unless otherwise specified

Symbol	Parameter	Condition	Min	Typical	Max	Units
TP_xo38.4	XO38.4 period		26.042-20ppm	26.042	26.042+20ppm	ns
TH_xo38.4	XO38.4 high time		10.4168	13.021	15.6252	ns
TL_xo38.4	XO38.4 low time		10.4168	13.021	15.6252	ns
TR_xo38.4	XO38.4 rise time				5	Ns
TF_xo38.4	XO38.4 fall time				5	ns

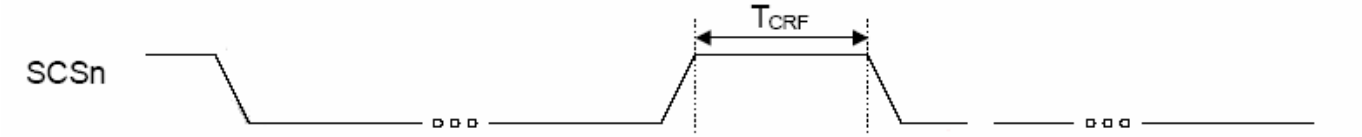
2-5. G-SPI Host Interface Specifications

Referred from Marvell hardware specifications

G-SPI Host Interface Transaction Timing



G-SPI Host Interface Inter-Transaction Timing



SPI Host Interface Timing Data

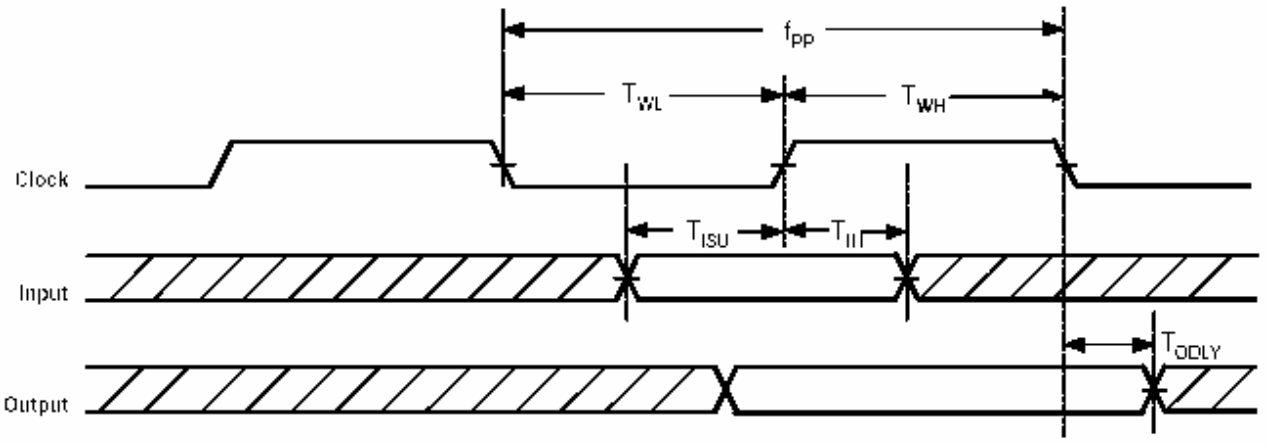
Over full range of values specified in the recommended operating conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SCK}	Clock Period		20			ns
T_{WH}	Clock high		5			
T_{WL}	Clock Low		9			
T_{WR}	Clock Rise Time				1	
T_{WF}	Clock Fall Time				1	
T_{H}	SDI Hold Time		2.5			
T_{SU}	SDI Setup Time		2.5			
T_{V}	SDO Hold Time		5			
T_{CSS}	SCSn Fall to Clock		5			
T_{CSH}	Clock to SCSn Rise		0			
T_{CRF}	SCSn Rise to SCSn Fall		400			

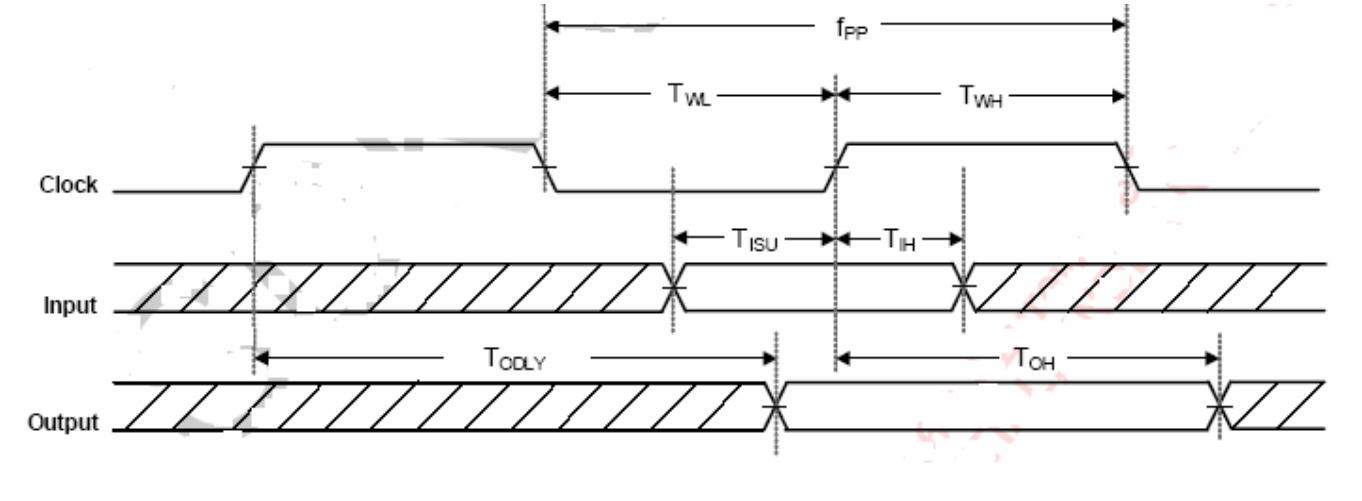
2-6. SDIO Host Interface Specifications

Referred from Marvell hardware specifications

SDIO Protocol Timing Diagram



SDIO Protocol Timing Diagram—High Speed Mode



SDIO Timing Data

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{pp}	CLK Frequency	Normal	0		25	MHz
		High Speed	0		50	
T_{WH}	CLK High Time	Normal	10			ns
		High Speed	7			
T_{WL}	CLK Low Time	Normal	10			
		High Speed	7			
T_{ISU}	Input Setup Time	Normal	5			
		High Speed	6			
T_{IH}	Input Hold Time	Normal	5			
		High Speed	2			
T_{ODLY}	Output Delay Time		0		14	
T_{OH}	Output Hold Time	High Speed	2.5			

2-7. Audio CODEC Interface

The AW-GH381 Audio Interface Unit(AIU) consists of an audio interface module.

2-7-1 Audio Interface

The Audio Interface in the AIU is an interface bridge between industry Audio CODECs and the AW-GH381.

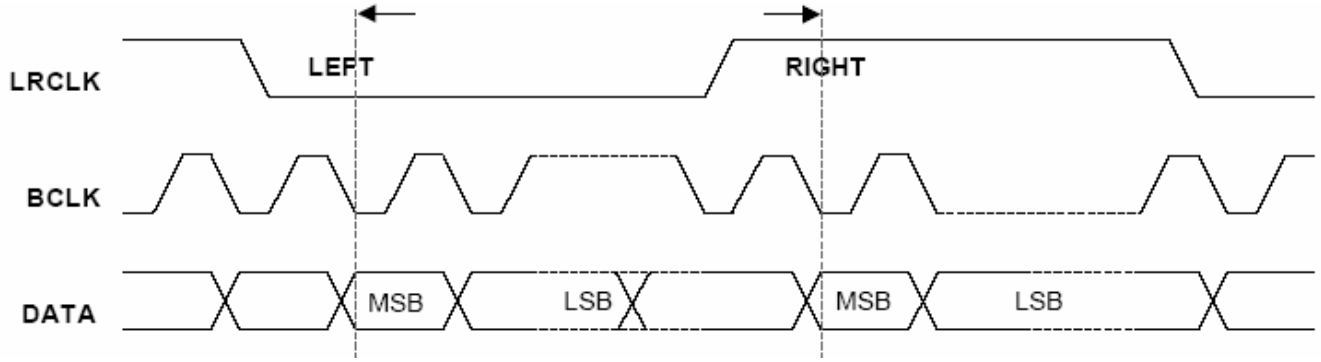
It interface with the Audio CODEC through I^2S, MSB-justified, LSB-justified or IEC60958 Compatible Audio CODEC Interface.

2-7-1.1Audio interface Signals

Pin No	Definition	Basic Description	Type	
28	BT_PCM_DOUT/ I2S_DOUT/ GPIO(12)	**PCM Mode**:BT_PCM_DOUT BT_PCM_DOUT output **AIU Mode:** I2S_DOUT I2S Audio output data(for playback)	I/O	
50	AIU_SPDIF/ GPIO(16)	**AIU Mode**:AIU_SPDIF,IEC60958 Compatible Audio CODEC Interface output data(for playback)	O	
54	BT_PCM_CLK/ I2S_BCLK/ GPIO(13)	**PCM Mode**:BT_PCM_CLK BT_PCM_CLK input/output output if device PCM master; input if device PCM slave) **AIU Mode**:12S_BCLK 12S Audio bit clock	I/O	
56	BT_PCM_SYNC/ I2S_LRCLK/ GPIO(14)	**PCM Mode**:BT_PCM_SYNC BT_PCM_SYNC input/output(output if PCM initiator, input if PCM target) **AIU Mode**:12S_LRCLK 12S Audio left/right clock	O	
57	BT_PCM_MCLK/ I2S_CCLK/ GPIO(15)	**PCM Mode**:BT_PCM_MCLK(optional) :BT_PCM_MCLK output Optional clock used for some CODECs **AIU Mode**:12S_CCLK Audio CODEC main clock	O	
58	BT_PCM_DIN/ I2S_DIN/ GPIO(11)	**PCM Mode**: BT_PCM_DIN BT_PCM data input signal **AIU Mode:** I2S_DIN I2S Audio input data (for recording)	I	

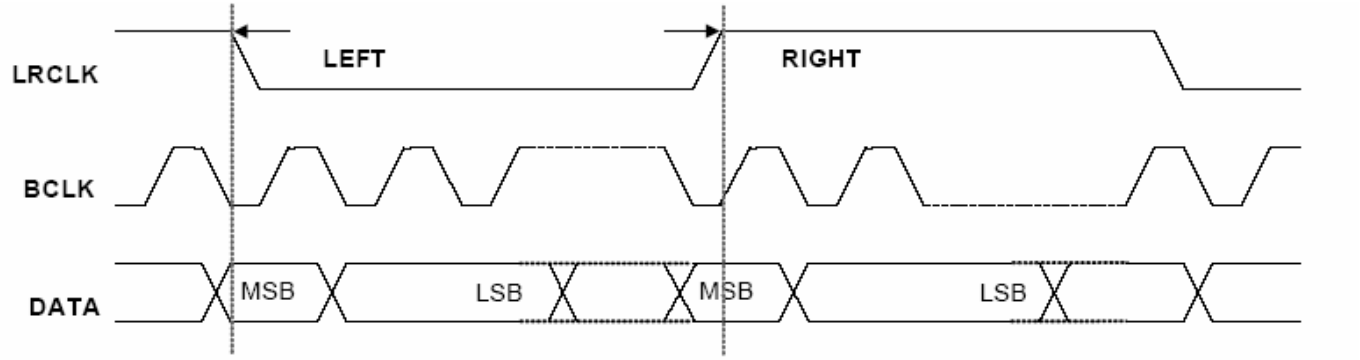
2-7-1.2 Protocol Description

2-7-1.2 .1 I^2S interface Protocol

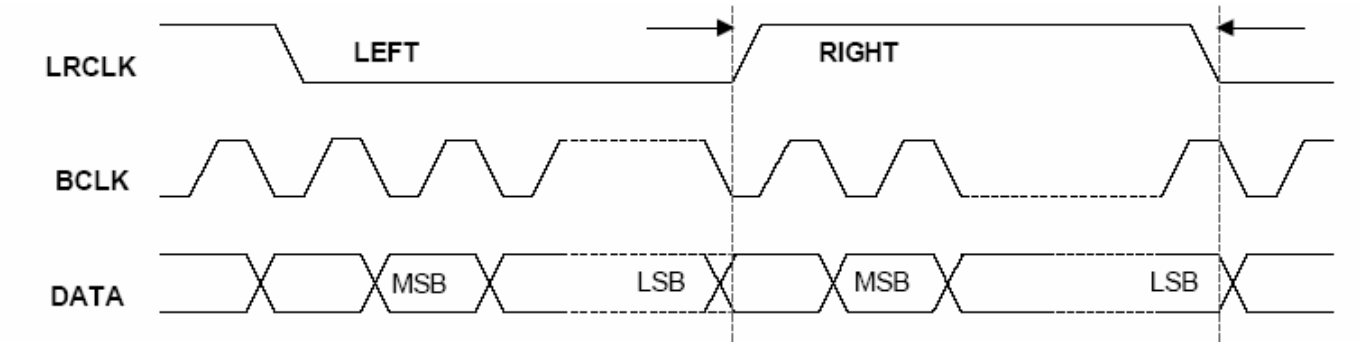


2-7-1.2 .2 Justified Protocol

MSB-Justified Protocol

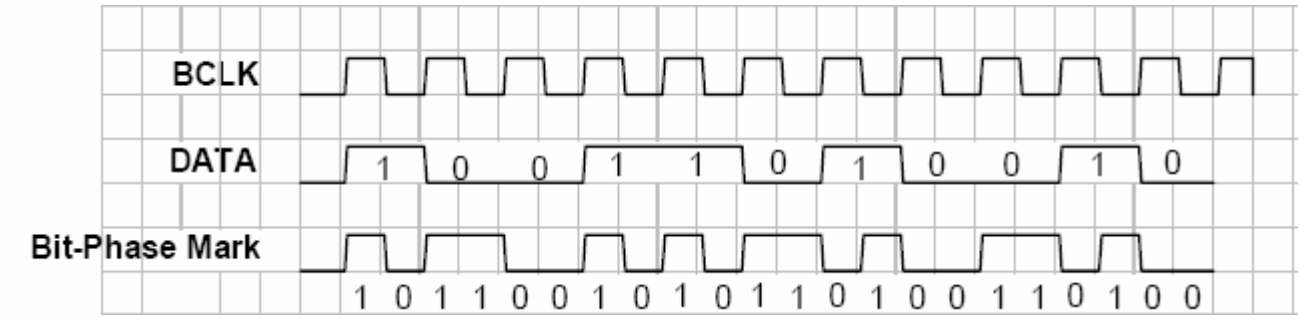


LSB-Justified Protocol

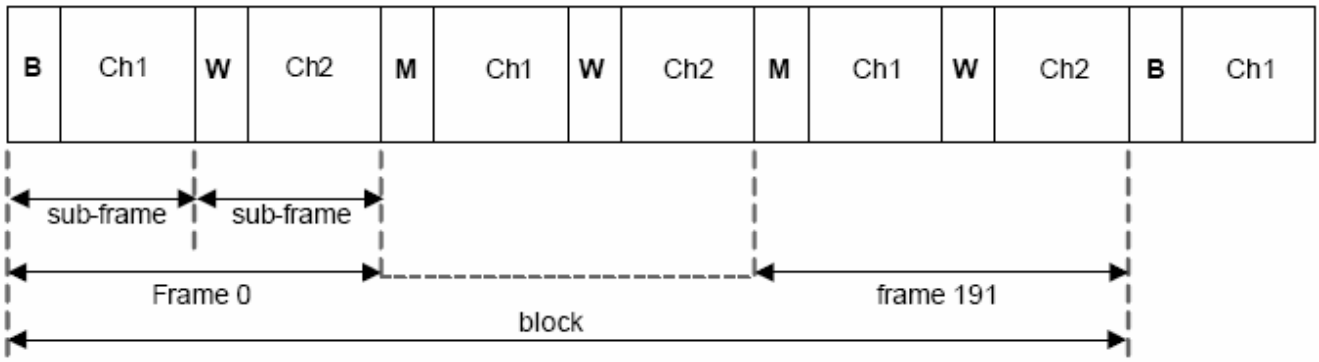


2-7-1.2 .3 IEC60958 Compatible Audio CODEC Interface Protocol

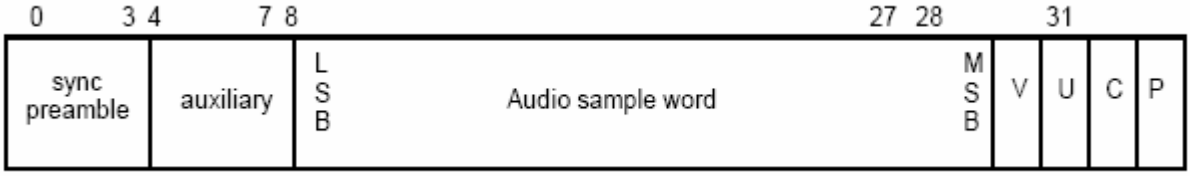
IEC60958 Compatible Audio CODEC Interface Encoding



IEC60958 Compatible Audio CODEC Interface Format Signal



IEC60958 Compatible Audio CODEC Interface Sub-Frame Format



IEC60958 Compatible Audio CODEC Interface Preambles

Preceding State	Channel Coding
B	11101000
M	11100010
W	11100100

2-7-1.3 Clock Frequency and Audio Data Resolution.

Audio Data may arrive with different input data formats with different sampling rates. The AIU uses an audio input clock of 22.5792MHz, 24.576MHz, 11.285MHz, or 12.288MHz to provide the appropriate CCLK and BCLK frequency to match sampling rates of each audio data format.

2-7-2. PCM Interface

The AW-GH381 supports a Pulse Code Modulation (PCM) interface that provides:

1. Master or slave mode
2. PCM bit width size of 8 bits or 16 bits
3. Up to 4 slots with configurable bit width and start positions
4. Short frame and long frame synchronization

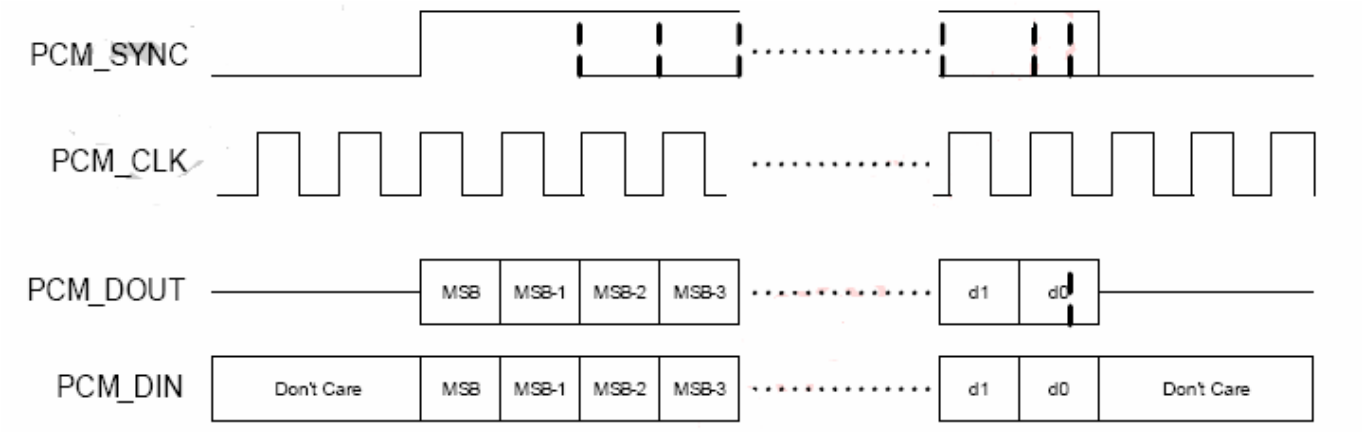
2-7-2.1. PCM Interface Signals

Pin No	Definition	Basic Description	Type	
28	BT_PCM_DOUT/ I2S_DOUT/ GPIO(12)	**PCM Mode**:BT_PCM_DOUT BT_PCM_DOUT output **AIU Mode:** I2S_DOUT I2S Audio output data(for playback)	I/O	
54	BT_PCM_CLK/ I2S_BCLK/ GPIO(13)	**PCM Mode**:BT_PCM_CLK BT_PCM_CLK input/output output if device PCM master; input if device PCM slave) **AIU Mode**:12S_BCLK 12S Audio bit clock	I/O	
56	BT_PCM_SYNC/ I2S_LRCLK/ GPIO(14)	**PCM Mode**:BT_PCM_SYNC BT_PCM_SYNC input/output(output if PCM initiator, input if PCM target) **AIU Mode**:12S_LRCLK 12S Audio left/right clock	O	
57	BT_PCM_MCLK/ I2S_CCLK/ GPIO(15)	**PCM Mode**:BT_PCM_MCLK(optional) :BT_PCM_MCLK output Optional clock used for some CODECs **AIU Mode**:12S_CCLK(optional) Audio CODEC main clock	O	
58	BT_PCM_DIN/ I2S_DIN/ GPIO(11)	**PCM Mode**: BT_PCM_DIN BT_PCM data input signal **AIU Mode:** I2S_DIN I2S Audio input data (for recording)	I	

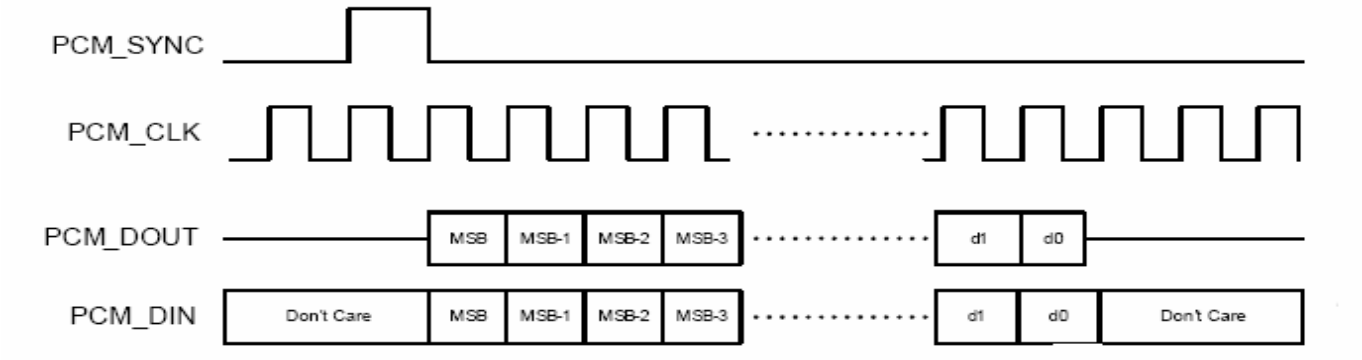
2-7-2.2. Protocol Description

The PCM interface supports long and short frame sync.

PCM Long Frame Sync



PCM Short Frame Sync



2-7-2.3.Modes of Operation

The PCM interface supports two modes of operation:

- PCM master
- PCM slave

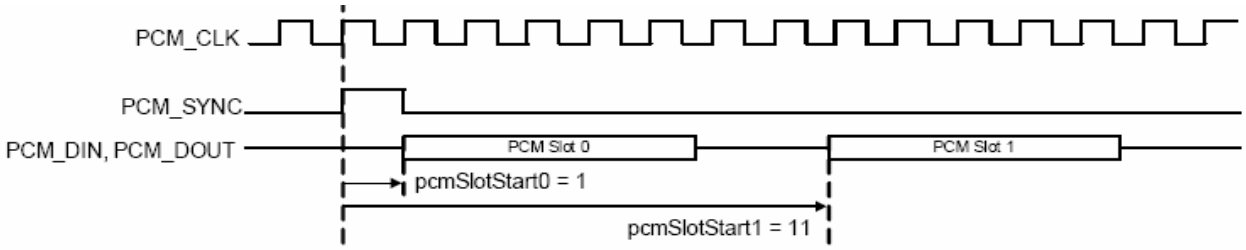
When in PCM master mode, the interface generates a 2MHz or a 2.048MHz PCM_CLK and 8kHz PCM_SYNC signal. An alternative PCM master mode is available that uses an externally generated PCM_CLK, but still generated the 8kHz PCM_SYNC. The external PCM_CLK must have a frequency that is an integer multiple of 8kHz. Supported frequencies are in the 512kH to 4MHz range.

When in PCM slave mode, the interface has both PCM_CLK and PCM_SYNC as inputs, thereby letting another unit on the PCM bus generate the signals.

The PCM Interface consists of up to four PCM slots(time divided) preceded by a PCM sync signal. Each PCM slot can be either 8 or 16 bits wide. The slots can be separated in times, but are not required to follow immediately after one other. The timing is relative to PCM_CLK.

This picture shows an example of a PCM burst with two slots. The burst starts with a PCM_SYNC and then follows the PCM burst. In the example, the PCM burst consists of two PCM slots(first one is 8 bites wide, second is 16 bits wide) separated with two PCM_CLK clock cycles. The PCM slots can be configured to start at an arbitrary point in time, and the start value is given relative to the tart of the PCM_SYNC. The timing of the four PCM slots must be such that slot 0 is always located before slot 1, slot 1 before slot 2, etc, It is possible to only use for example slot 1 and not slot 0.

PCM Burst with Two PCM Slots(example)



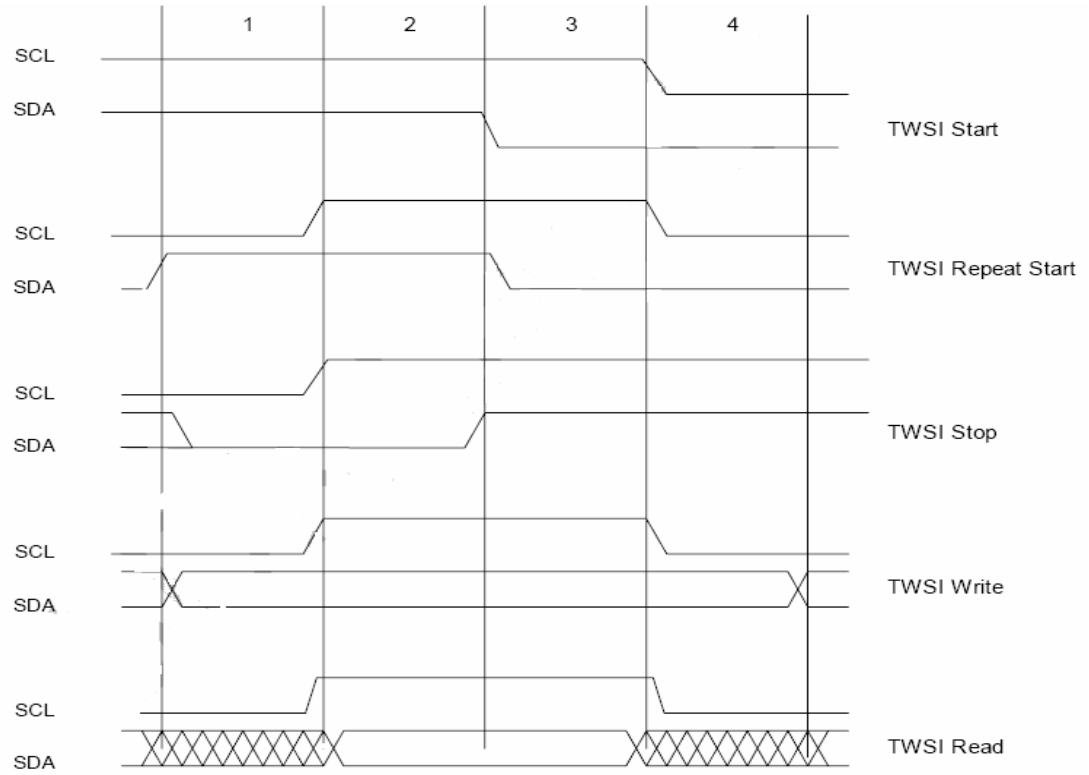
2-8. Control Interface

2-8-1 2-Wire Serial Interface

The AW-GH381 2-Wire Serial Interface(TWSI) unit is an interface bridge between a 2-wire serial bus and the CPU.

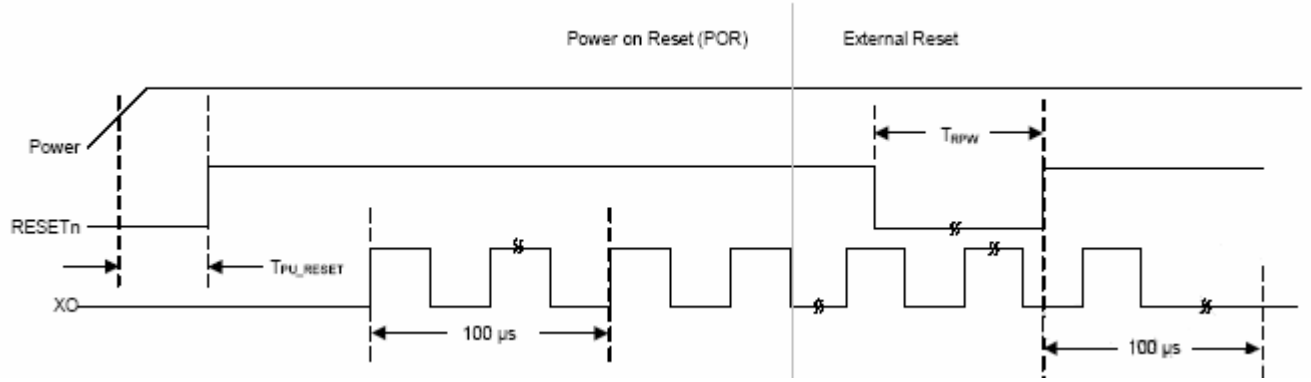
Pin No	Definition	Basic Description	Type	
59	AIU_TWSI_CLK/ GPIO(9)	**AIU Mode: AIU_TWSI_CLK** AIU_TWSI_CLKinput/output	I/O	
60	AIU_TWSI-DATA/ /GPIO(10)	**AIU Mode: AIU_TWSI-DATA** AIU_TWSI-DATA input/output	I/O	

TWSI (2-Wire Serial Interface) Protocol Timing Signaling



2-8-2 External Reset Specifications

Reset and Configuration Timing



Note: Pin 39 RESETn is not needed for proper operation due to internal power-on reset logic.

External RESET timing Requirements(Pin 39)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{PU-RESET}$	Valid power to RESETn de-asserted		0			ms
T_{RPW} (1)	Clock high		10	100 (2)		ns

(1) For external reset, the device reset time is T_{RPW} +300us.

(2) Minimum value guaranteed for a valid reset. Smaller values may trigger the reset circuit.

2-9 Pin Out Power Supply Use

VIO_X1	3V_IO	VIO_X2
RESTn	ANT_SEL_N	GPIO[9]
PDn	ANT_SEL_P	GPIO[10]
SD_DAT[1]/SPI_SDOn		GPIO[11]
SD_DAT[3]		GPIO[12]
SD_DAT[2]/SPI_SINTn		GPIO[13]
SD_DAT[0]/SPI_SCSn		GPIO[14]
SD_CMD/SPI_SDI		GPIO[15]
SD_CLK/SPI_CLK		GPIO[16]
EXT_CLK		GPIO[17]
SlEEP_CLK		ECSn
GPIO[0]		
GPIO[1]		
GPIO[2]		
GPIO[3]		
GPIO[4]		
GPIO[5]		
GPIO[6]		
GPIO[7]		
GPIO[8]		

3. Pin Definition

3-1. Pin Assignment

Pin No	Definition	Basic Description	Type	
1	GND			
2	RF IN/OUT	RF port for antenna or RF connector(Please keep matching circuit)		50Ohm @2.4GHz
3	GND			
4	GND			
5	BT_ANT	Bluetooth RF port(optional) (1)Signal antenna:Keep float (2)Dual Bluetooth antenna :50ohm matching Bluetooth antenna.		50Ohm @2.4GHz
6	UART_DSR/ GPIO(3)	UART DSR input: Data terminal ready output to the modem, data set, or peripheral device.	I	
7	EX_OSC_C/ GPIO(0)	External oscillator control	I/O	
8	NC			
9	3.3V_PA	3.3V PA power supply	P	
10	WLAN MAC_Wake/ GPIO(4)	WLAN MAC wake-up in /Interrupt in Software uses this pin or though SDIO as a method of getting the device out of deep sleep.	I/O	
11	LED out/ GPIO(1)	Transmit power or receive ready LED.	I/O	
12	GND			
13	SD_DAT[1]/ SPI_SDOn	SDIO 4-bit Mode: Data line bit[1] SDIO 1-bit Mode: Interrupt SDIO SPI Mode: Reserved G-SPI Mode: G-SPI Data Output(active low)	I/O	Note2
14	SD_DAT[3]	SDIO 4-bit Mode: Data line bit[3] SDIO 1-bit Mode: Reserved SDIO SPI Mode: Card Select(active low)	I/O	Note2
15	NC			
16	UART DTR/ GPIO(5)/ Sleep CLK selection	UART DTR out:Clear to send input from the modem data set, or peripheral device. Int sleep CLK: Series 100Kohm to ground Ext sleep CLK: Keep float : Keep float	O	
17	UART SINT/ GPIO(7)	UART SINT input: Serial data input from the modem, data shet or peripheral device.	I	
18	PDn	Full Power Down(active low as long as system need) 0=power down mode 1=normal mode (1)Connect to power down pin of host (2)Serial 100K ohm to VIO_X1 Note: Needs the external host to driver this pin high for normal operation. No internal pull-up on this pin.	I	
19	3V_IO	3V digital I/O power supply	P	
20	EXT_REF_CLK	External clock source 38.4MHz(keep)	I	
21	UART CTS/GPIO(8)	UART CTS input: Clear to send input from the modem, data set, or peripheral device.	I	
22	SLEEP_CLK	Clock input for external sleep clock **Note:** SLEEP_CLK is used by the WLAN MAC. The input clock frequency is typically 32kHz/32.768kHz/3.2kHz.The Bluetooth radio chip supply is 3.2kH.The WLAN requires 32kHz.	I	
23	NC			
24	GND			

Pin No	Definition	Basic Description	Type	
25	SD_DAT[2]/ SPI_SINTn	SDIO4-bit Mode: Data line bit[2]or Read Wait(optional) SDIO 1-bit Mode: Read Wait(optional) SDIO SPI Mode: Reserved G-SPI Mode: Active G-SPI Interrupt Output(active low)	I/O	Note2
26	SD_DAT[0]/ SPI_SCSn	SDIO 4-bit Mode: Data line bit[0] SDIO 1-bit Mode:Data line SDIO SPI Mode: Data output G-SPI Mode: G-SPI Chip Select Input(active low)	I	Note2
27	SD_CLK/ SPI_CLK	SDIO 4-bit Mode: Clock Input SDIO 1-bit Mode: Clock Input SDIO SPI Mode: Clock Input G-SPI Mode:G-SPI Clock Input	I	Note2
28	BT_PCM_DOUT/ I2S_DOUT/ GPIO(12)	**PCM Mode**:BT_PCM_DOUT BT_PCM_DOUT output **AIU Mode:** I2S_DOUT I2S Audio output data(for playback)	I/O	
29	SD_CMD/ SPI_SDI	SDIO 4-bit Mode: Command/Response SDIO 1-bit Mode: Command Line SDIO SPI Mode: Data Input G-SPI Mode: G-SPI Data Input	I/O	Note2
30	UART SOUT/ GPIO(6)/ Ref Clock Selection	UART SOUT out: Serial data output to the modem, data set, or peripheral device. Ref Clock Selection: Int Xtal: Series 100Kohm to ground Ext OSC: Keep NC	O	
31	ANT_SEL_P	Different Antenna Select Negative out Provides the antenna select negative control signal Default value is 1 **ANT_SEL_N ANT_SEL_P Antenna** **0 1 Antenna 1** **1 0 Antenna 0** **Note:** Also used as RF switch control for single Bluetooth/WLAN antenna configurations.	O	
32	NC			
33	ECSn	SDIO: Series 100Kohm to ground G-SPI: Keep float		*
34	SCLK	internal use		No connection
35	VIO_X2	1.8V/3.3V Digital Power Supply	P	
36	GND			
37	VDD18_X3	1.8V digital I/O and internal voltage regulator power supply	P	
38	VIO_X1	1.8V/3.3V Host Supply	P	
39	RESETn	RESETn: Reset(active low at least 10ns) (1)When the customer uses the RESETn mode, the SDIO/SPI interface must reboot. (2)Serial 100K ohm to VIO_X1	I	
40	1.2_EXT	1.2V digital power supply(could use internal 1.2V LDO) **Note**: Please parallel 10uF capacitor if use internal LDO.	P	
41	VDD18A	1.8V analog I/O power supply	P	
42	1.2V Reg_SEL	Ground: Use module internal LDO supply V1.2V Float : PM Chip supply 1.2 V (default in pad)		
43	Interface Select(1)	Host Interface Select	I/O	Note1
44	Interface Select(0)/ GPIO(17)	Host Interface Select	I/O	Note1
45	ANT_SEL_N	Different Antenna Select Negative out Provides the antenna select negative control signal Default value is 0 **ANT_SEL_N ANT_SEL_P Antenna** **0 1 Antenna 1** **1 0 Antenna 0** **Note:** Also used as RF switch control for single Bluetooth/WLAN antenna configurations.	O	

Pin No	Definition	Basic Description	Type	
46	GND			
47	GND			
48	GND			
49	GND			
50	AIU_SPDIF/ GPIO(16)	**AIU Mode**:AIU_SPDIF,IEC60958 Compatible Audio CODEC Interface output data(for playback)	O	
51	GND			
52	GND			
53	GND			
54	BT_PCM_CLK/ I2S_BCLK/ GPIO(13)	**PCM Mode**:BT_PCM_CLK BT_PCM_CLK input/output output if device PCM master; input if device PCM slave) **AIU Mode**:12S_BCLK 12S Audio bit clock	I/O	
55	TR3_N	Internal use		No connection
56	BT_PCM_SYNC/ I2S_LRCLK/ GPIO(14)	**PCM Mode**:BT_PCM_SYNC BT_PCM_SYNC input/output(output if PCM initiator, input if PCM target) **AIU Mode**:12S_LRCLK 12S Audio left/right clock	O	
57	BT_PCM_MCLK/ I2S_CCLK/ GPIO(15)	**PCM Mode**:BT_PCM_MCLK(optional) :BT_PCM_MCLK output Optional clock used for some CODECs **AIU Mode**:12S_CCLK Audio CODEC main clock	O	
58	BT_PCM_DIN/ I2S_DIN/ GPIO(11)	**PCM Mode**: BT_PCM_DIN BT_PCM data input signal **AIU Mode:** I2S_DIN I2S Audio input data (for recording)	I	
59	AIU_TWSI_CLK/ GPIO(9)	**AIU Mode:** AIU_TWSI_CLK AIU_TWSI_CLKinput/output	I/O	
60	AIU_TWSI-DATA/ /GPIO(10)	**AIU Mode:** AIU_TWSI-DATA AIU_TWSI-DATA input/output	I/O	
61	GND			
62	VDD25_EFUSE	Please keep series 100k ohm to ground and keep NC component pad to 1.8V(register pin)		
63	UART RTS/ GPIO(2)/ Multi-Function Selection	UART RTS output: Request to send output to the modem, data set, or peripheral device Multi-Function Selection: WLAN/BT SDIO: Series 100Kohm to ground WLAN single function SDIO: Keep NC	I/O	
64	GND			

***Pin 5 is optional for the customer's special request, please discuss with AzureWave engineer if you need this function.

Note1: **Host Interface select define table**

Pin No	Definition	Basic Description	Type	
43	Interface Select(1)	Host Interface Select: 10(Interface select) NN SDIO (default in pad)		
44	Interface Select(0)	NR GSPI **Note:** R mean this pin series 100K ohm to ground. N mean this pin float		

Note2: SDIO/G-SPI interface Pin

Pin No	Definition	Basic Description	Type	
13	SD_DAT[1]/ SPI_SDOn	SDIO 4-bit Mode: Data line bit[1] SDIO 1-bit Mode: Interrupt SDIO SPI Mode: Reserved G-SPI Mode: G-SPI Data Output(active low)	I/O	
14	SD_DAT[3]	SDIO 4-bit Mode: Data line bit[3] SDIO 1-bit Mode: Reserved SDIO SPI Mode: Card Select(active low)	I/O	
25	SD_DAT[2]/ SPI_SINTn	SDIO4-bit Mode: Data line bit[2]or Read Wait(optional) SDIO 1-bit Mode: Read Wait(optional) SDIO SPI Mode: Reserved G-SPI Mode: Active G-SPI Interrupt Output(active low)	I/O	
26	SD_DAT[0]/ SPI_SCSn	SDIO 4-bit Mode: Data line bit[0] SDIO 1-bit Mode:Data line SDIO SPI Mode: Data output G-SPI Mode: G-SPI Chip Select Input(active low)	I	
27	SD_CLK/ SPI_CLK	SDIO 4-bit Mode: Clock Input SDIO 1-bit Mode: Clock Input SDIO SPI Mode: Clock Input G-SPI Mode:G-SPI Clock Input	I/O	
29	SD_CMD/ SPI_SDI	SDIO 4-bit Mode: Command/Response SDIO 1-bit Mode: Command Line SDIO SPI Mode: Data Input G-SPI Mode: G-SPI Data Input	I/O	

Audio Codec/PCM Interface

Pin No	Definition	Basic Description	Type	
28	BT_PCM_DOUT/ I2S_DOUT/ GPIO(12)	**PCM Mode**:BT_PCM_DOUT BT_PCM_DOUT output **AIU Mode:** I2S_DOUT I2S Audio output data(for playback)	O	
50	AIU_SPDIF/ GPIO(16)	**AIU Mode**:AIU_SPDIF,IEC60958 Compatible Audio CODEC Interface output data(for playback)	O	
54	BT_PCM_CLK/ I2S_BCLK/ GPIO(13)	**PCM Mode**:BT_PCM_CLK BT_PCM_CLK input/output output if device PCM master; input if device PCM slave) **AIU Mode**:12S_BCLK 12S Audio bit clock	I/O	
56	BT_PCM_SYNC/ I2S_LRCLK/ GPIO(14)	**PCM Mode**:BT_PCM_SYNC BT_PCM_SYNC input/output(output if PCM initiator, input if PCM target) **AIU Mode**:12S_LRCLK 12S Audio left/right clock	I/O	
57	BT_PCM_MCLK/ I2S_CCLK/ GPIO(15)	**PCM Mode**:BT_PCM_MCLK(optional) :BT_PCM_MCLK output Optional clock used for some CODECs **AIU Mode**:12S_CCLK Audio CODEC main clock	O	
58	BT_PCM_DIN/ I2S_DIN/ GPIO(11)	**PCM Mode**: BT_PCM_DIN BT_PCM data input signal **AIU Mode:** I2S_DIN I2S Audio input data (for recording)	I	

UART Interface

Pin No	Definition	Basic Description	Type	
Data Bus				
17	UART SINT/GPIO(7)	UART SINT input: Serial data input from the modem, data set or peripheral device.	I	
30	UART SOUT/ GPIO(6)	UART SOUT out: Serial data output to the modem, data set, or peripheral device.	O	
Modem Control				
6	UART_DSR/ GPIO(3)	UART DSR input: Data terminal ready output to the modem, data set, or peripheral device.	I	
16	UART DTR/ GPIO(5)/ Sleep CLK select	UART DTR out:Clear to send input from the modem data set, or peripheral device. Int sleep CLK: Series 100Kohm to ground Ext sleep CLK: Keep float : Keep float	O	
21	UART CTS/GPIO(8)	UART CTS input: Clear to send input from the modem, data set, or peripheral device.	I	
63	UART RTS/ GPIO(2)	UART RTS output: Request to send output to the modem, data set, or peripheral device	O	

4. Cell Phone Co-Existence TX Noise Floor

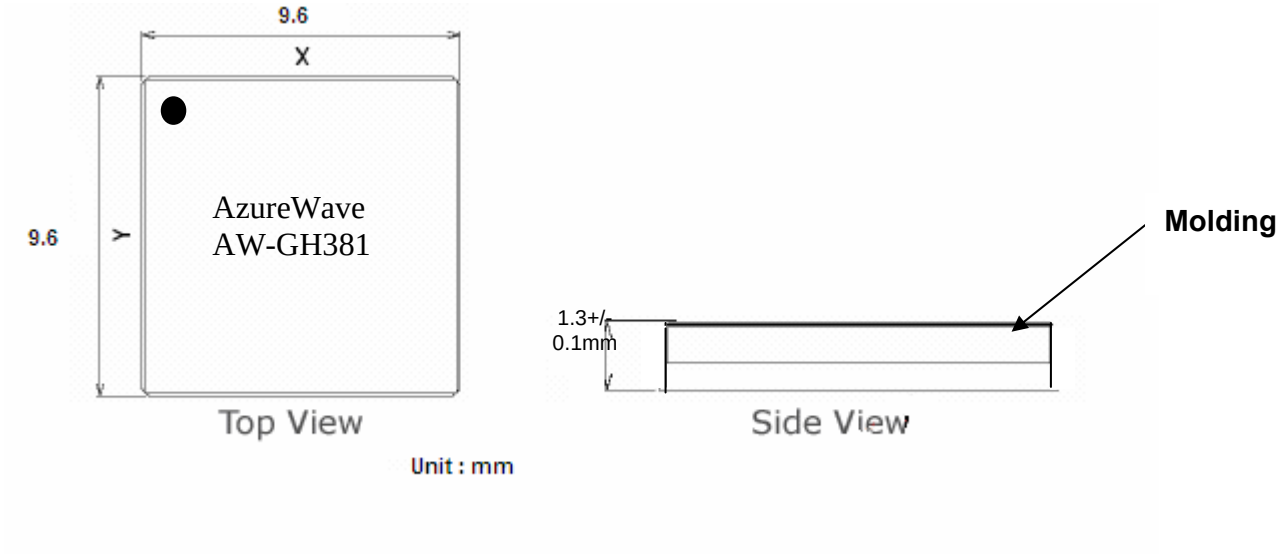
AW-GH381 module support good cell phone co-existence characteristically. The cell phone co-existence can fit in GSM/DCS/WCDMA/UMTS/3G system. Let's the handset system users can easy to build-up the WLAN sub-system in handset system. In the module, we reduce the interference between cell phone and WLAN by reduce the module maximum TX noise floor. We list the module maximum noise flow at antenna terminal in the follow table.

Standard	Down-Link Band	Target Tx Noise Floor at WLAN Ant.
GSM850	869-894	-155dBm/Hz
GSM900	925-960	-155dBm/Hz
DCS1800	1805-1880	-155dBm/Hz
PCS1900	1930-1990	-155dBm/Hz
W-CDMA	2110-2170	-155dBm/Hz

Note: Assume over the air is 15dB between Cell phone antenna to WLAN antenna.

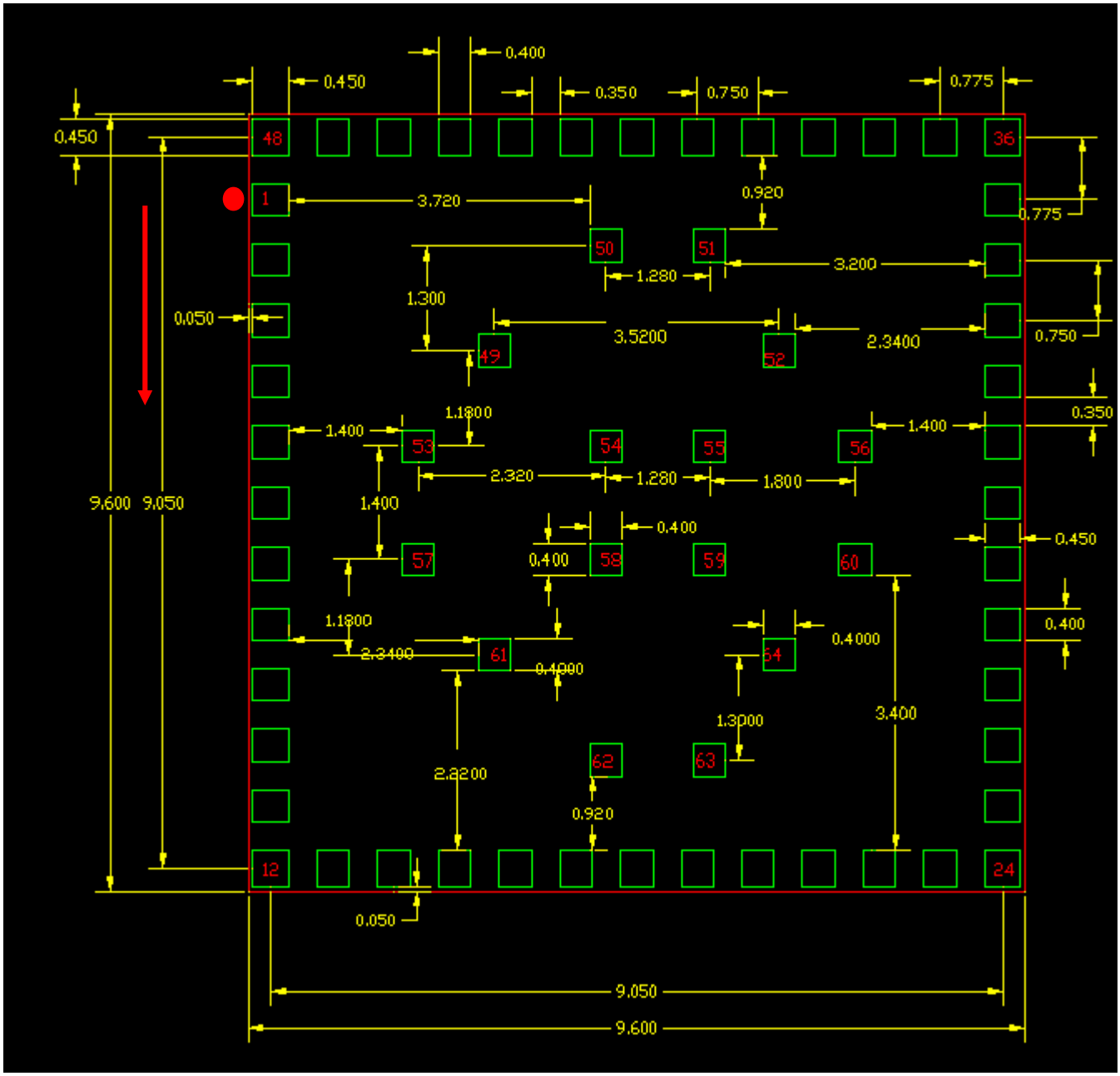
7. Mechanical Characteristics

The size and thickness of the AW-GH381 LGA package module is listed below:



AW-GH381 Top View PCB Layout FootPrint

Unit: mm

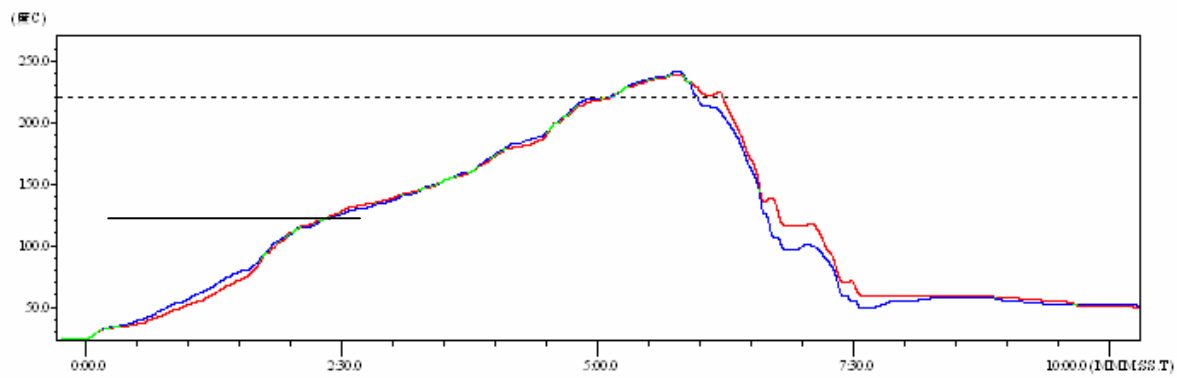


Note: AzurWave will provide AW-GH381 Top View FootPrint DXF file for customer reference.

5. Package Information

5-1. Recommended Reflow Profile

Reflow Soldering Profile



No	Item	Temperature(℃)	Time(sec)
1	Reflow Time	Time of above 220℃	40~60sec
2	Peak-Temp	245℃ max	

Note: 1. Recommend to supply N_2 for reflow oven

2. N_2 atmosphere during reflow (O_2<300ppm)

5-2. Device Handling Instruction(Module IC SMT Preparation)

5-2-1. Shelf life in sealed bag:12 months, At<30℃ and <60% relative humidity(RH)

5-2-2. After bag is opened, devices that will be

5-2-2-1. Baked for 24 hours at 125+-5℃ with tray

5-2-2-2. Re-baked required after last baked with window time 24 hours

5-2-3. Recommend to Oven bake with N2 supplied

5-2-4. Recommend end to Reflow Oven with N2 supplied

5-2-5. Baked required with 24 hours at 125+-5℃ before rework process for two modules, one is new module and two is board with module

5-2-6. Recommend to store at ≦10% RH with vacuum packing

5-2-7. If SMT process needs twice reflow:

5-2-7-1. Process flow: (1) Top side SMT and reflow → (2) Bottom side SMT and reflow

5-2-7-1-1. Case 1: Wifi module mound on Top side. Need to bake when bottom side process over 24 hours window time, no need to bake within 24 hours

5-2-7-1-2. Case 2: Wifi module mound on bottom side, follow normal bake rule before process

Note: Window time means from last bake end to next reflow start that has 24 hours space.