Circuit Description

1. Frequency configuration

The receiver utilizes double conversion superheterodyne. The first IF is 45.05MHz and the second IF is 455 KHz. The first local oscillator signal is supplied by PLL circuit. The PLL circuit in the transmitter generates the necessary frequencies.

2. Receiver

The receiver employs double conversion superheterodyne，designed to operate in the frequency range of 400 to 470MHz.

2.1 Front -end RF amplifier

An incoming signal from the antenna is applied to an RF amplifier (Q4) after passing through a transmit/receive switch circuit. After the signal is amplified , passing through a band pass filter BPF , the signal is filtered by a band pass filter to eliminate unwanted signal before it is passed to the first mixer.

2.2 First mixer

The signal from the RF amplifier is heterodyned with the first local oscillator signal from the PLL frequency synthesizer circuit at the first mixer (Q5) to create a 45.050MHz first IF (Q13) signal. The first IF signal is then fed through two monolithic crystal filters to further remove spurious signal.

2.3 IF amplifier

The first IF signal is amplified by Q13, and then enters U4 (FM processing IC). The signal is heterodyned again with a second local oscillator signal within U4 to create a 455 kHz second IF signal. The second IF signal is then fed through a 450 kHz ceramic filter to further eliminate unwanted signals before it is amplified and FM detected in U4.

2.4 AF amplifier

The recovered AF signal obtained from U4 is amplified by U2 handle, the processed AF signal passes through an AF volume contro and is amplified to a sufficient level to drive a loud speaker by an AF power amplifier.

2.5 Squelch

Part of the AF signal from the U4 enters the FM IC again, and produce the corresponding noise level go to the analog port of microprocessor (U2).U2 determines whether to output sounds from the speaker by checking whether the input voltage is higher or lower than the preset value.To output sounds from the speaker,U2 sends a high signal to the MUTE and AFCO lines through Q2.

2.6 Receiving signaling QT/DQT

300Hz and higher audio frequencies of the output signal from IF IC are entered the microprocessor and determines whether the QT or DQT matches the preset value, and control the MUTE and AFCO and the speaker output sounds according to the squelch results.

3. PLL frequency synthesizer

The PLL circuit generates the first local oscillator signal for reception and the RF signal for transmission.

3.1 PLL

The frequency step of the PLL circuit is 5 or 6.25 KHz. A 19.2MHz reference oscillator signal is divided at U3 by a mixed counter to produce 5 or 6.25 kHz reference frequency. The voltage controlled oscillator (VCO) output.The signal is buffer amplified by Q6, and then divided in U3 by a dual-module programmable counter. The divided signal is compared in phase with the 5 or 6.26 KHz reference signal in the phase comparator in U3. The output signal from the phase comparator is filtered through a low-pass filter and passed to the VCO to control the oscillator frequency.

3.2 VCO

The operating frequency is generated by Q11 in transmit and receive mode. The oscillator frequency is controlled by applying the VCO control voltage, obtained from the phase comparator, to the varactor diodes (D8). In receive mode causing RX-VCO(Q2) supplied and turn P2 on. In transmit mode

causing TX-VCO(Q11) supplied and turn P1 on. The outputs from Q2,Q11 are amplified by Q6 and sent to the buffer amplifiers.

4. Transmitter

4.1 Transmit audio

The modulation signal from the microphone is amplified by U2(RC4558), passes through a preemphasis circuit , and amplified by other U3 to perform IDC operation. The signal then passes though a low-pass filter(splatter filter) and cuts 3KHz and higher frequencies. The resulting signal goes to the VCO through the VCO modulation terminal for direct FM modulation.

4.2 QT/DQT encoder

A necessary signal for QT/DQT encoding is generated by U6 and FM-modulated to the PLL reference signals, Since the reference OSC does not modulate the loop characteristic frequency or higher ,modulation is performed at the VCO side by adjusting the balance.

4.3 VCO and RF amplifier

The transmit signal obtained from the VCO buffer amplifier Q6, is amplified by Q8、Q14. This amplified signal is passed to the power amplifier, Q10 、Q3 and Q2, which consists of a 2-stage FET amplifier and is capable of producing up to 5W of RF power.

4.4 ANT switch and LPF

The RF amplifier output signal is passed through a low-pass filter network to filter the second harmonic components and then applied to a transmit / receive switching circuit before it is passed to the antenna terminal. The transmit / receive switching circuit is comprised of ANT.SW. ANT.SW is turned on (conductive) in transmit mode and off (isolated) in receive mode.

4.5 APC

The automatic power control (APC) circuit stabilizes the transmitter output power at a predetermined level by sensing the drain current of the final

amplifier Field Effect Transistor (FET). The voltage comparator, U5, compares the voltage obtained from the above drain current with a reference voltage which is set using the microprocessor. The APC voltage is proportional to the difference between the sensed voltage and the reference voltage output from U5. This output voltage controls the gate of the FET power amplifier, which keeps the transmitter output power be varied by the microprocessor which in turn changes the reference voltage and hence, the output power.

5. Power supply

A 5V reference power supply for the control circuit is derived from an internal battery. This reference power supply is used to provide a 5V supply in transmit mode [TXV], a 5V supply in receive mode [RXV], and a 5V supply common in both modes [5C] based on the control signal sent from the microprocessor.