A2530R24A & A2530R24C Radio Module
Theory of Operation

The A2530R24A and A2530R24C modules operate in the global 2.4 GHz ISM/SRD frequency band. They can be used to implement a variety of networks, including point to point, point to multi-point, peer to peer and mesh networks.

Both modules operate in a similar manner except the antenna part where A2530R24A communicates through a built-in antenna, and A2530R24C communicates through an external antenna attached to a U.FL antenna port.

The description of the functional blocks is given as follows:

- Antenna
  - The antenna couples energy between the air and the module. The integral antenna and the external monopole antenna, both centered at 2441.75 MHz, provide a near omni-directional antenna pattern with high efficiency such that the application will work equally well in any direction. Note that the end radiation pattern depends not only on the antenna, but also the ground plane, enclosure and installation environment.
- Matching & Filtering
  - The matching provides the correct loading of the transmit amplifier to achieve the highest output power as well as the correct loading for the receive LNA to achieve the best sensitivity.
  - Filtering removes spurious signals to comply with regulatory intentional radiator requirements, provides reduced susceptibility to power supply and digital noise, and filters out RF and high frequency noise from the communication data and control link.
- TX/RX Chain
  - TX/RX chain handles transmitting and receiving of the communication data based on the radio register settings. It involves the coordination of several blocks including modulator, demodulator, AGC control, frequency synthesizer and frame control.
- Crystal
  - Crystal oscillator provides the necessary clock reference for the whole module operation. The A2530R24A and A2530R24C modules use a 32 MHz crystal.
- Power Management
  - Power management ensures a stable supply for the internal functions, as well as providing means for a low power sleep mode.
- CPU and Memory
  - The 8051 CPU core used in the CC2530 device is a single-cycle 8051-compatible core. It has three different memory-access buses (SFR, DAT and CODE/XDATA) with single-cycle access to SFR, DATA, and the main SRAM. It also includes a debug interface and an 18-input extended interrupt unit.

  - The memory arbiter connects the CPU and DMA controller with the physical memories and all peripherals through the SFR bus.
  - The 8-BK SRAM maps to the DATA memory space and to parts of the XDATA memory spaces. This is an ultralow-power SRAM that retains its contents even when the digital part us powered off.
  - 256 KB flash block provides in-circuit programmable non-volatile program memory for the device, and maps into the CODE and XDATA memory spaces. In addition to holding the program code, it also allows the application to save data that must be preserved such that it is available after restarting the device.
- I/O Controller
  - The I/O controller is responsible for all general-purpose I/O pins. The CPU can configure whether peripheral modules control certain pins or they are under software control, and if so, whether they are configured as input or output.