

A110LR09x Radio Modules Block Diagram

Below is a block diagram for each of the A110LR09A and A110LR09C modules.

• Antenna

O The antenna couples energy between the air and the AIR module. For applications where installations are done by an end user (non-professional), an omnidirectional antenna pattern is desired such that the application will work equally well in every direction. Similarly for peer to peer or point to multipoint applications, an omni-directional pattern is desired such that all nodes have a fair chance of communicating. The A110LR09A module has an integral antenna that is near omni-directional, whereas the A110LR09C has approved antenna options ranging from near omni-directional to shaped front/back patterns (useful for inline, professional installations). Note that the end radiation pattern depends not only on the antenna, but also on the ground plane, enclosure and installation environment.

Filtering

o Filtering removes spurious signals to comply with regulatory intentional radiator requirements.

Matching

 Matching provides the correct loading of the transmit amplifier to achieve the highest output power, as well as the correct loading for the receive LNA to achieve the best sensitivity.

Physical

o The physical layer provides conversions between data, symbol and RF signal.

MAC

• The MAC layer is part of the Logical Link Layer and provides frame handling, addressing and medium access services. For CE operations, part of the MAC is implemented in the S/W.

• Microcontroller Interface

• The microcontroller interface exposes registers and commands for the physical and MAC layers to a microcontroller.

• Power Management

 Power management ensures a stable supply for the internal functions, as well as providing means for a low power sleep mode (in which case, most of the transceiver is power off).



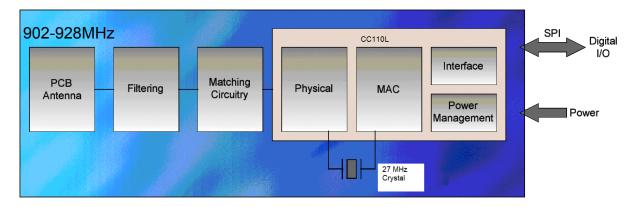


Figure 1 The functionality of the A110LR09A, using an integral antenna

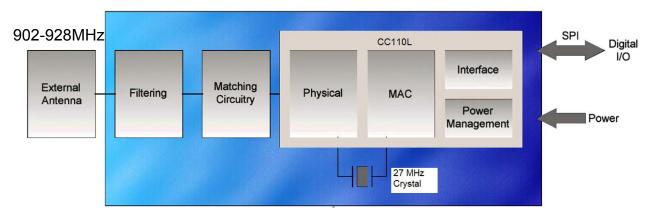


Figure 2 The functionality of the A110LR09C, using an external antenna.



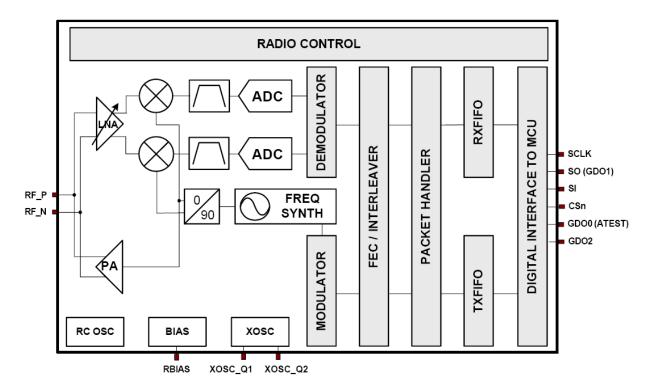


Figure 3 Transceiver IC block diagram.