- ROHS Compliant
- LGA Footprint
- Low Power Consumption
- Regulatory approvals for FCC, IC, ETSI
- Digital RSSI output
- Programmable channel filter bandwidth
- Programmable output power up to +1 dBm
- High sensitivity (–104 dBm at 2.4 kBaud, 1% packet error rate)
- Low current consumption (13.3 mA in RX, 250 kBaud, input well above sensitivity limit)
- Separate 64-byte RX and TX data FIFOs
- Fast startup time: 250us from SLEEP to Rx or Tx mode
- Data Rate: 1.2 – 500 Kbit/Sec
- Programmable data rate from 1.2 to 500 kBaud
- Sleep state: 0.4mA
- Idle State: 1.5mA

Performance

- Suitable for frequency hopping and multichannel systems due to a fast settling frequency synthesizer with 90 us settling time
- Suited for systems compliant with EN 300 328 and EN 300 440 class 2 (Europe), FCC CFR47 Part 15.247b and 15.249 (US)
- No regulatory "Intentional radiator" testing required to integrate module into end product. Simple certification labeling replaces testing.

1.4. Theory of Operation

The A2500R24C and A2500R24A are for low power wireless applications in the 2400MHz to 2483.5MHz global ISM/SRD band. The devices can be used to implement a variety of networks, including; point to point, point to multipoint, peer to peer and mesh networks

The A2500R24C and A2500R24A both interface to an application microcontroller via SPI bus. Physical and MAC layer functionality are accessed via the SPI bus, through addressable registers as well as execution commands. Data received or to be transmitted are also accessed through the SPI bus and are implemented as a FIFO register (64 bytes each for Tx and Rx).

To transmit, a frame of data is placed in the FIFO, this may include a destination address. A transmit command is given, which will transmit the data according to the initial setup of the registers. To receive data a receive command is given, which will listen for a transmission and when one occurs put the received frame in the FIFO. When neither transmit or receive is required the device can enter either an Idle mode, from which it can quickly re-enter receive or transmit mode or it can enter a low power sleep mode, from which a crystal startup is also required prior to transmit or receive operation.

Below a block diagram is given for each of the A2500R24C and A2500R24A modules.

- Antenna
    - The antenna couples energy between the air and the module. For applications where installations are done by an end user (non-professional), an omni-directional antenna pattern is desired, such that the application will work equally well in any direction. Similarly for peer to peer or point to multipoint application an omni-directional pattern is desired such that all nodes have a fair chance of communicating. The A2500R24A module has an integral antenna that is near omni-directional, whereas the A2500R24C has approved antenna options ranging from near omni-directional to shaped front/back patterns (useful for inline, professional installations). Note that the end radiation pattern

depend not only on the antenna, but also the ground plane, enclosure and installation environment.

- Filtering
  - Filtering removes spurious signals to comply with regulatory intentional radiator requirements.
- Matching
  - The matching provides the correct loading of the transmit amplifier to achieve the highest output power as well as the correct loading for the receive LNA to achieve the best sensitivity.
- Physical
  - The physical layer provides conversions between data, symbol and RF signal.
- MAC
  - The MAC layer is part of the Logical Link Layer and provides frame handling, addressing and medium access services.
- Microcontroller Interface
  - The microcontroller interface exposes registers and commands for the physical and MAC layers to a microcontroller.
- Power Management
  - Power management ensures a stable supply for the internal functions as well as providing means for a low power sleep mode, in which most of the transceiver is power off.