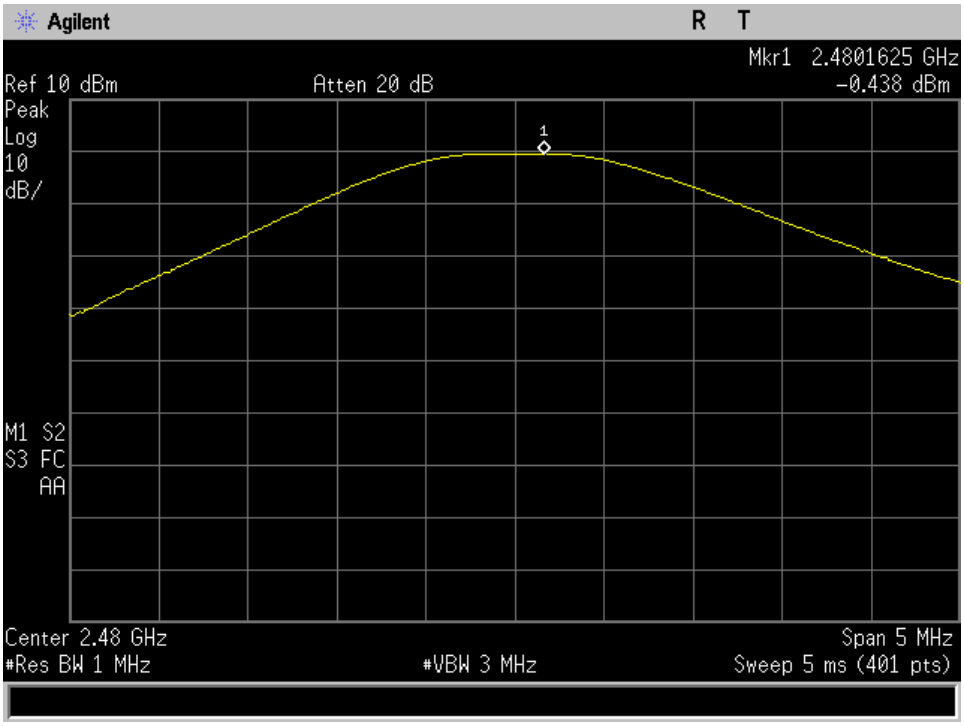
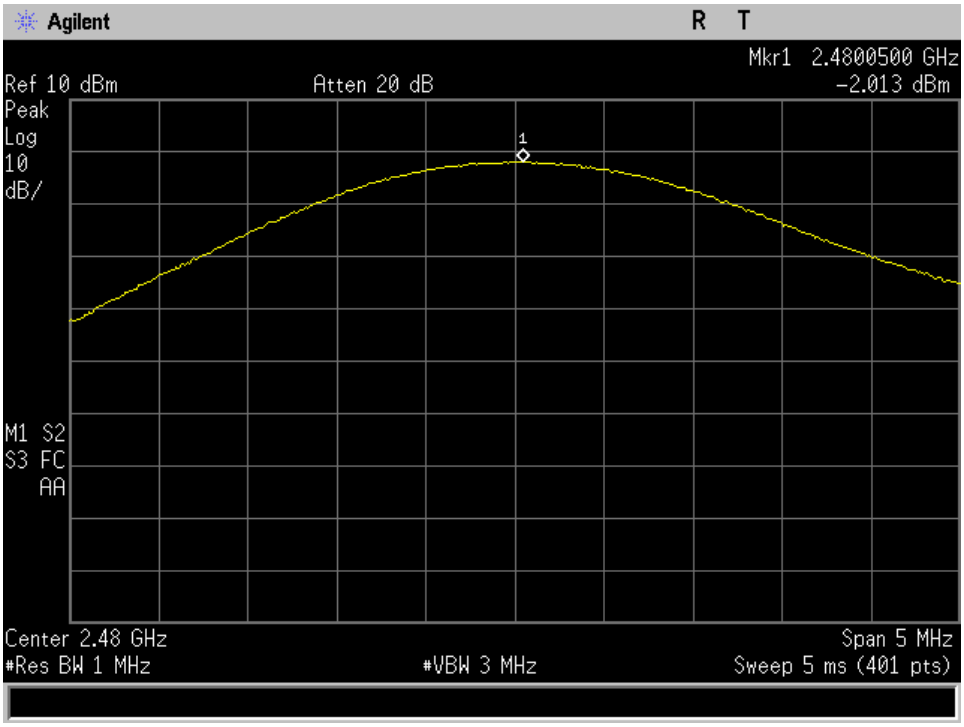
Annex A
Output Power

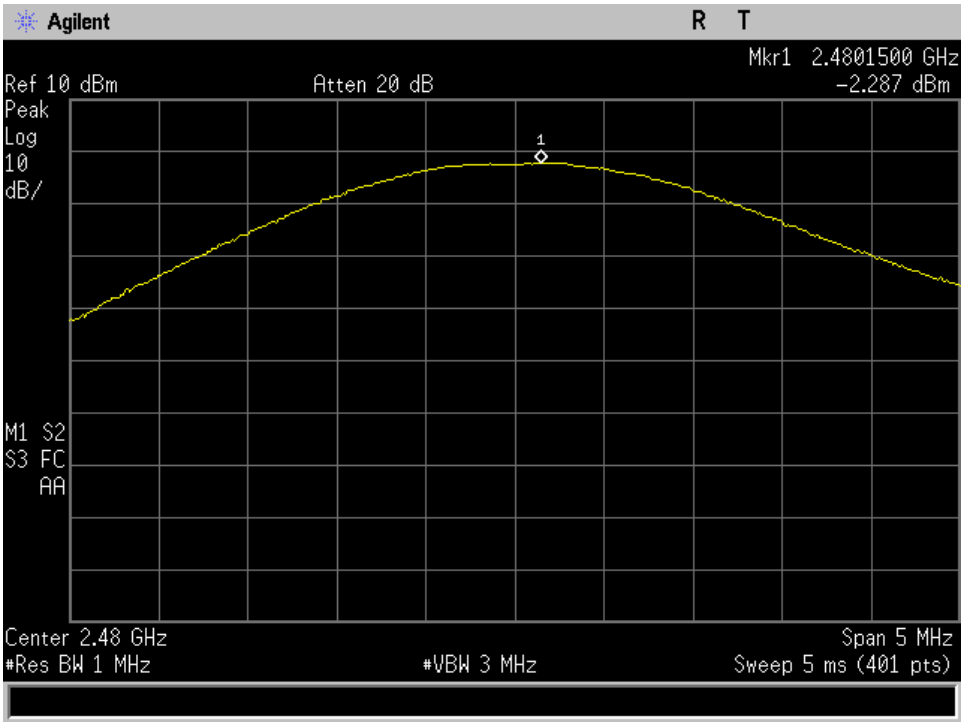
high ch DH1 GFSK



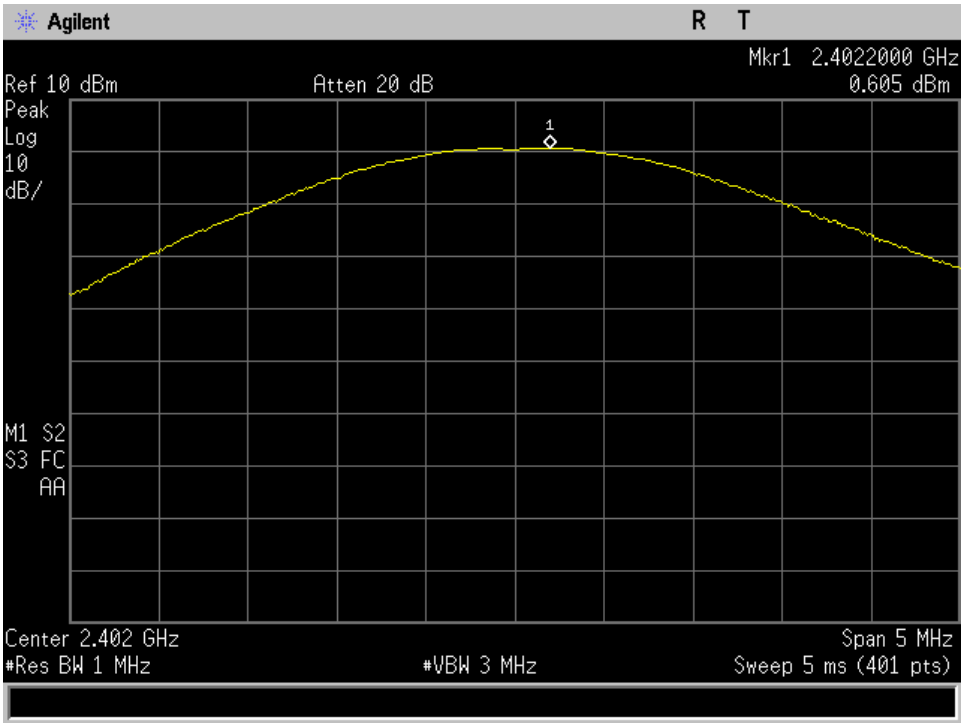
high ch DH1 QPSK



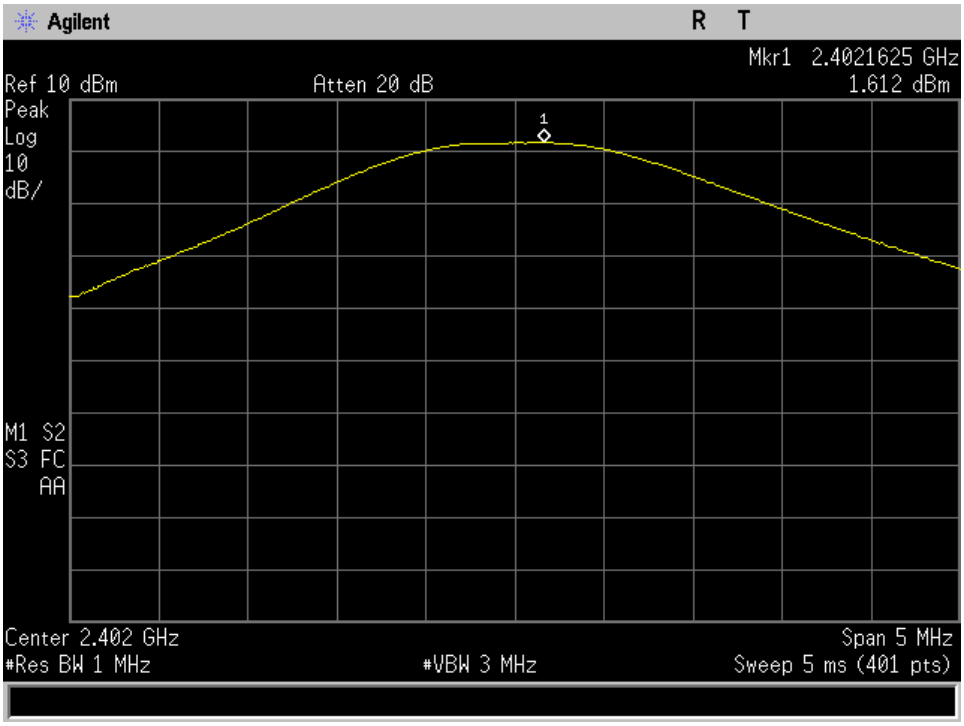
High DH1 8PSK



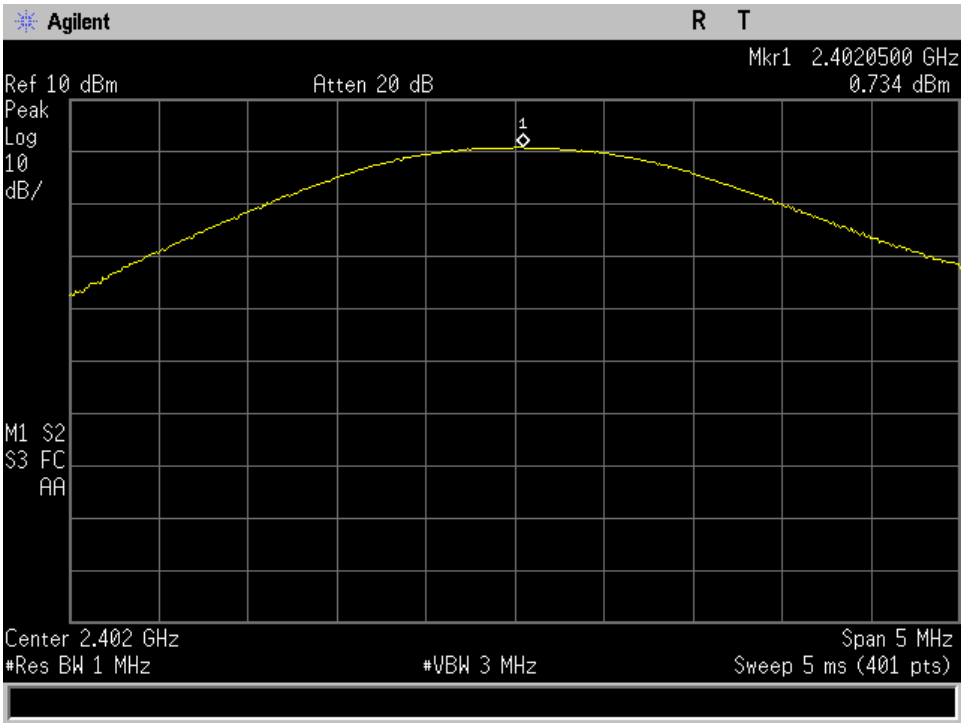
Low ch DH1 8PSK



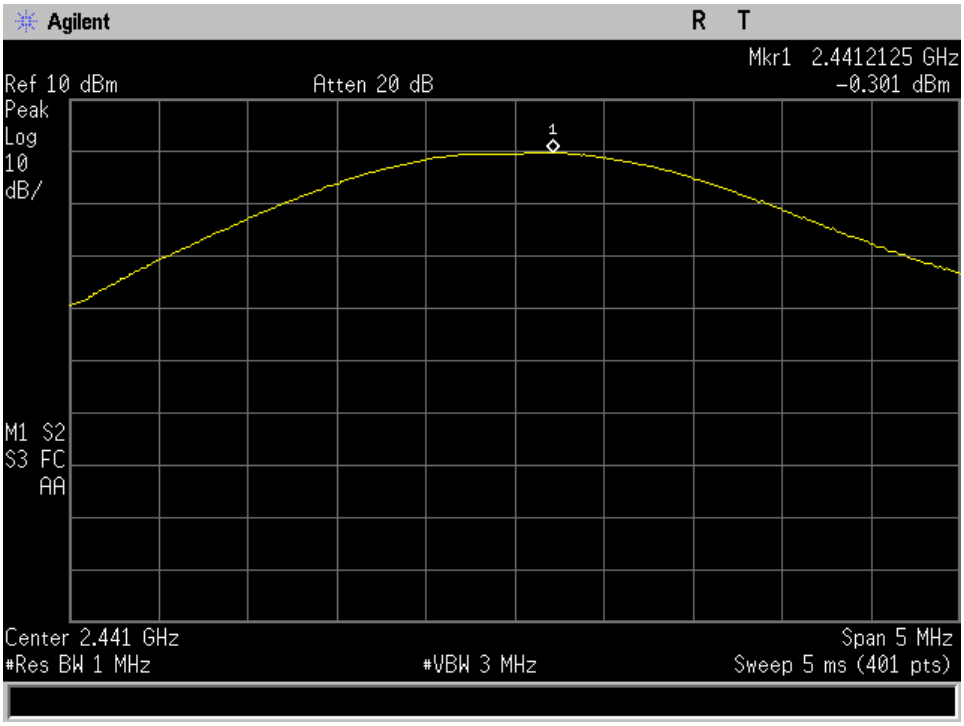
low ch DH1 GFSK



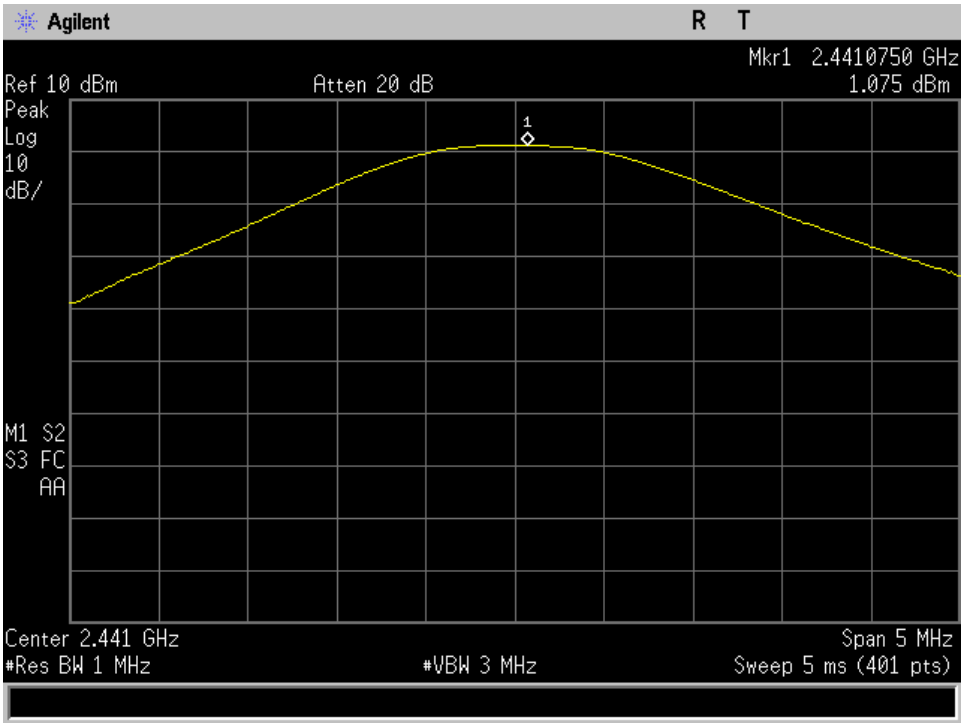
low ch DH1 QPSK



mid ch DH1 8PSK



mid ch DH1 GFSK



mid ch DH1 QPSK