Amp'ed RF
Wireless Technology

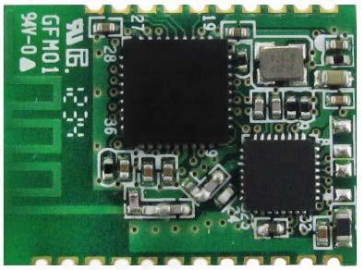
Fast Track Your Wireless Project
自由无线 放飞梦想

BT24 Datasheet

Amp'ed RF Technology, Inc.

Nov 11, 2012

BT24 Product Specification



15mm x 20mm

Description

Amp'ed RF Technology presents our BT24 Bluetooth module, low cost series. For applications requiring basic Bluetooth functionality, the BT24-LT is one of the most cost effective modules available. With support for both SPP and Apple IAP profiles, it can work with almost any mobile device or smart phone on the market, to quickly bring your wireless applications to market. The BT24-AUD module adds extra processing support for high-fidelity stereo audio applications.

The BT24 includes an integrated antenna, 13 GPIOs, SPI, I2C, PCM, DAC and A/D lines. Our standard abSerial and Amp'edUP Stack Lite are pre-flashed into the integrated flash memory. Customized firmware for peripheral device interaction, power optimization, security, and other proprietary features may be supported and can be ordered pre-loaded and configured.

BT24 Features

Bluetooth features

- Bluetooth qualified module
- Bluetooth v2.1+EDR
- Class 2 radio
- Range up to 60m LOS
- 400Kbps data throughput
- 128-bit encryption security

Hardware configuration

- Cortex-M3 microprocessor up to 72MHz
- 128K/256K bytes Flash memory
- 16K/48K bytes RAM memory
- UART, up to 921K baud
- SPI and I2C interfaces
- 13 general purpose I/O
- PCM audio interface
- 4 x12-bit A/D inputs
- 2 DAC output (BT24-AUD only)
- 1 LPO input

Embedded software

- Amp'edUP Bluetooth stack (SPP, IAP, A2DP, HID, HFP, OBEX)
- Support Apple iOS/MFI Bluetooth devices
- abSerial, AT command set
- BlueGuard, data encryption software (Optional)
- Mobile application software (Optional)

Additional documentation

- abSerial User Guide
- abSerial Reference Guide
- abSerial Configuration Guide

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1 Software Architecture

1.1 Lower Layer Stack

- Bluetooth v2.1+EDR
- Device power modes: active, sleep and deep sleep
- Wake on Bluetooth feature optimized power consumption of host CPU
- Authentication and encryption
- Encryption key length from 8 to 128 bits
- Persistent FLASH memory for BD Address and user parameter storage
- All ACL packet types.
- eSCO packet types: 2-EV3, 2-EV5, 3-EV3, 3-EV5
- Point to multipoint and scatternet support: 3 master and 7 slave links allowed (10 active links simultaneously)
- Sniff, and hold modes: fully supported to maximum allowed intervals
- Master slave switch, supported during connection and post connection
- Dedicated Inquiry Access Code, for improved inquiry scan performance
- Dynamic packet selection, channel quality driven data rate to optimize link performance
- Dynamic power control
- Bluetooth test modes per Bluetooth specification
- 802.11b/g/n co-existence: AFH
- Vendor specific HCI commands to support device configuration and certification test modes

1.2 Upper Layer Stack: Amp'ed UP Lite

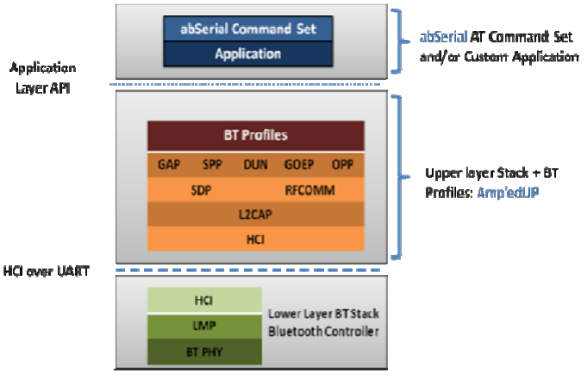
- SPP and IAP protocols
- RFComm, SDP, and L2CAP supported

1.3 HCI Interface

- Bluetooth v2.1 specification compliant
- HCI UART transport layer (H4)

1.4 AT Command Set: abSerial

- Please see *abSerial Reference Guide* for details



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2 Hardware Specifications

General Conditions (V_{IN}= 3.3V and 25°C)

2.1 Recommended Operating Conditions

Rating	Min	Typical	Max	Unit
Operating Temperature Range	-20	-	+60	°C
Supply Voltage V_{IN}	3.0	3.3	3.6	Volts
Signal Pin Voltage	-	3.3	-	Volts
RF Frequency	2400	-	2483.5	MHz

2.2 Absolute Maximum Ratings

Rating	Min	Typical	Max	Unit
Storage temperature range	-20	-	+80	°C
Supply voltage V_{IN}	-0.3	-	+5.0	Volts
I/O pin voltage V_{IO}	-0.3	-	+5.5	Volts
RF input power	-	-	-5	dBm

2.3 Current Consumption

Standard CPU speed, 8 MHz
- UART supports up to 480 Kbps
- Data throughput up to 300 Kbps
- abSerial v1.4 (installed firmware)

Modes (Typical Power Consumption)	Avg	Unit
ACL data 115K Baud UART at max throughput (Master)	29	mA
ACL data 115K Baud UART at max throughput (Slave)	29.5	mA
Connection, no data traffic, master	25	mA
Connection, no data traffic, slave	27	mA
Connection, 375ms sniff	2	mA
Standby, with deep sleep	160	uA
Page/Inquiry Scan, with deep sleep	2	mA

Stereo Audio (A2DP) mode
- SBC Codec at 44.1KHz sample rate
- I2S Output

Modes (Typical Power Consumption)	Avg	Unit
Sink, Streaming mode	46	mA

2.4 Selected RF Characteristics

Basic Data Rate

Parameters	Conditions	Typical	Unit
Antenna load		50	ohm

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Radio Receiver			
Sensitivity level	BER < .001 with DH5	-90	dBm
Maximum usable level	BER < .001 with DH1	0	dBm
Input VSWR		2.5:1	
Radio Transmitter			
Maximum output power	50 Ω load	+6	dBm
Initial Carrier Frequency Tolerance		0	kHz
20 dB Bandwidth for modulated carrier		0.9	MHz

2.5 I/O Operating Characteristics

Symbol	Parameter	Min	Max	Unit	Conditions
V_{IL}	Low-Level Input Voltage	-	0.7	Volts	V_{IN}, 3.6V
V_{IH}	High-Level Input Voltage	2.2	-	Volts	V_{IN}, 3.6V
V_{OL}	Low-Level Output Voltage	-	0.4	Volts	V_{IN}, 3.6V
V_{OH}	High-Level Output Voltage	3.0	-	Volts	V_{IN}, 3.6V
I_{OL}	Low –Level Output Current	-	4.0	mA	V_{OL} = 0.4 V
I_{OH}	High-Level Output Current	-	4.0	mA	V_{OH} = 3.3V
R_{PU}	Pull-up Resistor	80	120	KΩ	Resistor Turned On
R_{PD}	Pull-down Resistor	80	120	KΩ	Resistor Turned On

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2.6 Pin Assignment

Name	Type	Pin #	Description	ALT Function	5V Tolerant	Initial state
UART Interface						
RXD	I	8	Receive data		Y	
TXD	O	6	Transmit data		Y	
CTS	I	9	Clear to send (active low)		Y	
RTS	O	10	Request to send (active low)		Y	
Boot Loader						
Boot 0	I	2	Reserved			
Power and Ground						
V_{DD}		22	V_{DD}			
GND		21	GND			
Reset						
RESETN	I	3	Reset input (active low for 5 ms);		3.3V max	
GPIO – General Purpose Input/Output						
GPIO [0]	I/O	16	General Purpose Input/Output	SPI MISO	Y	Input pull down
GPIO [1]	I/O	17	General Purpose Input/Output	SPI MOSI	Y	Push-pull
GPIO [2]	I/O	18	General Purpose Input/Output	SPI SS	Y	Floating
GPIO [3]	I/O	1	General Purpose Input/Output	SPI CLK	Y	Input pull down
GPIO [4]	I/O	20	General Purpose Input/Output	ADC 0	3.3V max	Input pull down
GPIO [5]	I/O	11	General Purpose Input/Output	I2C SCL	Y	Input pull down
GPIO [6]	I/O	12	General Purpose Input/Output	I2C SDA	Y	Input pull up
GPIO [7]	I/O	13	General Purpose Input/Output		Y	Input pull up
GPIO [8]	I/O	4	General Purpose Input/Output	DAC 0	3.3V max	Input pull up
GPIO [9]	I/O	7	General Purpose Input/Output	DAC 1	3.3V max	Input pull up
GPIO [10]	I/O	5	General Purpose Input/Output	ADC 1	3.3V max	Input pull up
GPIO [11]	I/O	14	General Purpose Input/Output	OSC IN	Y	Input pull up
GPIO [12]	I/O	15	General Purpose Input/Output	OSC OUT	Y	Input pull up
LPO						
LPO	I/O	19	LPO Input		3.3V max	

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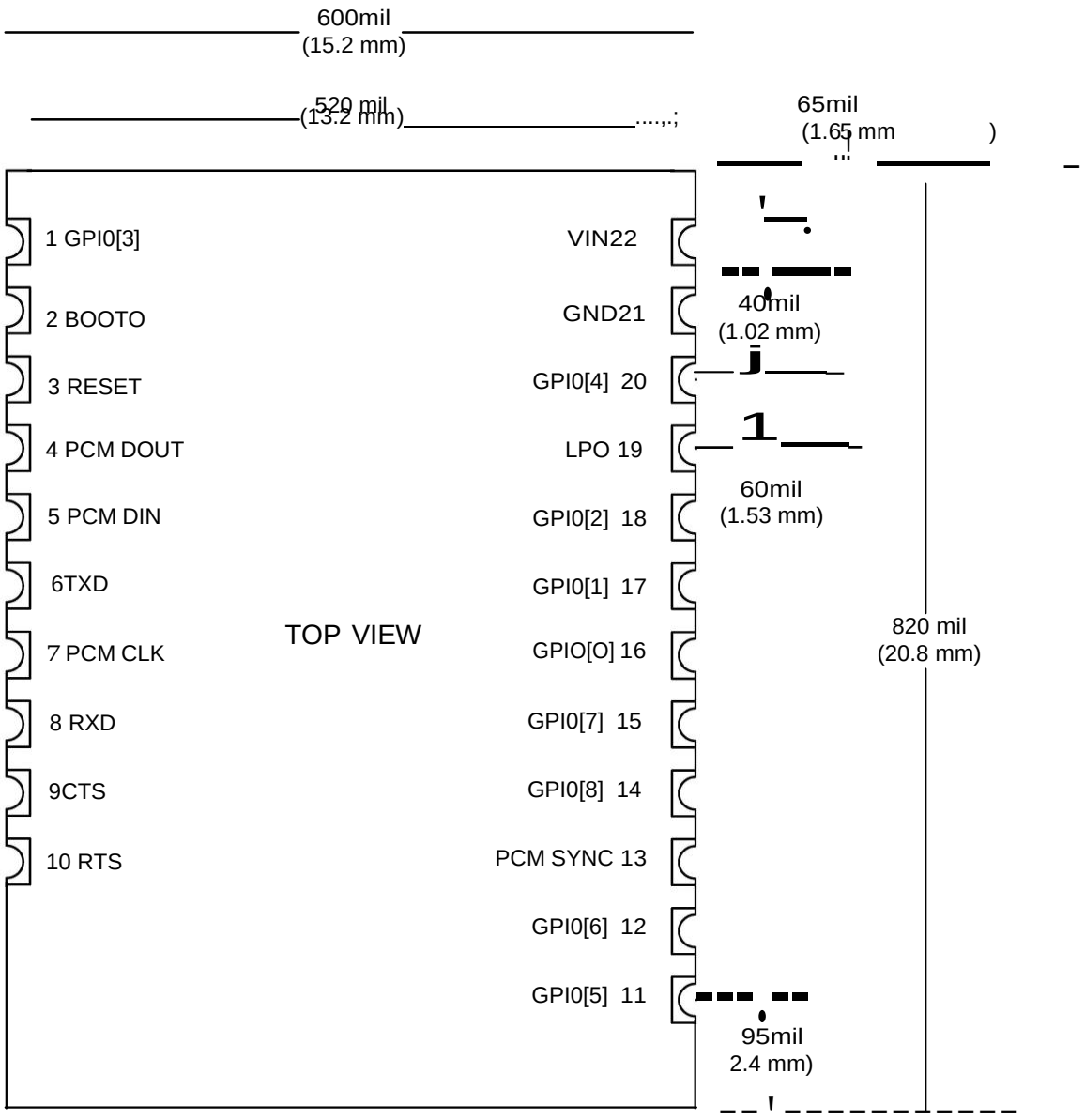
2.7 Layout Drawing

Size: 15 mm x 20 mm x 2.2 mm (height)



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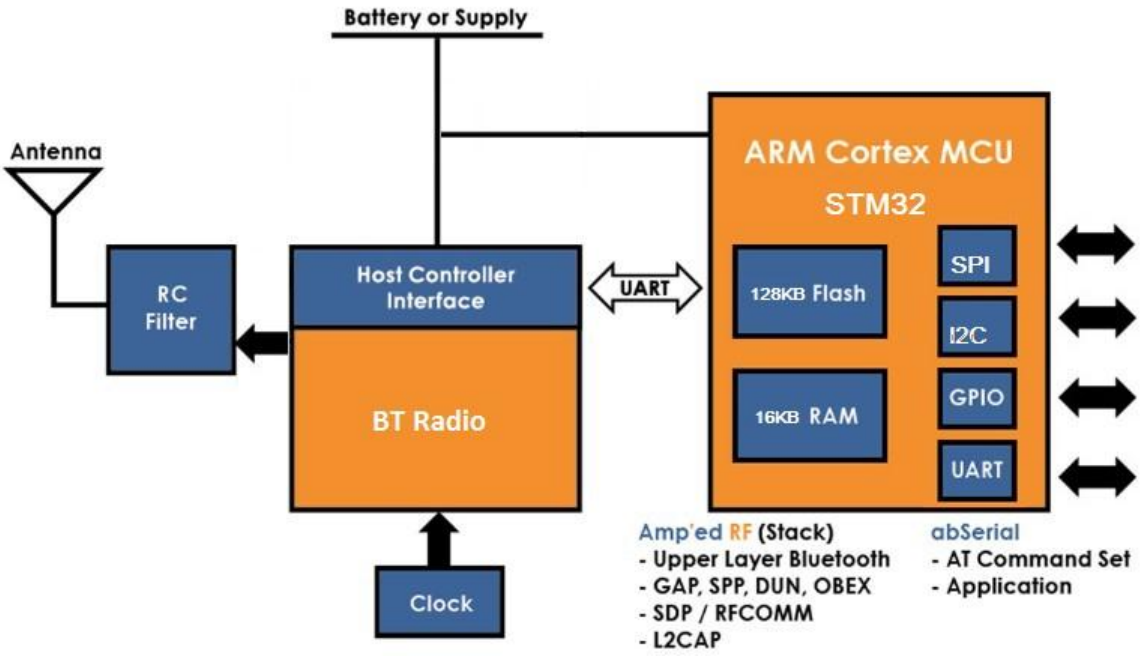
3 Module Block Diagram



4 Hardware Design

Amp'ed RF modules support UART, I2C, SPI, and GPIO hardware interfaces. Please note that the usage of these interfaces is dependent upon the firmware that is loaded into the module, and is beyond the scope of this document. The AT command interface uses the main UART by default.

Notes

- All unused pins should be left floating; do not ground.
- All GND pins must be well grounded.
- The area around the antenna should be free of any ground planes, power planes, trace routings, or metal for at least 6 mm in all directions.
- Traces should not be routed underneath the module.

4.1 Module Reflow Installation

The BT24 is a surface mount Bluetooth module supplied on a 22 pin, 4-layer PCB. The final assembly recommended reflow profiles are:

For RoHS/Pb-free applications, Sn96.5/Ag3.0/Cu0.5 solder is recommended.

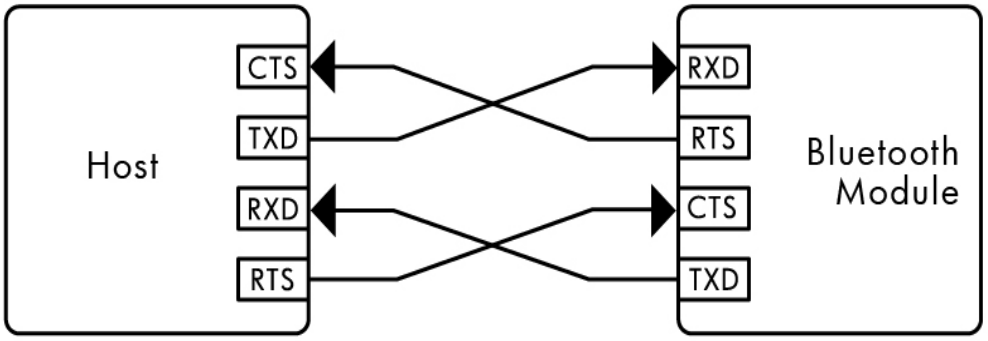
- Maximum peak temperature of 230° - 240°C (below 250°C).
- Maximum rise and fall slope after liquidous of < 2°C/second.
- Maximum rise and fall slope after liquidous of < 3°C/second.
- Maximum time at liquidous of 40 – 80 seconds.

4.2 GPIO Interface

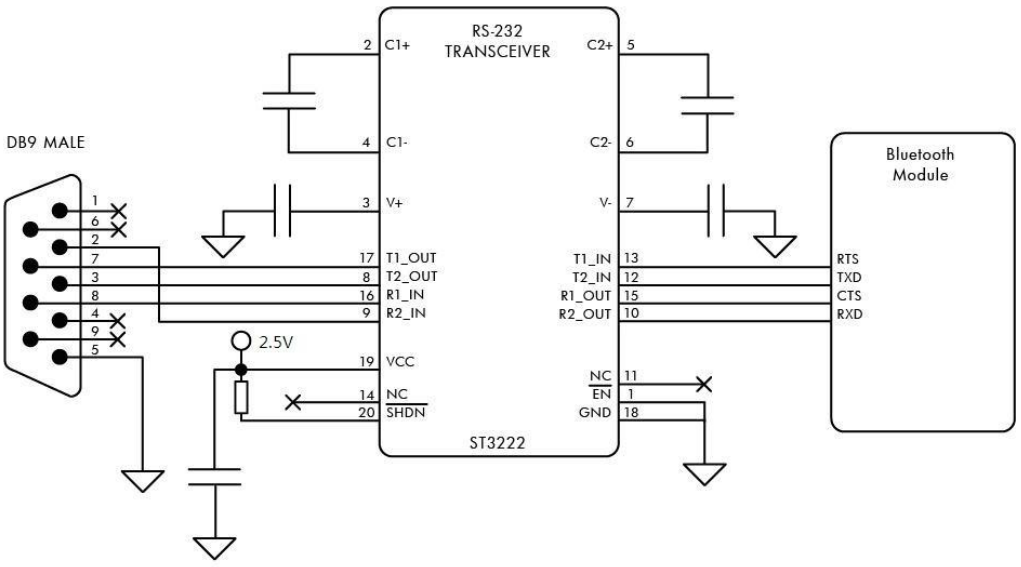
All GPIOs are capable of sinking and sourcing 4mA of I/O current.

4.3 UART Interface

The UART is compatible with the 16550 industry standard. Four signals are provided with the UART interface. The TXD and RXD pins are used for data while the CTS and RTS pins are used for flow control.



Connection to Host Device



Typical RS232 Circuit

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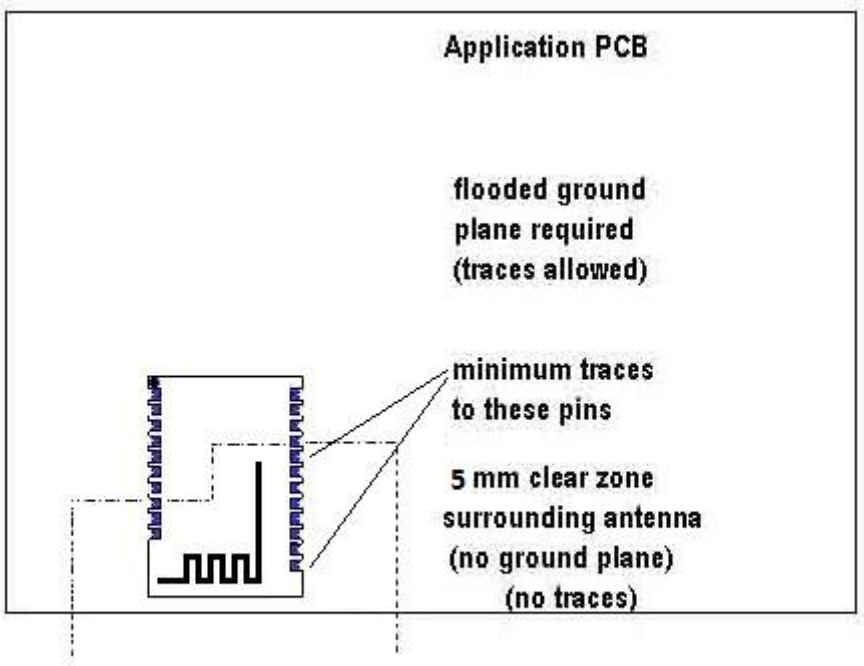
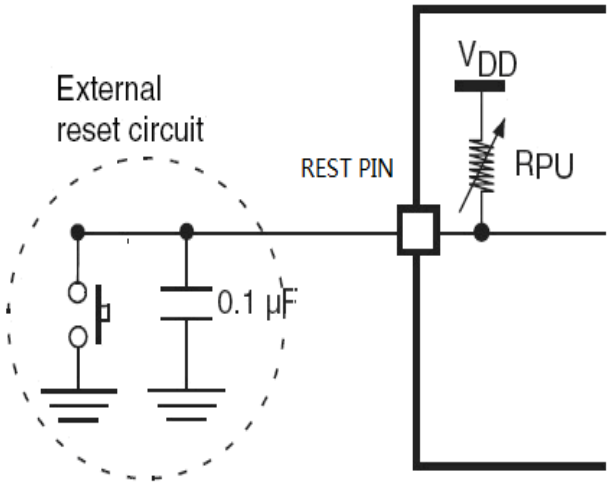
4.4 PCB Layout Guidelines



4.5 Reset Circuit

Two types of system reset circuits are detailed below.

4.5.1 External Reset Circuit:



Note: R_{PU} ranges from 30K ohm to 50K ohm internally.

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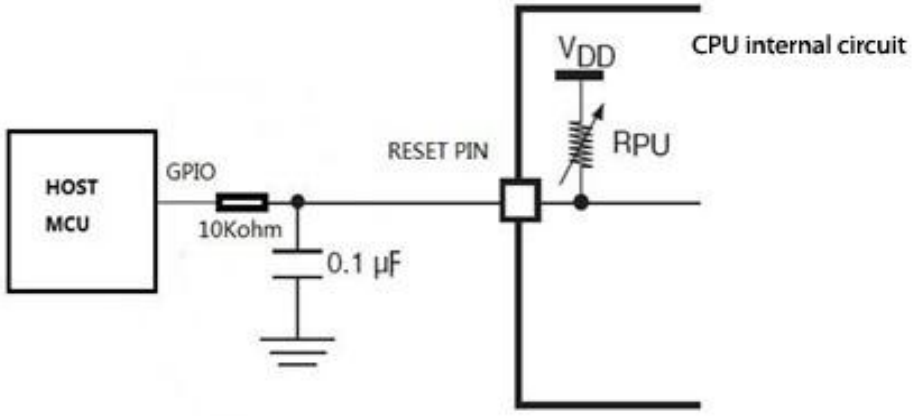
4.5.2 Internal Reset Circuit:



Notes:

- R_{PU} ranges from 30K ohm to 50K ohm internally.
- R_{RST} should be from 1K ohm to 10K ohm

4.6 External LPO Input Circuit

An optional low power oscillator input may be added to allow deep sleep and sniff modes.

LPO Parameters:

Frequency: 32.768 KHz

Tolerance: 150 ppm

Voltage Levels:

Low: 0.5 V

High: 1.8 V

Input Capacitance: 2.5 pF maximum

Configurations:

See configuration guide:

UseExtLPO

AllowSniff

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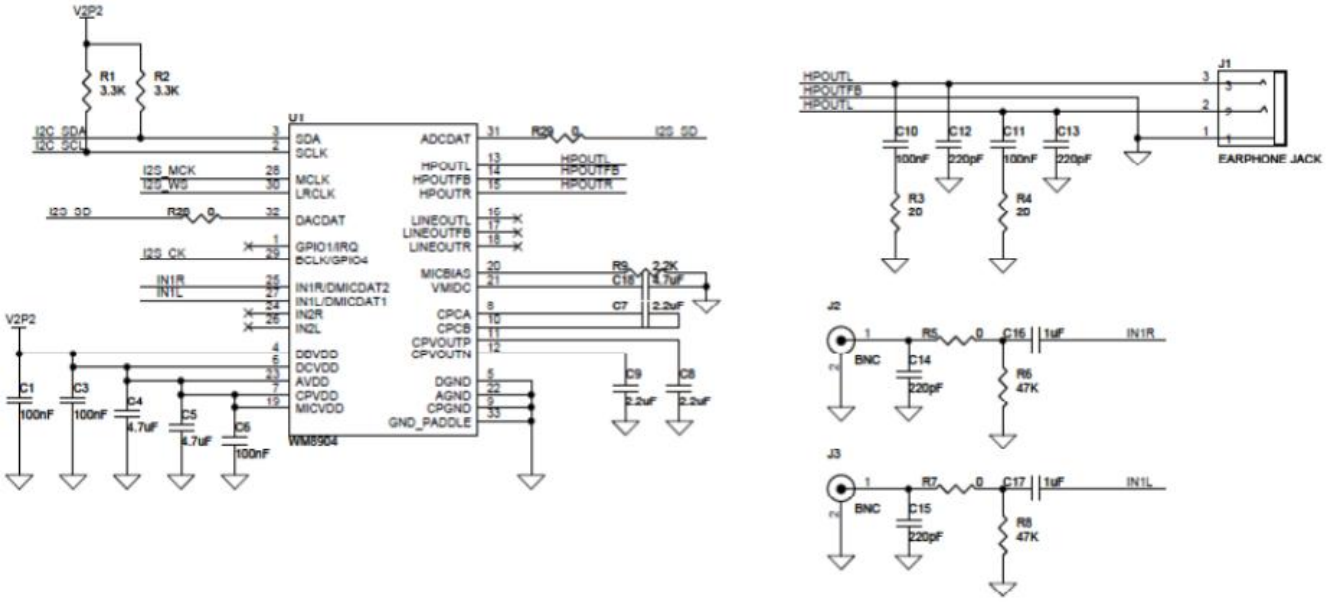
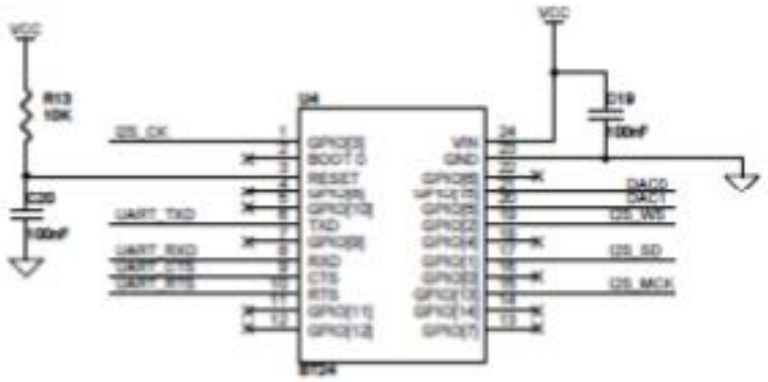
4.7 Audio application Reference Design



Part 1. WM8904



Part 2. BT Module

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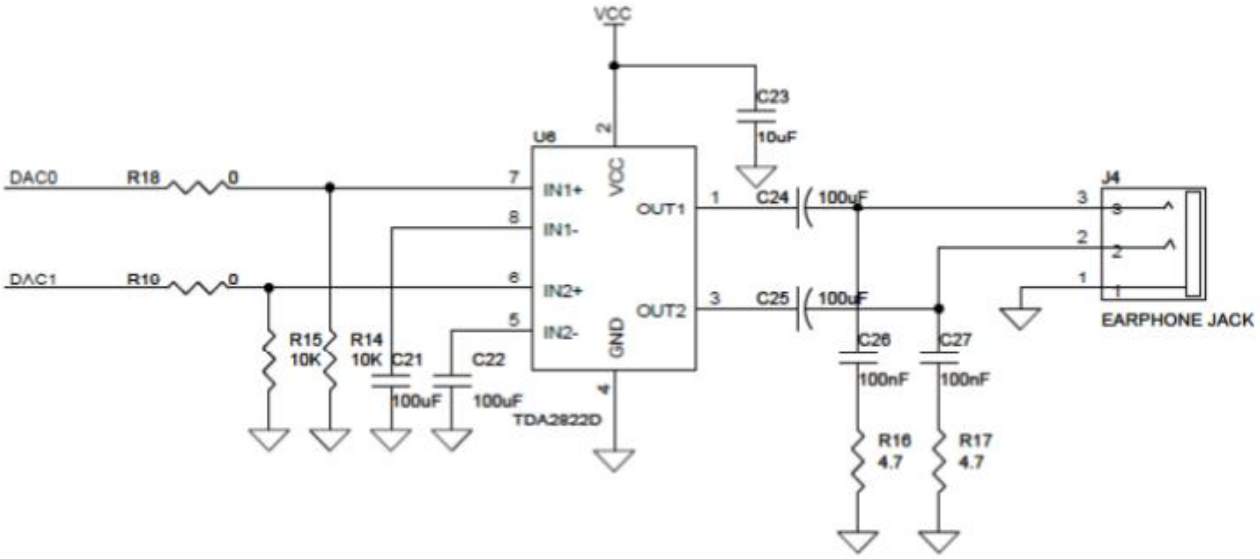

Part 3. Stereo DAC with Power Amp

5 Regulatory Compliance

This module has been tested and found to comply with the FCC Part15 and IC RSS-210 rules. These limits are designed to provide reasonable protection against harmful interference in approved installations. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Modifications or changes to this equipment not expressly approved by Amp'ed RF Technology may void the user's authority to operate this equipment.

5.1 Modular Approval, FCC and IC

FCC ID: X3ZBTMOD6

IC: 8828A-MOD6

In accordance with FCC Part 15, the BT24 is listed above as a Limited Modular Transmitter device. this is a limited modular approval, and any implementation in a host system must be authorized by a Class II permissive change or a verification by Amp´ed that the same conditions as shown in the original FCC Filing are met.

5.2 FCC Label Instructions

The outside of final products that contain a BT24 device must display a label referring to the enclosed module. This exterior label can use wording such as the following:

Contains Transmitter Module

FCC ID: X3ZBTMOD6

IC: 8828A-MOD6

Any similar wording that expresses the same meaning may be used.

6 Version Comparison Guide

	BT24-LT	BT24-AUD
BT Profiles	SPP, IAP, HID	A2DP, AVRCP, HFP ,HID, OBEX, SPP, IAP
RAM Memory	16K	48K
ROM Memory	128K	256K
CPU Speed	36MHz	72MHz
GPIO	9	13
ADC pins	1	4
DAC pins	0	2

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7 Ordering Information

Part Name	Description
BT24LT	Lite version
BT24-AUD	Supports stereo audio applications

8 Revision History

Data	Revision	Description
01-June-2012	1	First release
11-Nov-2012	1.1	Updated FCC and IC certifications
19-Nov-2012	1.2	Added BT24-AUD information Updated Pin assignment; Reference circuit

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