Semiconductors

AN10358

BGW200 Hardware Implementation Guide

Rev 1.3 — 17 July 2006 **Application note**

Document information

Info	Content
Keywords	BGW200, BGB203, BGB204, WLAN, Bluetooth, SiP, SDIO, SPI.
Abstract	This application note is intended to provide information necessary to design the BGW200 SiP into a product as quickly as possible to achieve fast time to market. This document will cover hardware, software and systems integration issues spanning the product development cycle from design and development through product implementation and mass production. In addition, information is provided to allow the end product to be designed to accept the BGW211 802.11g SiP later as a drop-in replacement for the BGW200; thus making it very easy to upgrade the product from 802.11b to 802.11g.

PHILIPS

Revision history

Rev	Date	Description
1.0	20050408	Initial release
1.1	20050520	Added power ON reset timing detail to Section 3.5.1. Added Section 3.10 “Tx Filter Suppliers”. Added Section 4 “802.11b Spectral Mask and FCC Certification”. Corrected Table 12 to specify MODE_3 and MODE_4 pins as no connects. Removed Evaluation kit support package from Section 17.
1.2	20060320	Clarified Section 5.4.1, SPI Boot from Host. Added more detail to Section 12, System Configuration Methodology. Updated Section 17, General Support. Added FAQs for supported regional domains and boot-up troubleshooting. General document update.
1.3	20060717	Changed document name to BGW200 Hardware Implementation Guide Remove WinCE 4.2 as a supported platform from Table 1. Added Table 3 in section 3.1 for Two Regulator Supply configuration. Removed section on firmware customization for GPIOs. Add FAQ for fast SPI CLK implementation. Added BGW200 Software Implementation Guide to List of References

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1. Introduction

The BGW200 System-in-a-Package (SiP) is a complete low-power, IEEE 802.11b solution in a miniature 10 x 15 x 1.3mm HVQFN-like 68 pin package. When combined with one of the standard software packages, the system delivers state-of-the-art performance with industry leading low-power performance thanks in part to its no-host-load architecture.

The no-host-load system architecture delivers truly optimal system standby performance as the host system can sleep while the BGW200 is in standby mode monitoring beacons – no host interaction is required. When the BGW200 processes a beacon that indicates incoming WLAN traffic for the client, the BGW200 will wake the host to initiate reception and data transfer to the host. Likewise, when the host processor is ready to send data, it can wake the BGW200 when ready to transmit.

WLAN + Bluetooth co-location is also bundled into the BGW200 system for those applications requiring both high speed, medium range and medium speed, short range data links, for example smart phones or feature phones that support wireless Bluetooth headsets. Philips Semiconductors is in a unique position to provide a complete, optimized WLAN + Bluetooth solution as a result of actively developing products for both of these popular connectivity technologies.

The BGW200 system provides the product developer with a complete WLAN plug-and-play solution that can be easily integrated with any of the standard platforms listed in **Table 1** below. Note - SDIO applications are not currently supported as indicated from their absence from the table; however, some information is provided in this guide for informational purposes only.

Table 1 - Supported Standard Platforms

Operating System (OS)	Host Processor	Host Interface
Windows CE 5.0	Intel PXA270 (Bulverde)	SPI
eLinux	Intel PXA270 (Bulverde)	SPI
eLinux	TI OMAP 1510	SPI

Each standard platform is designed to make the product development cycle as simple and as fast as possible to address fast time-to-market requirements. With the radio section residing entirely within the SiP, no longer is any RF “black magic” necessary to bring the product to market. The only RF design left to the developer is selecting appropriate antennas, a suitable Tx filter at the ANT_MAIN port for 2nd harmonic suppression and to address co-location issues, and routing 50-ohm traces between these components and the appropriate pins of the BGW200.

Note - all RF measurements contained herein do not include the Tx filter.

2. Features

Please refer to the BGW200 data sheet **[1]** for an extensive list of features supported by this product. The data sheet is also a source of more detailed design information as are numerous other documents referenced throughout this note.

Figure 1 below is a block diagram showing the major functional blocks inside the BGW200.

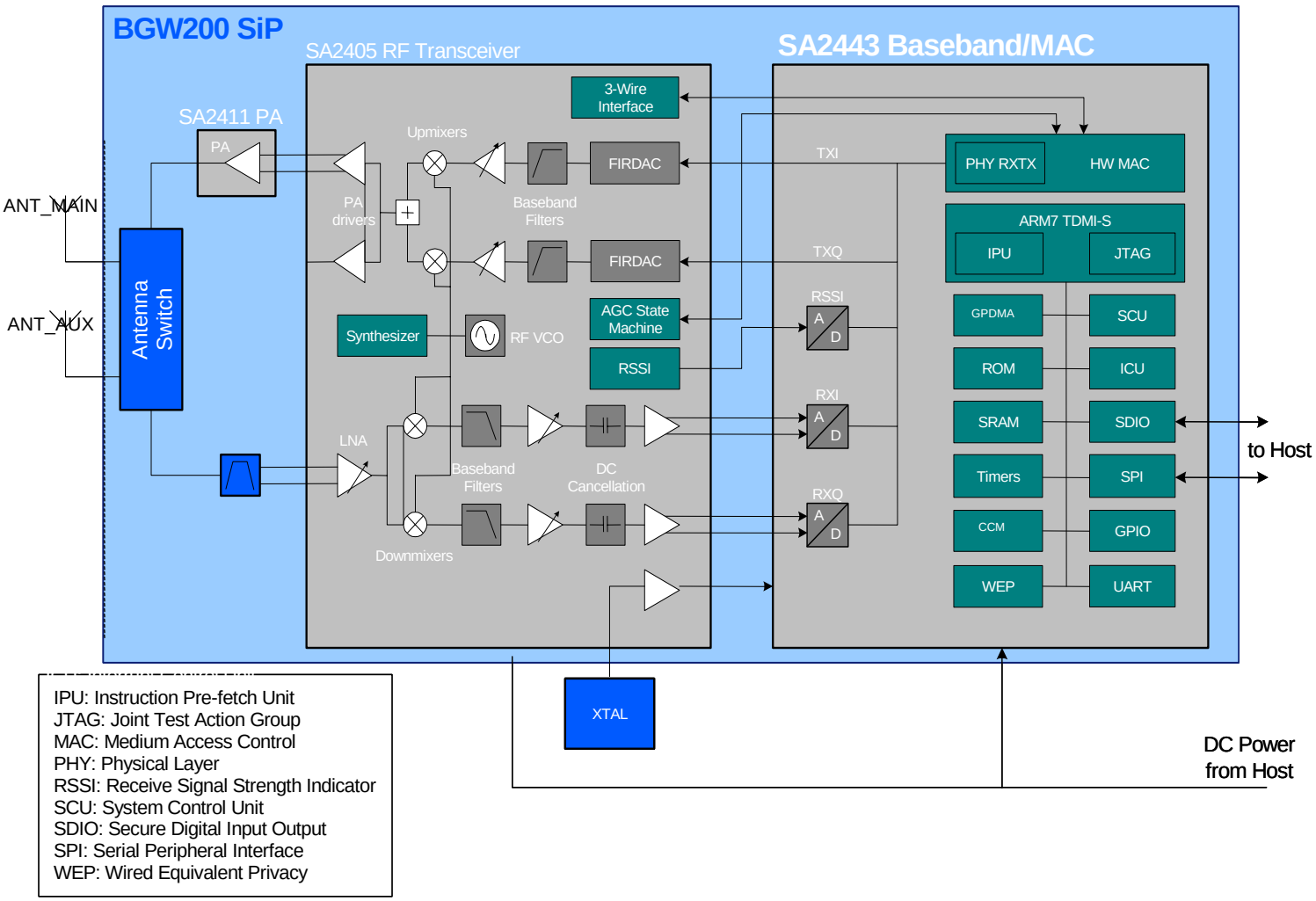

Figure 1 - BGW200 functional block diagram.

3. Hardware Design & Systems Integration

The level of integration achieved with the BGW200 simplifies considerably the integration of WLAN into the end product as exemplified by the reference schematic shown below for the SPI (Serial Peripheral Interface) embedded application. With clean supplies provided to the chip, and decoupling and control line filtering provided inside the SiP, the only external components typically required for the BGW200 are external antennas, the Tx filter for 2nd harmonic suppression and to address co-location issues, and the 44MHz crystal unit and associated capacitors to implement the Colpitts oscillator circuit. Voltage regulator circuitry are not shown as their implementation will vary with application.

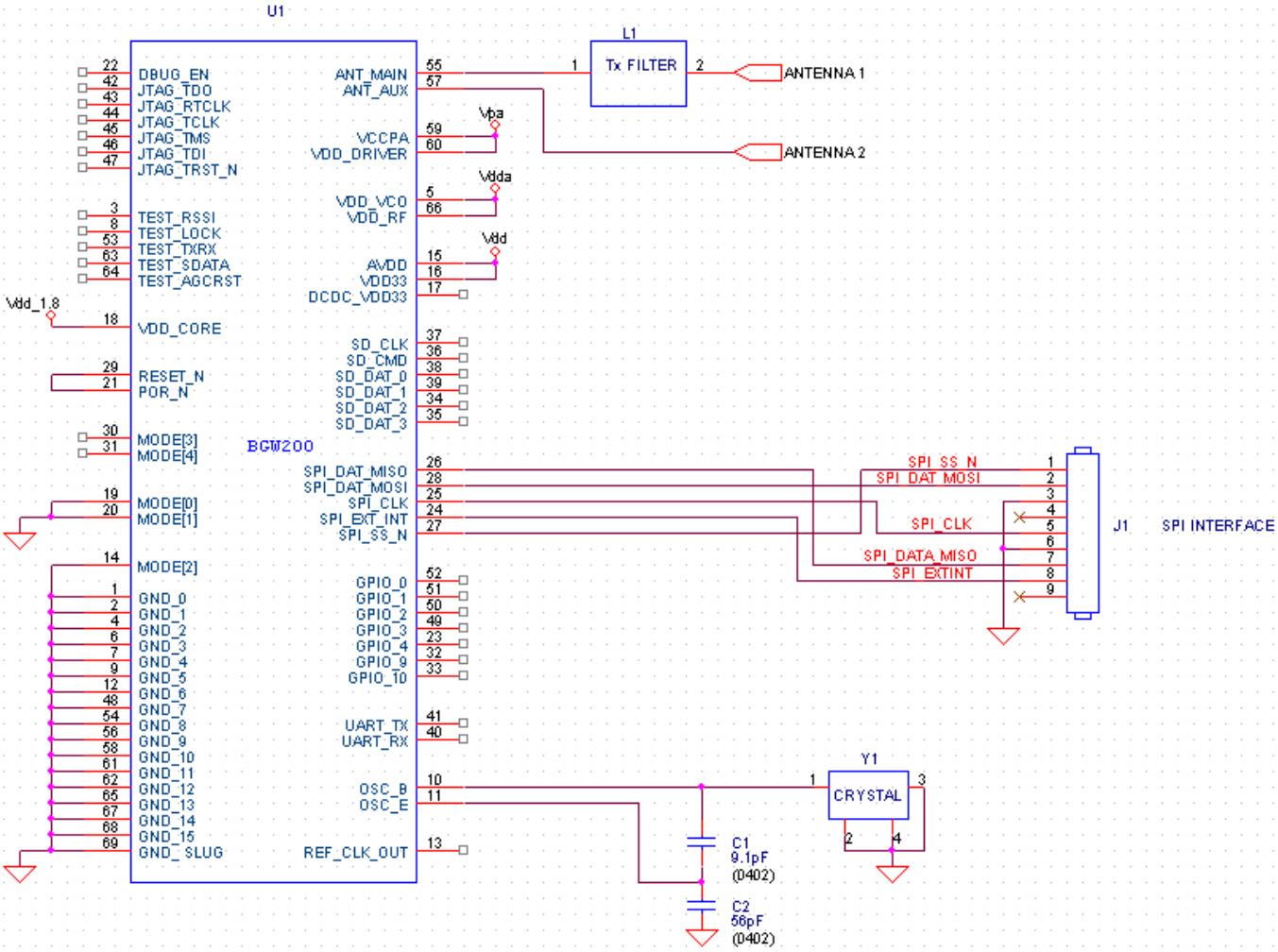

Figure 2 – BGW200 schematic for SPI embedded applications.

The remainder of this section will focus on presenting information to enable the designer to achieve a first-time-right design using the BGW200.

3.1 Icc by Supply Domain

The following tables are provided to allow the systems integrator to specify and design the voltage regulator or PMU (Power Management Unit) circuit for the BGW200. In **Table 2** four separate regulated supplies are shown but single 2.85V and 1.8V regulated supplies have also been used successfully and **Table 3** has been repartitioned to reflect this configuration.

Table 2 – Four regulator supply scheme with common 2.85V supplies.

Domain	Description	Voltage (V)	Max. Current (mA)
VDD_PA	PA 2.85V supply	2.85	250
VDD_DRIVER	PA driver 3V supply	2.85	
AVDD	Radio 3V supply, analog	2.85	95
VDD_VCO	VCO 3V supply, analog	2.85	
VDD_RF	Radio 3V supply, digital	2.85	
VDD_IO	BB 3V supply, digital	2.85	22
VDD_CORE	BB 1.8V supply	1.8	85

Table 3 - Two regulator supply scheme.

Domain	Description	Voltage (V)	Max. Current (mA)
VDD_PA	PA 2.85V supply	2.85	367
VDD_DRIVER	PA driver 3V supply		
AVDD	Radio 3V supply, analog		
VDD_VCO	VCO 3V supply, analog		
VDD_RF	Radio 3V supply, digital		
VDD_IO	BB 3V supply, digital		
VDD_CORE	BB 1.8V supply	1.8	85

Table 4 shows a slightly different scheme whereby split 3V supplies are implemented in order to operate the PA at its optimal 2.85V supply voltage while providing the flexibility to operate the rest of the SiP at a higher voltage (3.2V in this example) to allow the BGW200 to interface properly with the host processor. This would eliminate the possible need for additional level shifting circuitry should the host processor not be capable of 2.85V operation.

Table 4 - Four regulator supply scheme with split 3V supplies.

Domain	Description	Voltage (V)	Max. Current (mA)
VDD_PA	PA 2.85V supply	2.85	210
VDD_DRIVER	PA driver 3V supply	3.2	135
AVDD	Radio 3V supply, analog	3.2	
VDD_VCO	VCO 3V supply, analog	3.2	
VDD_RF	Radio 3V supply, digital	3.2	
VDD_IO	BB 3V supply, digital	3.2	22
VDD_CORE	BB 1.8V supply	1.8	85

3.2 Recommended BGW200 PCB Footprint

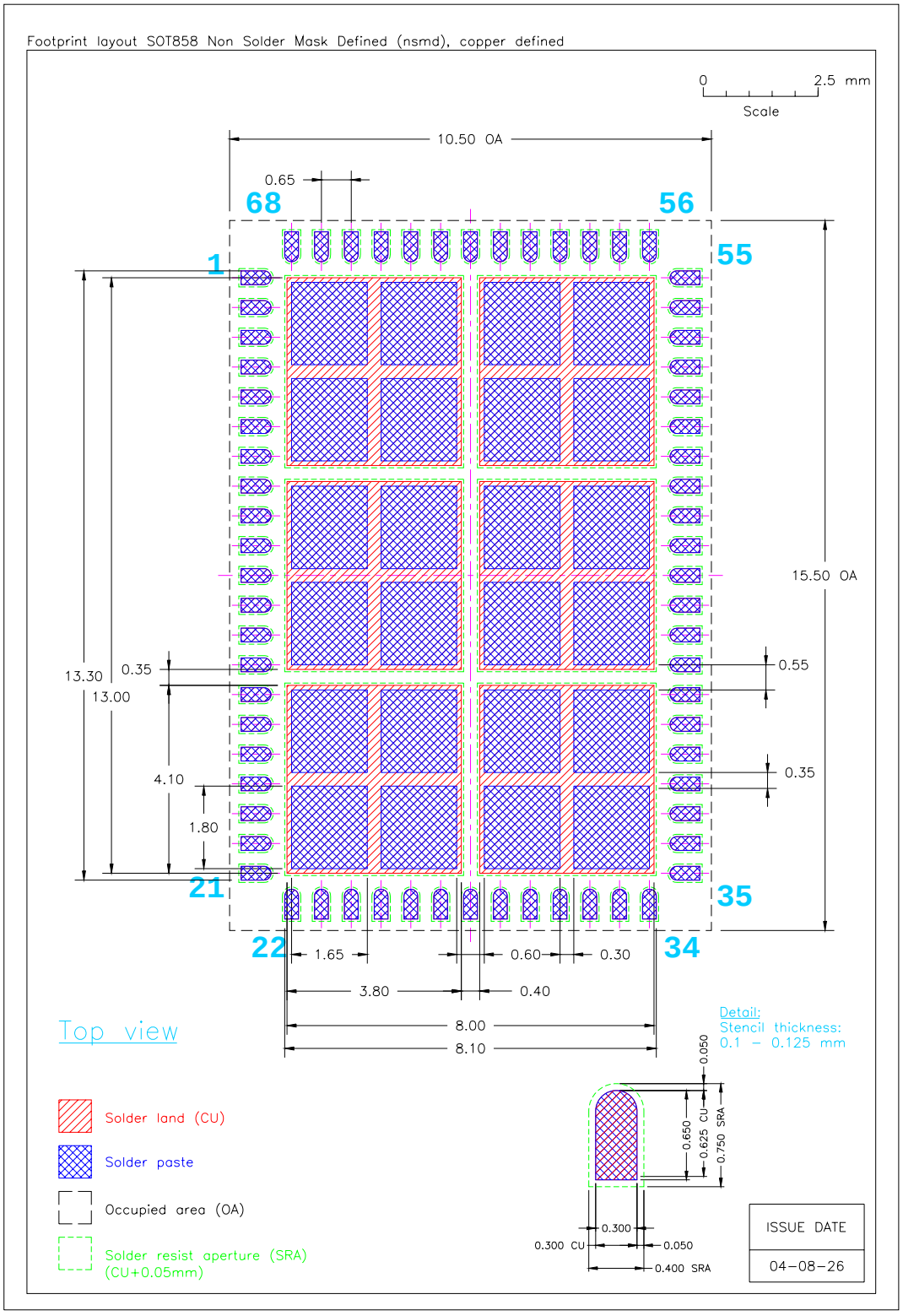

Figure 3 - Recommended BGW200 PCB footprint.

3.3 PCB Design and Layout Guidelines

PCB design and layout guidelines to consider when designing the BGW200 into the end product are provided below. The list is relatively short due to the level of integration achieved with the BGW200 resulting in a very simple board design as exemplified by the Nova evaluation board **[2][3][4][5][6]**.

1) Use 50-Ohm transmission lines for the antenna traces and keep the length to the antennas as short as possible. It is recommended that the transmission lines be made as wide as possible while assuring 50-Ohm characteristic impedance, to reduce insertion loss.
2) Grounding is very important in order to achieve optimal performance; thus, remove solder mask on the pads underneath the BGW200 (see **Figure 3** on the previous page) and make them GND planes to assure good grounding.
3) For the SPI or SDIO interfaces, minimize the trace lengths, keep traces equal in length, and avoid vias on these traces between the BGW200 and the host.
4) Keep the crystal and associated components as close as possible to the BGW200 OSC_B and OSC_E pins. It is also recommended that the crystal and associated components be kept on the same side of the PCB as the BGW200.
5) Power supply lines should not be routed close to or underneath the RF traces, or near the XTAL oscillator circuitry, and ensure that power supply related noise and ripple are kept to a minimum.
6) VCC traces should be designed to minimize the voltage drop from the power source to the BGW200. For example, the BGW200 nominally consumes 760mW at 15dBm Tx output power; thus, it is recommended that the VCC traces be at least 60 mils wide for 1 oz. Copper.
7) Providing pads for power supply line decoupling close to the pins of the BGW200 is recommended for initial prototype builds. Even though the supply lines are internally decoupled, this may not be enough depending upon the system and PCB layout.
8) For single antenna applications, the unused ANT2 port should be terminated with a 50-ohm resistor to GND.
9) For SDIO 1-bit applications, the unused SD_DAT2 and SD_DAT3 lines should be tied high to the 3V supply via a 47k pull-up resistor unless these pins are connected to the host processor which can then pull these pins high as required.
10) Unused pins can be left floating unless otherwise specified, e.g. unused SPI, UART, GPIO, mode pins and JTAG interface lines, except DBUG_EN which should be tied to GND for normal operation.
11) JTAG pins are for internal use only.

3.4 System Clocks

The BGW200 system requires two clocks for optimal low power performance, the main system clock running at 44 MHz and a power save sleep clock running at 32 kHz. The BGW200 is capable of deriving the 32 kHz sleep clock internally; however, for improved low power performance, using a more accurate, crystal-based 32 kHz sleep clock that is typically available from the host is also an option.

3.4.1 44 MHz Crystal Options

Two suppliers of the 44MHz crystal unit have been identified: TEW and Kyocera (formerly KSS). The recommended implementation of the 44MHz XO is the Colpitts configuration shown in the earlier reference schematics. The center frequency of the XO can easily be adjusted by changing C1 and if necessary C2 in the schematics above.

3.4.2 32 kHz Sleep Clock Options

There are two ways to derive the 32 kHz sleep clock for the BGW200, externally apply at GPIO4, or use the internal 1MHz/32kHz power save CLK. Which option to use depends upon the application. Slightly improved power saving is achieved using the external 32kHz clock options and a highly accurate, crystal-based clock source typically available in mobile, handheld products. This has the added advantage of also reducing BOM costs.

The system designer can easily select the 32 kHz sleep clock option by storing appropriate data in host non-volatile memory (NVM) that will be covered in **Section 11** of this document.

3.5 Reset Options

3.5.1 Power ON Reset

Stable 3V power to the BGW200 must be present prior to the application of the 1.8 core supply in order to ensure that power ON reset will be implemented properly. After the 1.8V supply voltage has stabilized, the SA2443 power ON reset circuit will wait ~4ms before initiating the system reset. This is necessary to allow time for the 44MHz system clock to stabilize.

In addition, all digital IO lines to the BGW200 must be held low until after the completion of the power ON reset in order to ensure that the device will boot properly. **Figure 4** below is a graphical representation of the power ON reset sequence to follow to ensure proper power up initialization and subsequent operation, where T1 and T2 represent the times when the 3V and 1.8V supplies achieve operational threshold. Since these times are unique to power supply design, it is recommended that the system designer measure T1 and T2 for their product and provide the necessary delay, T_{guard}, in SW.

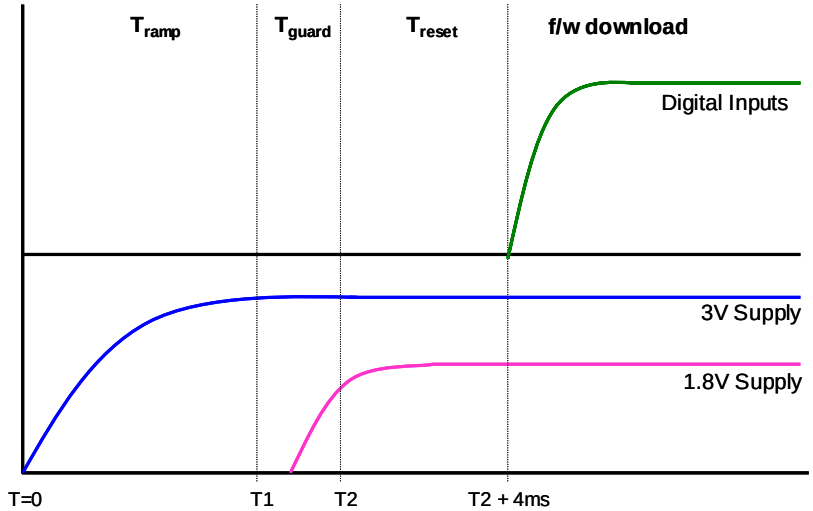

Figure 4 - Power ON Timing Diagram.

Note - the RESET_N pin is not intended to be used as a hardware reset pin but rather as an input for the power ON reset signal issued at the POR_N pin after the power up timer has expired.

3.5.2 Powering Down the Device

In order to not damage the BGW200 in the powered down state, all I/O lines to the BGW200 should be at 0V or GND prior to applying or removing DC power. This is to prevent damage to the ESD protection diodes inside the SiP and the keep the system from entering undefined states.

Also, to prevent putting the device into an undefined state where it could draw more DC current, all DC power should be removed from the device when powered down. That is to say, removing the 1.8V supply and leaving the 3V supply active (and vis versa) is not permissible.

3.5.3 Operational Reset

During normal operation, it may become necessary to reset the BGW200 and the method used must take into account the architecture of the SIP and all the possible conditions the SIP may be in upon application of the reset.

During normal operation, the BGW200 can be reset via software by writing the appropriate reset register **[1]**. However, in the case of a software hang the system may not be able to execute such a soft reset.

It may seem logical to utilize the chips RESET_N pin as a hardware reset input, however, while in sleep mode, the 44MHz CLK cannot be enabled using this method which eliminates this as a possible solution, especially considering that the BGW200 will spend most of its time in sleep mode in the typical application.

The only reliable way to reset the system is to cycle power to it and thus it is strongly recommended that this method be implemented. For embedded solutions this can typically be done without the end user being aware. The host can reset the BGW200 by simply disabling, then re-enabling the voltage regulators that power the SiP to execute a power ON reset. Not implementing this procedure could result in the end user having to remove and then re-install the battery to reset the BGW200 which is not acceptable.

3.6 Antenna Suppliers

There are many manufacturers of 2.4GHz antenna for the WLAN application and as antenna choice is very dependent upon the performance, size, and cost constraints of a particular design, choice of antenna is left up to the designer. PCB layout in and around the antenna has a direct impact on antenna performance, thus the antenna manufacturer typically provides very detailed PCB layout guidelines to ensure optimal performance. Please refer to the antenna manufacturer's PCB layout guidelines.

The following is a short list of possible 2.4 GHz WLAN antenna suppliers to assist the designer in the search for the best antenna for the job. The list is not exhaustive and is provided merely as an aid for initiating the search.

- Antenovo
- Etheronics
- Murata
- TDK
- Toko
- Walsin

3.7 EEPROM and Flash Memory Suppliers

During the evaluation and development stages of an OEM product and production stage of a module product, a serial Flash may be necessary to hold and download special test firmware to support evaluation and production test respectively. In these instances an Atmel AT25F1024 1-Mbit SPI serial Flash Memory or equivalent is recommended.

3.8 RF Shielding

Radiated emission measurements to date using BGW200 evaluation hardware indicate that an external RF shield will likely be required in the end item in order to pass regulatory radiated emission requirements. It should be noted however, that these measurements vary with PCB layout.

3.9 Tx Filter Suppliers

As already mentioned, external Tx filtering is needed on the ANT_MAIN output to achieve and additional 15dB attenuation of the Tx 2nd harmonic in order to achieve FCC compliance. It is recommended for design simplicity and minimal PCB foot print that a low-cost, ceramic type filter be used. The following is a short list of possible suppliers of these filters to assist the designer in the search for suitable solution. The list is not exhaustive and is provided merely as an aid for initiating the search.

- Epcos
- Murata
- Soshin

3.10 Nova Board Power Up Initialization

When bringing up a Nova board for the first time while connected to a suitable host via the SPI interface, the following power up check out and initialization sequence is recommended.

1) Verify all power supplies are configured for the proper voltages and polarity.
2) Set current limits on the power supply (if applicable) and apply power to the system.
3) Ensure that the power supplies to the Nova board are clean.
4) Verify the power on reset circuitry is configured properly.
5) Verify the proper boot mode is selected via the MODE(1) and MODE(2) pins, “00” for SPI host boot mode.

Table 5 - Boot Mode Selection

MODE[1]	MODE[0]	MODE
0	0	SPI-HOST
0	1	SPI-EEPROM
1	0	SDIO-HOST
1	1	SDIO-EEPROM

6) Verify all the Nova board jumper settings are properly set per the Nova Board Users Guide **[2]**.
7) Power up the host first and wait a few seconds, then power up the Nova board.
8) Verify that the system will power-up in the proper sequence as defined in Section 3.5.1 above.
9) Ensure that all host interface lines are connected.
10) Verify that the 44MHz CLK is on frequency (44 MHz +/-440 Hz) and adjust if necessary.
11) Monitor the host interface with a logic analyzer to ensure that the f/w is being downloaded properly.
12) Keep host interface cables as short as possible, less than 6” is recommended.
13) Capture the digital signals on the host interface with an oscilloscope and ensure that they are not distorted.
14) Verify that the Tx and Rx performance is functioning properly by downloading the test firmware into the BGW200 and using the PHY GUI test software **[10]** along with suitable RF test equipment.

4. 802.11b Spectral Mask and FCC Certification

The IEEE spectral mask specification for 802.11b, as originally laid down, may be somewhat tighter than absolutely necessary for acceptable system performance. Indeed many of the early 802.11b products from various manufacturers were unable to achieve this level of performance.

The concept of spectral mask is used in nearly all digital communication systems to control the amount of power that is spilt into adjacent channels. In the case of IEEE 802.11b the limits of this mask were derived using the best knowledge at the time and were agreed as depicted in Figure 5 below.

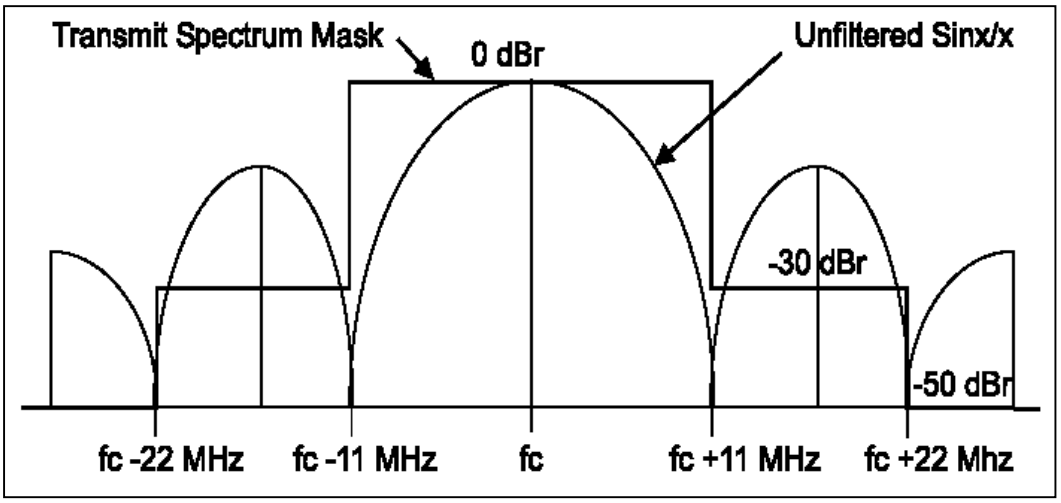

Figure 5 - IEEE 802.11b spectral mask requirements.

With the current technology vs. cost vs. power consumption tradeoffs, it is quite difficult to achieve –50dBr level requirement of 802.11b and extremely careful optimization needs to be performed.

IEEE 802.11a, and later IEEE 802.11g spectral mask requirements for OFDM modulation has a different spectral shape than that of 802.11b. Most notable are the lower limits of the mask, –40dBr instead of the more stringent –50dBr of 802.11b, as shown in **Figure 6** on the following page.

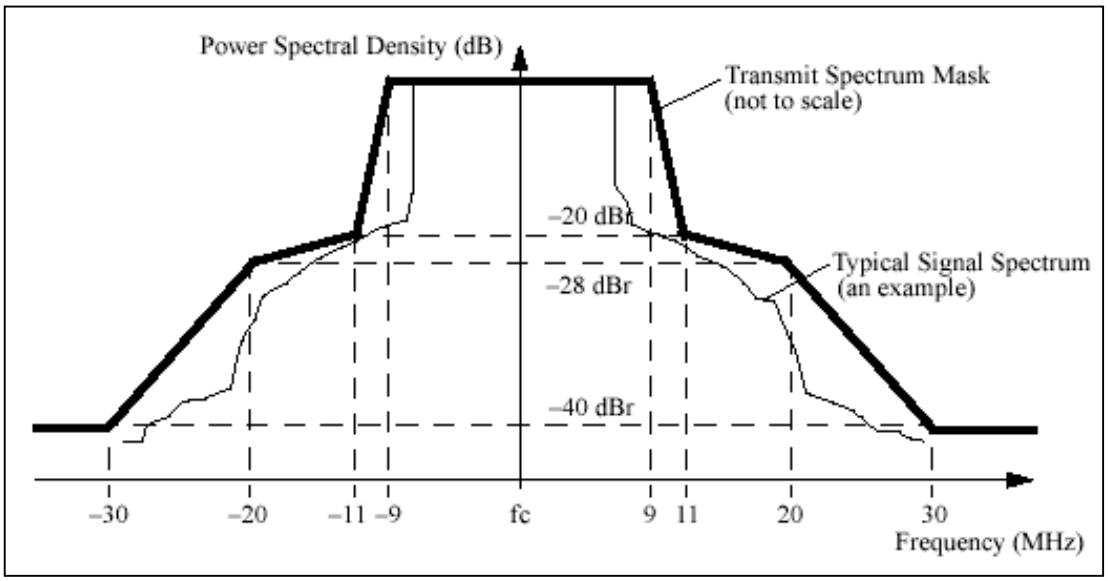

Figure 6 - IEEE 802.11a/g spectral mask requirements.

4.1 FCC Regulatory Certification

Most regulatory bodies set limits on the power that can be spilled into adjacent bands so that users in neighboring channels are not affected. Often the notion of spectral mask is used to guarantee compliance.

Figure 7 represents the 802.11b Tx signal on channels 1 and 3, the black and green waveforms, at +17dBm and +26dBm respectively. The bold red line at the top of the diagram represents the FCC maximum peak power limit of 1W for this band

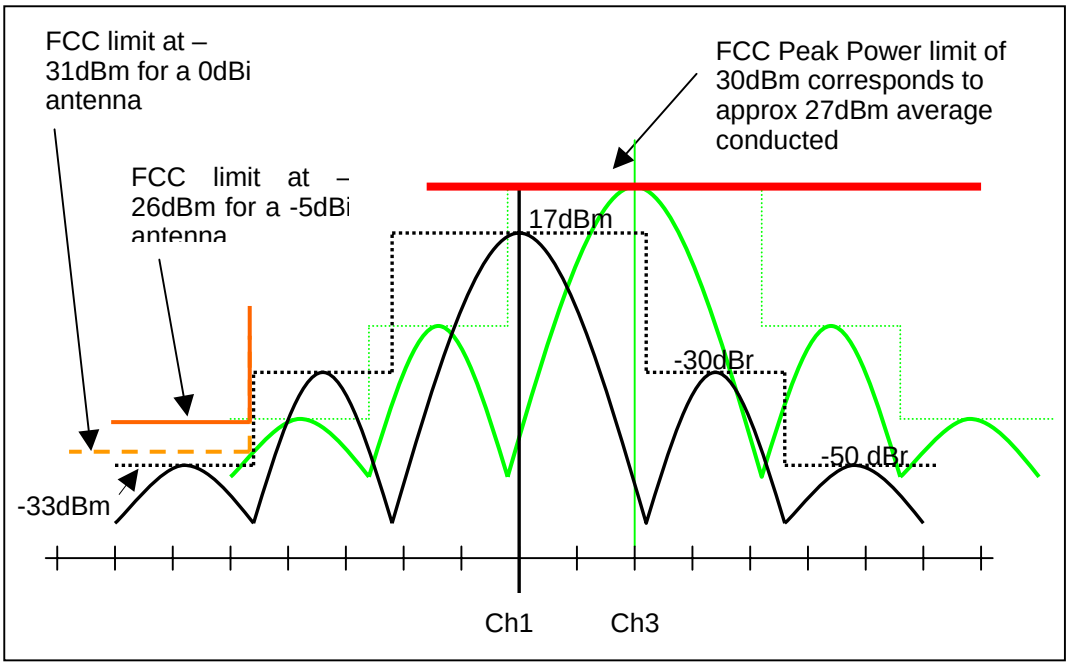

Figure 7 - IEEE 802.11b spectral mask and FCC requirements.

In order to convert the radiated FCC restricted band limit to a conducted measurement, the following equation is used where levels are expressed in dBm, and G_{max} is the maximum antenna gain.

$$L_{rb} = G_{\max} - 31.25$$

In many WLAN systems +17dBm is chosen as a maximum output power because in practice this provides sufficient range performance to suit most applications, thus **Figure 7** has been set up to illustrate this typical output power.

Now consider the case where the antenna gain is 0dBi. The corresponding conducted FCC limit is represented by the dashed orange line on the left of the diagram depicting 2dB margin between the 802.11b 2nd side lobe requirement and the FCC restricted band limit.

Minor violations of the –50dBr level will not impact the maximum allowable Tx power but will reduce the 2dB safety margin shown in the diagram. If it is required that the safety margin be increased, the Tx power can be reduced by a corresponding amount.

Hand held devices normally exhibit antenna gains of less than 0dBi, especially when non-optimal placement and antenna feed losses are taken into account. A typical antenna in a hand held device might have a peak gain of –5dBi and thus this case is illustrated in **Figure 7** by the solid orange line. In this more practical case it can be seen that the margin between the WLAN 2nd side lobe and the FCC limit is now approximately 7dB. It thus can be concluded that for the typical application, minor violations of the 802.11b –50dBr spectral mask requirement will have no impact on the ability to achieve FCC certification.

Channels that are not near the edge of the band are not affected, in terms of FCC requirements, by violations of the –50dBr 2nd side lobe requirement because the relevant limit is a total Tx power of 26dBm, and few systems achieve power levels this high.

While Philips Semiconductors strongly supports standardization and strives to fully comply with the recommendations, certain compromises are often permissible to produce cost-effective, practical systems that in the end satisfy market requirements.

Perhaps most importantly of all, is to understand clearly if such compromises will adversely impact the end user experience. In the case of minor spectral mask failures at the –50dB level, there will be no serious impact at all.

4.2 Increasing Margin for FCC Compliance

Since the BGW200 is only marginal to the FCC restricted band limits at the lower data rates, and at the band edges, a 2dB Tx output power back-off feature on channels 1 and 11 can be implemented to obtain an additional 2dB of margin at the cost of Tx output power on these channels. This feature is implemented as part of the Tx Calibration feature discussed later in Section 10 of this note.

5. Software Architecture and Integration

This section is intended to provide a brief overview of the software architecture of the Host (Master) and Target [Slave] communication driver for the BGW200 as depicted in **Figure 8** below. This architecture is common to all standard platforms. Please refer to the BGW200 Software Implementation Guide **[7]** for more detailed information.

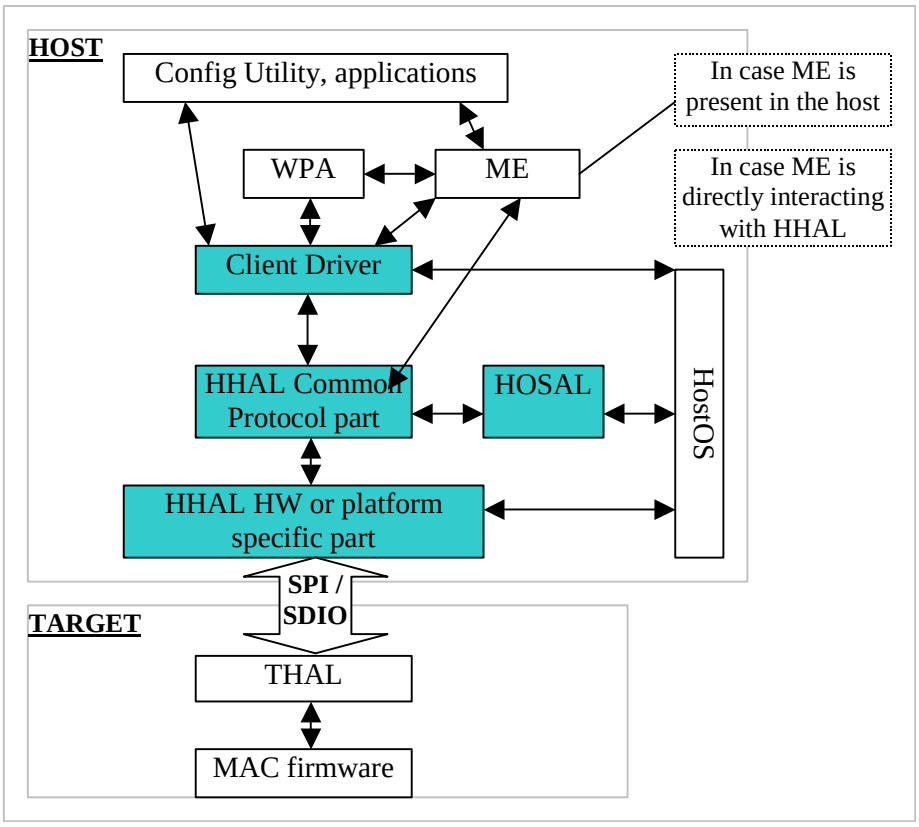

Figure 8 - Software architecture and major components.

A brief explanation of each of the highlighted modules above is provided below.

5.1 Client Driver

The Client Driver provides connectivity between the OS and applications running on the host, and the Host Hardware Abstraction Layer (HHAL). This driver uses the HHAL API's. This layer is dependent on the Host OS.

5.2 HHAL layer

The HHAL layer serves as the host side interface abstraction for the SPI/SDIO interface. This has two parts, the **HHAL_Common** part that is common across all platforms and the **HHAL_Platform** part that is different for different platforms. The protocol part deals with the packet transfer to Target Hardware Abstraction Layer (THAL) that obeys a handshaking protocol. The **HHAL_Platform** part provides low level read, write, and data transfer routines using the OS/platform provided resources [e.g., DMA]

5.3 HOSAL

The Host Operating System Abstraction Layer (HOSAL) is the operating system abstraction on the host side that is provided to make the **HHAL_Common** part independent of the host OS. Currently this layer provides support for the following two operating systems…

- Linux
- WinCE.net/Pocket PC

This module contains API's supplied mainly to HHAL for abstracting it from the underlying OS. The API's include the following.

1) OS and related structure initialization
2) Memory management
3) Timer
4) Que
5) Interrupt
6) Thread
7) Event
8) Lock

5.4 Boot Loader

The Boot Loader is the component that manages the loading of the MAC Image into Internal SRAM for execution. There are four boot load options and the method used is determined by the MODE[0] and MODE[1] settings as shown previously in **Table 4**. If the boot loader is booting from target EEPROM (SPI) then the host processor is not involved; however, the host processor is involved for either of the boot from host options.

5.4.1 SPI Boot from Host

This section explains how the boot loader communicates with the host over the SPI interface to first download the config parser image, and then how the config parser communicates with the host to download the MAC image. The downloads from the host are achieved using the following procedure…

1) The boot loader code enables the DMA interrupts and then programs the DMA addresses to download the config parser image (address 0x26040 to 0x28000). It then writes 0x24 into *S2M Mailbox register2* to indicate to the host that the boot loader is ready to receive the config parser image.
2) The host, which already should have been booted, then polls *S2M_MB2* for the value 0x24.
3) As soon as the host reads the value 0x24 in the *S2M_MB2* it will then DMA the config parser image.
4) The host informs the Target that the DMA is complete by writing 0xA5 into register M2S_SR2.
5) The Target responds by writing 0x42 into register S2M_MB2 and then starts executing the Config Parser.
6) The Config Parser notifies the Host that it is ready to receive a command by writing 0x26 into register S2M_MB2.
7) The Host sends the address command by writing 0xFE into register M2S_SR3
8) The Host writes the start address of an internal memory region to be loaded into registers M2S_SR0 thru 2. The lower 8 bits of the start address must always be 0x0. Bits 15:8 of the start address are written to M2S_SR0, bits 23:16 to M2S_SR1, and bits 31:24 to M2S_SR2 (always right-aligned into bits 7:0 of the respective register)

9) The Host also writes the number of 32-Kbyte data blocks that are to be downloaded for the given memory region, into register M2S_SR3

10) The Target informs the Host that it has programmed the DMA address register and is ready for the actual DMA transfer by writing 0x27 into register S2M_MB2

11) Now the Host performs the DMA transfer via the DMA command sequence.

12) When the Host has finished the DMA transfer of a data block, it writes the number of completed transfers to register M2S_SR2

13) The Target responds with its own internal transfer count, written to S2M_SR3 (should always be the same value as written by the Host)

14) If more data blocks for the given memory region need to be downloaded, sequence 11) through 13) continue until all data blocks of the given memory region have been downloaded.

15) If all memory regions required for the Target to operate the MAC program have been successfully downloaded, the Host writes 0xFF into register M2S_SR3. In response, the Target terminates the Config Parser and jumps to the start of the MAC program and executes the program.

5.4.2 SPI Boot from EEPROM.

This section explains how boot loader downloads the config parser image from EEPROM via the SPI interface, and how the config parser subsequently manages the download of the MAC image from the same EEPROM. Burn the config parser and MAC images in serial flash/serial EEPROM as shown in **Figure 9** below.

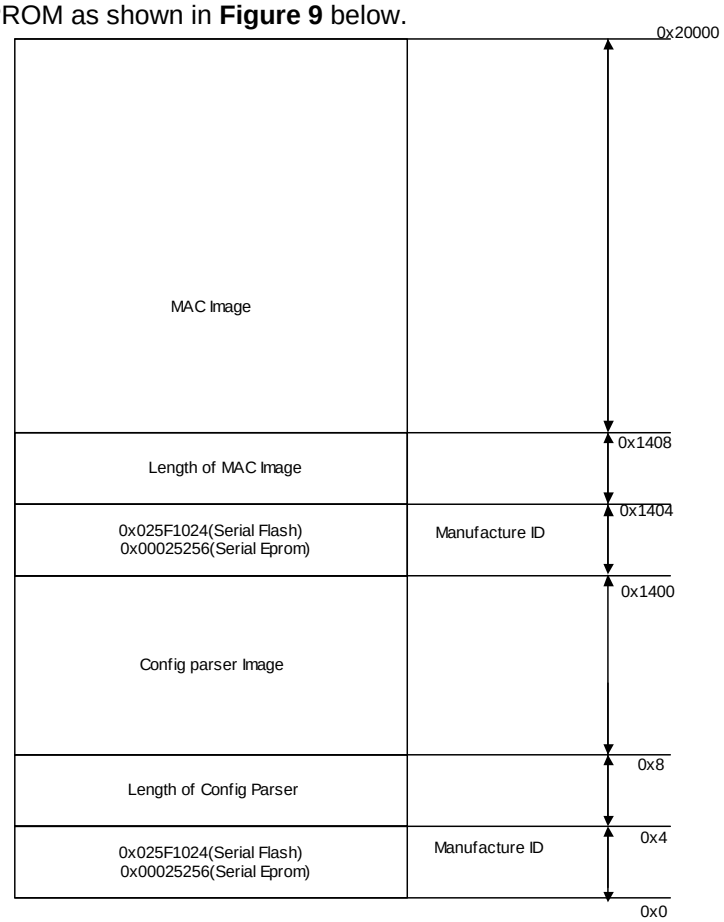

Figure 9 – EEPROM content for SPI host download applications.

1) The boot loader first reads the manufacture's ID (4 bytes) at offset 0x0 to identify whether a Serial EEPROM or Serial Flash device is being used.
2) The boot loader then reads the length of the config parser image at offset 0x4, the length of the image at offset 0x8, and then proceeds to download the image.
3) After completely downloading the config parser image, an SRAM4-ROM swap is executed.
4) The config parser then reads the length of the MAC image at offset 0x1404 and starts to download the MAC image at offset 0x1408, copying it into SRAM4 starting at address 0x0.
5) The MAC image then starts executing from address 0x0.

5.4.3 SDIO Boot From Host.

This section explains how the boot loader communicates with the host to download the config parser image via the SDIO interface, and how the config parser communicates with the host to download the MAC image. The downloads from the host are achieved using the following procedure

1) The boot loader waits for the card ready bit to be set. As soon as the SDIO card is inserted into the WinCE device the card ready bit is set and the boot loader proceeds to program the CIS (Card Information Structure) and to set the function IO bit on the program register.
2) The boot loader then enables the DMA interrupts and programs the DMA address to download the config parser image to, namely address 0x26040 to 0x28000. It writes 0x24 into *S2M Mail box register2* to indicate to the host that it is ready to receive the config parser image.
3) The host should boot up first and begin polling *S2M Mailbox register2* looking for value 0x24.
4) As soon as the value 0x24 is read from *S2M Mailbox register2* it DMAs the config parser image.
5) After completely downloading the config parser image, the boot loader receives an interrupt and jumps to address 0x26040 to start executing the config parser image.
6) The config parser polls the *S2M Scratch pad register3* until a value 0x1 is read from the host indicating the end of this operation.
7) The config parser then programs the DMA to address 0x38000 to down load the first 32 bytes of the MAC image from the host.
8) As soon as it programs the DMA address, it writes 0x26 into the *S2M Mailbox register2* to inform the host that it is ready to down load the first 32 kByte block of the MAC image.
9) The Host driver calculates the number of iterations required to download MAC image in 32 kByte blocks and writes this value into *S2M Scratch pad register3*.
10) As soon as Host driver reads value 0x26 in *S2M Mailbox register2* it DMA's the first 32k of MAC image.
11) When the DMA transfer is complete, the config parser receives an interrupt to reprogram the DMA address to 0x8000 (SRAM1). This process continues until the entire MAC image is downloaded.
12) Upon completion of the download of the MAC image, the config parser performs an SRAM4-ROM swap by setting the 7^{th} bit in the *SCU_CFG register* and starts executing the MAC image from address 0x0.

5.4.4 SDIO Boot From EEPROM

This section explains how the boot loader downloads the config parser image from EEPROM, and how the config parser then manages the download of the MAC image. The downloads from EEPROM are achieved using the SPI interface however the host interface is SDIO. The following procedure is used…

1) Burn the CIS (Card information structure) config parser image and the MAC image in serial EEPROM or Flash device as shown in **Figure 10** below.

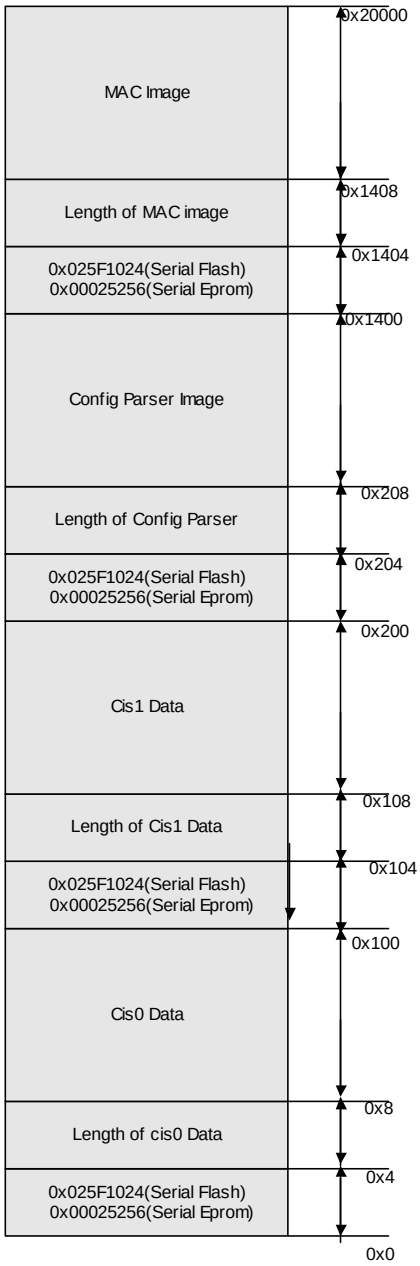

Figure 10 - EEPROM contents for SDIO NIC card applications.

2) Note that initially the ARM clock runs at 1MHz and the boot loader waits for the card ready bit to be set. As soon as the SDIO card is inserted into the WinCE device the card ready bit is set, the boot loader proceeds to program the CIS (Card Information Structure) and to set the function IO bit on the program register.

3) It then reads the config parser image at offset 0x200 and proceeds to download the image.

4) Upon completion of the config parser image download, an SRAM4-ROM swap is executed.

5) The config parser then reads the length of the MAC image at offset 0x1404 and starts to download the MAC image at offset 0x1408, copying it into SRAM4 starting at address 0x0.

6) The MAC image then starts executing from address 0x0.

5.5 Porting Guidelines

Porting from the Philips supplied reference software to another hardware or software system IS NOT trivial. As Philips does not have the available resources to support these activities directly, Philips has partnered and is supporting a number of Independent Design Houses (IDHs) around the world that can provide software design services if needed. It is left up to the end customer to work out the contract details with the IDH themselves…it is not necessary to involve Philips.

The following is a very brief overview of the porting effort and is not to be construed to mean or imply that porting effort is trivial or easy.

5.5.1 Driver

The driver follows the initialization sequence shown in **Figures 11** and **12**, thus there are wait states in the driver that the developers must take into account when porting.

Only one MLME request should be sent to the target at any given time as driver must wait for the MLME confirm to be returned. This approach is used because multiple MLME pending requests could cause conflict in the configuration state. In addition, there is no timeout mechanism implemented in the HHAL layer for MLME requests.

5.5.2 HOSAL

The HOSAL should be designed so as not to change the HHAL. The HOSAL needs to be designed and tested with the HHAL provided so that testing scenarios not exercised by the HHAL can be eliminated.

5.5.3 HHAL Platform Layer

The HHAL Platform Layer needs to be designed and tested for the HHAL Common layer. Similar precautions must be taken for HHAL Interrupt Service Requests (ISRs)/callbacks registered by the HHAL Common layer to the HHAL Platform layer.

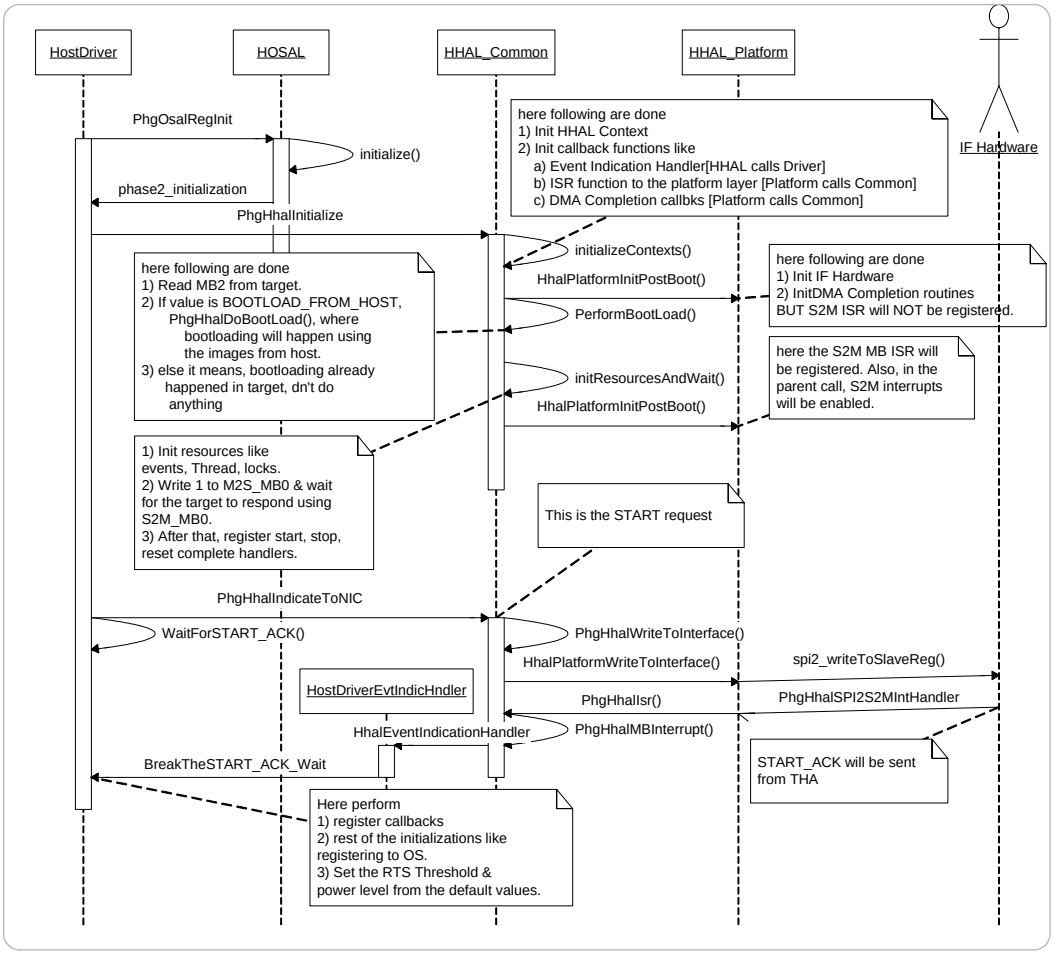

Figure 11 – Initialization flow diagram.

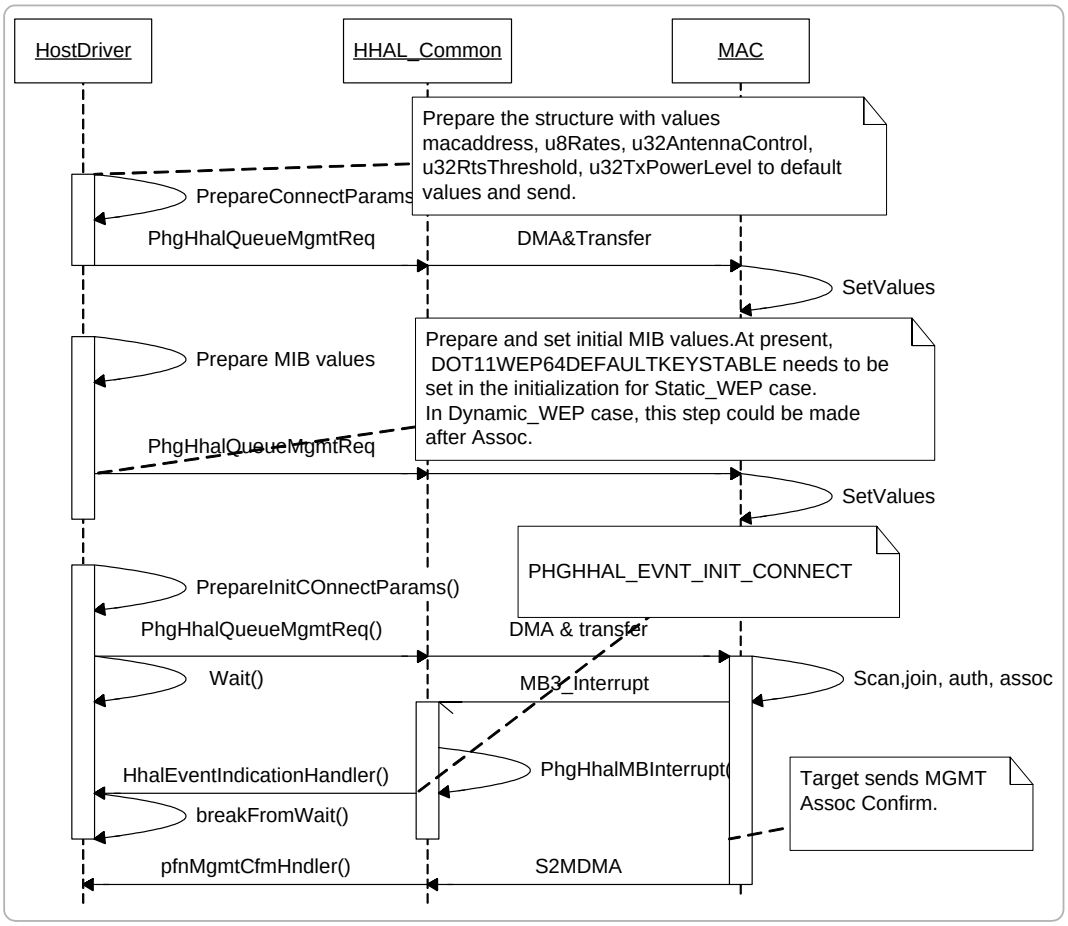

Figure 12 – Init connect flow diagram.

6. Nova Board Typical Performance

This section summarizes the typical performance of the BGW200 on the Nova evaluation and development board based upon measurements taken on three different boards across voltage, frequency and supported data rates.

6.1 Receiver Performance

The following tables summarize the typical Rx performance averaged over three Nova evaluation boards at room temperature with no external Tx filter.

6.1.1 ANT_Main Results

Table 6 - Nova board minimum Rx sensitivity on ANT_Main.

1Mbs Data Rate

		2.7V	2.85V	3.0V
Ch	Preamble	Sens (dBm)	Sens (dBm)	Sens (dBm)
1	Long	-92	-93	-94
6	Long	-91	-93	-92
11	Long	-90	-93	-91
14	Long	-89	-91	-90

2Mbs Data Rate

		2.7V	2.85V	3.0V
Ch	Preamble	Sens (dBm)	Sens (dBm)	Sens (dBm)
1	Long	-88	-91	-89
6	Long	-88	-90	-88
11	Long	-88	-89	-88
14	Long	-87	-89	-87

5.5Mbs Data Rate

		2.7V	2.85V	3.0V
Ch	Preamble	Sens (dBm)	Sens (dBm)	Sens (dBm)
1	Long	-84	-85	-85
6	Long	-84	-85	-83
11	Long	-83	-84	-82
14	Long	-83	-83	-82

11Mbs Data Rate

		2.7V	2.85V	3.0V
Ch	Preamble	Sens (dBm)	Sens (dBm)	Sens (dBm)
1	Long	-84	-85	-84
6	Long	-84	-85	-83
11	Long	-83	-84	-82
14	Long	-83	-83	-82

6.1.2 ANT_AUX Results

Table 7 - Nova board minimum Rx sensitivity on ANT_AUX.

1Mbs Data Rate

		2.7V	2.85V	3.0V
Ch	Preamble	Sens (dBm)	Sens (dBm)	Sens (dBm)
1	Long	-92	-92	-94
6	Long	-91	-92	-92
11	Long	-90	-91	-91
14	Long	-90	-90	-90

2Mbs Data Rate

		2.7V	2.85V	3.0V
Ch	Preamble	Sens (dBm)	Sens (dBm)	Sens (dBm)
1	Long	-89	-89	-89
6	Long	-88	-89	-88
11	Long	-88	-88	-88
14	Long	-89	-87	-87

5.5Mbs Data Rate

		2.7V	2.85V	3.0V
Ch	Preamble	Sens (dBm)	Sens (dBm)	Sens (dBm)
1	Long	-84	-84	-85
6	Long	-84	-84	-83
11	Long	-84	-83	-82
14	Long	-83	-83	-82

11Mbs Data Rate

		2.7V	2.85V	3.0V
Ch	Preamble	Sens (dBm)	Sens (dBm)	Sens (dBm)
1	Long	-85	-84	-84
6	Long	-84	-84	-83
11	Long	-84	-83	-82
14	Long	-83	-83	-82

6.2 Transmitter Performance

The following tables summarize the typical Tx performance averaged over three Nova evaluation boards at room temperature with no external Tx filter.

Table 8 - Nova board Tx performance on Channels 1 and 6.

CH 1 (2412 MHz)						CH 6 (2437Mhz)				
2.7V						2.7V				
bit rate	**1**	**2**	**5.5**	**11**		**bit rate**	**1**	**2**	**5.5**	**11**
Pout (Gain C)	16.7	16.7	16.8	16.8		Pout (Gain C)	16.3	16.4	16.5	16.5
SM LSB1	33.0	33.3	33.9	34.3		SM LSB1	33.2	33.4	34.4	34.5
SM LSB2	33.2	33.6	32.8	33.8		SM LSB2	34.1	35.0	33.7	34.7
SM USB1	55.6	55.8	61.6	58.8		SM USB1	55.7	55.7	61.9	58.6
SM USB2	49.9	50.5	58.2	54.3		SM USB2	50.9	51.4	58.1	55.1
EVM (IEEE pk)	15.0	27.7	17.7	21.7		EVM (IEEE pk)	15.0	22.7	19.7	20.3
Carrier Supr[1] (dB)	na	22.7	na	na		Carrier Supr[1] (dB)	na	22.8	na	na
2nd Harm.[2] (dBm)	-31.3	-34.0	-37.9	-43.4		2nd Harm.[2] (dBm)	-31.8	-34.4	-38.4	-43.7
3rd Harm.[2] (dBm)	-43.1	-43.8	-47.3	-48.5		3rd Harm.[2] (dBm)	-45.3	-44.1	-47.3	-48.6
2.85V						2.85V				
bit rate	**1**	**2**	**5.5**	**11**		**bit rate**	**1**	**2**	**5.5**	**11**
Pout (Gain C)	16.8	16.8	16.9	16.8		Pout (Gain C)	16.5	16.4	16.4	16.44
SM LSB1	33.3	33.5	34.2	34.3		SM LSB1	34.3	35.2	35.3	35.2
SM LSB2	33.9	34.3	33.3	34.4		SM LSB2	34.6	35.0	34.3	35.4
SM USB1	54.6	54.8	61.5	58.2		SM USB1	55.0	54.5	61.1	57.9
SM USB2	50.4	51.4	58.1	54.8		SM USB2	49.4	49.6	57.2	55.5
EVM (IEEE pk)	13.3	31.3	18.7	21.3		EVM (IEEE pk)	12.7	24.3	15.0	20.3
Carrier Supr[1] (dB)	na	23.6	na	na		Carrier Supr[1] (dB)	na	23.2	na	na
2nd Harm.[2] (dBm)	-33.0	-31.5	-34.6	-32.0		2nd Harm.[2] (dBm)	-31.2	-31.4	-34.1	-31.6
3rd Harm.[2] (dBm)	-38.5	-38.9	-40.6	-38.0		3rd Harm.[2] (dBm)	-39.2	-39.4	-40.6	-38.9
3.0V						3.0V				
bit rate	**1**	**2**	**5.5**	**11**		**bit rate**	**1**	**2**	**5.5**	**11**
Pout (Gain C)	17.2	17.1	17.3	17.1		Pout (Gain C)	16.8	16.7	16.8	16.7
SM LSB1	33.3	33.3	33.7	34.3		SM LSB1	34.8	35.9	35.3	35.8
SM LSB2	33.9	34.9	33.3	34.5		SM LSB2	34.6	34.7	34.4	35.2
SM USB1	55.9	53.1	61.2	56.4		SM USB1	53.5	53.4	61.3	56.8
SM USB2	50.1	50.9	58.0	54.2		SM USB2	49.0	49.4	57.5	52.9
EVM (IEEE pk)	19.0	31.0	20.7	28.3		EVM (IEEE pk)	16.0	28.7	23.7	23.3
Carrier Supr[1] (dB)	na	23.7	na	na		Carrier Supr[1] (dB)	na	23.5	na	na
2nd Harm.[2] (dBm)	-31.8	-33.1	-35.0	-32.0		2nd Harm.[2] (dBm)	-31.5	-31.7	-34.6	-32.0
3rd Harm.[2] (dBm)	-40.2	-41.3	-41.1	-40.1		3rd Harm.[2] (dBm)	-41.0	-41.3	-42.4	-40.7

Notes: [1]Measurement performed at 2Mbs only as the carrier leakage is most prominent at this data rate.

[2]Measurement made without an external Tx filter. An external Tx filter is required to improve these figures by 15 to 20dB in order to pass FCC requirements with comfortable margin.

Table 9 - Nova board Tx performance, Channels 11 and 14.

CH 11 (2462 MHz)						CH 14 (2484 MHz)				
2.7V						2.7V				
bit rate	**1**	**2**	**5.5**	**11**		**bit rate**	**1**	**2**	**5.5**	**11**
Pout (Gain C)	16.1	16	16.1	16.1		Pout (Gain C)	15.9	15.8	15.8	15.89
SM LSB1	33.3	34.4	34.9	35.4		SM LSB1	35.1	35.5	35.6	36.1
SM LSB2	33.9	35.3	34.5	35.6		SM LSB2	35.2	35.6	34.8	35.8
SM USB1	54.6	55.8	63.2	59.0		SM USB1	56.1	57.0	63.4	59.5
SM USB2	50.4	50.9	58.5	54.7		SM USB2	51.0	51.0	58.8	54.8
EVM (IEEE pk)	13.3	15.7	15.3	18.0		EVM (IEEE pk)	13.0	17.0	15.0	16.0
Carrier Supr[1] (dB)	na	23.6	na	na		Carrier Supr[1] (dB)	na	23.3	na	na
2nd Harm.[2] (dBm)	-32.4	-35.2	-39.0	-44.5		2nd Harm.[2] (dBm)	-32.8	-35.5	-39.5	-44.9
3rd Harm.[2] (dBm)	-45.0	-45.5	-48.6	-50.0		3rd Harm.[2] (dBm)	-45.3	-45.8	-48.7	-50.2
2.85V						2.85V				
bit rate	**1**	**2**	**5.5**	**11**		**bit rate**	**1**	**2**	**5.5**	**11**
Pout (Gain C)	16.6	16.5	16.5	16.5		Pout (Gain C)	16.5	15.8	16.5	16.3
SM LSB1	34.7	35.6	35.2	35.8		SM LSB1	35.0	35.2	35.2	35.7
SM LSB2	34.4	34.6	34.5	35.4		SM LSB2	35.2	35.6	34.7	35.9
SM USB1	55.9	55.4	62.3	58.8		SM USB1	55.2	55.5	65.2	58.6
SM USB2	50.0	50.6	57.8	54.2		SM USB2	51.5	51.4	58.9	55.3
EVM (IEEE pk)	15.2	16.0	15.3	18.0		EVM (IEEE pk)	14.7	16.0	15.3	16.0
Carrier Supr[1] (dB)	na	23.3	na	na		Carrier Supr[1] (dB)	na	23.1	na	na
2nd Harm.[2] (dBm)	-31.9	-31.9	-34.8	-32.3		2nd Harm.[2] (dBm)	-33.9	-33.1	-36.2	-33.2
3rd Harm.[2] (dBm)	-31.9	-39.1	-40.4	-38.1		3rd Harm.[2] (dBm)	-33.9	-39.3	-40.1	-38.7
3.0V						3.0V				
bit rate	**1**	**2**	**5.5**	**11**		**bit rate**	**1**	**2**	**5.5**	**11**
Pout (Gain C)	16.9	16.8	16.9	16.9		Pout (Gain C)	16.8	16.7	16.7	16.7
SM LSB1	35.1	35.1	35.4	36.0		SM LSB1	35.0	35.4	35.3	35.7
SM LSB2	34.8	35.3	34.2	35.0		SM LSB2	35.7	35.7	34.6	36.0
SM USB1	53.9	53.9	62.3	57.2		SM USB1	54.0	53.8	62.2	57.1
SM USB2	50.0	50.2	57.5	53.8		SM USB2	51.3	51.9	58.8	54.8
EVM (IEEE pk)	18.7	22.0	19.0	21.2		EVM (IEEE pk)	17.0	18.3	20.7	20.7
Carrier Supr[1] (dB)	na	23.4	na	na		Carrier Supr[1] (dB)	na	23.7	na	na
2nd Harm.[2] (dBm)	-32.1	-32.3	-35.2	-32.4		2nd Harm.[2] (dBm)	-33.3	-33.3	-36.4	-35.2
3rd Harm.[2] (dBm)	-39.8	-41.3	-42.4	-41.0		3rd Harm.[2] (dBm)	-42.2	-41.8	-42.7	-41.9

Notes: [1]Measurement performed at 2Mbs only as the carrier leakage is most prominent at this data rate.

[2]Measurement made without an external Tx filter. An external Tx filter is required to improve these figures by 15 to 20dB in order to pass FCC requirements with comfortable margin.

7. WiFi Certification

The WiFi certification methodology for the BGW200 system was designed to take advantage of the commonality of the BGW200 firmware across all supported platforms. To achieve this end, a complete WiFi 802.11b test set-up was procured to enable internal WiFi interoperability pre-testing prior to going for official WiFi certification at an outside lab, which costs on the order of $8,000.00 per visit.

Due to the hardware limitations of the host processor, the targeted WiFi interoperability performance for the BGW200 system are the 802.11b requirements set forth in the WiFi PDA Interoperability Test Plan, Version 1 **[8]** as summarized in the test plan below that is used for the BGW200 software releases.

	Test Description	Reqmnt PDA
	OOB Verification	N/A
	Configurability	N/A
	Initial Ping	N/A
DT1	PureS1 Atheros AP **(B50-C1)**	2.438
DT2		2.297
DT3		0.21
DT2	NAV (NAV/PLCP @ 80% DT2)	<3.972
DT2	PLCP (NAV/PLCP @ 80% DT2)	<3.972
DT1	PureS2 Broadcom AP w/ WPA-PSK **(B100-C2)**	2.425
DT2		2.316
DT3		0.21
DT1	PureS3 Cisco AP w/ WPA-PSK+Frag-500 **(B150-C3-F500)**	1.4
DT2		2.371
DT3		0.273
DT1	PureS4 Intersil AP w/ WPA-TLS **(B200-C5-R256)**	1.94
DT2		1.68
DT3		0.21
DT1	PureS5 Atheros AP w/ WPA-TLS **(B500-C6-R256-F500)**	1.494
DT2		1.89
DT3		**0.322**
DT1	PureS6 Cisco AP w/ WEP64 **(B50-C8-R256)**	2.367
DT2		2.294
DT3		0.21
DT1	PureS7 Broadcom AP w/ WEP64 **(B100-C9)**	2.493
DT2		2.397
DT3		0.21
DT1	PureS8 Globespan/Intersil AP w/ WPA-TLS **(B150-C11-R256)**	2.029
DT2		1.89
DT3		**0.31**
DT1	SI1 - Creator Globespan IBSS w/ Defrag-384-CH3	0.63
DT2		1.05
DT1	SI2 - Creator Atheros IBSS w/ WEP64-CH11-R300	1.19
DT2		2.1
DT1	SI3 - Joiner w/ WEP64-CH4 Intel-R256	1.968
DT2	IBSS Multicast RX	2.213
	IBSS Multicast TX	0.038
		0.038
DT1	SI4 - Joiner Atheros-CH5	1.317
DT2	Boradcom IBSS w/ Defrag-400-R300	2.468
DT3	Boradcom IBSS w/ Defrag-400-R300	0.037
DT4		0.038
	Multicast 1 - Boradcom AP w/ WEP64	N/A
	Multicast 2 - Cisco AP w/ WPA-PSK	N/A
	Same Mode Roaming with WPA-TLS	N/A
	Same Mode Roaming using WPA-PSK	N/A

Figure 13 - WiFi Alliance 802.11b Interoperability requirements for PDAs.

WiFi Certification of the WinCE 4.2/Mainstone2/SPI platform was achieved on September 22, 2004 at an official WiFi certification lab and the official test report is provided in **Appendix A**.

For the WinCE OSs it was determined that the DT3 throughputs that can be achieved were slightly less than the WiFi Alliance requirements established for PDAs and smart phones. This finding was consistent with results obtained by other prominent manufacturers of similar equipment who had already submitted and obtained WiFi Alliance approval for reduced DT3 throughput performance due to limitations in the computing power in these type of products. This took the form of an Application Specific Device (ASD) waiver document submitted to, and approved in advance by the WiFi Alliance prior to the official testing date at the lab. Thus, based upon prior industry precedence, an ASD waiver template is provided in **Appendix B** for products seeking WiFi certification with the BGW200 system.

For the other Linux based standard platforms, there are no plans to take these through official WiFi certification testing, but rather to test them on the internal Philips WiFi Interoperability set-up to gain confidence that these releases will pass when the time comes in the end application.

8. Module and System Evaluation

Special test firmware is available that allows the designer to quickly evaluate the IEEE 802.11b PHY performance of the BGW200 on the Nova board. A set of test macros are made available at the API (Application Program Interface) that allow the BGW200 to be put into a number of test modes for RF performance evaluation with suitable RF test equipment. Please refer to the System Test Environment Specification **[9]** for more detail.

Through this API the BGW200 can be put into transmit continuous or bursted and receive continuous modes, on any channel, for any supported data rate, and antenna port. In addition, the API allows the user to read and write to registers in the baseband and transceiver sections of the BGW200 should additional, application specific configuration data be required.

For manual evaluation, the PHY GUI test tool, running on a Windows PC, provides a quick and easy way to evaluate the Nova board in the lab. Please refer to PHY GUI Test Software User Manual **[10]** for detailed information about test options and associated instructions on how to use the tool.

If automatic test and evaluation tools are available, then the API can be called directly using test script running on a suitable PC. Please refer to the Washington System Test Environment Set-up Guide **[11]** for detailed instruction for setting up the test and evaluation PC.

8.1 Test Set-up

The setup consists of a test PC connected to the BGW200 Nova eval board via UART as depicted in **Figure 14**. The UART interface is used for booting as well as for command and control.

The test firmware running on the BGW200 is designed for test purposes and differs from the “normal” firmware that will be running on the final product. The test firmware deploys the so-called ADI interface (Arm DFC interface). A TCP/IP server runs on the tester PC. The serial server is a Java application in order to be platform independent. It may be called from any PC connected to the network. On top of the serial server runs a functional layer and the API that can be accessed by an additional application, e.g. either a test script or GUI referenced above.

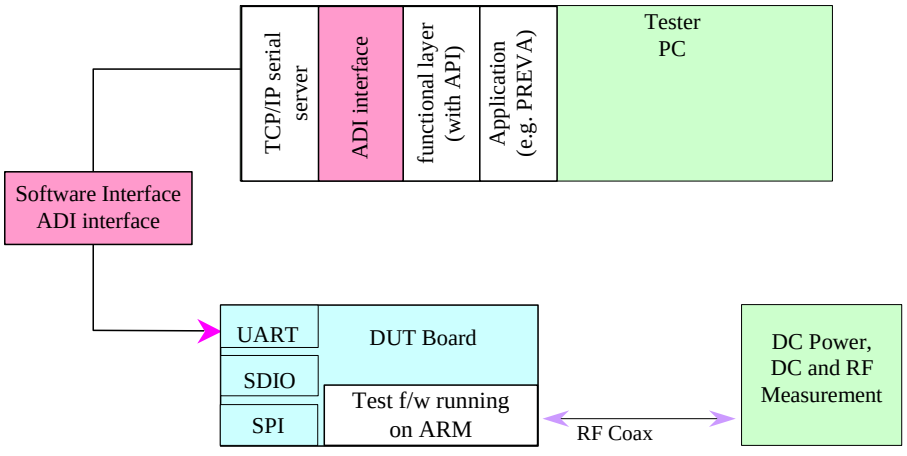

Figure 14 - Module production test set-up.

9. Embedded System Test

After the BGW200 has been integrated into the end product, the SIP module must be able to be tested while embedded in the host system. This might be either a customer designed board or an external host system. In this case, protocol and network functionality are also important.

Since radio performance and protocol compliance need to be tested, the setup will deploy two firmware versions:

1) test firmware for testing radio performance.
2) normal firmware for testing protocol and network functionality.

The customer might use any of the three interfaces (UART, SPI or SPIO) for this purpose, and since the host system is not known, it is left as the responsibility of the designer to develop an application on the host to interface to the BGW200 ADI interface.

The special test firmware introduced in the previous section is the same one used for embedded systems; hence, please refer to the System Test Environment Specification [9] for more details.

9.1 Test Set-up

The test setup consists of a test PC connected to the host system as depicted in **Figure 15**. In this case the host controller lies between the BGW200 and the tester PC, hence, the need for the designer to write the necessary bridge software to make the test API accessible at the host system test port.

Once again the test firmware running on the BGW200 is designed for test purposes and differs from the “normal” firmware that will be running on the final product.

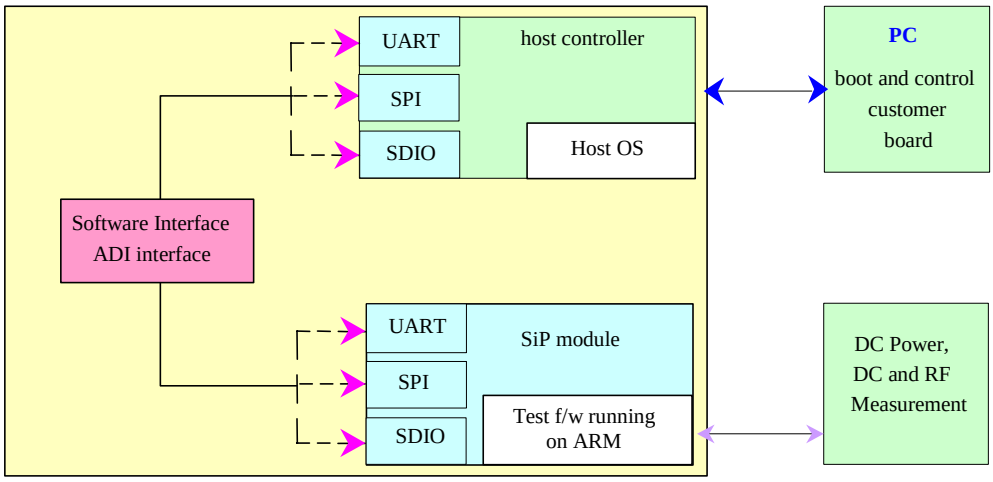

Figure 15 - Test methodology for embedded systems.

10. BGW200 Tx Calibration Option

This section provides an overview of the method of adjusting the transmitter output power to reduce Tx output power variation during normal operation of the system. The need to make these adjustments depends on the customer requirement, e.g. Tx output power accuracy, operating power supply and temperature ranges. Refer to the BGW200 System Configuration App Note **[12]** for more detailed information.

The method implemented is divided into two parts:

1) a factory calibration step to compensate for unit- to-unit variation.
2) a correction process that operates in the background during normal operation to automatically correct for changes in temperature, frequency and data rate.

The Tx output power control is achieved via a 4 bit (0 to 15 dB nominal) Tx gain and voltage control register in the SA2405A RF transceiver IC. This is the only gain control available for both calibration and subsequent correction. Each Tx gain step is nominally 1dB but some gain compression occurs limiting the effective Tx output power control range to approximately 12dB and accuracy to about +/-1dB.

10.1 Factory Calibration

During factory calibration a reference measurement is made to define a reference operating point for the system. The reference point can be defined in up to 4 dimensions by the following parameters:

- Supply voltage
- Temperature
- Frequency
- Tx gain setting

Depending upon the system requirements, all or some of these parameters can be used. At the factory calibration step these variables are defined and saved in host NVM (Non Volatile Memory) to define the reference point from which the correction algorithm will derive adjustments to be made to the Tx Gain setting of the radio in order to maintain the desired Tx output power level..

10.2 Correction Algorithm

Each reference parameter results in a gain offset from the reference point. An offset value is derived for each parameter by using look-up table data supplied by Philips Semiconductors that fully characterizes the typical performance of the BGW200 across the 4 dimensions listed above. This table is stored in host NVM (non volatile memory). A cumulative offset value is then continually derived and applied by programming a new Tx gain value into the radio whenever necessary.

Voltage correction simply applies an offset dependent upon the deviation of supply voltage from the reference value. It is assumed that supply voltage effects are independent of both temperature and frequency effects. This assumption significantly reduces the amount of data storage and collection that is necessary to implement the algorithm.

Temperature and frequency effects are combined into a single offset value.

10.3 Host Requirements

In order to effectively implement the Tx correction option in a product the host system must provide an accurate temperature sensor reading to the BGW200.

In addition, operating supply voltage must either be supplied as a fixed value or provided as an input to the BGW200.

11. Power Management

The power management feature implemented in the BGW200 and associated system drivers is a key feature and market differentiator for the BGW200. The effective implementation of the power management modes is in accordance with the IEEE 802.11b standard . The BGW200 WLAN STA (station) may be in one of the following power states:

- **Awake:** STA is fully powered.
  - This is shown as CAM (continuously active mode) mode in the Philips 802.11b NDIS driver configuration utility.
- **Doze:** STA is in power save mode and consumes very little power.
  - This is shown as Fast PSP (power save protocol) mode in the Philips 802.11b NDIS driver configuration utility.
- **Deep Sleep:** STA is completely powered off and incapable of associating with any BSS.

The manner in which a STA transitions between power states is determined by the STA's Power Management mode. These modes are summarized in the table below and in greater detail in the Power Management Utility App Note **[13]**.

The user has the choice of enabling or disabling Power Management. When enabled, the STA informs the AP (access point) that Power Management mode has been selected. Once the STA receives confirmation from the AP, it can enter power save mode but still maintain synchronization with the network by periodically waking up to monitor beacon traffic from the AP.

To change Power Management modes, a STA shall inform the AP through a successful frame exchange initiated by the STA. The Power Management bit in the Frame Control field of the frame sent by the STA indicates the Power Management mode the STA shall adopt.

To change from Doze to Awake state, the STA shall perform a clear channel assessment (CCA) to gain access to medium so that it can transmit its intentions to the AP. It will not transmit this message until a frame sequence is detected by which it can correctly set its NAV, or until a period of time equal to the ProbeDelay has transpired.

Active mode or AM	The STA may receive frames at any time. In Active mode, a STA shall be in the Awake state. A STA on the polling list of a PCF shall be in Active mode for the duration of the CFP.
Power Save or PS	STA listens to selected beacons (based upon the ListenInterval parameter of the MLME-Associate.request primitive) and sends PS-Poll frames to the AP if the TIM element in the most recent beacon indicates a directed MSDU buffered for that STA. The AP shall transmit buffered directed MSDUs to a PS STA only in response to a PS-Poll from that STA, or during the CFP in the case of a CF-Pollable PS STA. In PS mode, a STA shall be in the Doze state and shall enter the Awake state to receive selected beacons, to receive broadcast and multicast transmissions following certain received beacons, to transmit, and to await responses to transmitted PS-Poll frames or (for CF-Pollable STAs) to receive contention-free transmissions of buffered MSDUs.
Deep Sleep	The STA, while in this mode, is incapable to receive frames at any time from any BSS.

The BGW200 NDIS drivers come with four power save modes (accessible with the Philips 802.11b NDIS configuration utility) to provide the most flexibility in Power Management resolution.

- **CAM:** Power Management disabled, i.e. fully powered mode.

- **Max PSP:** Power Management fully enabled with user selectable listen interval for maximum power savings.
- **Fast PSP:** Power Management enabled but for a fixed listen interval for good power savings.
- **Deep Sleep:** Power down state that requires the user to manually re-activate prior to resuming normal operation.

12. System Configuration Methodology

The system architecture employed for the BGW200 is designed to allow the designer to customize and optimize the design by simply updating a parameter set that is stored in host Non Volatile Memory (NVM) in the form of an nvram.txt file. This section provides an overview of the method employed for the BGW200. Refer to the nvram Customization Tool User Manual **[14]** for more detailed information.

These are some of features that will be user configurable via storing appropriate data into NVM with some end user selectable features made accessible via the driver.

12.1 End User Selectable Features

The following is a list of the typical features that will be made end user selectable via the driver independent of the nvram.txt file.

- Power save mode select/ON/OFF
- Radio ON/OFF
- Channel selection
- SSID
- DHCP mode select/ON/OFF
- Mode select Infrastructure/Adhoc/Auto
- Beacon/Listen interval
- WEP mode select/ON/OFF
- WEP key
- WPA mode select/ON/OFF
- WPA key
- QoS ON/OFF
- Normal or test f/w select

12.2 Manufacturer Selectable Features

The following is a list of the design features and parameters the system designer will be able to control during manufacturing process via nvram.txt or registry settings.

- MAC address
- Regulatory domain

12.3 Designer Selectable Features

The following is a list of the design features and parameters the system designer will be able to control via host nvram.txt. These parameters will be read and implemented by the BGW200 f/w upon power ON and system reset.

- Version no.
- Link Adaptation ON/OFF
- Tx output power set
- Sleep clock source select
- Antenna diversity ON/OFF
- Bluetooth coexistence ON/OFF
- GPIO configuration
- Hardware specific parameters, e.g. Rx front end loss, etc.

12.4 Host Requirements

The host requirements for implementing the system configuration methodology are less than 1k bytes of available NVM.

13. Antenna Diversity

The BGW200 supports receive antenna diversity but not transmit antenna diversity. For transmission, only ANT_MAIN can be used, hence the following note.

Note: use ANT_MAIN for applications requiring only a single antenna.

As with any spatial diversity implementation, to be effective the two antennas must be separated by at least a quarter wavelength. For some highly integrated products this may not be possible or desirable so the Antenna Diversity feature can be enabled or disabled by storing the appropriate data in host NVM as described in the previous Section.

There are two methods for determining which antenna is best to use for reception: Energy detect or Barker detect.

13.1 Energy Detection

The Energy detect approach uses the RSSI (Receive Signal Strength Indicator) measurement capabilities of the SA2405 radio transceiver. An RSSI measurement is made for each antenna at the beginning of each receive burst and the antenna with the best RSSI is selected for packet reception. The Energy detect method is fast and simple and in most cases fairly effective; however, because the RSSI measurement will include both desired and undesired signals and interferers it may not achieve the desired results in all situations.

13.2 Barker Detection

The Barker detect approach makes the decision further down into the receive chain after the Barker code detection circuit in the SA2443A baseband IC. In so doing the antenna quality measurement and subsequent decision can be based entirely on the desired signal as undesired signals and interferers have effectively been removed at this point. It is thus inherently more accurate. On the down side, the system will consume a little more power as more of the receive chain must be activated as and the system will take longer to make a signal quality assessment as compared to Energy detect.

13.3 Algorithm

Simulation and measured results indicate that the Energy detect method provides a 1 to 2 dB improvement in the case of a long preamble, and no improvement in the case of a short preamble. In addition, no improvement was observed for either long or short preamble for Barker detect. Thus, the BGW200 system supports the Energy detect method of antenna diversity.

When enabled, the Antenna Diversity algorithm will be executed during preamble reception at the beginning of every IEEE 802.11b receive packet, and the best antenna selected for the data reception that immediately follows. The receiver will stay in this configuration for the duration of the packet, or until the packet should be lost due to poor signal quality for example. The algorithm will be executed again upon receipt of the next receive packet.

14. WLAN + BT Co-location

WLAN is becoming a key enabler for the convergence of voice and data applications in mobile appliances such as cellular phones and PDAs where other radio technologies already exist **[15]**. It is thus necessary to ensure that WLAN can operate seamlessly while co-located in such products with other radio technologies and vis versa. Thus, in this and the following section, co-location of the BGW200 in such products is investigated.

Many cellular phones today, especially higher-end smart phones and feature phones, use Bluetooth technology to enable the use of Wireless Bluetooth headsets. Co-location with Bluetooth in these type of products poses challenges to either system as both are operating in the same 2.4GHz frequency band, i.e. co-channel interferers, as shown in the Figure below. Compounding the possibility for interference is the fact the Bluetooth and WLAN radios are located in very close proximity in these products, sometimes sharing the same antenna.

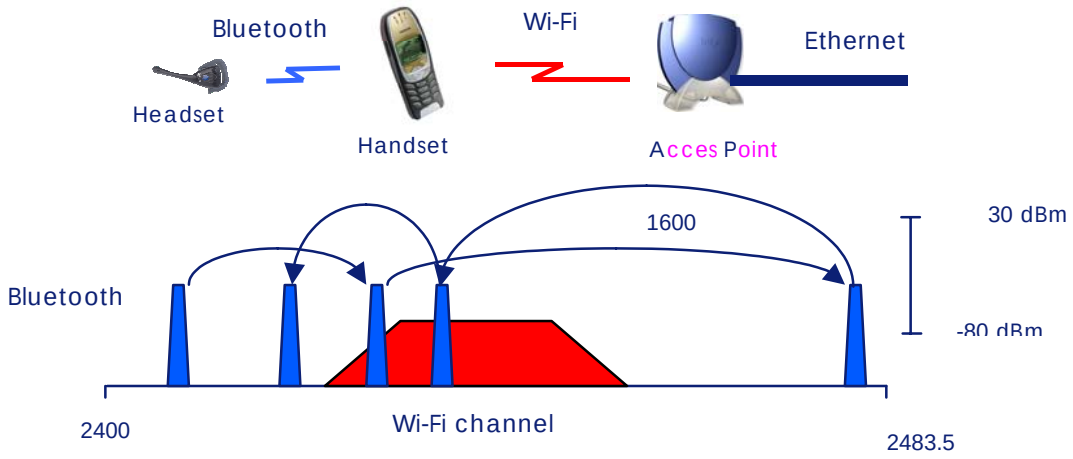

Figure 16 - WLAN / Bluetooth coexistance overview.

Interference between WLAN and Bluetooth can occur as a result of either of the following scenarios:

- Transmit power of one system degrading the receiver of the other system
- Two simultaneous transmitting systems generating unwanted spurs

In order to address these issues it is clear that WLAN and Bluetooth cannot operate as independent, autonomous systems, i.e. the two systems must be linked in such a way where at least one system knows what the other is doing or intends to do. Thus, to enable the co-location of WLAN and Bluetooth in the same device, the integration of the two systems must be done in such a way as to…

- Ensure that WLAN and Bluetooth do not transmit at the same time.
- Allow WLAN or Bluetooth to try to receive while the other is transmitting.
- Allow WLAN and Bluetooth to receive at the same time.

14.1 WLAN + Bluetooth Co-location Methods

The IEEE 802.15 recommended practice describes four possible methods that can be used to avoid simultaneous transmission but does not mandate that any be used. The mechanisms fall into two categories: collaborative and non-collaborative.

14.2 Non-Collaborative Mechanisms

Non-Collaborative Mechanisms imply no communication between WLAN and Bluetooth exists and thus are generally simpler to implement. The following two techniques are presented as ways to adjust Bluetooth operation to minimize interference with 802.11.

1. **Adaptive Packet Selection (APS)** whereby smaller data packets are used in a coexistence scenario so that when collisions do occur, the impact on WLAN performance will be reduced.
2. **Adaptive Frequency Hopping (AFH)** where by the system adjusts the Bluetooth hop sequence to avoid operating in the occupied WLAN channel. AFH was defined to address WLAN and Bluetooth coexistence and thus is not capable of addressing the additional challenges posed by co-location of the two technologies into the same product.

14.3 Collaborative Mechanisms

Collaborative Mechanisms involve some level communication between WLAN and Bluetooth to enable sharing of the medium. They are thus are more complicated to implement then non-collaborative methods. The following three techniques are proposed and involve adjusting both WLAN and Bluetooth operation to minimize interference.

1. **Alternating Wireless Medium Access (AWMA)** allows the sharing of the Wireless medium by allocating WLAN and Bluetooth each a fixed amount of time for access. While this addresses the co-location issues and is relatively simple to implement, it is not very efficient or intelligent as it offers no way to assign Bluetooth voice packets priority in order to avoid having negative impacts on the user experience. WLAN throughput will also be degraded even when there is no Bluetooth traffic present.
2. **Packet Traffic Arbitration (PTA)** defines a system protocol that employs an arbitration algorithm by which WLAN and Bluetooth contend for the medium. While more complicated to implement then AWNA or AFH, it is intelligent and provides a arbitration mechanism by which WLAN and Bluetooth continually contend for the medium while also providing Bluetooth with a way to get priority for voice packets so as not to degrade the user experience. Likewise, WLAN throughput is not affected when there is no Bluetooth traffic.
3. **Deterministic Spectral Excision (DSE)** proposes that an adjustable WLAN notch filter tuned and synchronized to the Bluetooth hop sequence be deployed to notch-out the narrow band Bluetooth interferer. Implementing this however is technologically challenging from both the hardware and the software perspectives.

14.4 BGW200 Solution for Co-location

PTA was chosen as the optimal way to address the WLAN and Bluetooth co-location issues in the mobile solutions from Philips Semiconductors. As Philips is actively developing both WLAN and Bluetooth products, it is in a unique position to provide complete, optimized, plug-and-play solutions consisting of both hardware and software that implements PTA with no intervention required by the product designer or the end user.

The PTA implementation for the BGW200 and BGB203/4 family of products uses a simple four-line interface as shown in the Figure below.

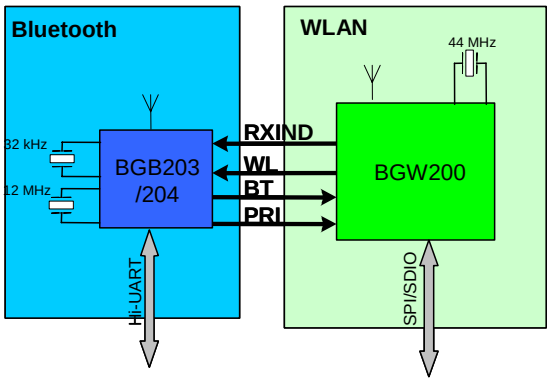

Figure 17 - BGW200 + BGB203/204 co-location functional block diagram.

Two lines are used for medium access arbitration (WL and BT), one line to indicate Bluetooth priority packets (PRI), and one line to indicate WLAN packets (RXIND). Special hardware features were added to the BGW200 to support medium access arbitration. Only software modifications were required for the Bluetooth system in order to enable Bluetooth master and slave support.

The exact GPIO mapping between the BGW200 and the BGB203/204 are as follows:

Table 10 - BGW200 + BGB203/204 Interface.

BGW200 Pin	Interface Line	BGB203/204 Pin
GPIO_0/WL	**WL**	GPIO13
GPIO_1/BT	**BT**	GPIO12
GPIO_2/PRI	**PRI**	GPIO11
GPIO_3/RXIND	**RXIND**	GPIO14

15. WLAN + Cellular Phone Co-location

In this section an overview of WLAN co-location issues in GSM and CDMA mobile phones is presented along with how they can be mitigated with the BGW200. The following effects were analyzed to ascertain the effects of co-location of WLAN in mobile phones:

- Effect of WLAN Tx on GSM/CDMA Rx sensitivity.
- Effect of GSM/CDMA Tx on WLAN Rx sensitivity.
- On board noise coupling issues (power supply, ground path).
- Spurious products (reference oscillators products).
- Cross modulation in the GSM/CDMA PA from the WLAN Tx signal.
- Cross modulation in the WLAN PA with the GSM/CDMA Tx signal.

For the analysis, an assumption was made that the main coupling path is through antennas and that sufficient isolation exists on the PCB between the WLAN and GSM/CDMA radios.

The Figure below is a pictorial representation of the issues, in the frequency domain, resulting from co-locating WLAN in a GSM/CDMA mobile phone..

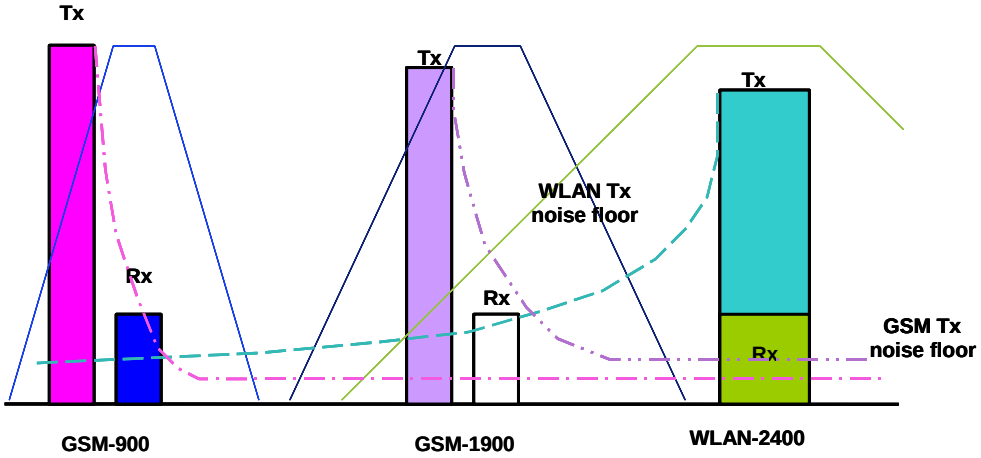

Figure 18 - WLAN and cell phone co-location issues.

15.1 WLAN Tx Impact GSM/CDMA Rx

The following table summarizes the analysis and assumptions made to determine the WLAN transmitter effects on the GSM and CDMA receiver.

Table 11 - WLAN Tx impact on GSM/CDMA Rx

	GSM 900	GSM 1900	CDMA 900	CDMA 1900	
WLAN Tx Power	18.0	18.0	18.0	18.0	dBm
WLAN Tx to GSM/CDMA antenna isolation	-20.0	-20.0	-20.0	-20.0	dB
GSM/CDMA Rx front-end filter attenuation	-40.0	-30.0	-25.0	-25.0	dB
WLAN Tx power at GSM/CDMA Rx LNA input	-42.0	-32.0	-27.0	-27.0	dBm

From the this analysis the following conclusions can be drawn:

- The GSM/CDMA receiver will not desense due to LNA+Mixer gain compression caused by the WLAN transmit signal because most GSM/CDMA receivers have 1dB input compression points >-22dBm and can thus handle a –27dBm WLAN Tx signal without compressing.
- The GSM/CDMA receiver will not desense due to IM2 products generated by the WLAN transmit signal because GSM/CDMA receivers typically have very high input IP2s on the order of +60dBm or higher.
- **Issue:** The GSM/CDMA receiver will however desense due to the WLAN Tx noise floor in the 900 and 1900 MHz bands as the BGW200 Tx noise floor in the CEL/PCS Rx band will be around –135dBm/Hz and assuming 20dB isolation between WLAN and GSM antennas, this translates to ~-155dBm/Hz at the GSM/CDMA receiver input.

Solution: A High pass filter with ~30dB attenuation at 900 and 1900 MHz is needed.

15.2 GSM/CDMA Tx Impact on WLAN Rx

The following table summarizes the analysis and assumptions made to determine the GSM and CDMA transmitter effects on the WLAN receiver.

Table 12 - GSM/CDMA Tx Impact on WLAN Rx

	GSM 900	GSM 1900	CDMA 900	CDMA 1900	
GSM/CDMA Tx Power	33.0	33.0	23.0	23.0	dBm
WLAN Rx to GSM/CDMA antenna isolation	-20.0	-20.0	-20.0	-20.0	dB
WLAN Rx front-end filter attenuation	-40.0	-30.0	-40.0	-30.0	dB
GSM/CDMA Tx power at the WLAN Rx input	-27.0	-20.0	-37.0	-27.0	dBm

From the above analysis the following conclusions can be drawn:

- The WLAN receiver will not desense due to GSM/CDMA Tx noise floor as the GSM/CDMA Tx noise floor in the 2400MHz band will be approximately –160dBm/Hz at the GSM/CDMA antenna with 20dB of additional isolation remaining between the WLAN and GSM antennas.
- **Issue:** The WLAN receiver can only handle input signals up to ~-30dBm without compressing and thus will desense due to LNA+Mixer gain compression caused by the GSM/CDMA Tx signal.

Solution: A High pass filter with ~15dB attenuation at 900 and 1900 MHz is needed.

15.3 WLAN Tx Cross Modulation effects on GSM Tx

The following is an analysis of the cross modulation effects a WLAN transmitter can have on a GSM transmitter.

GSM-900 PA output power: 34 dBm

WLAN Tx output power: 18 dBm
GSM & WLAN antenna isolation: 20 dB
WLAN Tx signal at the GSM antenna = 18 - 20 = -2 dBm
PA LPF attenuation at 2.4 GHz = 40 dB
WLAN Tx signal at the GSM-900 PA Output : -42 dBm

Conclusion: Since the WLAN signal is 76 dB below the GSM-900 PA output, any cross modulation products generated will be insignificant.

15.4 GSM Tx Cross Modulation effects on WLAN Tx

The following is an analysis of the cross modulation effects the GSM transmitter can have on a WLAN transmitter.

-WLAN PA output power: 19 dBm

- GSM Tx output power: 30 dBm
- GSM & WLAN antenna isolation: 20 dB
- GSM Tx signal at the WLAN antenna= 30-20 = 10 dBm
- GSM Tx signal at the WLAN PA Output (10 dBm – 1 dB): 9 dBm

Issue: The GSM transmitter signal will generate spurious products due to cross modulation in the WLAN PA.

Solution: A High pass filter with ~30dB attenuation at 1900 MHz is needed.

15.5 Solving the Co-location Issues

A high pass filter in front of the WLAN transceiver that provides 30dB of attenuation of the 1900MHz band will allow co-location of WLAN and GSM/CDMA radios by eliminating desense caused by noise floor, IP2 and cross modulation. WLAN Rx sensitivity degradation due to the HPF will be ~0.5 to 1dB and the HPF will add ~$0.25 to the overall BOM cost as this filter is not integrated in the BGW200.

16. BGW211 Migration

One of the key features of the BGW200 is the ease of migration to the next generation IEEE 802.11g SiP from Philips, the BGW211. This section will identify the hardware and software items to consider for achieving a drop-in upgrade to the BGW211.

16.1 Hardware Considerations

16.1.1 Crystal Oscillator Circuit

As shown in **Figure 19**, with the addition of two extra SMT components (C3 and C4) on the BGW200 PCB layout the BGW211 XO circuit can also be accommodated on the same board. The XTAL unit in the case of the BGW200 is 44MHz where as for BGW211 it can be either of the following: 13, 19.2, 20, 26, 38.4 or 40 MHz.

Since the BGW211 is designed to operate at reference clock frequencies commonly found in cellular phones, a XTAL unit may not be necessary if the host clock can be shared with the BGW211. In this instance, the host clock can be connected directly to XTAL_I, leaving XTAL_O open.

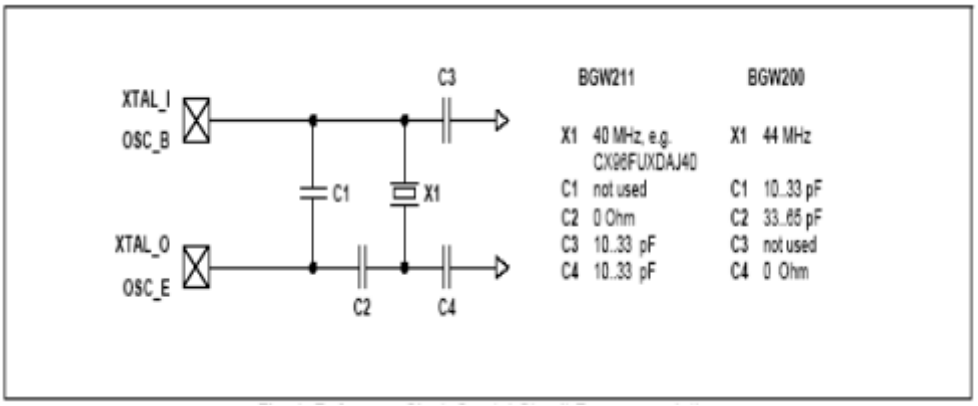

Figure 19 - XTAL schematic for accommodating either BGW200 or BGW211.

16.1.2 Voltage Regulator Circuit

The 1.8V regulated supply to the BGW200 ARM7 core, must be changed to 1.2V core supply required for the BGW211.

16.1.3 WLAN + Bluetooth Co-location

The 3.3V-to-1.8V level shifters required to interface the BGW200 to the BGB203/204 Bluetooth SiPs from Philips Semiconductors, are not required for the BGW211 as Pin 17 VDD_BT has been provided so that the BGW211's Bluetooth interface can be operated off of the same supply as that of the BGB203/204 Bluetooth SiP being used.

16.1.4 Other Pinning Considerations

Table 12 on the following page is a BGW200/BGW211 pin-to-pin cross-reference table for the BGW200 and the BGW211.

Note that test pins are used to support production test of the module and are not meant to be used in the final application; thus, these pins need not be compatible for the BGW200 and BGW211.

Table 13 - BGW200 / BGW211 Pinning Cross-Reference Table.

Pin	BGW200 Pin	Description	BGW211 Pin	Description
Differences Color Code:				
		Minor - not important for ODM/OEM customers		
		Significant - change of external circuitry necessary		
1	GND		AGND	
2	GND		AGND	
3	TEST_RSSI	Test pin; do not connect	NC	
4	GND		AGND	
5	VDD_VCO		VDD_VCO	
6	GND		AGND	
7	GND		BT_CLK_REQ	BT clock request input
8	TEST_LOCK	Test pin; do not connect	OSC32K_O	32 kHz crystal oscillator; output
9	GND		OSC32K_I	32 kHz crystal oscillator; input
10	OSC_B	(see Fig.3)	XTAL_I	(see Fig.3)
11	OSC_E	(see Fig.3)	XTAL_O	(see Fig.3)
12	GND		AGND	
13	REFCLK_OUT		REFCLK_OUT	
14	MODE_2	Connect to GND	MODE_2	
15	VDDRF33		VDD_A	
16	VDD_IO	Common I/O supply	VDD_IO	I/O digital supply voltage
17	NC	Connect to 1.8 V	VDD_BT	Bluetooth digital supply voltage
18	VDD_CORE	1.8 V core supply	VDD_CORE	1.2 V core supply
19	MODE_0		MODE_0	
20	MODE_1		MODE_1	
21	POR_N		POR_N	
22	DBUG_EN	Test pin; do not connect	BT_CLK_OUT	BT clock output
23	GPIO_4	GPIO / CLK32K input	CLK32K_IN	
24	SPI_EXT_INT		SPI_EXT_INT	
25	SPI_CLK		SPI_CLK	
26	SPI_DAT_MISO		SPI_DAT_MISO	
27	SPI_SS_N		SPI_SS_N	
28	SPI_DAT_MOSI		SPI_DAT_MOSI	
29	RESET_N		RESET_N	
30	MODE_3	Connect to GND	MODE_3	
31	MODE_4	Connect to VDD33	MODE_4	
32	GPIO_9		CEL_CLK_REQ	Cellular clock request output
33	GPIO_10	GPIO / SPI slave select	SPI_SS_OUT_N	SPI slave select; input
34	SD_DAT_2		SD_DAT_2	
35	SD_DAT_3		SD_DAT_3	
36	SD_CMD		SD_CMD	
37	SD_CLK		SD_CLK	
38	SD_DAT_0		SD_DAT_0	
39	SD_DAT_1		SD_DAT_1	
40	UART_RX		UART_RX	
41	UART_TX		UART_TX	
42	JTAG_TDO		JTAG_TDO	

Pin	BGW200 Pin	Description	BGW211 Pin	Description
43	JTAG_RTCLK		JTAG_RTCLK	
44	JTAG_TCLK		JTAG_TCLK	
45	JTAG_TMS		JTAG_TMS	
46	JTAG_TDI		JTAG_TDI	
47	JTAG_TRST_N		JTAG_TRST_N	
48	GND		AGND	
49	RXIND	VDD_IO supply domain	RXIND	VDD_BT supply domain
50	PRI	VDD_IO supply domain	PRI	VDD_BT supply domain
51	BT	VDD_IO supply domain	BT	VDD_BT supply domain
52	WL	VDD_IO supply domain	WL	VDD_BT supply domain
53	TEST_TXRX		AUX_DAC_OUT	Auxiliary DAC output
54	GND		AGND	
55	ANT_MAIN		ANT_MAIN	
56	GND		AGND	
57	ANT_AUX		ANT_AUX	
58	GND		AGND	
59	VDD_PA		VDD_PA_0	
60	VDD_DRIVER		VDD_PA_1	
61	GND		AGND	
62	GND		AGND	
63	TEST_SDATA	Test pin; do not connect	SDA	Test pin / I²C interface data line
64	TEST_AGCRESET	Test pin; do not connect	SCL	Test pin / I²C interface clock line
65	GND		AGND	Analog ground
66	AVDD		VDD_RF	
67	GND		AGND	
68	GND		AGND	
69	GND		AGND	
70	GND		AGND	
71	GND		DGND	
72	GND		DGND	
73	GND		AGND	
74	GND		AGND	

16.1.5 Software Considerations

Software changes associated with the upgrade of a design from the BGW200 to the BGW211will be completely transparent to the designer whose effort will be limited to running IEEE 802.11g production test on the BGW211 as opposed to IEEE 802.11b tests for the BGW200.

Changes made to a few key software modules are described below.

16.1.6 HHAL module

The host interfaces to this module will not change moving from 11b to 11g. Internal structures in the control and data paths will have some minimal changes to accommodate the additional data rates for 11g, but these will be transparent to the user software operating above this layer.

16.1.7 Client Driver

Structural changes to this module will be needed to provide support for 11g data rates. The changes, which mainly involve expanding the parameter set for the OIDs, will be completely internal to this module.

16.1.8 MMI (Man Machine Interface)

Small changes in the MMI residing on the host system may be required to accommodate the expanded capabilities and features sets of an IEEE 802.11g system.

17. General Support

Technical design-in and sales support is available worldwide from your local Philips Semiconductors sales offices and design-in partners whom we have engaged with. In most instances this will be most efficient way to receive timely support.

17.1 Ordering Samples

Contact your local Philips Semiconductors sales person to request samples, evaluation kits, software and literature.

17.2 Development Kits

The BGW200 development kit is designed to allow the customer to do their own software development and customization for either an OEM end product or reference design. The hardware piece of the kit is available for $1,500 and contains the following items:

- Nova BGW200 Evaluation board
- Set of antennas
- AC/DC power adaptor
- SPI Interface cable for Mainstone2 (MS2) development platform.

In order to complete the development environment, the customer will need to procure additional hardware and software items such as an Intel MS2 developers platform, Linux or WinCE OSs, etc., at an additional cost of approximately $6,000 and thus must be carefully considered by each customer.

Philips reference software is provided separately under license. The recipient of the software, whether the end customer or an IDH, must have entered into a Software Licensing Agreement with Philips before the software package can be provided

17.3 Software Licensing Agreements

There are two types of Software Licensing Agreements (SLA) and the one that is most applicable depends upon the business model or model(s) of each customer. A brief description of each SLA is provided to aid the customer in identifying the SLA that is most applicable.

Please contact your local Philips Semiconductors sales person when ready to start the SLA processes. This process can take anywhere between a couple of days to a couple of weeks depending upon the comments and exceptions taken from the baseline document.

17.3.1 OEM Product Development SLA

The OEM Product Development SLA is an agreement between Philips Semiconductors and the customer that allows the customer to receive working software object and source code for the development and customization of WLAN enabled OEM products using the BGW200. With this SLA, the customer can distribute working object code along with his product but cannot distribute source code.

The product development SLA is thus for customers developing end item, WLAN-enabled OEM products that will be shipped with working object code only

17.3.2 Software Development SLA

The Software Development SLA is an agreement between Philips Semiconductors and the customer that allows the customer to receive and distribute working software source code for the evaluation, customization and if necessary porting of the BGW200 low power, IEEE 802.11b WLAN system to other hardware platforms or OSs.

The Software Development SLA is thus for customers who are developing WLAN-enabled reference designs that must be delivered to their customers with working software object and source code. For these engagement models there is a need for the end customer to receive working object and source code for the final development and customization of the final product.

18. Frequently Asked Questions

This section is a compilation of frequently asked Questions and Answers that have arisen during the course of supporting BGW200 design-ins. The FAQs have been categorized to facilitate searches.

18.1 Market and Applications:

Q: What security modes are supported?
A: WEP 64 and 128 and WPA-TLS and PSK.

Q: Does the SDIO interface's SPI mode have the same functionality as the SPI2 interface?
A: No. The SPI mode on the SDIO interface is not supported in software.

Q: What is being done to specifically address the mobile phone for voice applications (other than size and power)?
A: We are working with our mobile and cordless phone chip set groups to provide complete WLAN enabled reference designs to address this market. 802.11e QOS will be supported.

Q: Does BGW200 interface and drivers work with other processors from Philips like Sysol, Melody, PNX1500, Leco, ViperII, SAA7752?
A: Yes it can but the customer will have to port software to the new processor.

Q: Is there any processing cycles left in ARM7 in the BGW200? Can the customer use it to add more application software?
A: Yes, some to support planned additions to the supported feature set. Much more constrained on memory side however, where what is available will be used for added features.

Q: How many IBSS nodes are supported?
A: The BGW200 can support up to 6 IBSS nodes.

18.2 Hardware

Q: What functional blocks are each of the 7 BGW200 supply domains powering?
A: VDD_PA: 3V analog supply to the SA2411 power amplifier.
VDD_DRIVER: 3V analog supply to the SA2405 PA driver.
VDD_VCO: 3V analog supply to the SA2405 VCO circuitry.
AVDD: 3V analog supply to the SA2405 analog blocks.
VDD_RF: 3V digital supply to the SA2405.
VDD_IO: 3V digital supply to the SA2443A IO blocks.
VDD_CORE: 1.8Vdigital supply to the SA2443A ARM7 core.

Q: What degree of Tx power control is available?
A: Approximately 12dB overall in fifteen ~1dB gain steps.

Q: How should the MODE(0) and MODE(1) pins be set?
A: This is determined by the application as follows…

Application/Boot Mode	MODE(1)	MODE(0)
SPI embedded/boot from host via SPI	0	0
Test mode/boot from EEPROM via SPI	0	1
SDIO embedded/boot from EEPROM via SPI	1	0
SDIO NIC/boot from host via SDIO	1	1

Q: What if anything does the customer have to do for mass production, e.g. shielding, and certifications?
A: It is recommended that the designer incorporate a shield into his design just in case it proves necessary. Each platform will be supported with software that will pass IEEE 802.11b WiFi certification in the end product. FCC certification issues are also addressed inside, and if necessary outside the SIP as described in this note.

Q: Is there a hardware reset pin available on the BGW200?
A: The RESET_N reset pin is not intended to be used as a hardware reset pin but rather as an input for the power ON reset signal issued at the POR_N pin at initial power up. During normal operation, the BGW200 can be reset via software by writing the appropriate register. Should it become necessary to reset the BGW200, the best way to do so would be to cycle power. This can be done in a typical embedded application by sampling disabling then re-enabling the voltage regulators that are supplying power to the SIP adhering to the power up sequence described in the Q and A above.

Q: How much and what type of internal memory is available?
A: 1.25Mbit SRAM, 256kbit ROM.

Q: What fab technologies are utilized in the BGW200?
A: The SA2443A baseband IC is fabricated in 0.18um CMOS and the SA2405 radio transceiver IC is fabricated in Qubic 3 BiCMOS.

Q: When using SDIO 1-bit mode, how should SD_DAT2 and SD_DAT3 be configured?
A: If these lines are not controlled by the host processor, SD_DAT2 must be pulled high and SD_DAT3 can be pulled high or left floating.

18.3 Software

Q: What OSs are currently supported?
A: WinCE 4.2 and 5.0 and Linux 2.4. Symbian upon request through 3rd parties.

Q: How much host NVM (Non Volatile Memory) is required to support the BGW200?
A: Approximately 350 kBytes of which ~130 kBytes is the actual MAC f/w downloaded into the SA2443A baseband IC inside the BGW200. The difference is the driver, test f/w, system configuration data, etc., that reside on the host.

Q: Can the customer modify the ARM7 MAC on BGW200?
A: No, the baseband MAC firmware is only available as object code as the customer need not touch this layer of software to integrate the BGW200 into his product.

Q: How is roaming implemented with the BGW200?
A: In WinCE.net, roaming is taken care of by Windows Zero Config (WZC). With WZC the user can set a list of preferred APs that WZC can send scan requests via the driver to the BGW200. The BGW200 scans and sends back a list of APs detected. WZC then decides, per the users preferred list, which AP to associate with.

Once associated to an AP, WZC will still send scan requests to the BGW200 every 30 seconds to execute background scans. Thus the driver will keep updating the detected AP list to keep it up-to-date. Moving out of range of the associated AP will be indicated by 5 consecutive missed beacons. When this occurs, the BGW200 will send a message to WZC indicating that it has been disconnected from the AP. From the last updated AP list and the users preferred AP list, WZC will tell the BGW200 to send a connect request to another preferred AP. Re-association to another AP is therefore automatic.

18.4 System Architecture

Q: Can the host read the RSSI data from the Washington system?
A: Yes, RSSI is read at the beginning of every packet so the RSSI register should be read by the host soon thereafter for best accuracy.

Q: What CCA (Clear Channel Assessment) modes are supported?
A: CCA modes 1, 4 and 5 are currently supported. It should be noted that CCA mode 1, which uses energy detection, is not reliable in the presence of in-band interference but does offer power saving advantages because it does not require that the entire Rx chain to be enabled. The BGW200 implements adaptive threshold detection to mitigate the effects of varying degrees of background noise in the channel but this does not combat interference.

Q: What is meant by "zero-host load"?
A: No MAC processing on the host and when in power save mode, the host can sleep while the BGW200 monitors and processes beacon traffic.

18.5 System Integration

Q: What is the proper sequence for applying power to the BGW200?
A: Stable 3V power must be provided to the BGW200 prior to application of the 1.8V supply in order to ensure proper execution of the power ON reset. After the 1.8V supply voltage has stabilized, the SA2443 power ON reset circuit will wait ~4ms before initiating the system RESET to allow the 44MHz system clock time power up and stabilize.

Q: How are the BGW200 GPIOs used in a typical application?
A: GPIOs{0], [1], [2] and [3] are reserved for co-location applications with Bluetooth. GPIO[4] can be used as an external 32kHz CLK input. GPIO[9] is not used and GPIO[10] is typically used as a EEPROM chip select.

Q: How can data throughput be measured benchmarked against other solutions?
A: Chariot throughput measurements are the industry standard for comparing throughput performance between different solutions. Thus Chariot throughput data is used to benchmark the BGW200 system. If customers wish to repeat these results in their lab then they will need to have access to a Chariot license.

Q: How can a customer run a simple throughput test with the BGW200 evaluation kit?
A: A utility called Udptx is provided with the evaluation kit to allow customers to run such a test between the target BGW200 + host system (.e.g. Mainstone2 or OMAP) through an AP to suitable Windows PC running the same utility.

Q: How do you wake up the BGW200 when it is in Sleep and Deep Sleep modes?

A: In Doze mode this is done automatically based upon the listen interval negotiated with the AP. A wake timer in the BGW200 is set to wake-up the device automatically in time to receive the next scheduled beacon. Deep sleep mode is different. This implies no wake timer is set so the BGW200 is only partially alive and operating off of its 32kHz sleep CLK. Partially alive in the sense that interface with the host is still active. Thus the host can simply write data into a target mailbox register to initiate the wake-up sequence in the BGW200 as long as this interrupt is enabled as it is in f/w baselines provided by Philips Semiconductors.

Q: What should be done if the BGW200 fails to boot properly at power up?
A: The following systematic approach can be used to troubleshoot SPI-boot-from-host problems should they occur:

1) Verify the 44MHz XO is on frequency and tune if necessary. Requirement is 44MHz +/-25ppm over temperature and product life…+/-10 ppm is recommended.
2) Ensure that DC power is applied in the proper sequence as described in Section 3.5.1 of this note. Failure to do so could put the BGW200 into an undefined, non-responsive state.
3) Check signal quality/pulse shapes and voltage levels of the SPI CLK, MISO, MOSI and SS lines. Resistively terminate if required.
4) Verify proper SPI timing between the CLK, MISO, MOSI and SS lines. Timing requirements (T_{DL}, T_{SU} and T_H) can be found in the BGW200 product datasheet. For a 13MHz SPI CLK, the system is set-up for MOSI and MISO to clock data on the falling edge and sample data on the rising. For higher CLK speeds this may have to be changed and can be done via nvram.txt. Please contact Philips for technical support should this be required.

If the SPI bus looks clean then the next step is to verify that message exchanges across the bus are working properly.

5) The contents of the following registers can be read to determine how far the boot up sequence progressed prior to stopping:

   a) 0x24 in S2M_MB2 indicating the Target is ready for config parser download.
   b) 0xA5 in M2S_SR2 indicating the host has completed the config parser DMA.
   c) 0x42 in S2M_MB2 indicating the Target has started config parser execution.
   d) 0x26 in S2M_MB2 indicating the Target has completed config parser execution.

At this point the host sets-up the DMA transfer by programming the DMA address registers and storing the number of 32 kbyte data blocks to transfer in M2S_MB3.

   e) 0x27 in S2M_MB2 indicating the Target is ready to DMA the firmware image.

6) When the DMA transfer is completed the host writes the number of transfers completed into M2S_SR2.
7) The Target then responds with its own count of the number of transfers completed storing this value in S2M_SR3.
8) If more 32 kbyte data blocks are still to be downloaded, steps 5c) through 7) are repeated until all data blocks have been downloaded.

If all of the above checks out, the device should be booting properly and able to connect to operate normally. If not, this could be an indication of radio issues that are difficult to quantify without specialized WLAN RF test equipment. Radio performance can perhaps be evaluated in a less quantitative manner by using a WLAN packet sniffer tool. If the sniffer tool is not capable of recovering the transmitted packets, this would be an indication that the radio performance may be poor.

Q: How does the BGW200 wake the host when the SDIO interface is used?
A: This covered as part of the SDIO protocol implemented on both the host and BGW200 side, unlike in the case when the SPI interface is used and separate SPI_EXT_INT line must be used to allow the BGW200 to wake the host.

Q: What is the power status of SPI lines when the BGW200 in DOZE and Deep sleep mode?
A: The SDIO and SPI host interfaces remain active in these modes, so if the mailbox interrupts are enabled as it is with the standard f/w releases from Philips, the host can wake-

up the BGW200 simply by writing to one of the local mailbox registers. Refer to the SPI2 and SDIO interface sections of the BGW200 data sheet.

Q: What are the maximum supported SPI and SDIO clock rates?
A: The maximum supported SPI CLK speed is 66 MHz (also the maximum CLK speed for the BGW200 ARM7 core) vs. 25 MHz Max. for the SDIO CLK. For more detailed information on the SPI and SDIO host interfaces, please refer to the applicable sections in the BGW200 data sheet [1].

Q: What changes are necessary to operate at higher SPI CLK speeds?
A: The default configuration for the BGW200 is SPI data clocked on the rising edge for MOSI and on the falling edge for MISO. For the BGW200 the edge to use is configurable in the MISO direction. At 13MHz the CLK period is 76ns and there is plenty of margin.

At say 50MHz because the CLK period is only 20ns, the 10ns MAX delay for the BGW200 for leaves no room for setup time at the host. For example if Tsetup=5ns for the host, Tperiod_max=2*(Tdelay+Tsetup) =2*(10ns + 5ns)=30ns or ~33MHz. That is to say, for SPI CLK > 33MHz you will need to reprogram the SPI2 configuration register to switch to the rising edge for MISO. This can be done by appending the following to element 0x30 in nvram...

00 02 B8 8C 00 00 00 80 FF FF FF 7F

Q: How can a customer run a simple throughput test with the BGW200 evaluation kit under Linux (e.g. MS2/SPI)? Is a standard tool like iperf supported or is there a Philips stress tool.
A: This can be done using the following test set-up and procedure…

1) Windows PC#1 (IP address 192.168.1.10) connected via crossover cable to interface eth0 on MS2 (SPI/Linux/MS2) + NOVA (IP address 192.168.1.1).
2) MS2 (SPI/Linux/MS2) + NOVA eth1 (IP address 192.169.2.111) connected wirelessly to an AP (IP address 192.168.2.0).
3) Connect the AP via ethernet cable to Windows PC#2 (IP address 192.168.2.1).
4) Issue the following commands on the MS2 hyperterminal.
   [root@Linux tmp]ping 192.168.2.1
   [root@Linux tmp]ifconfig eth0 192.168.1.1
   [root@Linux tmp]ifconfig eth1 192.168.2.111 up
   [root@Linux tmp]echo 1 > /proc/sys/net/ipv4/ip_forward
6) Execute UDPTx on Windows PC #1, execute UDPRx on Windows PC #2 and monitor bi-directional UDP throughput.

Q: What regulatory domains are supported?
A: The following regional domains for channel access control are supported and selectable via nvram.txt.

North America:	CH1-11
ETSI:	CH1-13
Mexico:	CH10-11
France/Singapore:	CH10-13
Japan:	CH1-13 (operation on CH14 is NOT supported)

Q: What is the default sleep CLK configuration for the system?
A: The default configuration of the system is to operate in Sleep mode from the internal sleep clock. GPIO4 is thus configured in the nvram.txt file accordingly and no external clock source should thus be applied to this pin as high current will be drawn. Enabling ext 32 KHz CLK mode can be done via nvram. Contact local Philips technical support personale for further information.

19. List of References

[1] BGW200 Data Sheet

[2] Nova Board Users Guide

[3] Nova board schematics

[4] Nova board bill of materials

[5] Nova board fab drawing

[6] Nova board layout

[7] AN10490 BGW200 Software Implementation Guide

[8] WiFi Interoperability Test Plan, Version 1, WiFi Alliance

[9] System Test Environment Specification

[10] UM10130, PHY GUI Test software User Manual

[11] Washington Test Environment Set-Up Guide

[12] AN10390, BGW200 System Configuration App Note

[13] AN10359, Philips IEEE 802.11b Power Management Utility App Note

[14] UM10144, nvram Customization Tool User Manual

[15] How 802.11b/g WLAN and Bluetooth can play Together, White Paper, June 2004, document no. 9397-750-13426

Appendix A

Official WiFi Certification test report for the WinCE 4.2/Mainstone2/SPI standard platform.

Agilent Technologies

Interoperability Test Lab
Wi-Fi Certification Test Results Report

PDA Test

Test Plan
802.11B + WPA - Station

Original Test Date
9/22/2004

Customer
Philips

Test Plan Version
2.2

Date Test Passed
9/22/2004

Certification ID: WI02510
Chip Vendor: Philips
Device Model: M2ASTER2
Device Type: PDA
Firmware: 4
MAC Address: 00A0A1A2A3A4
Test Engineer: David Lancaster
Test Lab: Santa Clara, California
Overall Test Result: Pass

Test Description	Reference Value	Measured Value	Pass/ Fail	Comment
OOB Verification	N/A	N/A	Pass	
Configurability	N/A	N/A	Pass	
Initial Ping	N/A	N/A	Pass	
PureS1	2.438	3.948	Pass	
	2.297	4.758	Pass	
	0.210	0.409	Pass	
PureS2	2.425	4.962	Pass	
	2.316	4.924	Pass	
	0.210	0.361	Pass	
PureS3	1.400	2.898	Pass	
	2.371	4.566	Pass	
	0.273	0.356	Pass	
PureS4	1.940	3.617	Pass	
	1.680	4.513	Pass	
	0.210	0.319	Pass	
PureS5	1.494	2.625	Pass	
	1.890	4.625	Pass	
	0.322	0.378	Pass	
PureS6	2.367	4.182	Pass	
	2.294	4.745	Pass	
	0.210	0.378	Pass	
PureS7	2.493	4.861	Pass	
	2.397	4.986	Pass	
	0.210	0.379	Pass	
PureS8	2.029	3.786	Pass	
	1.890	4.531	Pass	
	0.310	0.319	Pass	

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Testing performed in accordance with the official Wi-Fi Alliance test plan
Wireless/Wireline Decodes Provided Courtesy of WildPackets, Inc. (AiroPeek).

1

Agilent Technologies

Interoperability Test Lab
Wi-Fi Certification Test Results Report

PDA Test

Test Plan
802.11B + WPA - Station

Original Test Date
9/22/2004

Customer
Philips

Test Plan Version
2.2

Date Test Passed
9/22/2004

Certification ID: WI002510
Chip Vendor: Philips
Device Model: M2ASTER2
Device Type: PDA
Firmware: 4
MAC Address: 00A0A1A2A3A4
Test Engineer: David Lancaster
Test Lab: Santa Clara, California
Overall Test Result: Pass

Test Description	Reference Value	Measured Value	Pass/ Fail	Comment
SI1	0.630	5.020	Pass	
	1.050	4.045	Pass	
SI2	1.190	3.577	Pass	
	2.100	4.324	Pass	
SI3	1.968	4.078	Pass	
	2.213	3.952	Pass	
	0.038	0.080	Pass	
	0.038	0.076	Pass	
SI4	1.317	4.066	Pass	
	2.467	4.389	Pass	
	0.037	2.464	Pass	
	0.038	3.305	Pass	
Multicast 1	N/A	N/A	Pass	
Multicast 2	N/A	N/A	Pass	
NAV	3.806	1.289	Pass	NAV/PLCP @ 80% ref
PLCP	3.806	1.542	Pass	NAV/PLCP @ 80% ref
Same Mode Roaming with Authentication Server	N/A	N/A	Pass	
Same Mode Roaming Using PSK	N/A	N/A	Pass	
Countermeasure Tests	N/A	N/A	Pass	
Negative Tests	N/A	N/A	Pass	
Non-Association with WEP AP	N/A	N/A	Pass	
Non-Association with AP Not Using WPA	N/A	N/A	Pass	

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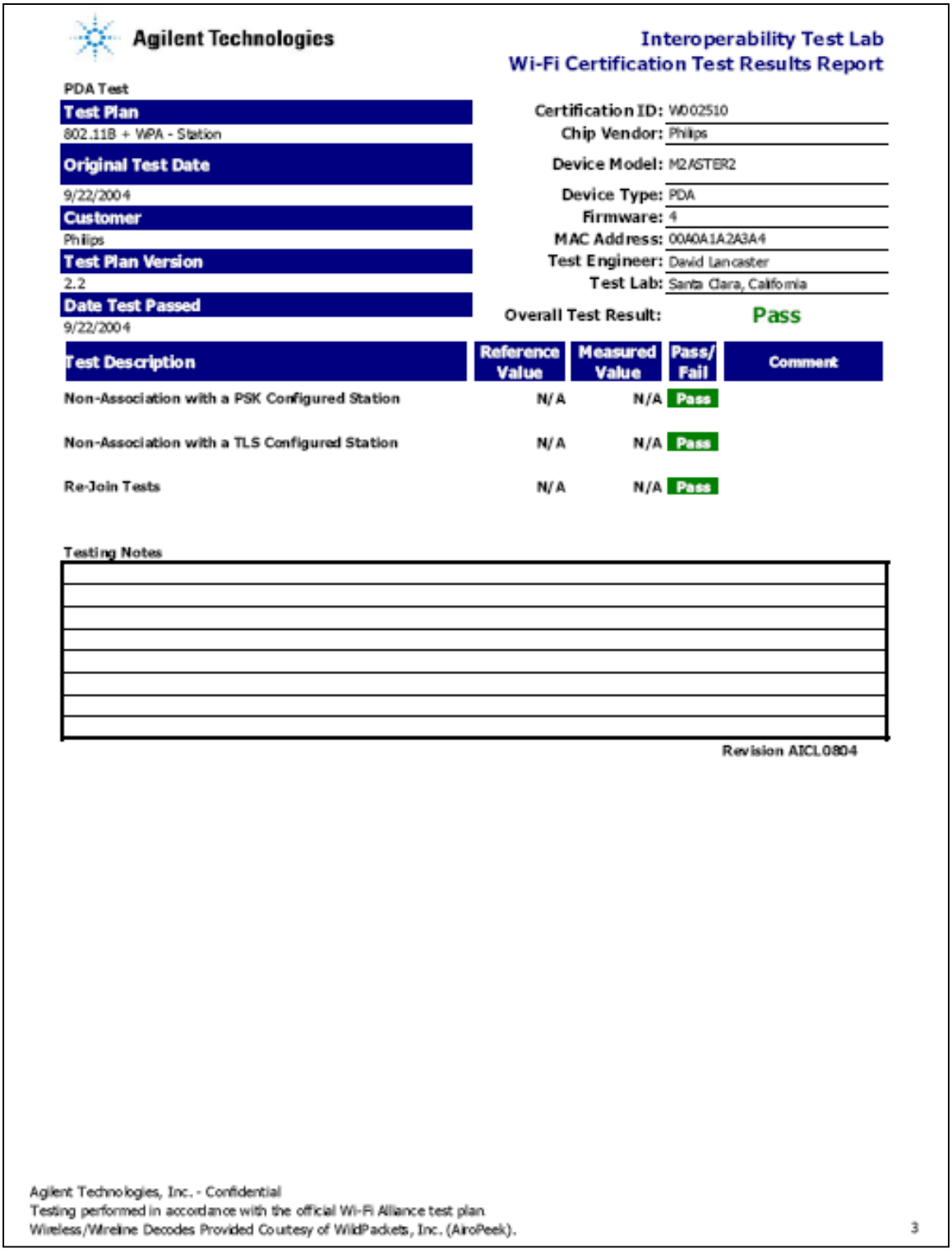
Wireless/Wireline Decodes Provided Courtesy of WildPackets, Inc. (AiroPeek).

2



Agilent Technologies

Interoperability Test Lab
Wi-Fi Certification Test Results Report

PDA Test

Test Plan
802.11B + WPA - Station

Original Test Date
9/22/2004

Customer
Philips

Test Plan Version
2.2

Date Test Passed
9/22/2004

Certification ID: WI02510
Chip Vendor: Philips
Device Model: M2ASTER2
Device Type: PDA
Firmware: 4
MAC Address: 00A0A1A2A3A4
Test Engineer: David Lancaster
Test Lab: Santa Clara, California

Overall Test Result: Pass

Test Description	Reference Value	Measured Value	Pass/ Fail	Comment
Non-Association with a PSK Configured Station	N/A	N/A	Pass	
Non-Association with a TLS Configured Station	N/A	N/A	Pass	
Re-Join Tests	N/A	N/A	Pass	

Testing Notes

Revision AICL0804

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Wireless/Wireline Decodes Provided Courtesy of WildPackets, Inc. (AiroPeek).

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Appendix B

Example ASD proposal letter to be used for products seeking WiFi certification with the BGW200.

Application Specific Device Proposal Document

For STA of 802.11b WiFi product certification

Station Under Test consists of an 802.11b SPI module within a Smart Phone supported by Windows CE.

The Station Under Test is to be tested according to **the WiFi 802.11b with WPA System interoperability Test Plan for IEEE 802.11b Devices (version 2.2**) and the **WiFi PDA Interoperability Test Plan (version 1.0).**

The following changes will be applied to the standards test plan announced above:

- Replace OS with Windows CE in all tests
- Use Chariot End point, supplied with the Smart Phone to be tested
- Use the following throughput values to replace standard PDA requirement:

STA Throughput Values

S3DT3	0.195
S5DT3	0.230
S8DT3	0.222

20. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

21. Licenses

Purchase of Philips I²C components

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

Purchase of Philips RC5 components

Purchase of Philips RC5 components conveys a license under the Philips RC5 patent to use the components in RC5 system products conforming to the RC5 standard UATM-5000 for allocation of remote control commands defined by Philips.

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