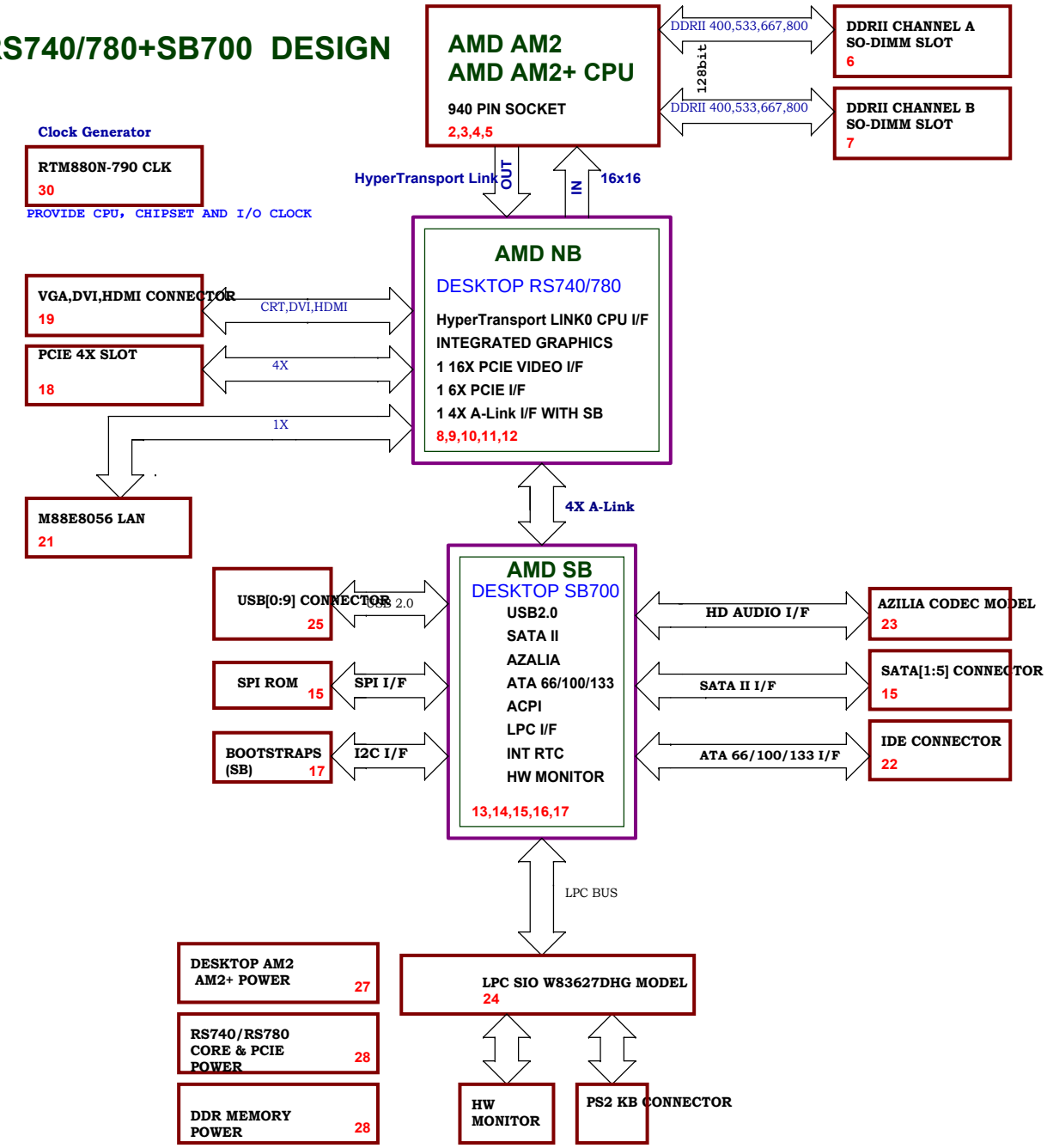
RS740/780+SB700 DESIGN



J&W

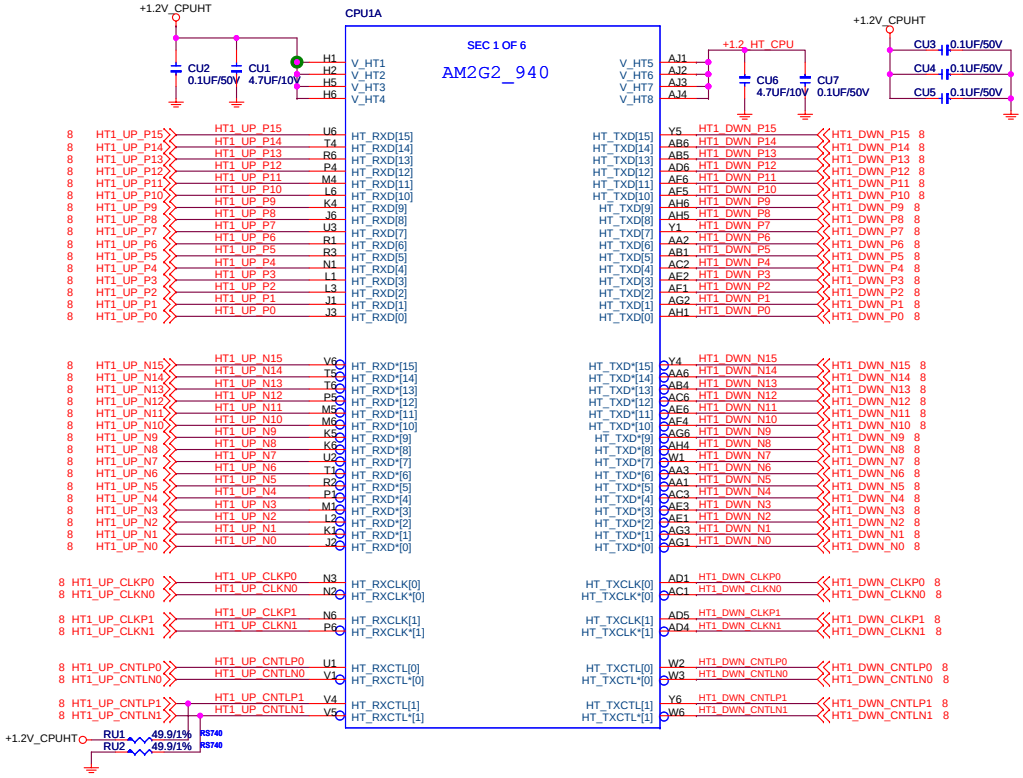
Title: COVER SHEET

Size	Document Number	Rev
Custom	RS740/780+SB700+AM2/AM2+	1.0

Date: Monday, August 18, 2008 Sheet 1 of 34

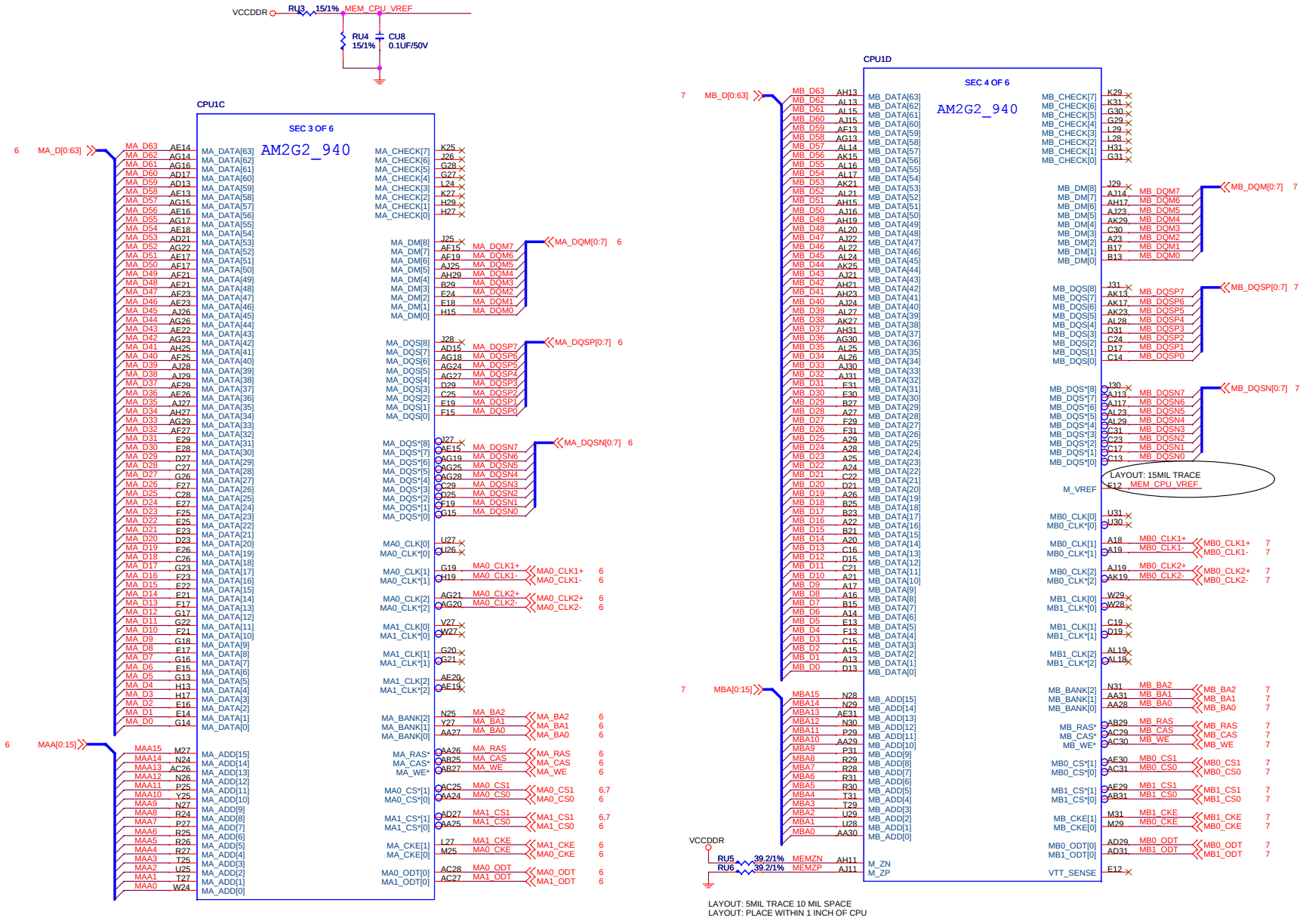
Clawhammer HT Interface

LAYOUT: Place HT bypass caps on topside
near unconnected Clawhammer HT Link

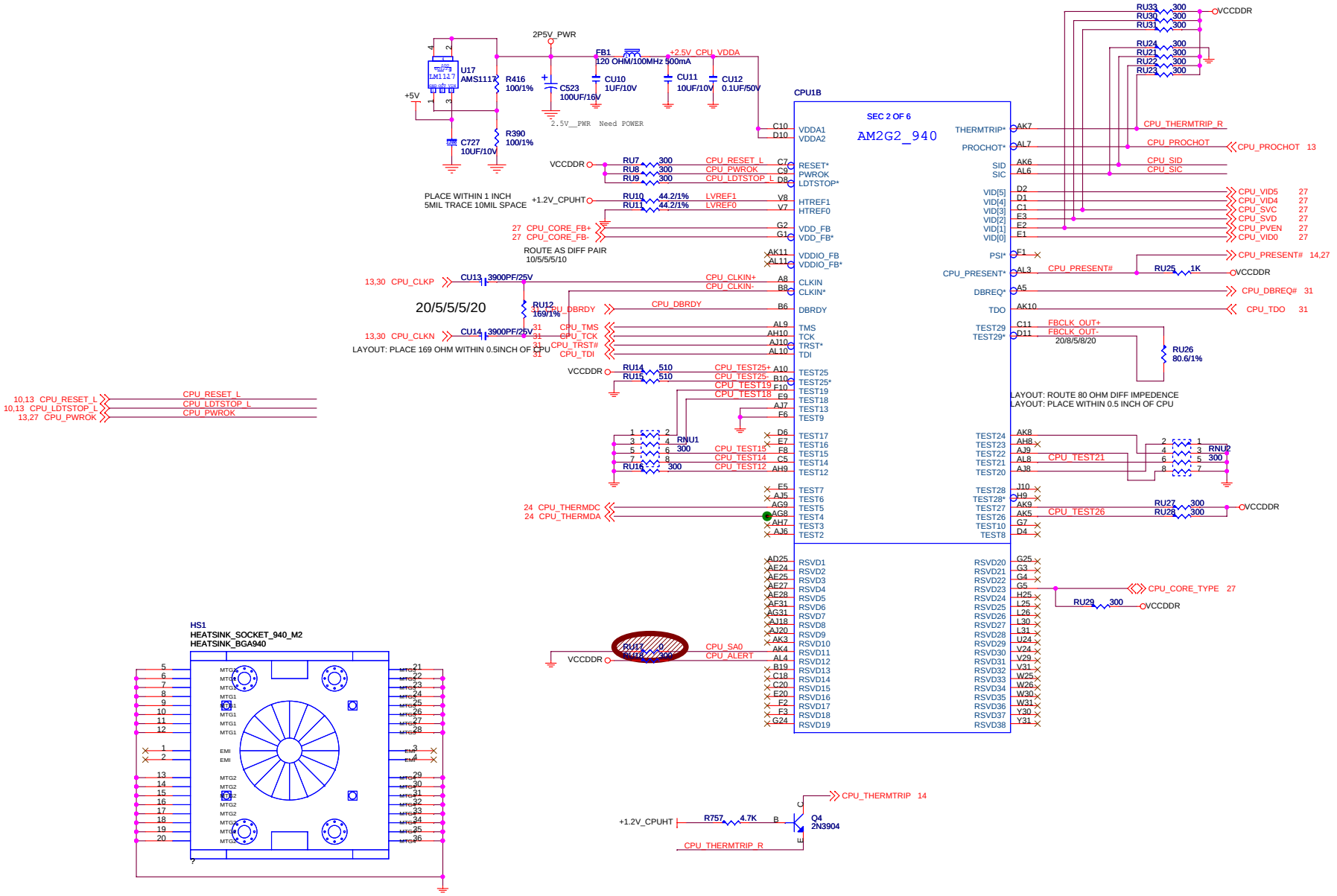


Title	AM2+ HT I/F
Size	Custom
Document Number	RS740/780+SB700+AM2+
Rev	1.0
Date:	Monday, August 18, 2008
Sheet	2 of 34

Clawhammer DDR Interface

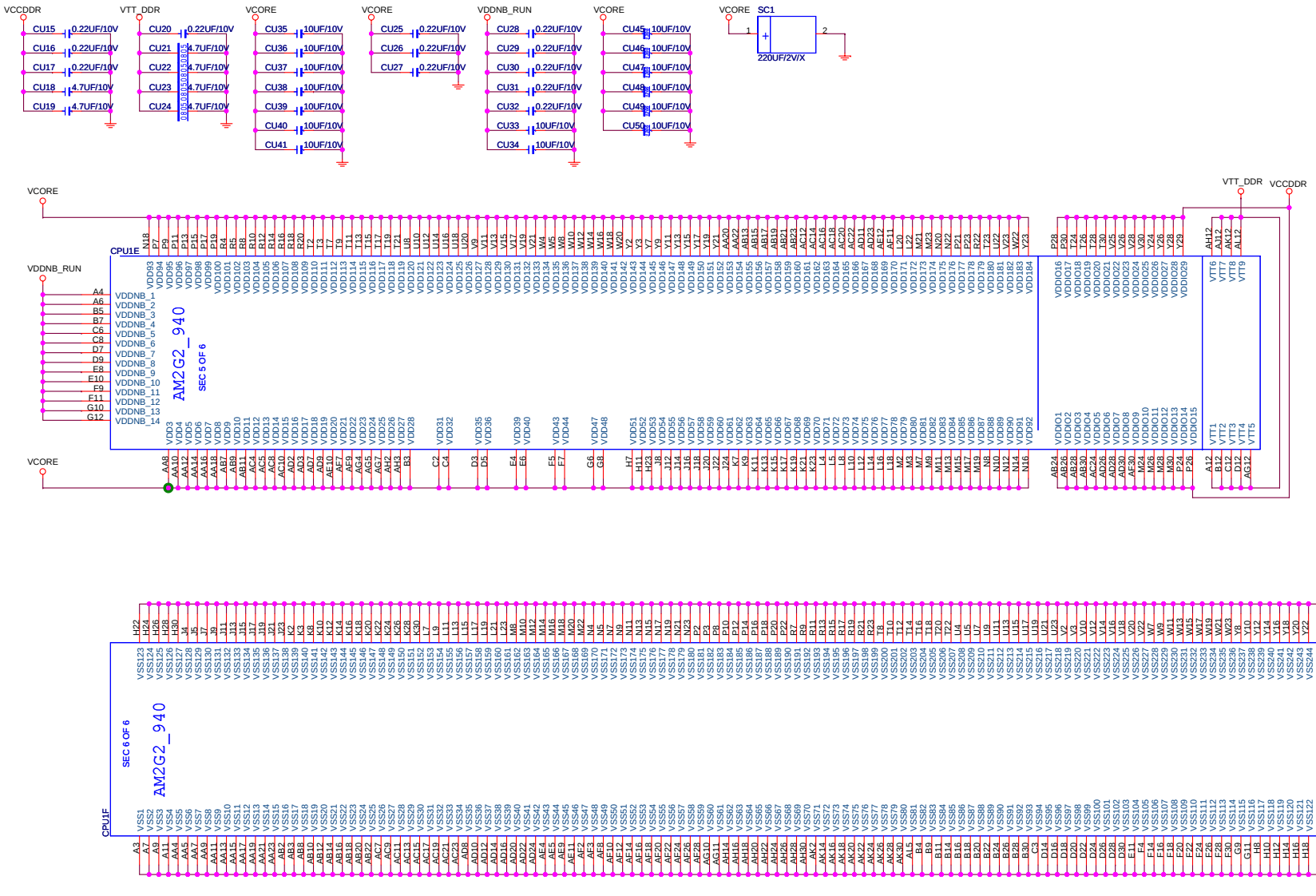


J&W			
Title	AM2+ DDRII I/F		
Size: Custom	Document Number: RS740/780+SB700+AM2+		Rev: 1.0
Date: Monday, August 18, 2008	Sheet 3 of 34		

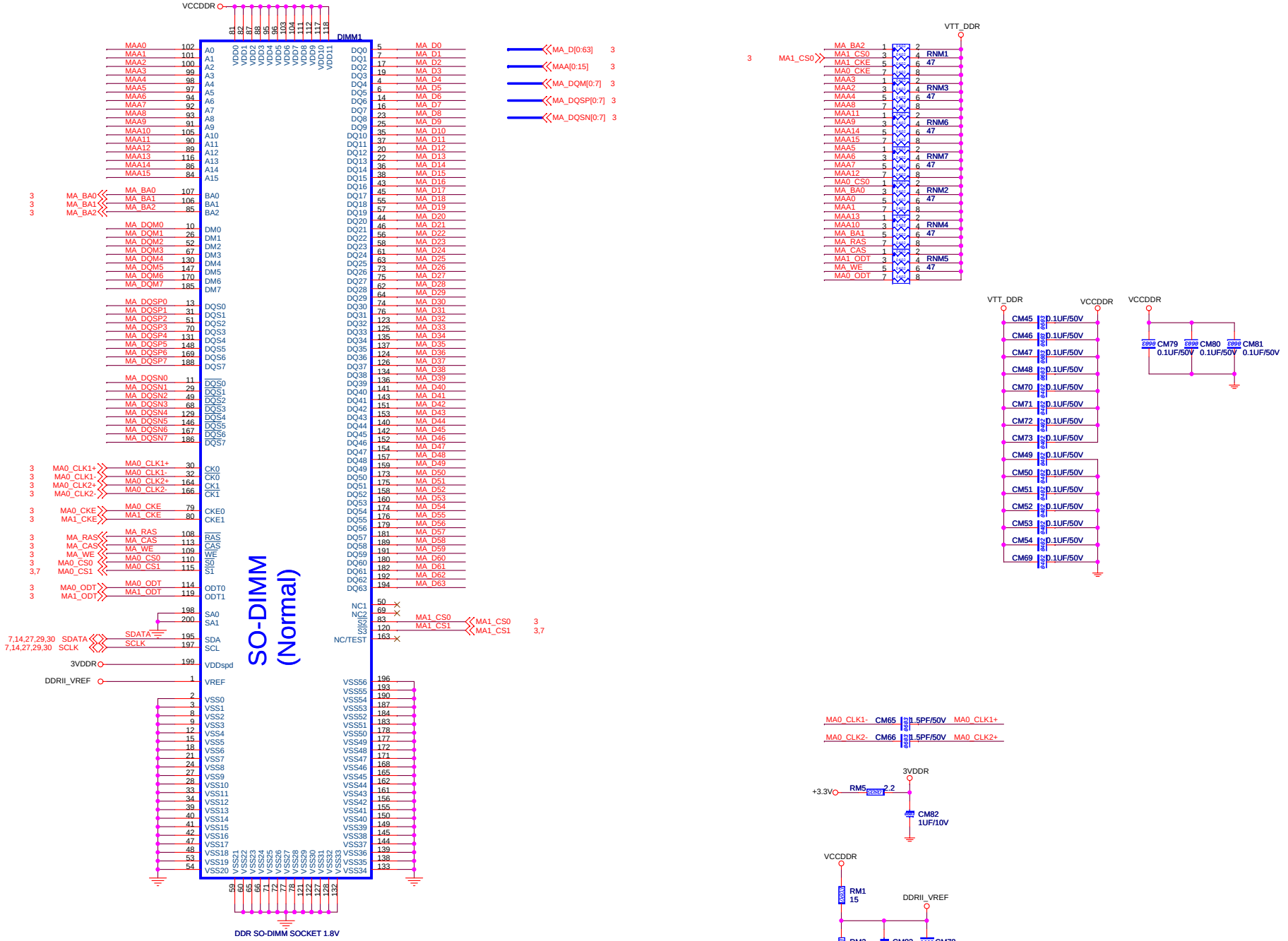


J&W

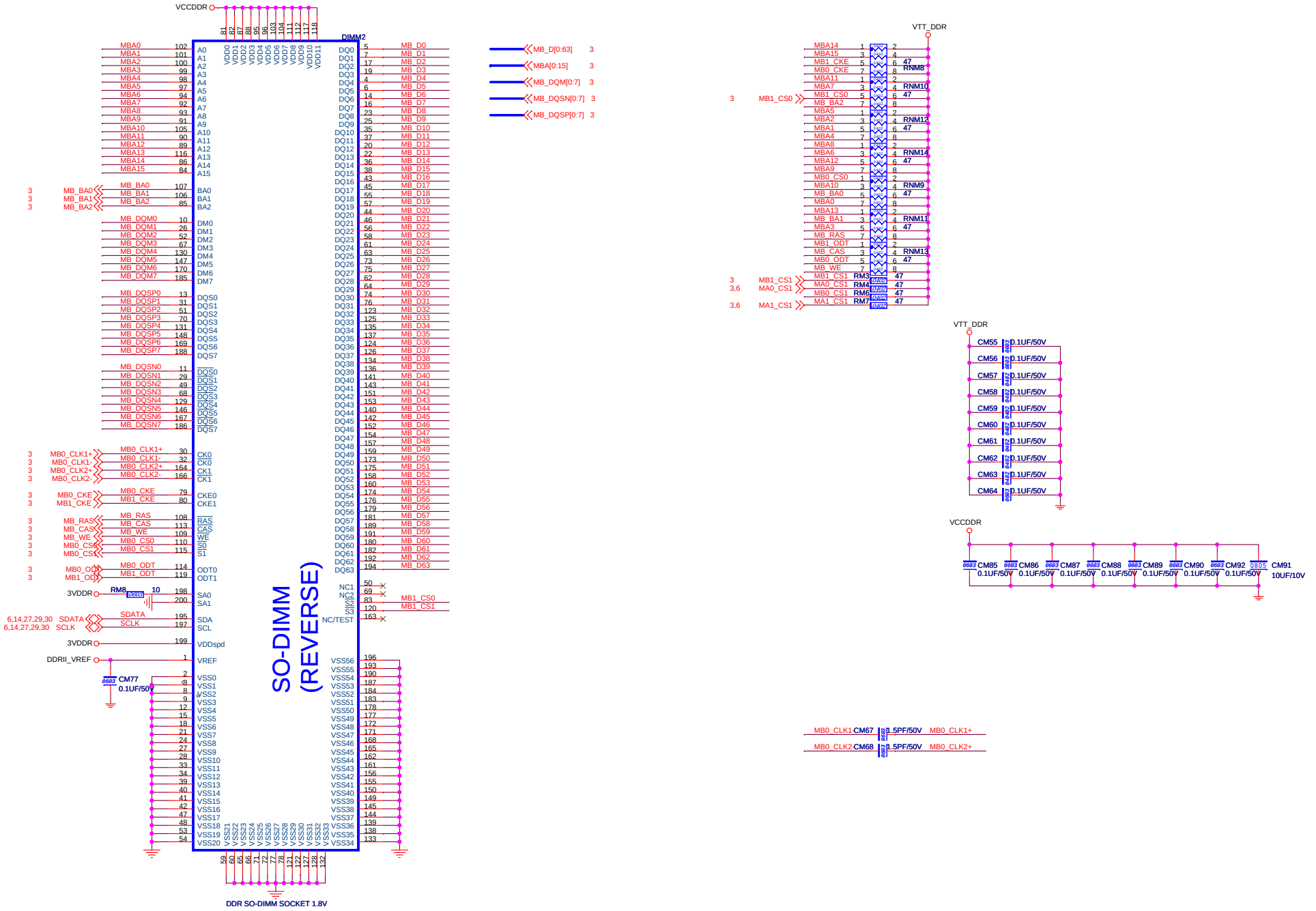
Title	AM2+ CNTL/MISC I/F	
Size: Custom	Document Number: RS740/780+SB700+AM2+	Rev: 1.0
Date: Monday, August 18, 2008	Sheet 4 of 34	



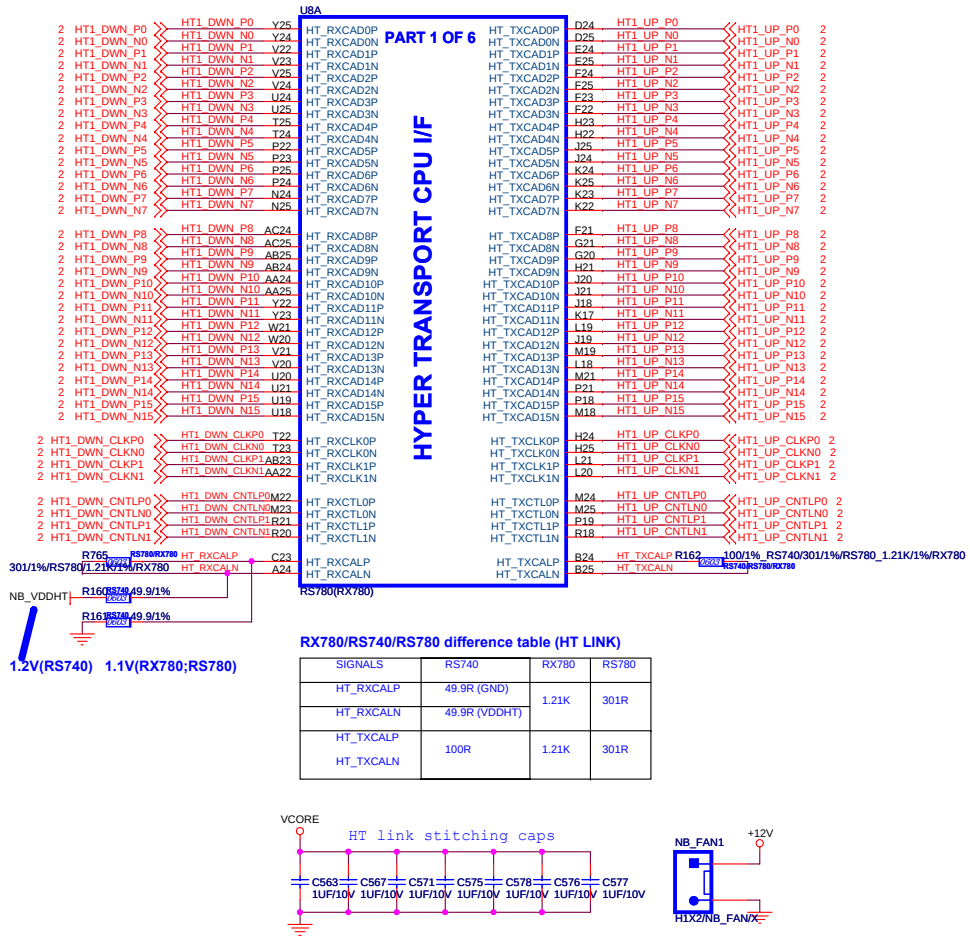
Title	AM2+ POWER
Size	Custom
Document Number	RS740/780+SB700+AM2+
Rev	1.0
Date:	Monday, August 18, 2008
Sheet	5 of 34

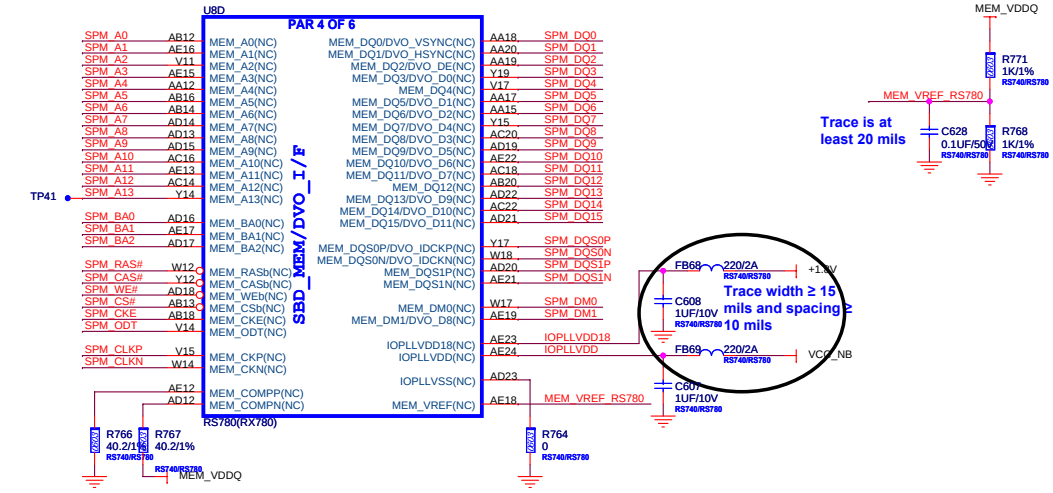


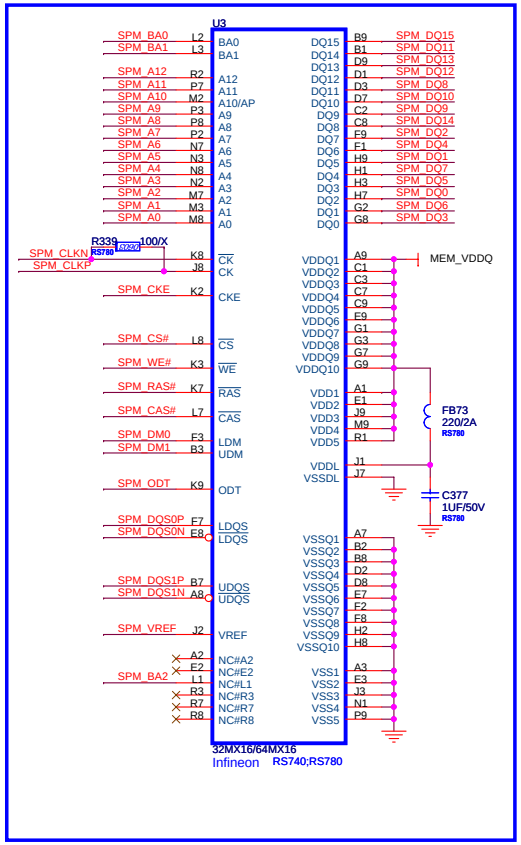
J&W		
Title	DDRII SLOT1-CHANNEL A0	
Size: Custom	Document Number: RS740/780+SB700+AM2+	Rev: 1.0
Date: Monday, August 18, 2008	Sheet 6 of 34	

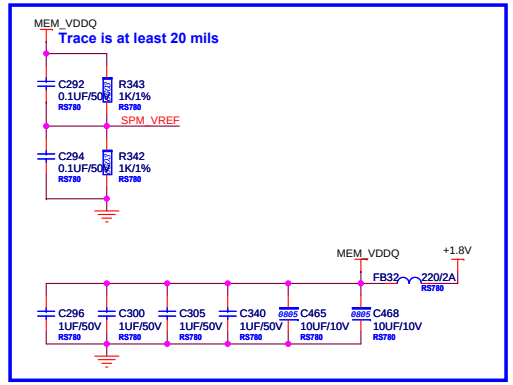


Title	DDRII SLOT2-CHANNEL B0
Size	Custom
Document Number	RS740/780+SB700+AM2+
Rev	1.0
Date:	Monday, August 18, 2008
Sheet	7 of 34









RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP	100R	1.21K	301R
HT_TXCALN			

DDR2 SIDE PORT MEMORY DEVICES
16Mx16 HYNIX HY5PS561621AFP-25
32Mx16 QIMONDA HYB18T512161B2F-25
64Mx16 SAMSAUNG K4N1G164QQ-HC25

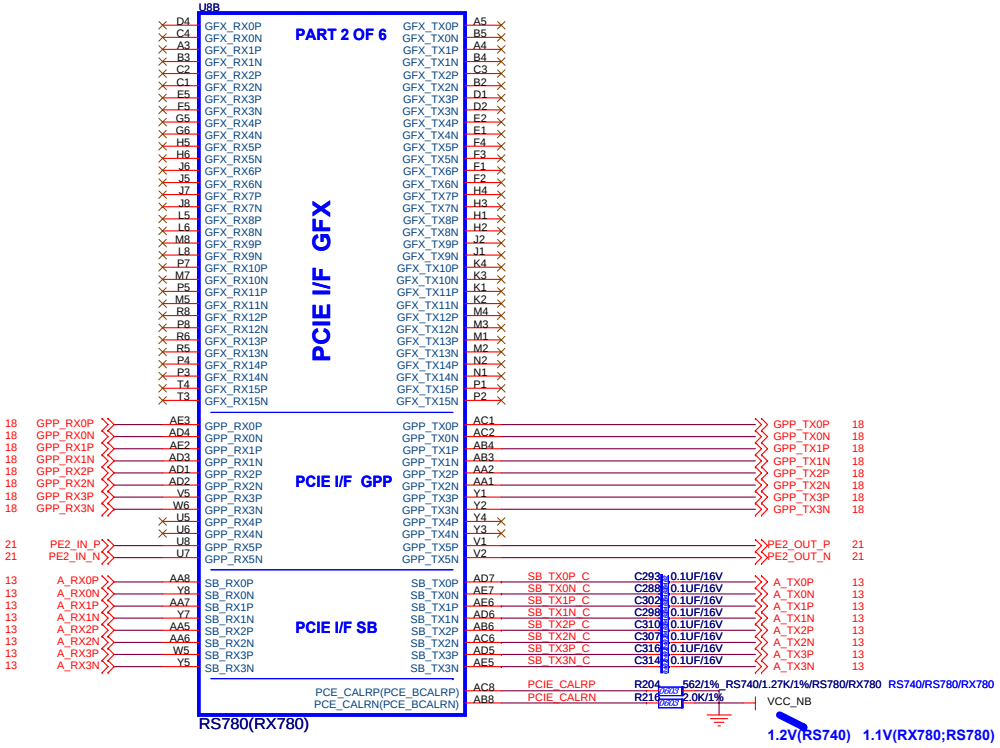
DDR3 SIDE PORT MEMORY DEVICES
64Mx16 HYNIX HY5TQ1G431ZNFP-G8

J&W

Title: **RS740/780 HT I/F SIDE MEMORY**

Size	Document Number	Rev
Custom	RS740/780+SB700+AM2+	1.0

Date: Monday, August 18, 2008 Sheet 8 of 34



RX780/RS740/RS780 GPP difference table

	RS740	RX780/RS780
PCE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RX780/RS740/RS780 GPP Routing table

	RS740	RX780/RS780
GPP X4 CONNECTOR	GPP[2:0]	GPP[3:0]
GPP X1 CONNECTOR		GPP4
GIGABIT ETHERNET	GPP3	GPP5

RS780 Display Port Support (muxed on GFX)

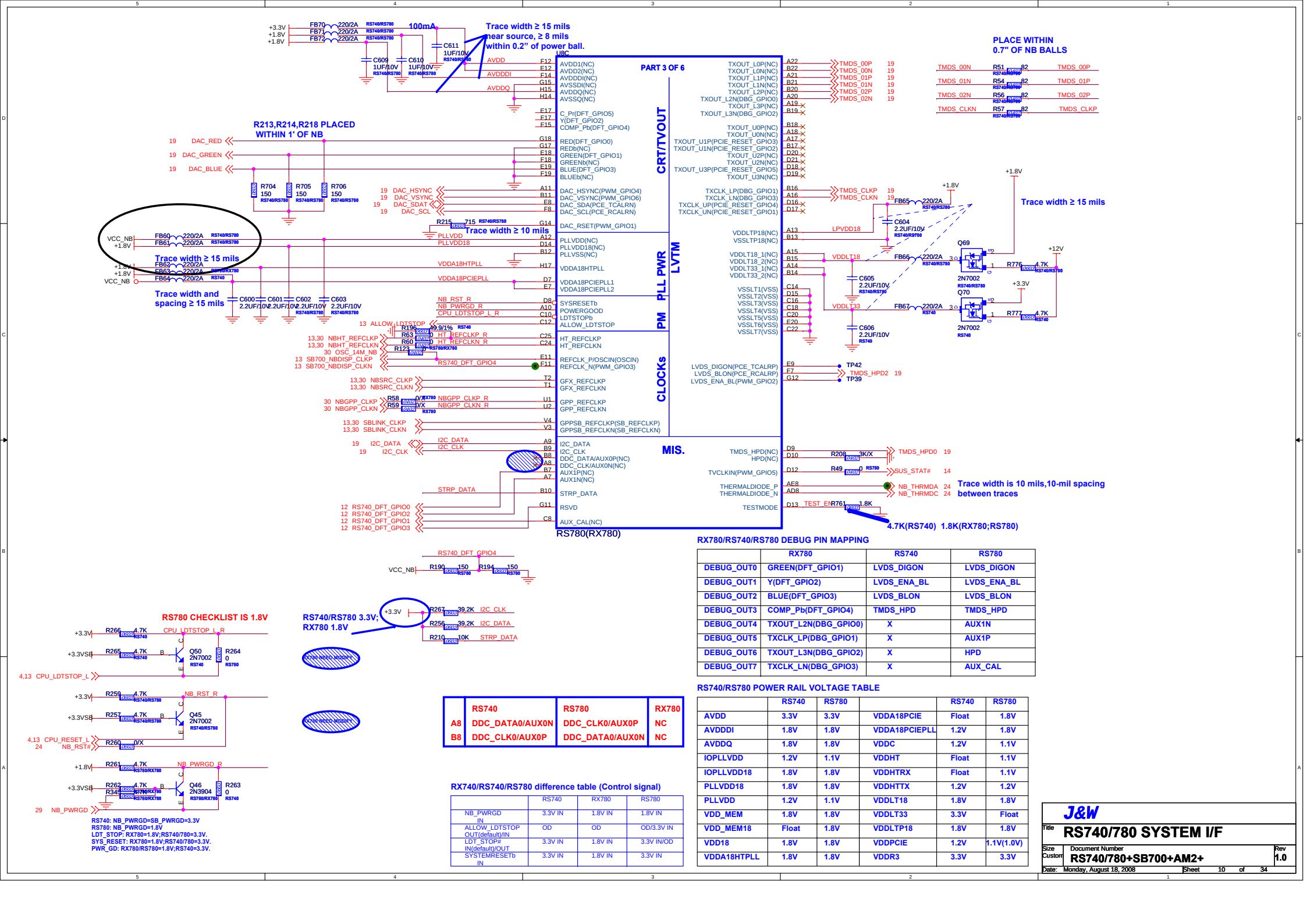
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

J&W

Title: RS740/780 PCIE I/F

Size: Custom | Document Number: RS740/780+SB700+AM2+ | Rev: 1.0

Date: Monday, August 18, 2008 | Sheet 9 of 34



RX780/RS740/RS780 DEBUG PIN MAPPING

	RX780	RS740	RS780
DEBUG_OUT0	GREEN(DFT_GPIO1)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	Y(DFT_GPIO2)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	BLUE(DFT_GPIO3)	LVDS_BLON	LVDS_BLON
DEBUG_OUT3	COMP_Pb(DFT_GPIO4)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

RS740/RS780 POWER RAIL VOLTAGE TABLE

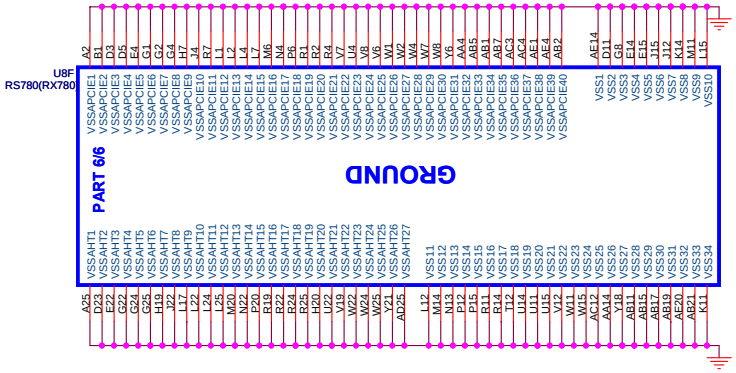
	RS740	RS780		RS740	RS780
AVDD	3.3V	3.3V	VDDA18PCIE	Float	1.8V
AVDDDI	1.8V	1.8V	VDDA18PCIEPLL	1.2V	1.8V
AVDDQ	1.8V	1.8V	VDDC	1.2V	1.1V
IOPLLVDD	1.2V	1.1V	VDDHT	Float	1.1V
IOPLLVDD18	1.8V	1.8V	VDDHTRX	Float	1.1V
PLLVDD18	1.8V	1.8V	VDDHTTX	1.2V	1.2V
PLLVDD	1.2V	1.1V	VDDLT18	1.8V	1.8V
VDD_MEM	1.8V	1.8V	VDDLT33	3.3V	Float
VDD_MEM18	Float	1.8V	VDDLTP18	1.8V	1.8V
VDD18	1.8V	1.8V	VDDPCIE	1.2V	1.1V(1.0V)
VDDA18HTPLL	1.8V	1.8V	VDDR3	3.3V	3.3V

	RS740	RS780	RX780
A8	DDC_DATA0/AUX0N	DDC_CLK0/AUX0P	NC
B8	DDC_CLK0/AUX0P	DDC_DATA0/AUX0N	NC

RX740/RS740/RS780 difference table (Control signal)

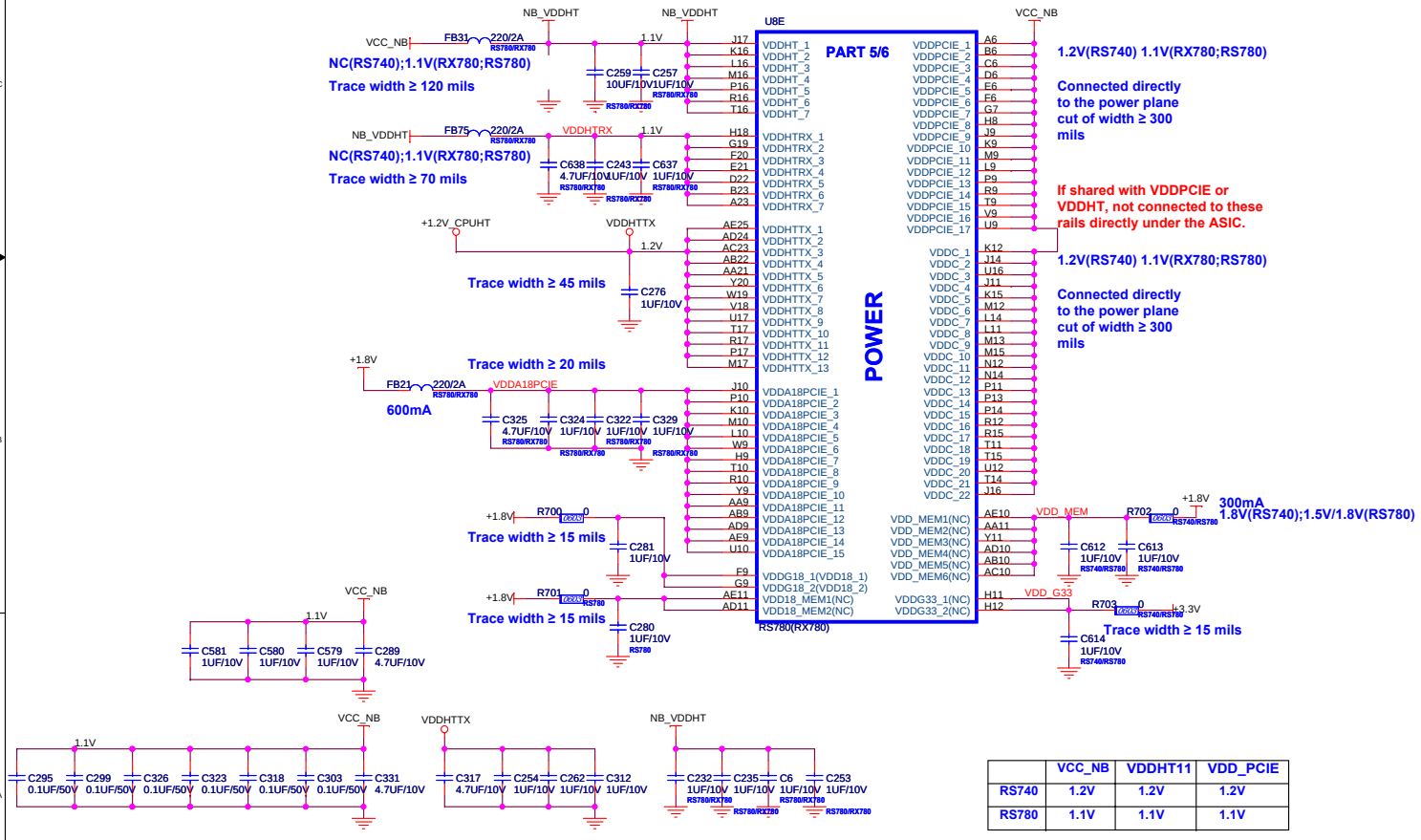
	RS740	RX780	RS780
NB_PWRGD IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OD	OD	OD/3.3V IN
LDT_STOP# IN(default)/OUT	3.3V IN	1.8V IN	3.3V IN/OD
SYSTEMRESETb IN	3.3V IN	1.8V IN	3.3V IN

Title	RS740/780 SYSTEM I/F
Size	Custom
Document Number	RS740/780+SB700+AM2+
Rev	1.0
Date:	Monday, August 18, 2008
Sheet	10 of 34



RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC



	VCC_NB	VDDHT11	VDD_PCIE
RS740	1.2V	1.2V	1.2V
RS780	1.1V	1.1V	1.1V

Title	RS740/780 POWER
Size	Custom
Document Number	RS740/780+SB700+AM2+
Rev	1.0
Date:	Monday, August 18, 2008
Sheet	11 of 34

RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8

Note: for RX780 (RX780_DFT_GPIO1) to 1K accordingly

Note: for RX780, change following pull-down resistor to 1K accordingly (RX780_DFT_GPIO5)

Note: for RX780, change following pull-down resistor to 1K accordingly
(RX780_DFT_GPIO4)
(RX780_DFT_GPIO3)
(RX780_DFT_GPIO2)

Note: for RX780, change following pull-down resistor to 1K accordingly (RX780_DFT_GPIO0)

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740: pin DFT_GPIO1
RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#  GREEN E18
```

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

```
Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740/RS780); Disable (RX780)
0 : Enable  (RS740/RS780); Enable(RX780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC
```

C_PR E17

RS740: STRAP_PCIE_SB/GPP_CFG[2:0] (Pins: RS740_DFT_GPIO[4:2])

```
These pin straps are used to configure PCI-E GPP mode.
111: register defined (register default to Config E)   default
110: 4-0-0-0-0   Config A
101: 4-4-0-0-0   Config B
100: 4-2-2-0-0   Config C
011: 4-2-1-1-0   Config D
010: 4-1-1-1-1   Config E
others: register defined (default to Config E)
```

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins: RX780_DFT_GPIO[4:2])

```
111: 1-1-1-1-1-1   Mode L   default
110: 1-1-1-1-1-1   Mode L
101: 2-0-2-0-2-0   Mode C2
100: 2-0-2-0-1-1   Mode K
011: 2-0-1-1-1-1   Mode E
010: 1-1-1-1-1-1   Mode L
001: 4-0-0-0-1-1   Mode C
000: 4-0-0-0-2-0   Mode B
```

DFT_GPIO2: Y F17
DFT_GPIO3: BLUE E19
DFT_GPIO4: COMP_PB F15

RS780: STRAP_PCIE_GPP_CFG[2:0] (configure thru register setting)

```
1-1-1-1-1-1   Mode L   default
1-1-1-1-1-1   Mode L
2-0-2-0-2-0   Mode C2
2-0-2-0-1-1   Mode K
2-0-1-1-1-1   Mode E
1-1-1-1-1-1   Mode L
4-0-0-0-1-1   Mode C
4-0-0-0-2-0   Mode B
```

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

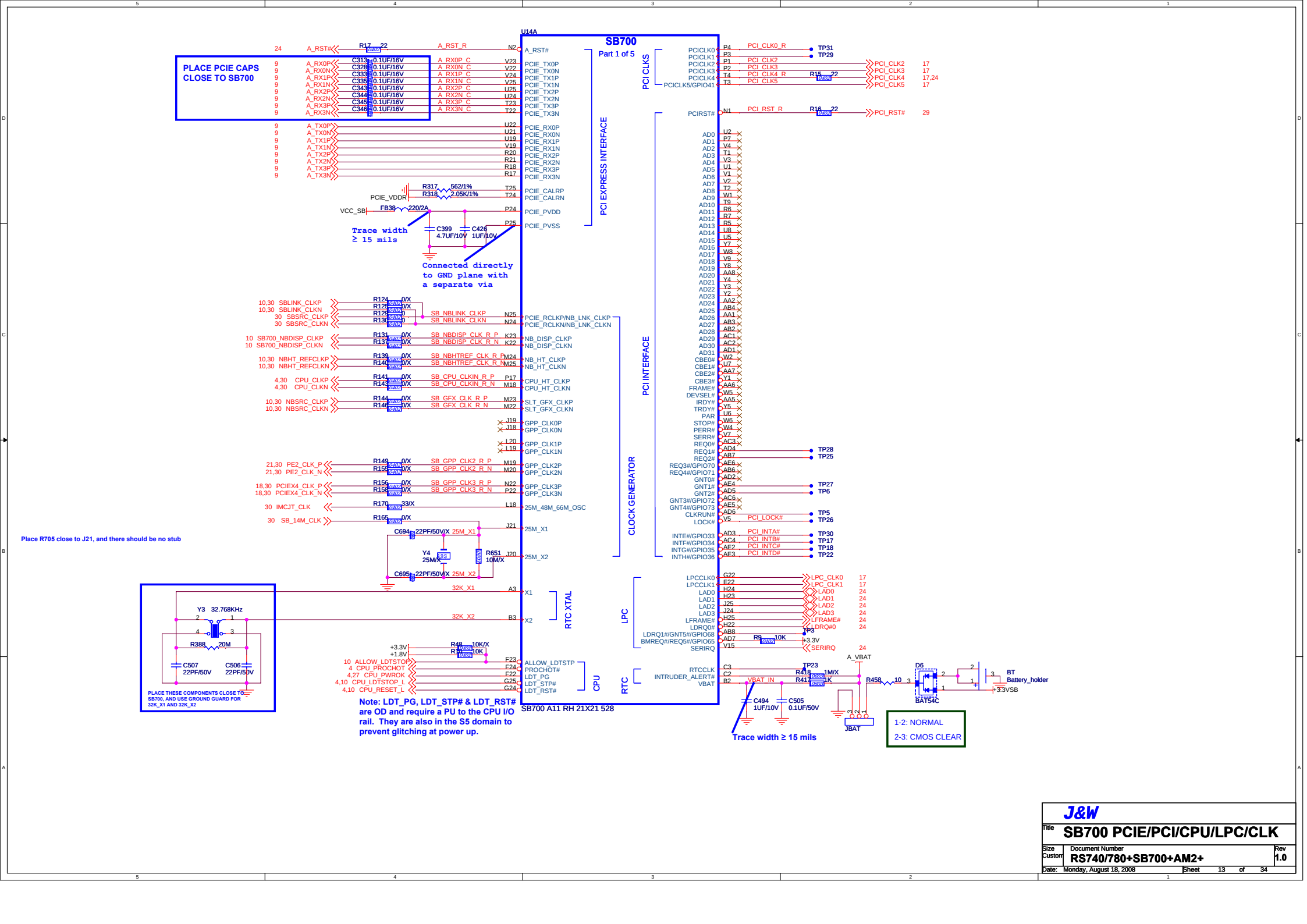
```
Enables Side port memory
1.  Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS740:  pin DFT_GPIO0
RS780:  pin HSYNC
RX780:  Not Appicable
```

RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

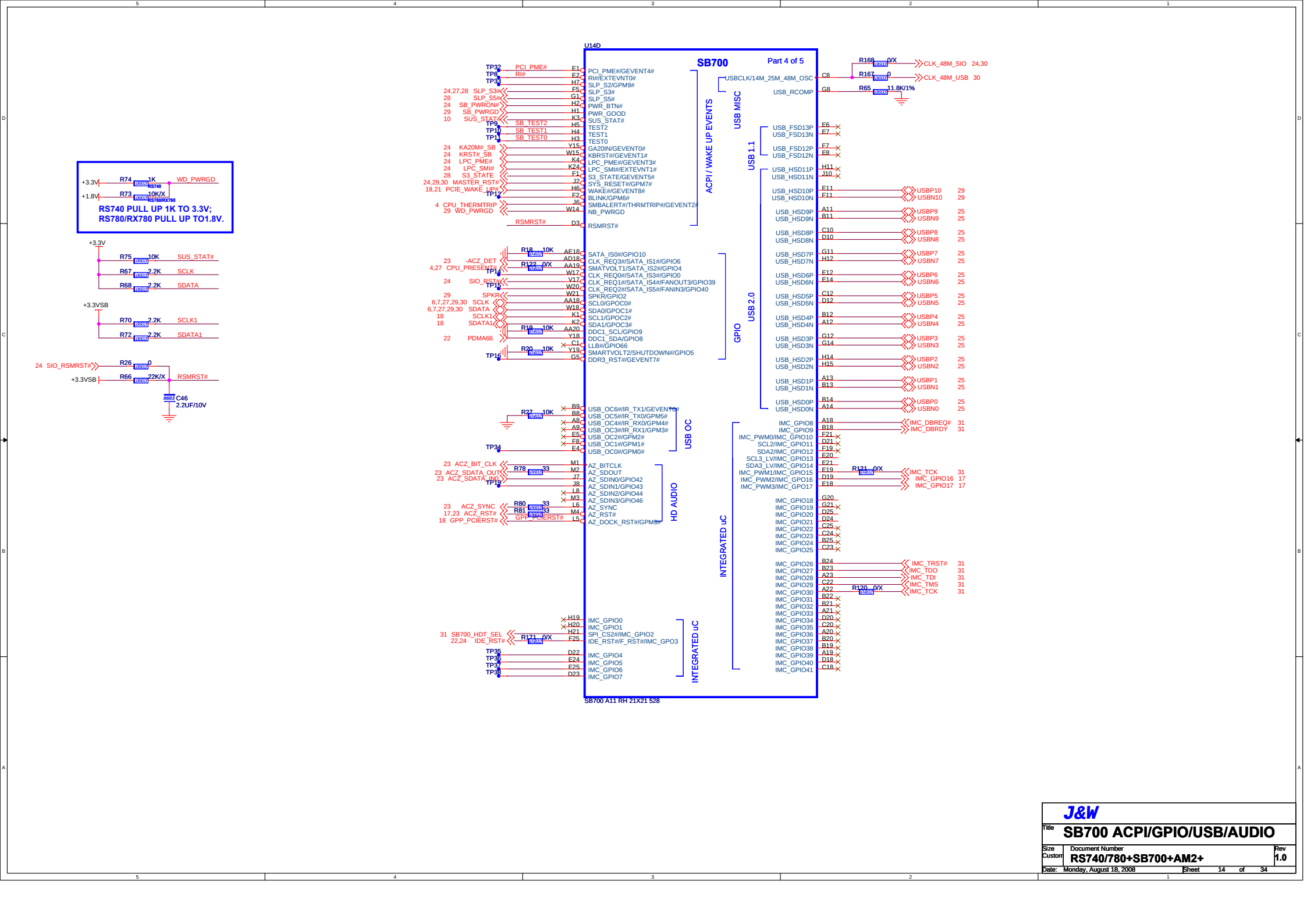
```
Enables Test debug bus
using PCIE bus
1.  Disable (can be enabled
     thru nbcfg register)
0 : Enable
RX780: pin DFT_GPIO0
RS780: configurable thru register
          setting only
RS740: Not supported
```

RED C48

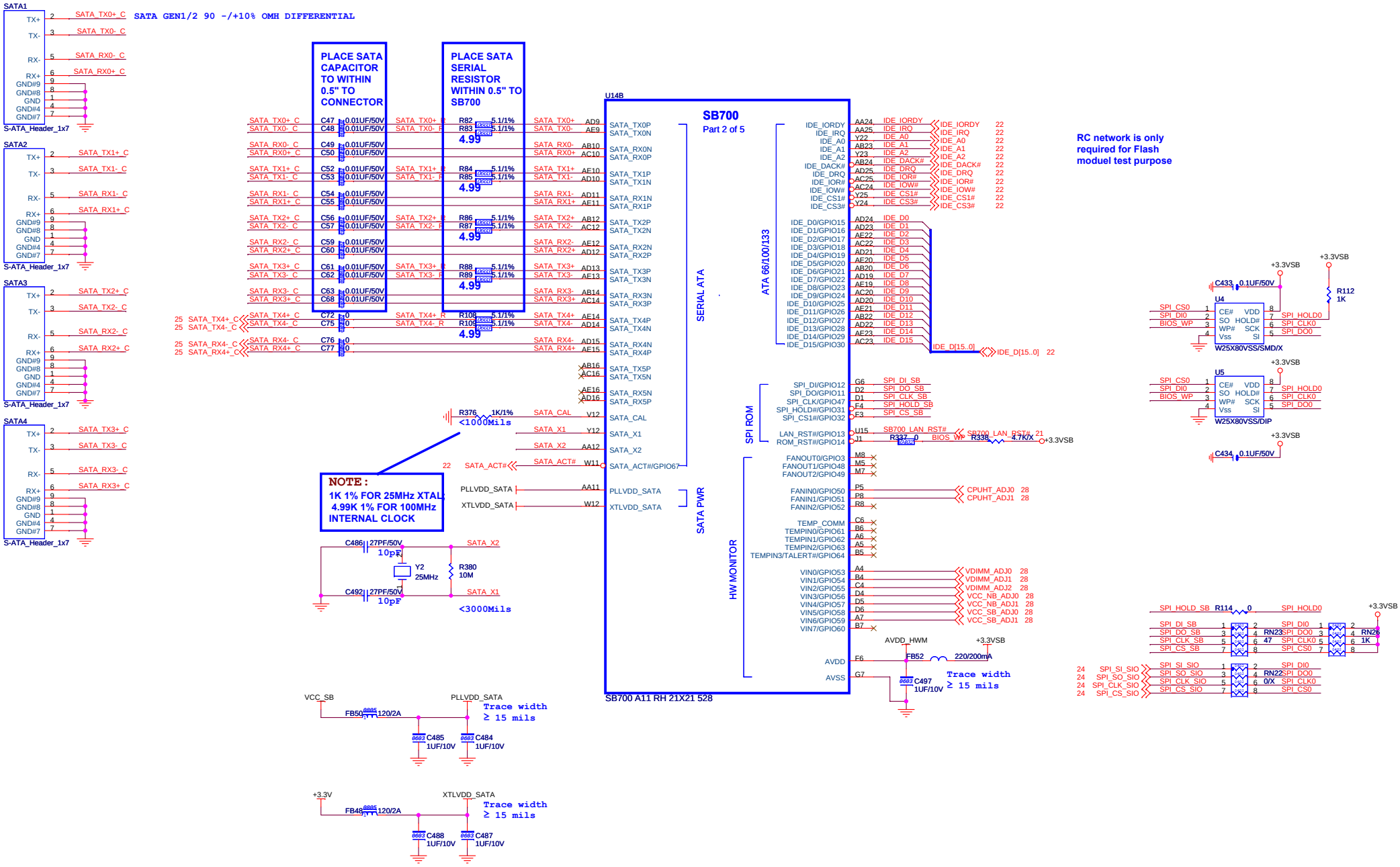
J&W		
Title: RS740/780 STARPS		
Size: Custom	Document Number: RS740/780+SB700+AM2+	Rev: 1.0
Date: Monday, August 18, 2008	Sheet 12 of 34	



J&W		
Title	SB700 PCIE/PCI/CPU/LPC/CLK	
Size: Custom	Document Number: RS740/780+SB700+AM2+	Rev: 1.0
Date: Monday, August 18, 2008	Sheet 13 of 34	



J&W			
Title	SB700 ACPI/GPIO/USB/AUDIO		
Size: Custom	Document Number: RS740/780+SB700+AM2+		Rev: 1.0
Date: Monday, August 18, 2008	Sheet 14 of 34		


SATA1
SATA2
SATA3
SATA4
S-ATA_Header_1x7
SATA GEN1/2 90 -/+10% OMH DIFFERENTIAL
PLACE SATA CAPACITOR TO WITHIN 0.5" TO CONNECTOR
PLACE SATA SERIAL RESISTOR WITHIN 0.5" TO SB700
U14B
SB700
Part 2 of 5
SERIAL ATA
SATA PWR
ATA 66/100/133
SPI ROM
HW MONITOR
SB700 A11 RH 21X21 528
RC network is only required for Flash moduel test purpose
NOTE :
1K 1% FOR 25MHz XTAL
4.99K 1% FOR 100MHz
INTERNAL CLOCK
Trace width ≥ 15 mils
W25X80VSS/SMD/X
W25X80VSS/DIP
+3.3VSB
AVDD_HWM
FB52 220/200mA
C497 1UF/10V
C485 1UF/10V
C484 1UF/10V
C488 1UF/10V
C487 1UF/10V
Y2 25MHz
R380 10M
C486 27PF/50V 10pF
C492 27PF/50V 10pF
SATA_X2
SATA_X1
<3000Mils
<1000Mils
SATA_CAL
SATA_ACT#
PLLVDD_SATA
XTLVDD_SATA
VCC_SB
+3.3V
FB50 120/2A
FB48 120/2A
J&W
SB700 SATA/IDE/HWM/SPI
Size Custom
Document Number RS740/780+SB700+AM2+
Rev 1.0
Date: Monday, August 18, 2008
Sheet 15 of 34

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

Connected directly to the power plane

1.8V: Flash module mode
3.3V: IDE mode

Trace width ≥ 50 mils

Trace width ≥ 100 mils

Trace width ≥ 50 mils

Trace width ≥ 50 mils (25 mils for AVDDTX and 25 mils for AVDDRX) or to power plane

Connected directly to the power plane with width ≥ 100 mils

Trace width ≥ 30 mils

Trace width ≥ 20 mils or to power plane

Trace width ≥ 15 mils

Trace width ≥ 10 mils

Trace width ≥ 15 mils

Trace width ≥ 15 mils

Trace width ≥ 15 mils

Trace width ≥ 15 mils with 10 mils spacing to other nets

U14C

SB700

Part 3 of 5

POWER

PCI/GPIO I/O

CORE S0

IDE/FLSH I/O

CLKGEN I/O

A-LINK I/O

3.3V_S5 I/O

CORE S5

SATA I/O

USB I/O

PLL

SB700 A11 RH 21X21 528

U14E

SB700

GROUND

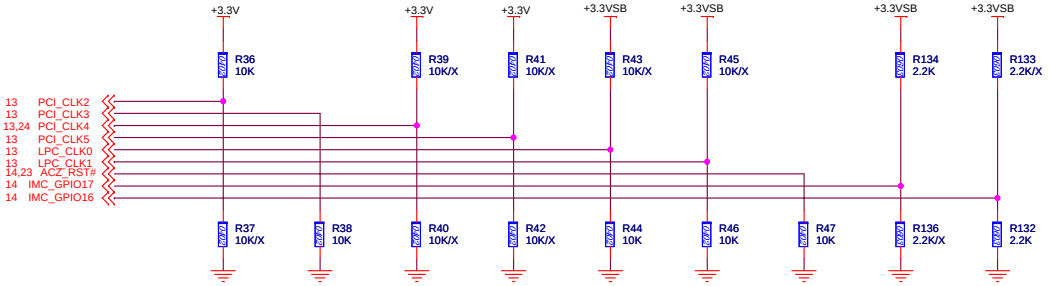
Part 5 of 5

SB700 A11 RH 21X21 528

Title	SB700 POWER & DECOUPLING
Size	Custom
Document Number	RS740/780+SB700+AM2+
Rev	1.0
Date:	Monday, August 18, 2008
Sheet	16 of 34

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, H = Reserved	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT

A12
1=IMC ENABLED
0=IMC DISABLED

A12
1=ENABLE PCI MEM BOOT
0=DISABLE PCI MEM BOOT

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

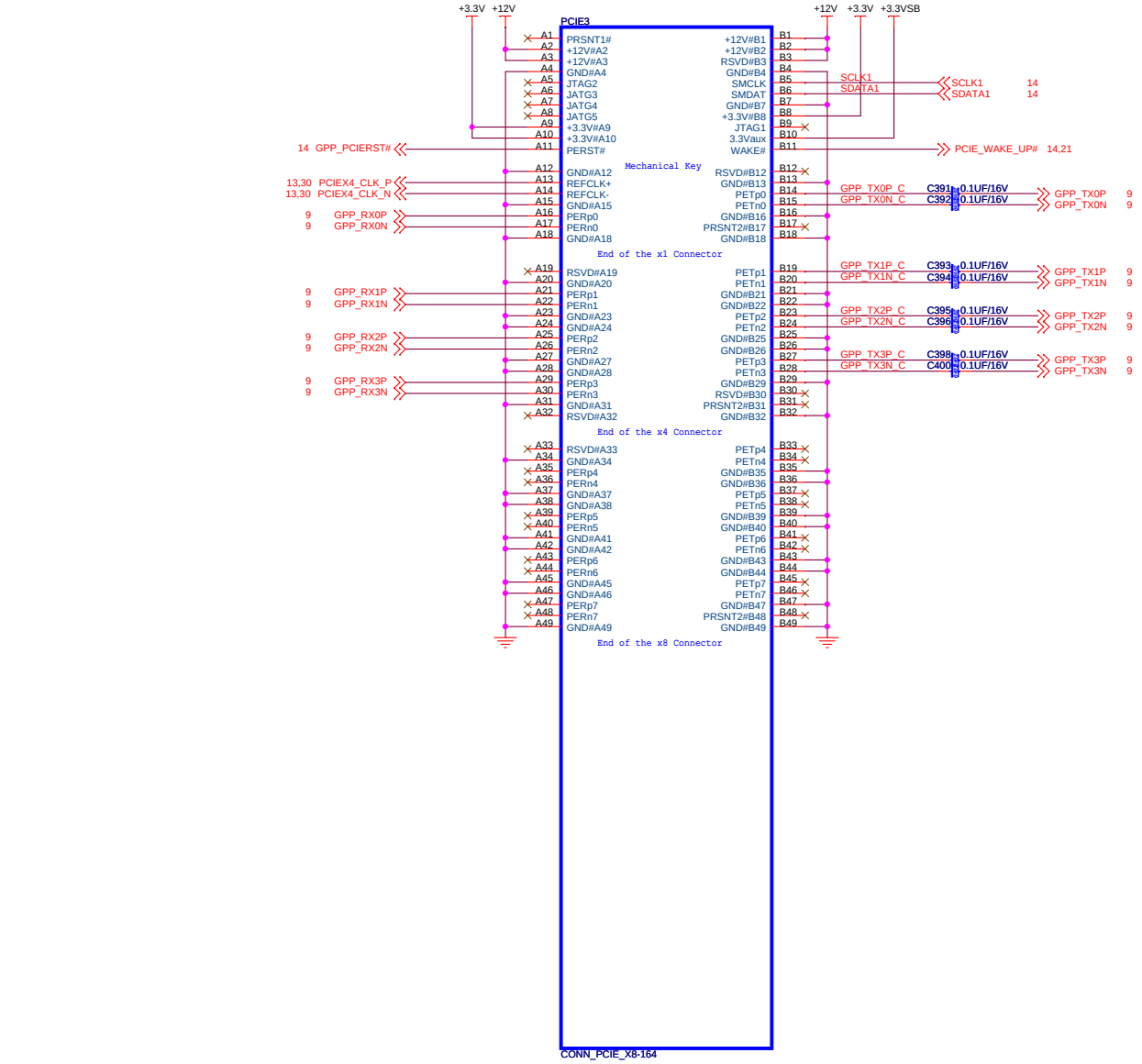
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

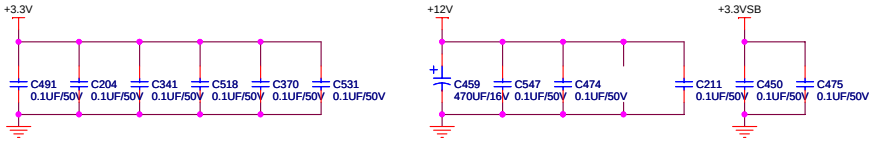
J&W

Title: SB700 STRAPS

Size: Custom | Document Number: RS740/780+SB700+AM2+ | Rev: 1.0

Date: Monday, August 18, 2008 | Sheet 17 of 34



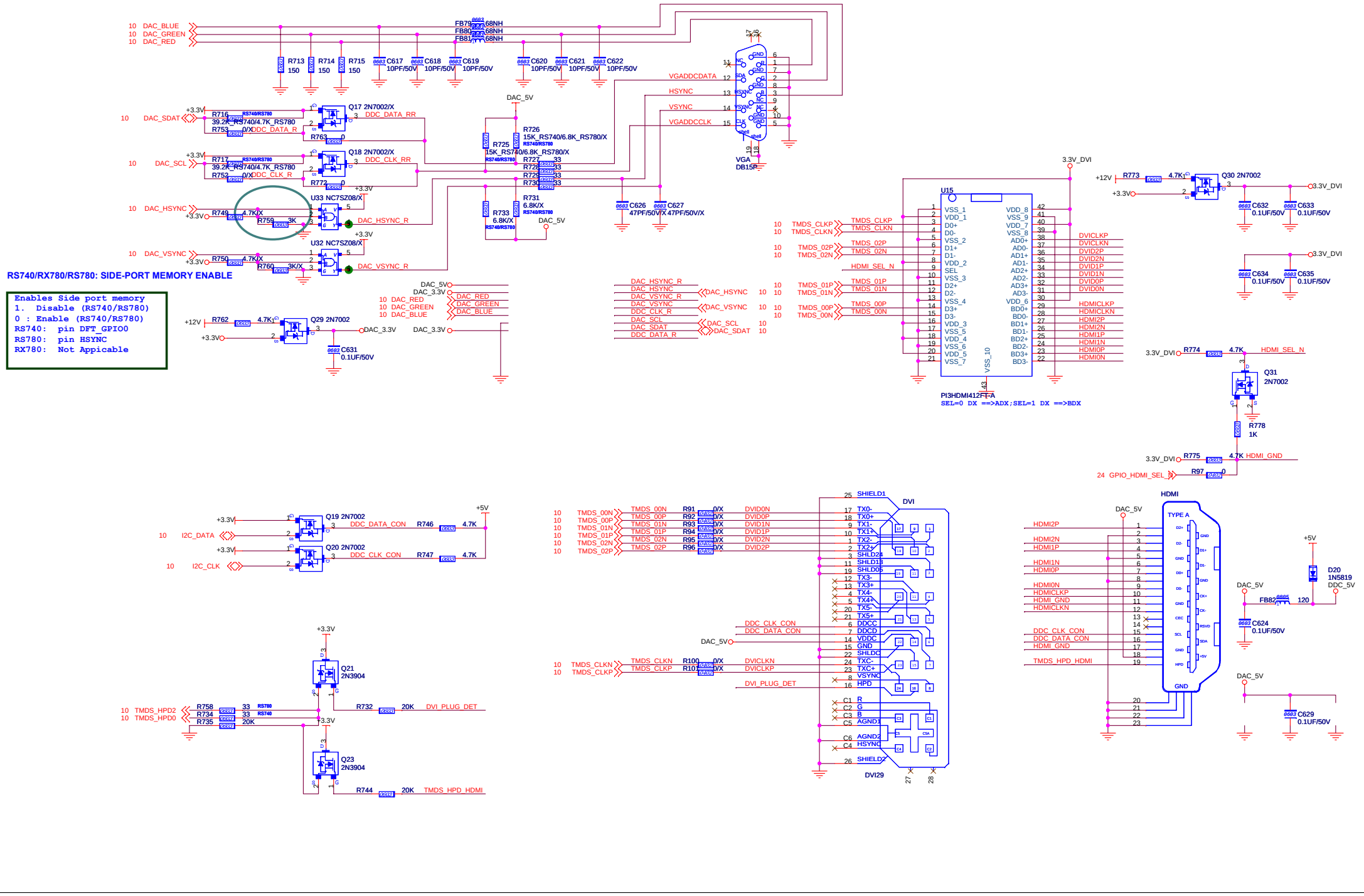


J&W

Title: PCIEX16 SLOT

Size	Document Number	Rev
Custom	RS740/780+SB700+AM2+	1.0

Date: Monday, August 18, 2008 Sheet 18 of 34

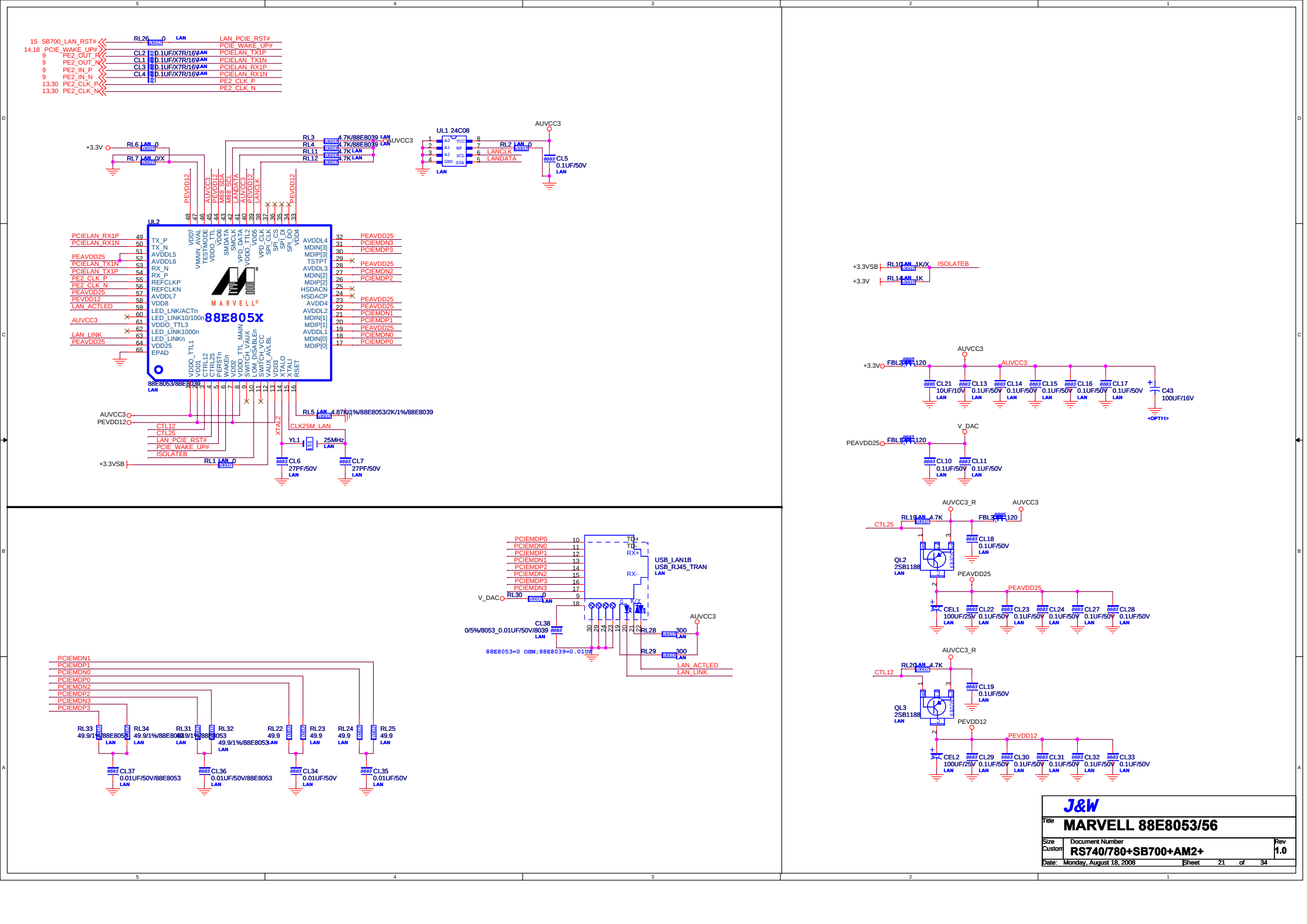

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE
Enables Side port memory
1. Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS740: pin DFT_GPIO0
RS780: pin HSYNC
RX780: Not Appicable
DAC_BLUE
DAC_GREEN
DAC_RED
DAC_SDAT
DAC_SCL
DAC_HSYNC
DAC_VSYNC
VGADDCDATA
HSYNC
VSYNC
VGADDCCLK
VGA DB15P
DDC_DATA_RR
DDC_CLK_RR
DAC_HSYNC_R
DAC_VSYNC_R
DAC_5V
DAC_3.3V
PI3HDMI412FT-A
SEL=0 DX ==>ADX;SEL=1 DX ==>BDX
HDMI_SEL_N
HDMI_GND
GPIO_HDMI_SEL
I2C_DATA
I2C_CLK
DDC_DATA_CON
DDC_CLK_CON
DVI_PLUG_DET
TMDS_HPD_HDMI
DVI
HDMI
TYPE A
DVI29

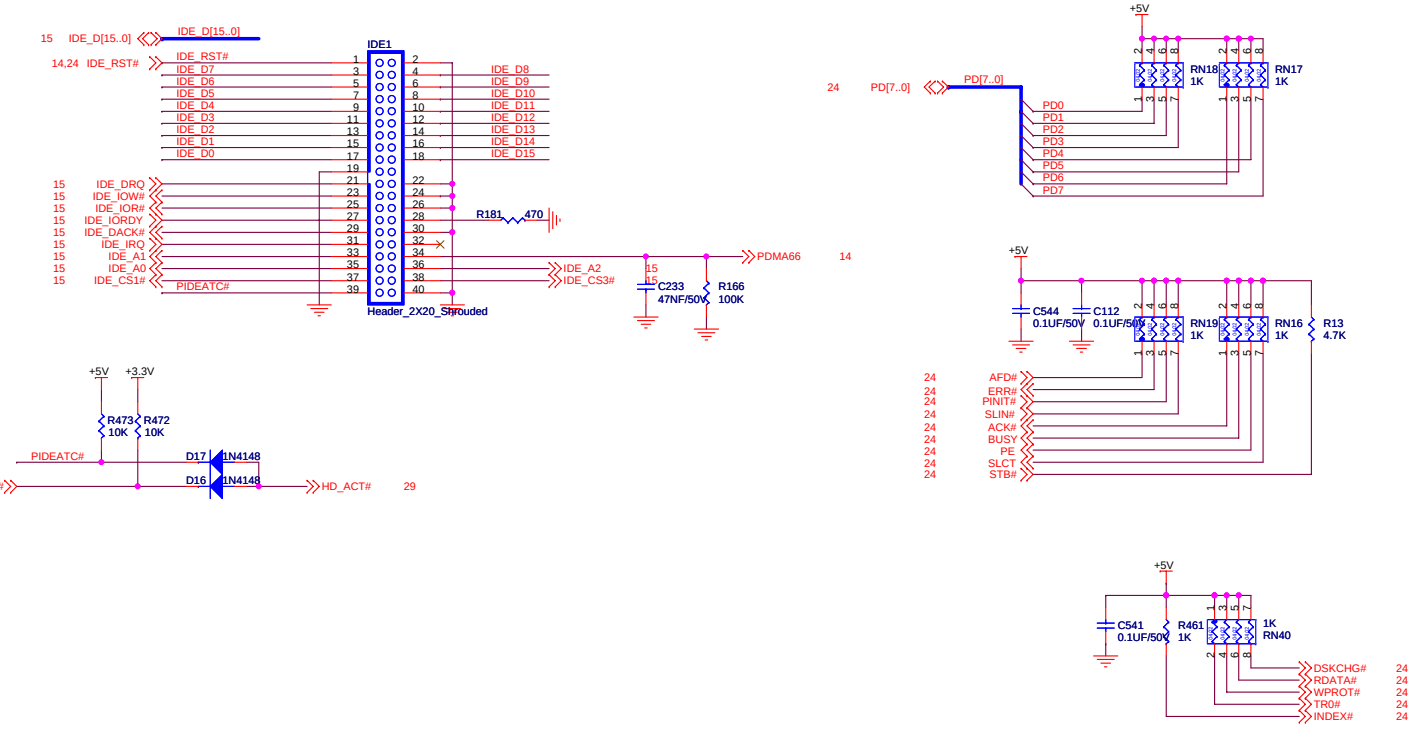
J&W

Title: PCI TSB43AB22A 1394

Size: Custom | Document Number: RS740/780+SB700+AM2+ | Rev: 1.0

Date: Monday, August 18, 2008 | Sheet 20 of 34


15 SB700_LAN_RST#
14,18 PCIE_WAKE_UP#
9 PE2_OUT_P
9 PE2_OUT_N
9 PE2_IN_P
9 PE2_IN_N
13,30 PE2_CLK_P
13,30 PE2_CLK_N
RL26 0 LAN
LAN_PCIE_RST#
PCIE_WAKE_UP#
CL2 0.1UF/X7R/16V LAN
CL1 0.1UF/X7R/16V LAN
CL3 0.1UF/X7R/16V LAN
CL4 0.1UF/X7R/16V LAN
PCIELAN_TX1P
PCIELAN_TX1N
PCIELAN_RX1P
PCIELAN_RX1N
PE2_CLK_P
PE2_CLK_N
+3.3V
RL6 LAN_0
RL7 LAN_0/X
RL3 4.7K/88E8039 LAN
RL4 4.7K/88E8039 LAN
RL11 4.7K LAN
RL12 4.7K LAN
AUVCC3
UL1 24C08
RL2 LAN_0
LANCLK
LANDATA
CL5 0.1UF/50V LAN
PEVDD12
AUVCC3
M68_SCL
M68_SDA
SMCLK
SMDATA
VPD_DATA
VPD_CLK
SPI_CS
SPI_DI
SPI_DO
UL2
PCIELAN_RX1P
PCIELAN_RX1N
PEAVDD25
PCIELAN_TX1N
PCIELAN_TX1P
PE2_CLK_P
PE2_CLK_N
REFCLKP
REFCLKN
PEAVDD25
PEVDD12
LAN_ACTLED
AUVCC3
LAN_LINK
PEAVDD25
TX_P
TX_N
AVDDL5
AVDDL6
RX_N
RX_P
REFCLKP
REFCLKN
AVDDL7
VDD8
LED_LNK/ACTn
LED_LINK10/100n
VDDO_TTL3
LED_LINK1000n
LED_LINKn
VDD25
EPAD
MARVELL
88E805X
88E8053/88E8039
LAN
AVDDL4
MDIN[3]
MDIP[3]
TSTP1
AVDDL3
MDIN[2]
MDIP[2]
HSDACN
HSDACP
AVDD4
AVDDL2
MDIN[1]
MDIP[1]
AVDDL1
MDIN[0]
MDIP[0]
PEAVDD25
PCIEMDN3
PCIEMDP3
PEAVDD25
PCIEMDN2
PCIEMDP2
PEAVDD25
PEAVDD25
PCIEMDN1
PCIEMDP1
PEAVDD25
PCIEMDN0
PCIEMDP0
AUVCC3
PEVDD12
CTL12
CTL25
LAN_PCIE_RST#
PCIE_WAKE_UP#
ISOLATEB
RL5 LAN 4.87K/1%/88E8053/2K/1%/88E8039
CLK25M_LAN
YL1
25MHz
LAN
CL6 27PF/50V LAN
CL7 27PF/50V LAN
+3.3VSB
RL1 LAN_0
+3.3VSB
RL10 LAN_1K/X
ISOLATEB
+3.3V
RL14 LAN_1K
AUVCC3
+3.3V
FBL2 120
AUVCC3
CL21 10UF/10V LAN
CL13 0.1UF/50V LAN
CL14 0.1UF/50V LAN
CL15 0.1UF/50V LAN
CL16 0.1UF/50V LAN
CL17 0.1UF/50V LAN
C43 100UF/16V
<OPT11>
V_DAC
PEAVDD25
FBL1 120
CL10 0.1UF/50V LAN
CL11 0.1UF/50V LAN
PCIEMDP0
PCIEMDN0
PCIEMDP1
PCIEMDN1
PCIEMDP2
PCIEMDN2
PCIEMDP3
PCIEMDN3
TD+
TD-
RX+
RX-
USB_LAN1B
USB_RJ45_TRAN
LAN
V_DAC
RL30 0
CL38 0/5%/8053_0.01UF/50V/8039
88E8053=0 OHM;88E8039=0.01UF
RL28 300
RL29 300
AUVCC3
LAN_ACTLED
LAN_LINK
AUVCC3_R
AUVCC3
CTL25
RL19 LAN 4.7K
FBL3 120
CL18 0.1UF/50V
QL2 2SB1188
PEAVDD25
PEAVDD25
CEL1 100UF/25V LAN
CL22 0.1UF/50V LAN
CL23 0.1UF/50V LAN
CL24 0.1UF/50V LAN
CL27 0.1UF/50V LAN
CL28 0.1UF/50V LAN
AUVCC3_R
CTL12
RL20 LAN 4.7K
CL19 0.1UF/50V LAN
QL3 2SB1188
PEVDD12
PEVDD12
CEL2 100UF/25V LAN
CL29 0.1UF/50V LAN
CL30 0.1UF/50V LAN
CL31 0.1UF/50V LAN
CL32 0.1UF/50V LAN
CL33 0.1UF/50V LAN
PCIEMDN1
PCIEMDP1
PCIEMDN0
PCIEMDP0
PCIEMDN2
PCIEMDP2
PCIEMDN3
PCIEMDP3
RL33 49.9/1%/88E8053 LAN
RL34 49.9/1%/88E8053 LAN
RL31 49.9/1%/88E8053 LAN
RL32 49.9/1%/88E8053 LAN
RL22 49.9 LAN
RL23 49.9 LAN
RL24 49.9 LAN
RL25 49.9 LAN
CL37 0.01UF/50V/88E8053 LAN
CL36 0.01UF/50V/88E8053 LAN
CL34 0.01UF/50V LAN
CL35 0.01UF/50V LAN
J&W
Title
MARVELL 88E8053/56
Size Custom
Document Number
RS740/780+SB700+AM2+
Rev 1.0
Date: Monday, August 18, 2008
Sheet 21 of 34

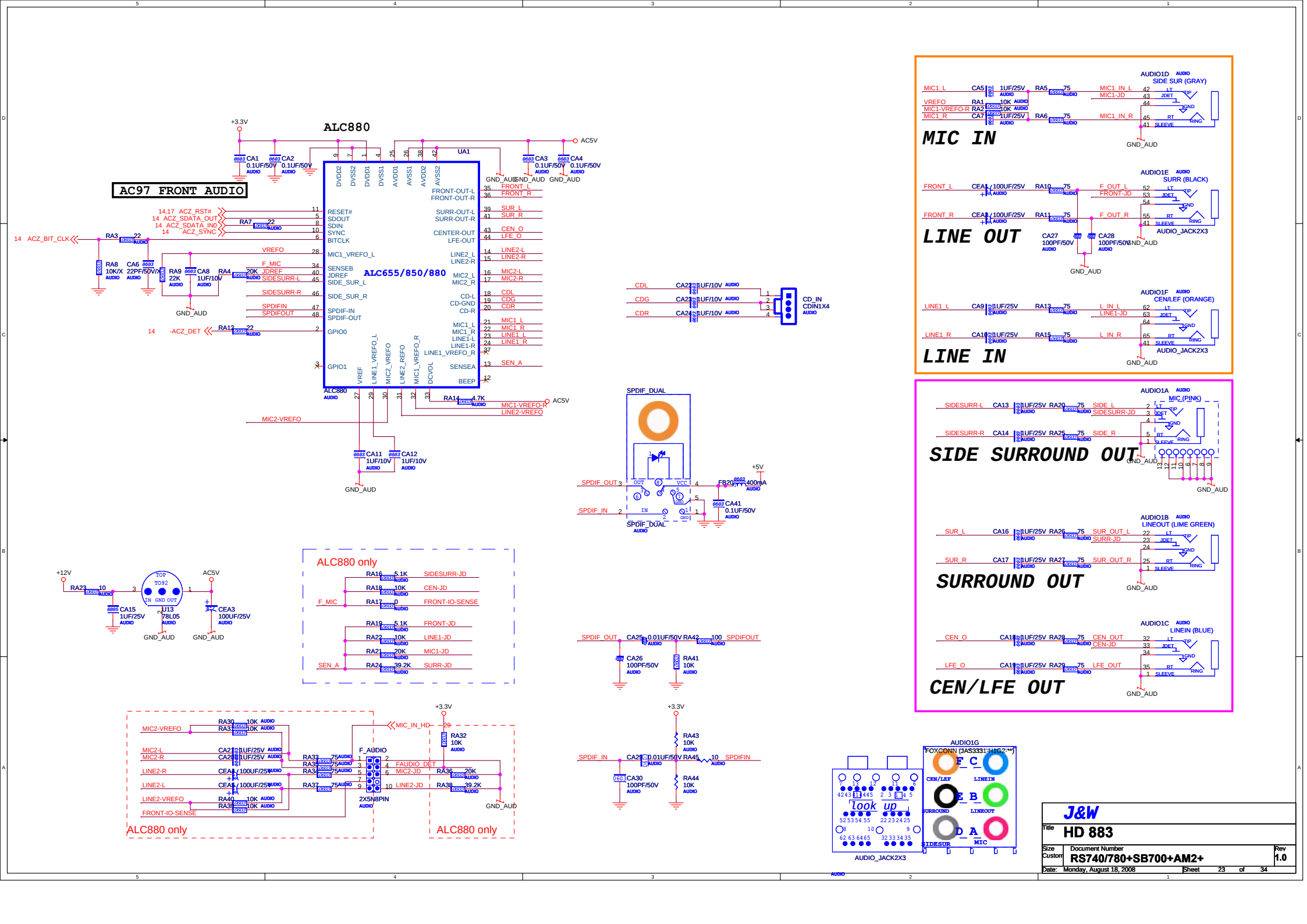


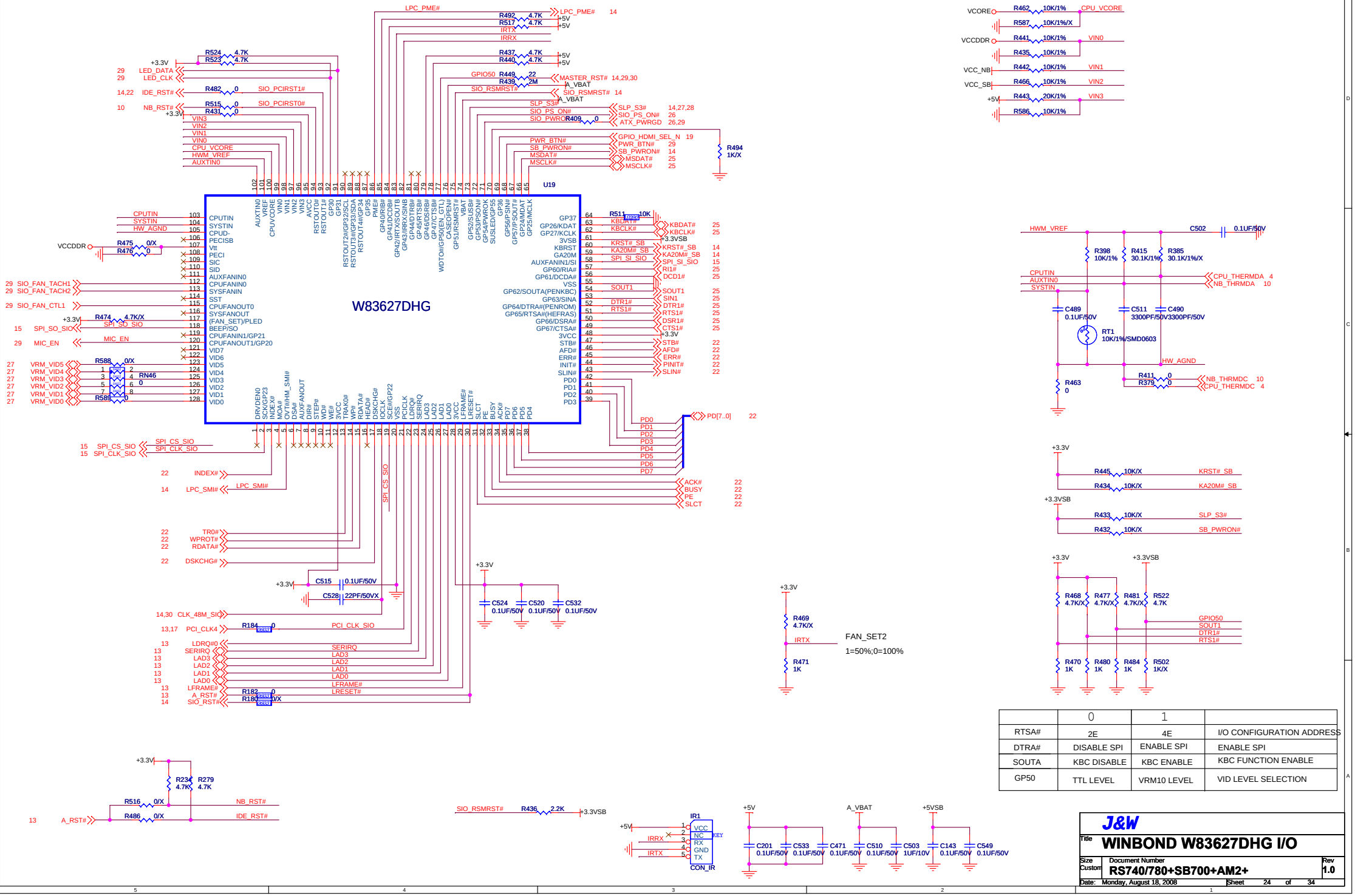
J&W

Title: IDE,FDD,LPT

Size: Custom | Document Number: RS740/780+SB700+AM2+ | Rev: 1.0

Date: Monday, August 18, 2008 | Sheet 22 of 34


ALC880
AC97 FRONT AUDIO
ALC655/850/880
ALC880 only
ALC880 only
ALC880 only
MIC IN
LINE OUT
LINE IN
SIDE SURROUND OUT
SURROUND OUT
CEN/LFE OUT
SPDIF_DUAL
CD_IN
AUDIO_JACK2X3
2X5N8PIN
J&W
HD 883
RS740/780+SB700+AM2+
Monday, August 18, 2008



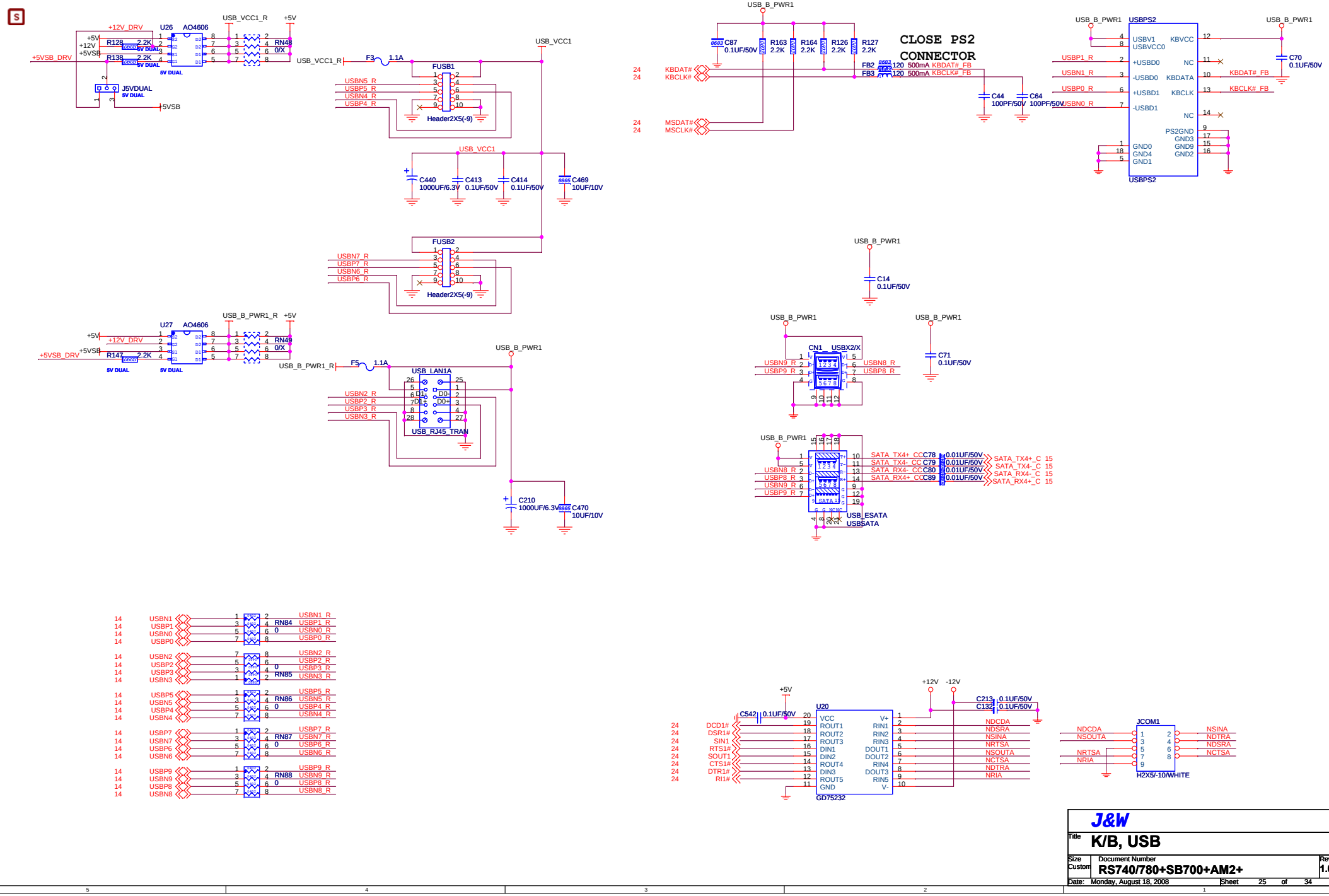
	0	1	
RTSA#	2E	4E	I/O CONFIGURATION ADDRESS
DTRA#	DISABLE SPI	ENABLE SPI	ENABLE SPI
SOUTA	KBC DISABLE	KBC ENABLE	KBC FUNCTION ENABLE
GP50	TTL LEVEL	VRM10 LEVEL	VID LEVEL SELECTION

J&W

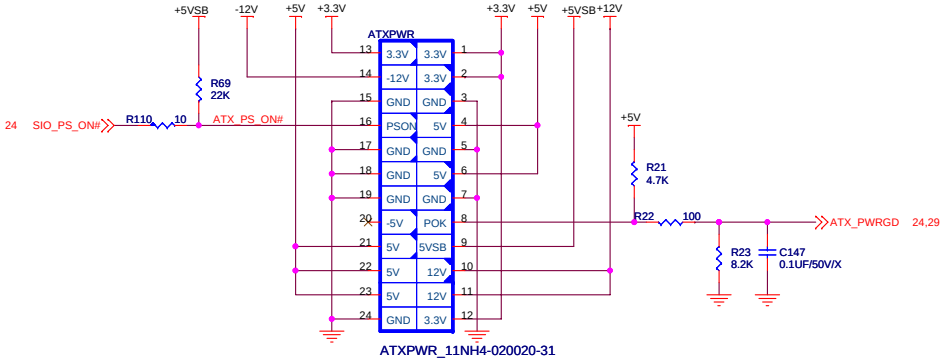
Title: WINBOND W83627DHG I/O

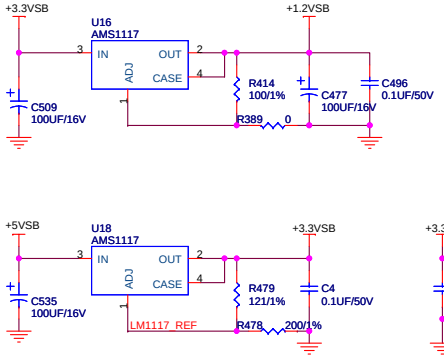
Size: Custom | Document Number: RS740/780+SB700+AM2+ | Rev: 1.0

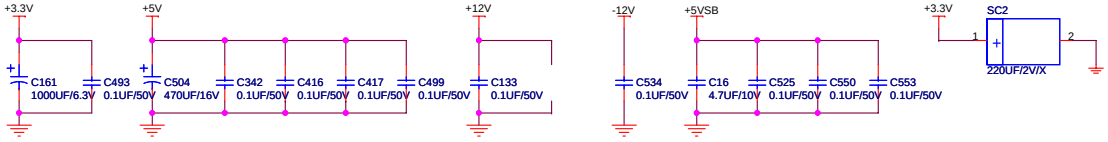
Date: Monday, August 18, 2008 | Sheet 24 of 34

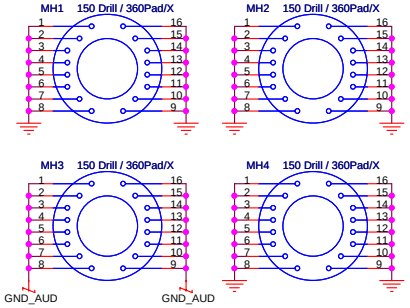


J&W		
Title	K/B, USB	
Size: Custom	Document Number: RS740/780+SB700+AM2+	Rev: 1.0
Date: Monday, August 18, 2008	Sheet 25 of 34	



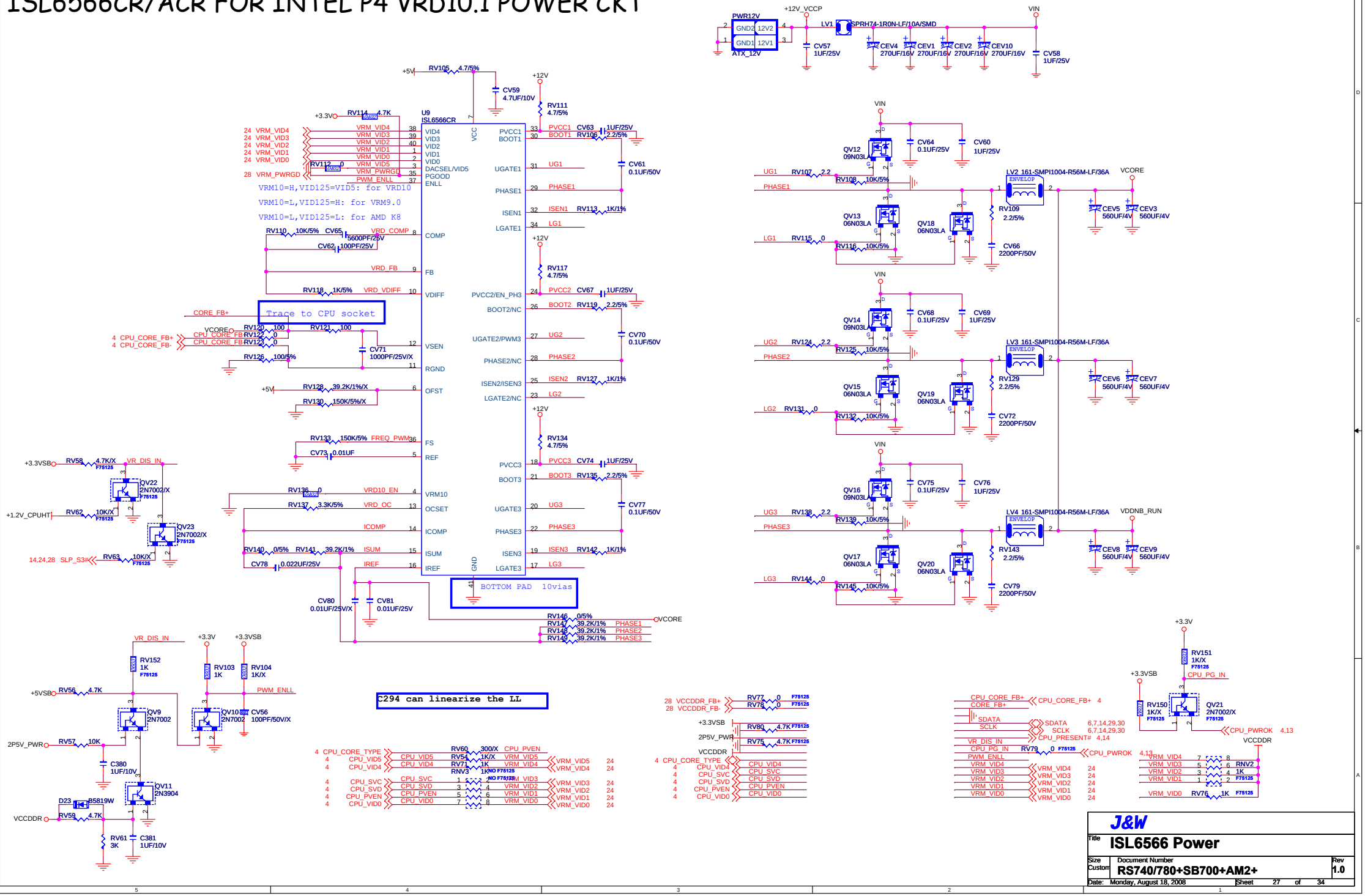


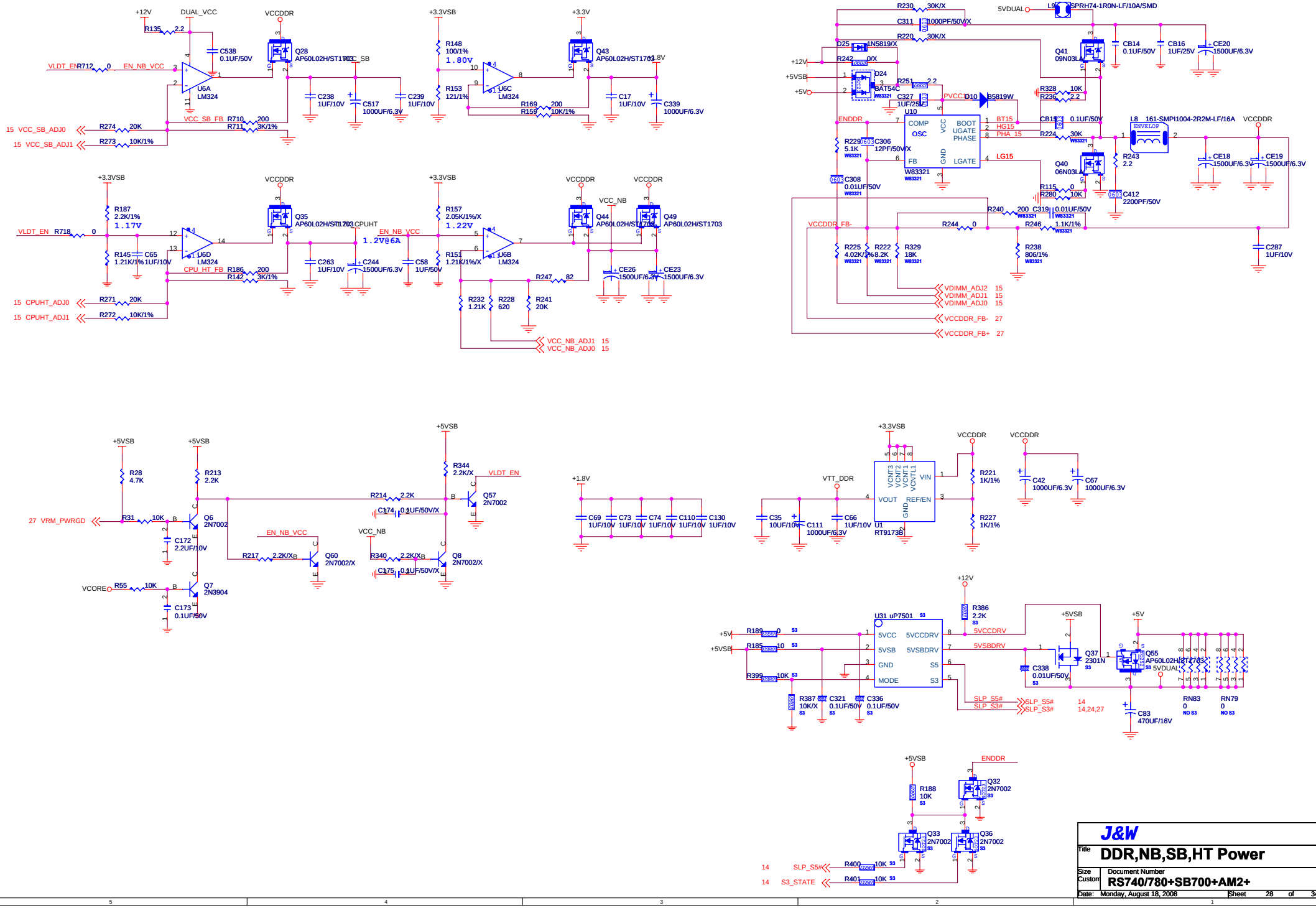




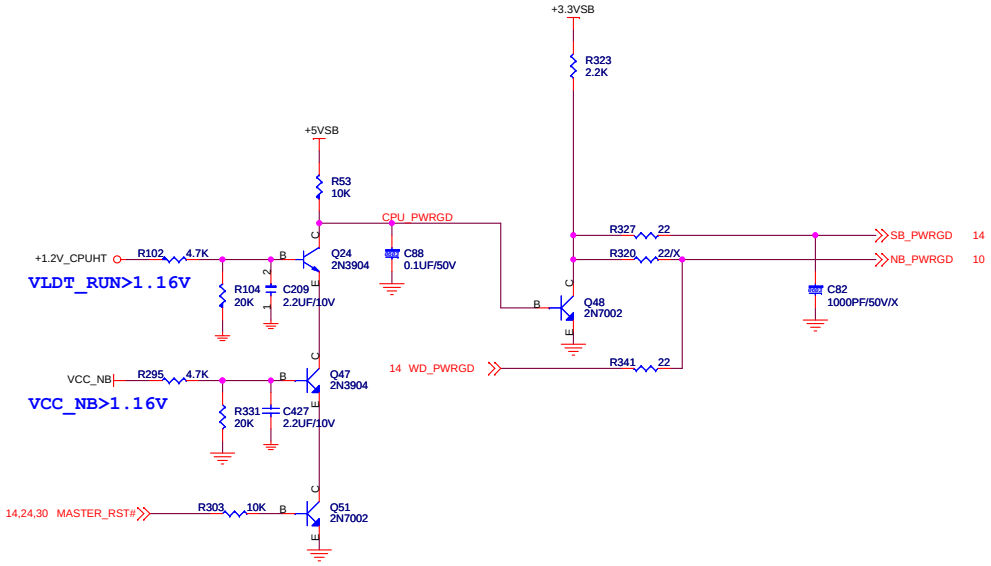
J&W		
Title: ATX CONNECTOR		
Size: Custom	Document Number: RS740/780+SB700+AM2+	Rev: 1.0
Date: Monday, August 18, 2008	Sheet 26 of 34	

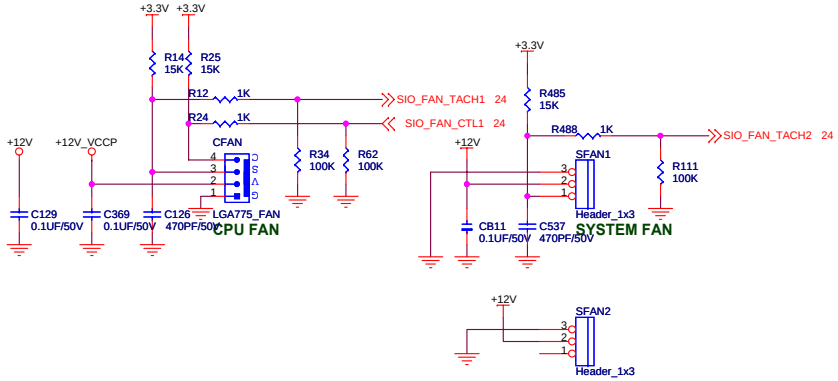
ISL6566CR/ACR FOR INTEL P4 VRD10.1 POWER CKT

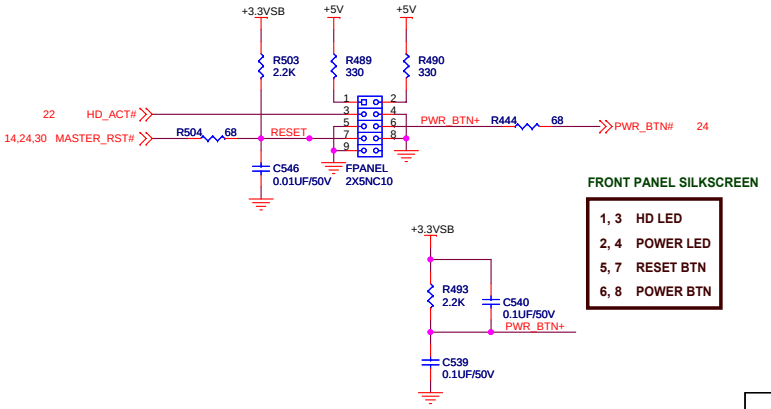


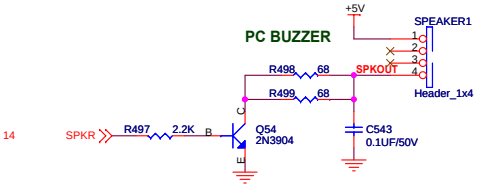

+12V
DUAL_VCC
VCCDDR
R135 2.2
C538 0.1UF/50V
VLDT_EN R712 0 EN_NB_VCC
Q28 AP60L02H/ST1703
VCC_SB
U6A LM324
VCC_SB_FB R710 200 R711 3K/1%
15 VCC_SB_ADJ0
15 VCC_SB_ADJ1
R274 20K
R273 10K/1%
C238 1UF/10V
C517 1000UF/6.3V
C239 1UF/10V
+3.3VSB
R148 100/1% 1.80V
R153 121/1%
U6C LM324
R169 200 R159 10K/1%
+3.3V
Q43 AP60L02H/ST1703
1.8V
C17 1UF/10V
C339 1000UF/6.3V
+3.3VSB
VCCDDR
R187 2.2K/1% 1.17V
VLDT_EN R718 0
U6D LM324
R145 1.21K/1% C65 1UF/10V
CPU_HT_FB R186 200 R142 3K/1%
Q35 AP60L02H/ST1703
CPUHT
1.2V@6A
EN_NB_VCC
C263 1UF/10V
C244 1500UF/6.3V
C58 1UF/50V
+3.3VSB
R157 2.05K/1%/X 1.22V
R151 1.21K/1%/X
U6B LM324
VCCDDR
VCC_NB
Q44 AP60L02H/ST1703
Q49 AP60L02H/ST1703
R247 82
CE26 1500UF/6.3V
CE23 1500UF/6.3V
15 CPUHT_ADJ0
15 CPUHT_ADJ1
R271 20K
R272 10K/1%
R232 1.21K
R228 620
R241 20K
VCC_NB_ADJ1 15
VCC_NB_ADJ0 15
R230 30K/X
C311 1000PF/50V/X
R220 30K/X
5VDUAL
L9 SPRH74-1R0N-LF/10A/SMD
D25 1N5819/X
R242 0/X
+12V
+5VSB
+5V
D24 BAT54C
R251 2.2
C327 1UF/25V
PVCCIO
D10 B5819W
Q41 09N03LA
CB14 0.1UF/50V
CB16 1UF/25V
CE20 1500UF/6.3V
R328 10K
R236 2.2
ENDDR
U10
COMP
OSC
VCC
BOOT
UGATE
PHASE
GND
LGATE
FB
BT15
HG15
PHA_15
LG15
W83321
CB15 0.1UF/50V
L8 161-SMPI1004-2R2M-LF/16A
ENVELOPE
VCCDDR
R224 30K
R229 5.1K
C306 12PF/50V/X
R243 2.2
Q40 06N03LA
CE18 1500UF/6.3V
CE19 1500UF/6.3V
C308 0.01UF/50V
R115 0
R280 10K
C412 2200PF/50V
R240 200 C319 0.01UF/50V
VCCDDR_FB-
R244 0
R246 1.1K/1%
R225 4.02K/1%
R222 8.2K
R329 18K
R238 806/1%
C287 1UF/10V
VDIMM_ADJ2 15
VDIMM_ADJ1 15
VDIMM_ADJ0 15
VCCDDR_FB- 27
VCCDDR_FB+ 27
+5VSB
R28 4.7K
R213 2.2K
27 VRM_PWRGD
R31 10K
Q6 2N7002
C172 2.2UF/10V
VCORE
R55 10K
Q7 2N3904
C173 0.1UF/50V
R214 2.2K
C174 0.1UF/50V/X
EN_NB_VCC
R217 2.2K/X
Q60 2N7002/X
VCC_NB
R340 2.2K/X
Q8 2N7002/X
C175 0.1UF/50V/X
R344 2.2K/X
VLDT_EN
Q57 2N7002
+1.8V
C69 1UF/10V
C73 1UF/10V
C74 1UF/10V
C110 1UF/10V
C130 1UF/10V
+3.3VSB
VTT_DDR
VCNT3
VCNT2
VCNT1
VCNTL1
VIN
VOUT
REF/EN
GND
U1 RT9173B
C35 10UF/10V
C111 1000UF/6.3V
C66 1UF/10V
R221 1K/1%
R227 1K/1%
VCCDDR
C42 1000UF/6.3V
C67 1000UF/6.3V
+12V
+5V
+5VSB
R189 0
R185 10
R399 10K
U31 uP7501
5VCC
5VSB
GND
MODE
5VCCDRV
5VSBDRV
S5
S3
R386 2.2K
5VCCDRV
5VSBDRV
R387 10K/X
C321 0.1UF/50V
C336 0.1UF/50V
SLP_S5#
SLP_S3#
Q37 2301N
C338 0.01UF/50V
Q55 AP60L02H/ST1703
5VDUAL
C83 470UF/16V
RN83 0
RN79 0
14 SLP_S5#
14 S3_STATE
R400 10K
R401 10K
R188 10K
Q32 2N7002
Q33 2N7002
Q36 2N7002
J&W
Title
DDR,NB,SB,HT Power
Size Custom
Document Number
RS740/780+SB700+AM2+
Rev 1.0
Date: Monday, August 18, 2008
Sheet 28 of 34

RESET, FANS & SPKR



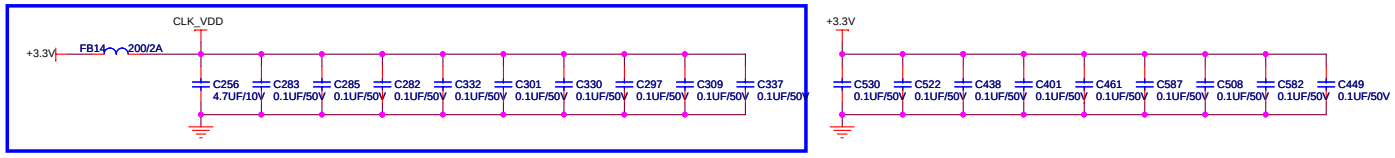






J&W

Title	F_Panel, PWR_GD	
Size: Custom	Document Number: RS740/780+SB700+AM2+	Rev: 1.0
Date: Monday, August 18, 2008	Sheet 29 of 34	

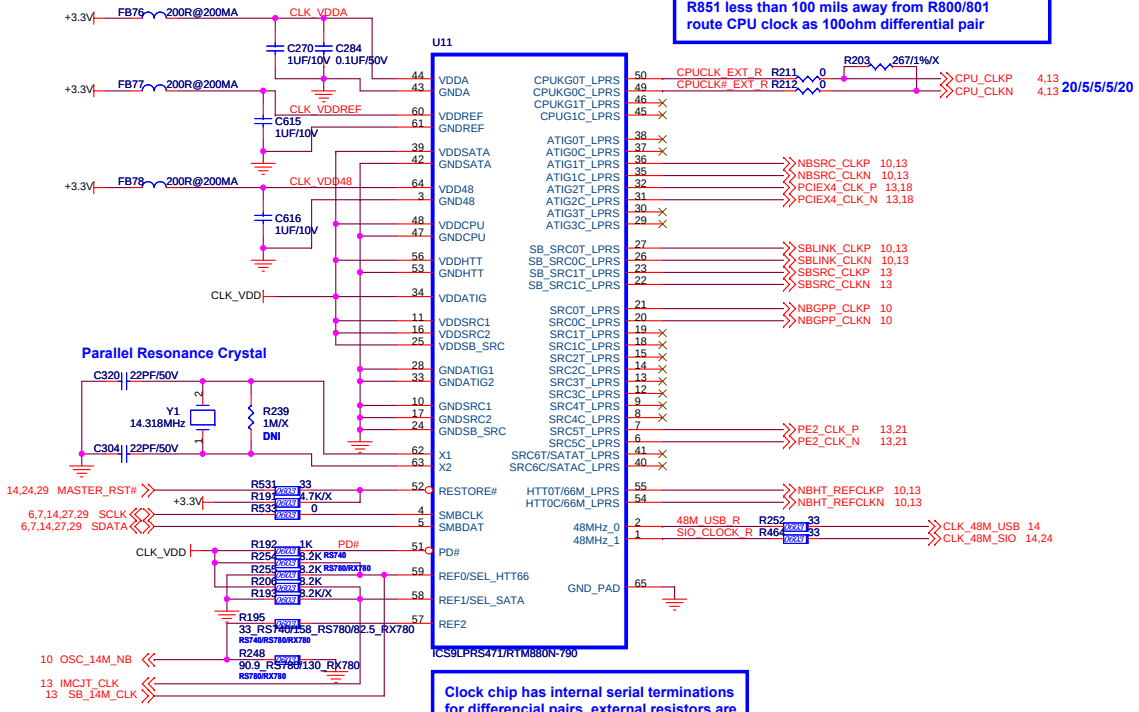


1- PLACE ALL THE SERIES TERMINATION RESISTORS
AS CLOSE TO ICS9LPRS472 AS POSSIBLE

2- ROUTE ALL SRCCLKTx AND SRCCLKCx
AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TOICS9LPRS472
POWER PIN

Place R211/212 less than 500 mils away from ICS
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLCOK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLCOK

FSB4	FSB3	FSB2	FSB1	FSB0	CPU	HTT(single) SEL_HTT=1	HTT(Differential) SEL_HTT=0	VCO	SRC	ATiG[3:0]	SB_SRC
0	1	1	1	1	200M	66M	100M	600M	100M	100M	100M

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases

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Title: RS740/780 CLOCK Gen

Size: Custom | Document Number: RS740/780+SB700+AM2+ | Rev: 1.0

Date: Monday, August 18, 2008 | Sheet 30 of 34