RS740/780+SB700+AM2G2

LiuZH Confidential

REV 1.0 Update: MAY 14,2007

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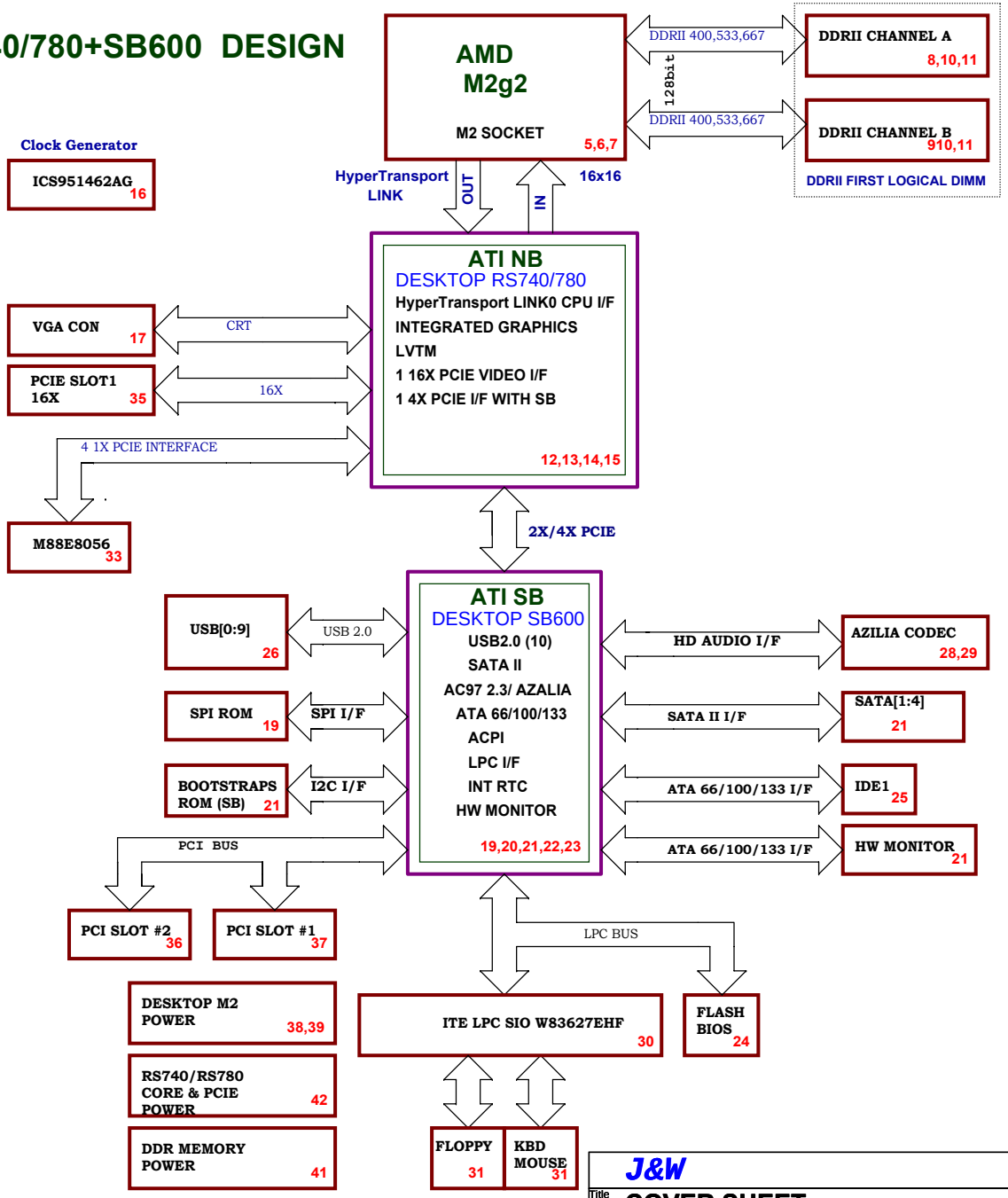
Rs740/780+SB600 DESIGN



J&W

Title: COVER SHEET

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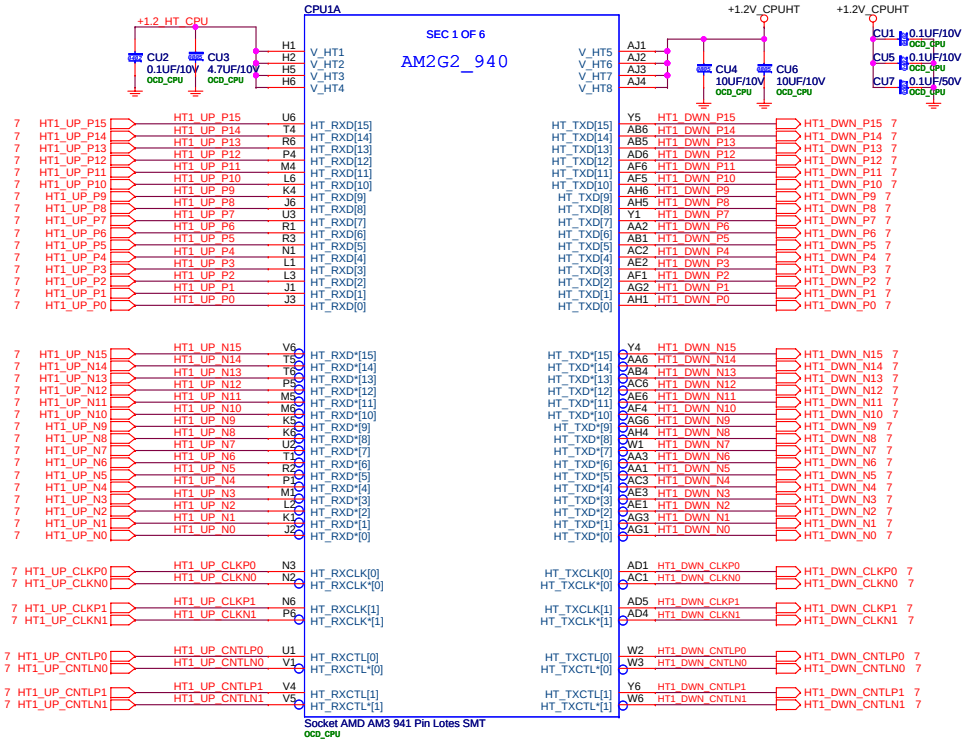
Clawhammer HT Interface

LAYOUT: Place HT bypass caps on topside
near unconnected Clawhammer HT Link



R106 AND R107 MUST BE NEAR CPU AND PADS NEED ON CTL TRACE TO AVOID STUB

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Title: AM2+ HT I/F			
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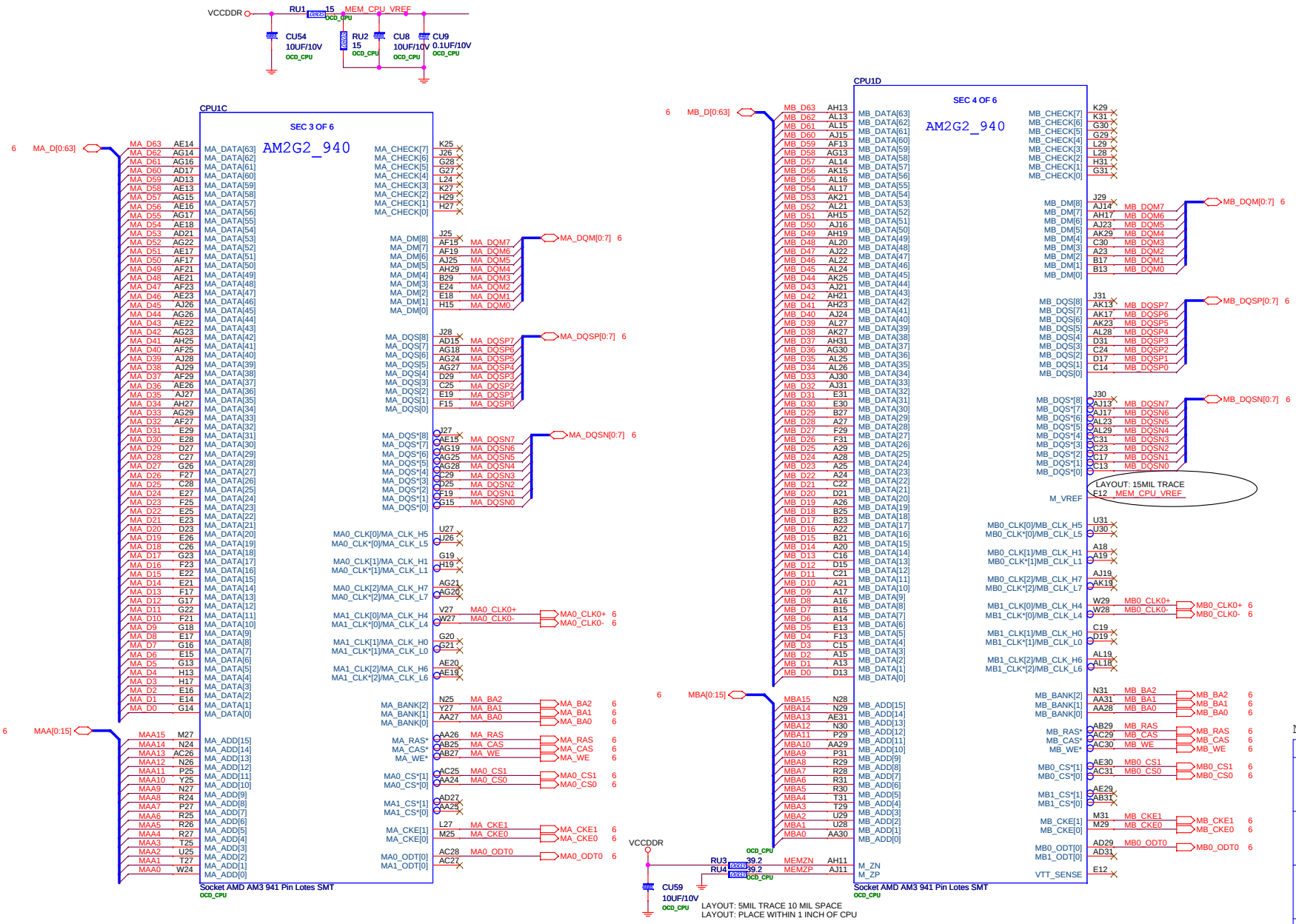
Clawhammer DDR Interface



MEMORY CLOCK TRANSLATION

DIMM	DDR3 Memory Signal	CPU Signal
DIMM A0	MEM_MA0_CLK1	MA_CLK2
	MEM_MA0_CLK0	MA_CLK4
DIMM A1	MEM_MA1_CLK1	MA_CLK5
	MEM_MA1_CLK0	MA_CLK3
DIMM B0	MEM_MB0_CLK1	MB_CLK2
	MEM_MB0_CLK0	MB_CLK4
DIMM B1	MEM_MB1_CLK1	MB_CLK5
	MEM_MB1_CLK0	MB_CLK3

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Title: AM2+ DDRII I/F

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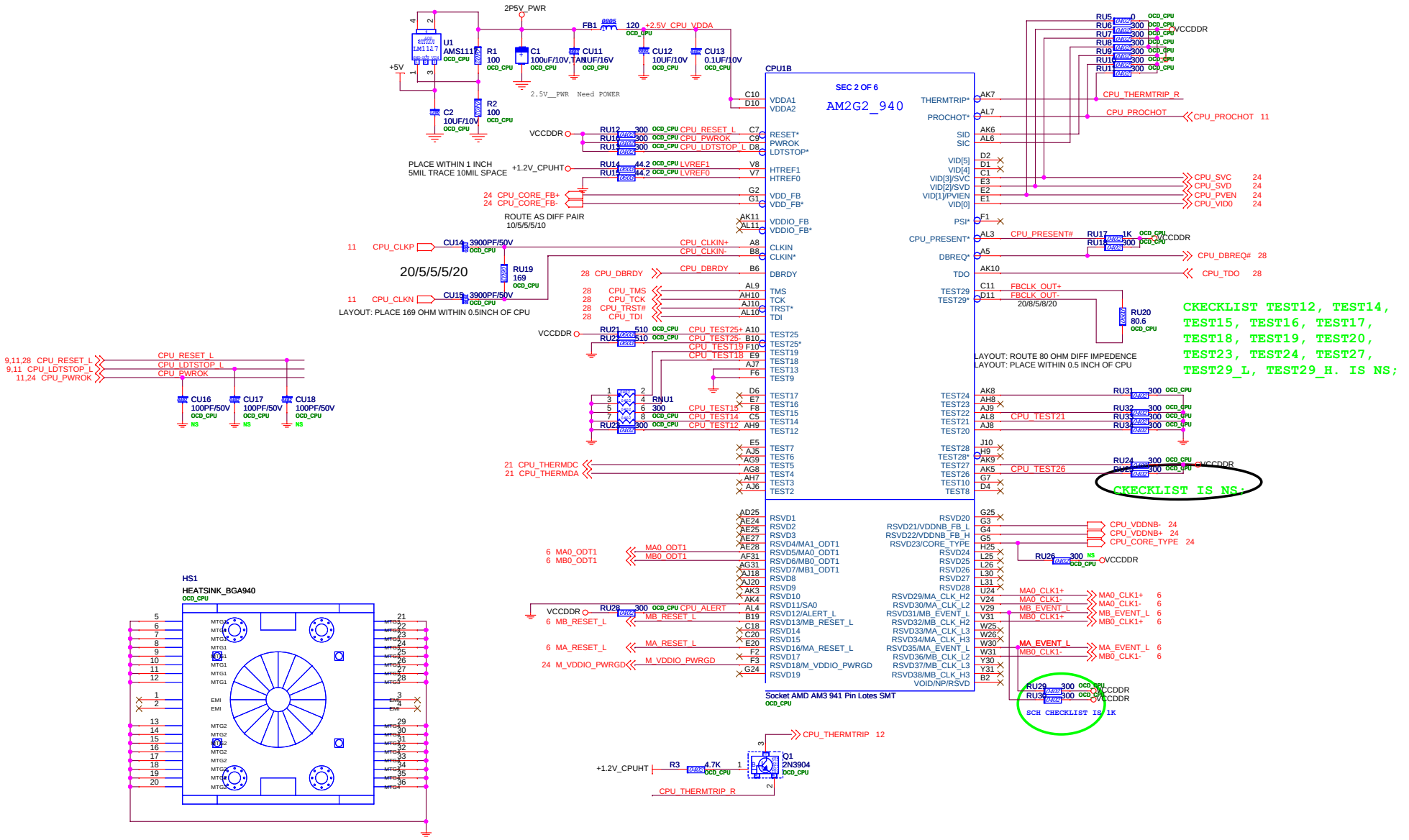

J&W			
Title	AM2+ CNTL/MISC I/F		
Size: Custom	Document Number: RS880+SB850+AM3		Rev: 1.0
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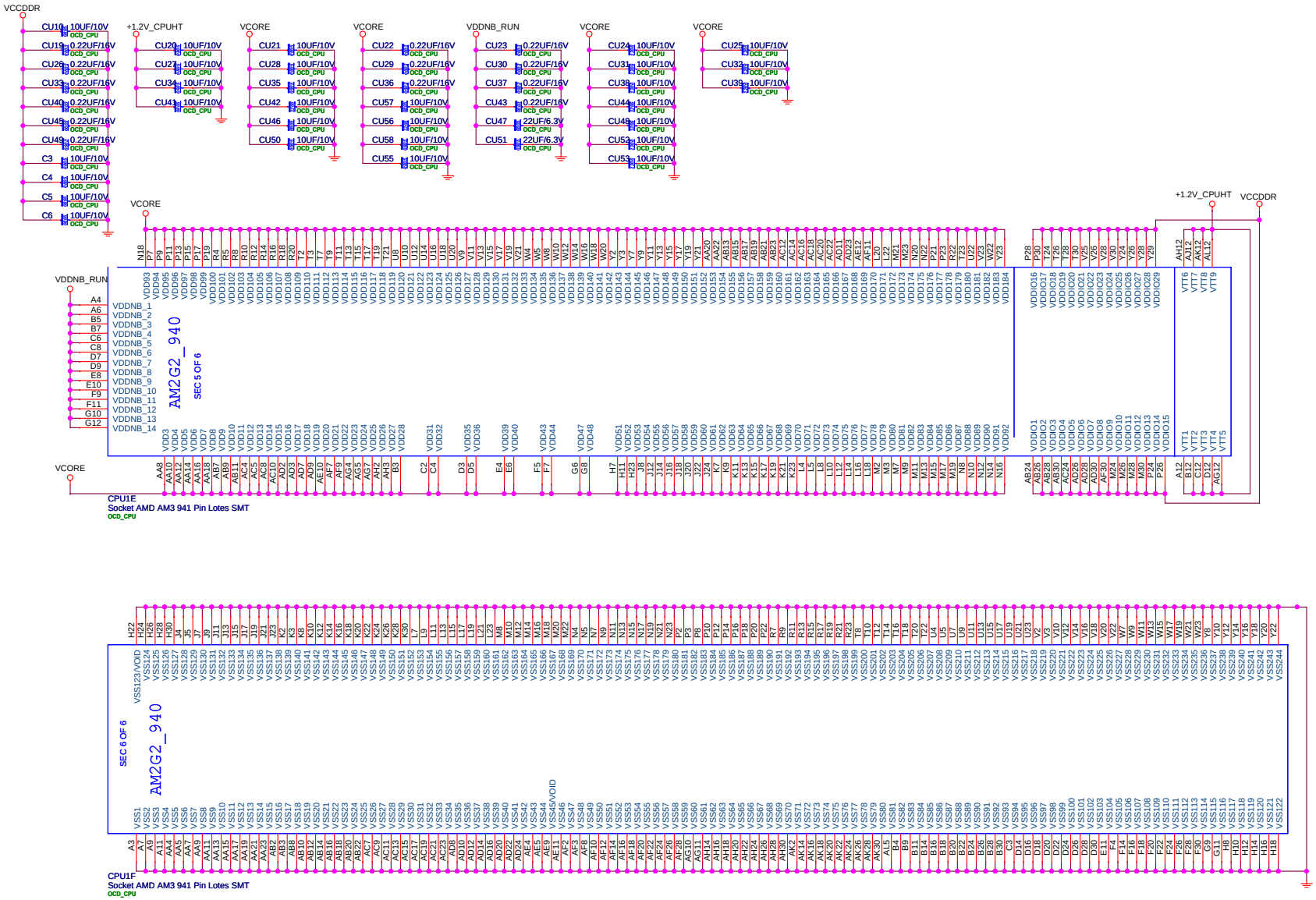

Title	AM2+ POWER		
Size: Custom	Document Number: RS880+SB850+AM3		Rev: 1.0
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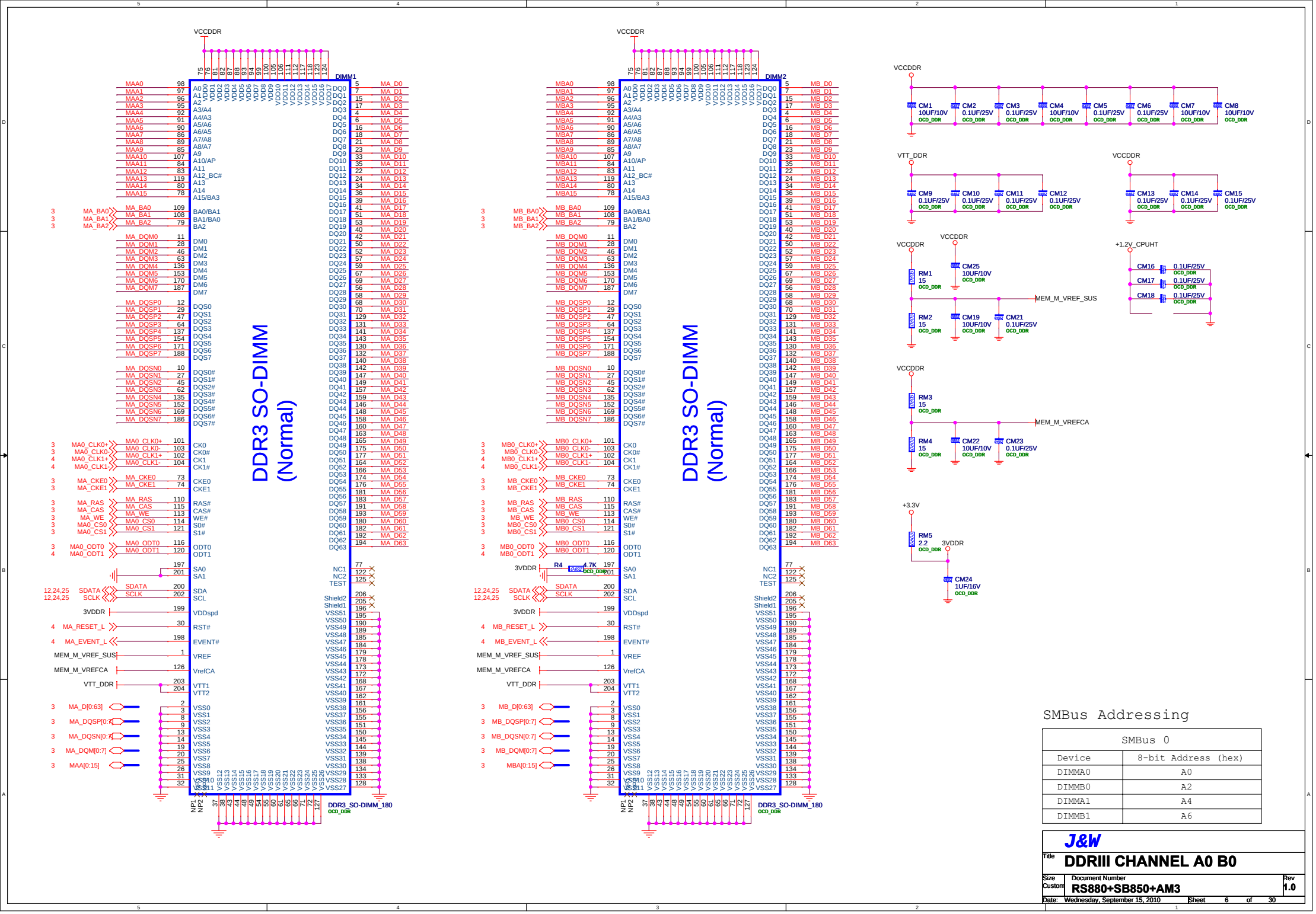
DDR3 SO-DIMM (Normal)
DIMM1
DIMM2
VCCDDR
DDR3_SO-DIMM_180
OCD_DDR
SMBus Addressing
SMBus 0
Device
8-bit Address (hex)
DIMMA0
A0
DIMMB0
A2
DIMMA1
A4
DIMMB1
A6
J&W
Title
DDRIII CHANNEL A0 B0
Size
Custom
Document Number
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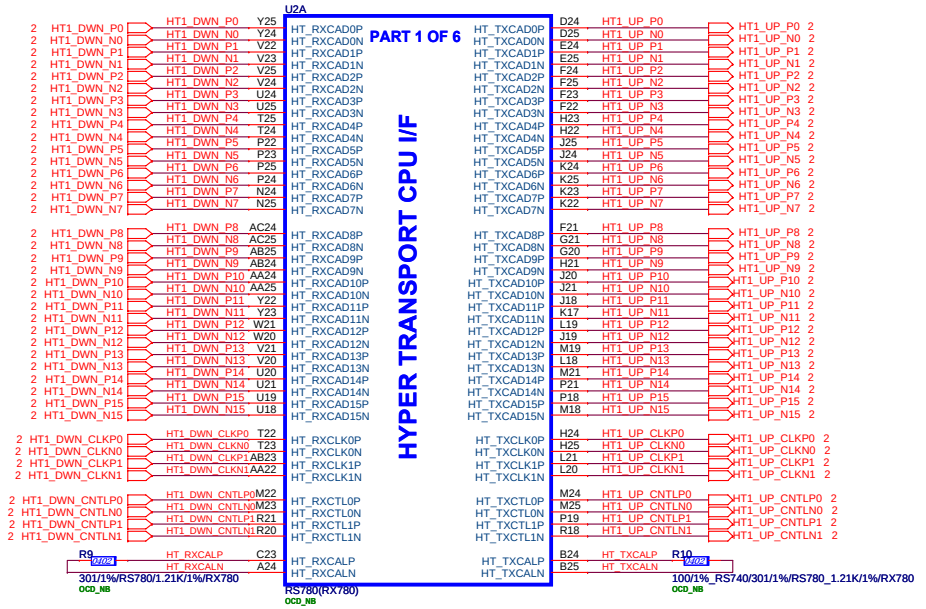

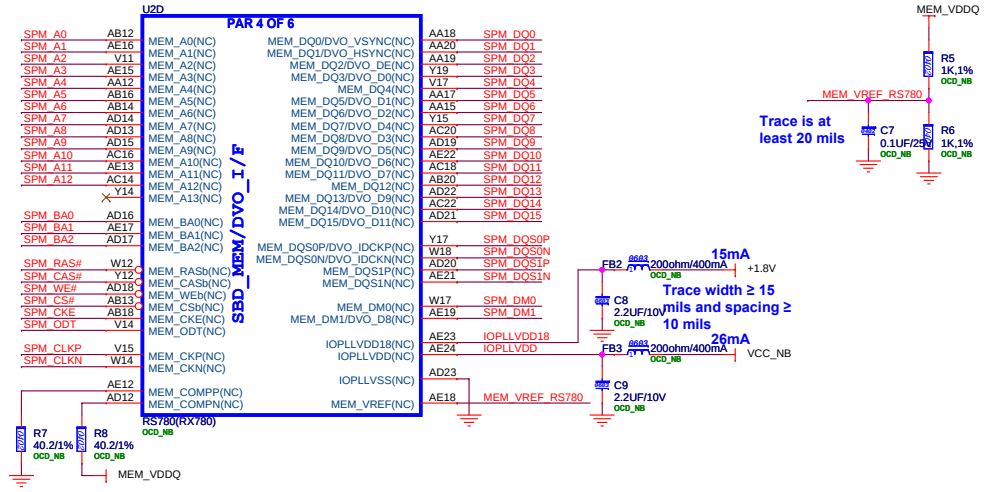

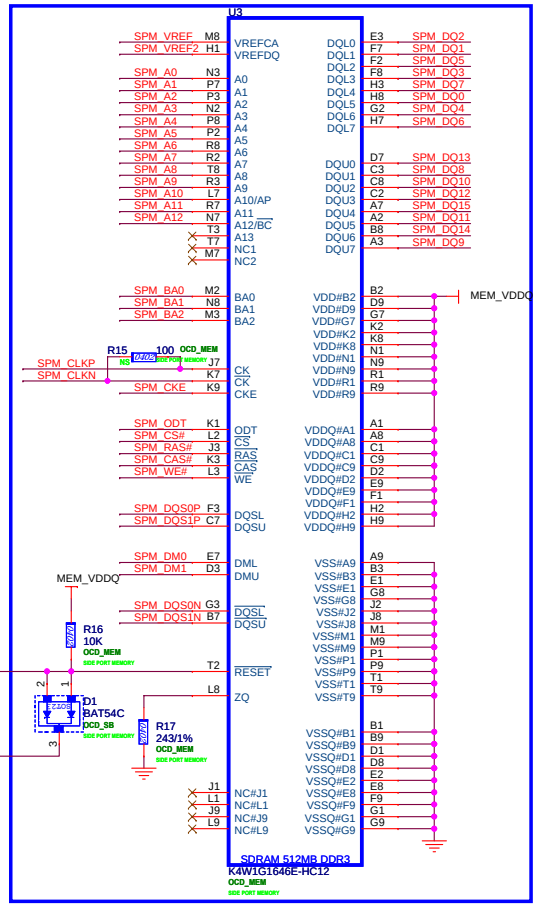

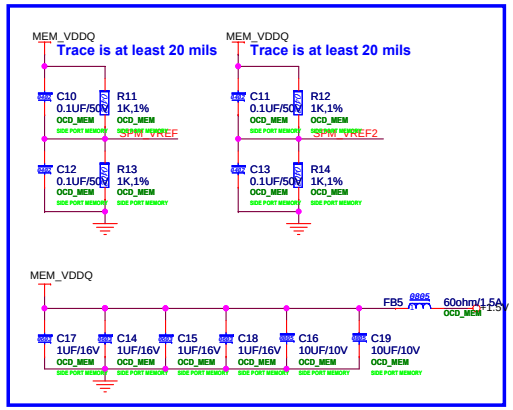

RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP HT_TXCALN	100R	1.21K	301R

DDR2 SIDE PORT MEMORY DEVICES

16Mx16 HYNIX HY5PS561621AFP-25

32Mx16 QIMONDA HYB18T512161B2F-25

64Mx16 SAMSAUNG K4N1G164QQ-HC25

DDR3 SIDE PORT MEMORY DEVICES

64Mx16 HYNIX HY5TQ1G431ZNFP-G8

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Title: **RS740/780 HT I/F SIDE MEMORY**

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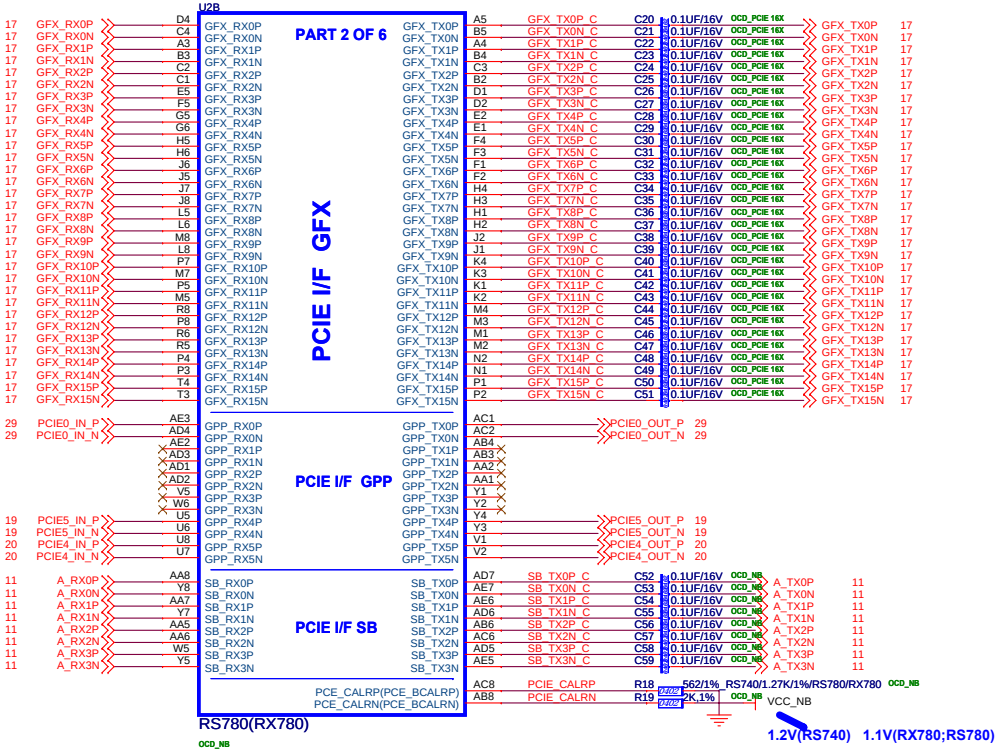

RX780/RS740/RS780 GPP difference table

	RS740	RX780/RS780
PCE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RX780/RS740/RS780 GPP Routing table

	RS740	RX780/RS780
GPP X4 CONNECTOR	GPP[2:0]	GPP[3:0]
GPP X1 CONNECTOR		GPP4
GIGABIT ETHERNET	GPP3	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

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Title: RS740/780 PCIE I/F

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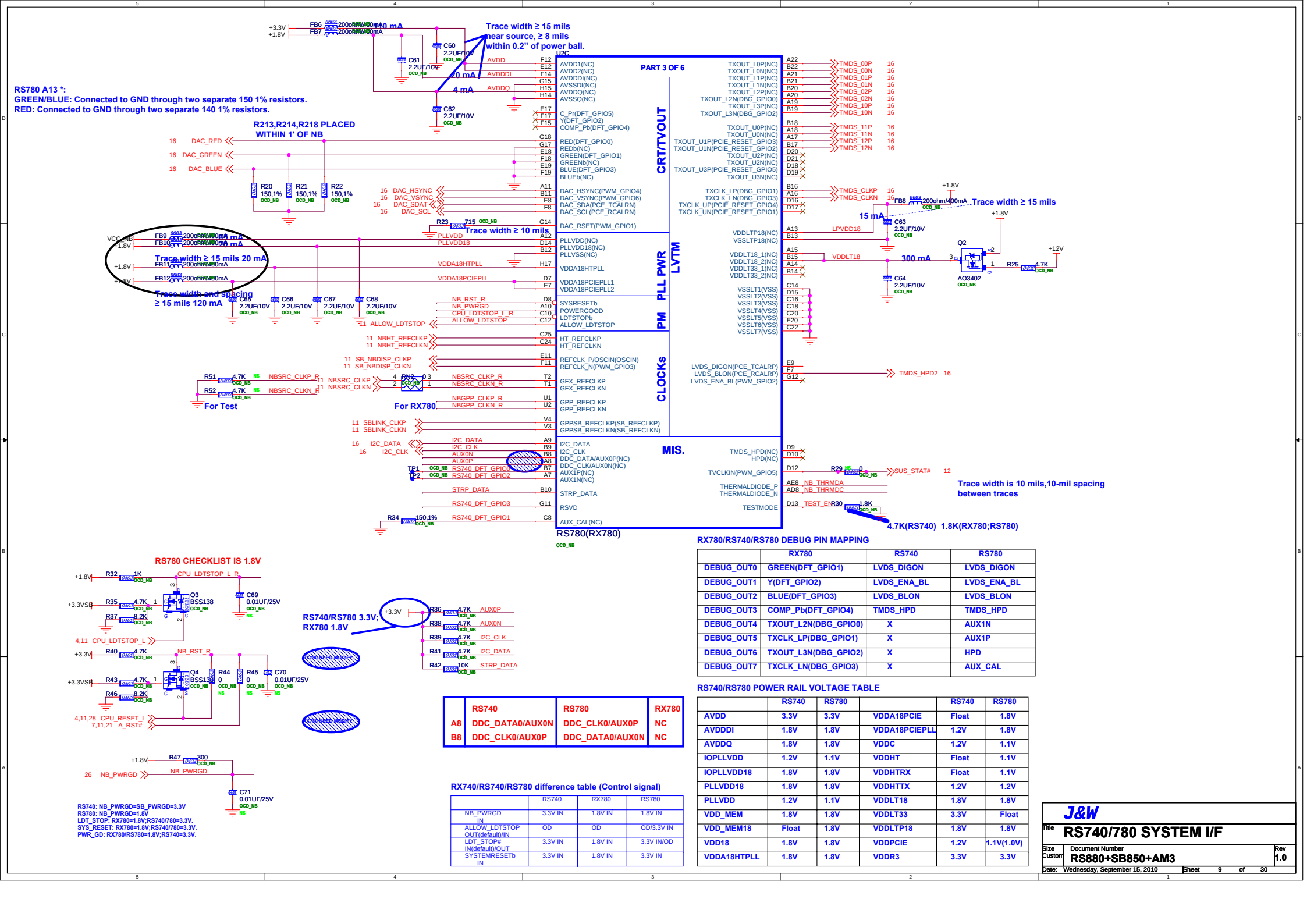

	RS740	RS780	RX780
A8	DDC_DATA0/AUX0N	DDC_CLK0/AUX0P	NC
B8	DDC_CLK0/AUX0P	DDC_DATA0/AUX0N	NC

RX740/RS740/RS780 difference table (Control signal)

	RS740	RX780	RS780
NB_PWRGD IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OD	OD	OD/3.3V IN
LDT_STOP# IN(default)/OUT	3.3V IN	1.8V IN	3.3V IN/OD
SYSTEMRESETb IN	3.3V IN	1.8V IN	3.3V IN

RX780/RS740/RS780 DEBUG PIN MAPPING

	RX780	RS740	RS780
DEBUG_OUT0	GREEN(DFT_GPIO1)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	Y(DFT_GPIO2)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	BLUE(DFT_GPIO3)	LVDS_BLON	LVDS_BLON
DEBUG_OUT3	COMP_Pb(DFT_GPIO4)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

RS740/RS780 POWER RAIL VOLTAGE TABLE

	RS740	RS780		RS740	RS780
AVDD	3.3V	3.3V	VDDA18PCIE	Float	1.8V
AVDDDI	1.8V	1.8V	VDDA18PCIEPLL	1.2V	1.8V
AVDDQ	1.8V	1.8V	VDDC	1.2V	1.1V
IOPLLVDD	1.2V	1.1V	VDDHT	Float	1.1V
IOPLLVDD18	1.8V	1.8V	VDDHTRX	Float	1.1V
PLLVDD18	1.8V	1.8V	VDDHTTX	1.2V	1.2V
PLLVDD	1.2V	1.1V	VDDLT18	1.8V	1.8V
VDD_MEM	1.8V	1.8V	VDDLT33	3.3V	Float
VDD_MEM18	Float	1.8V	VDDLTP18	1.8V	1.8V
VDD18	1.8V	1.8V	VDDPCIE	1.2V	1.1V(1.0V)
VDDA18HTPLL	1.8V	1.8V	VDDR3	3.3V	3.3V

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Title: RS740/780 SYSTEM I/F

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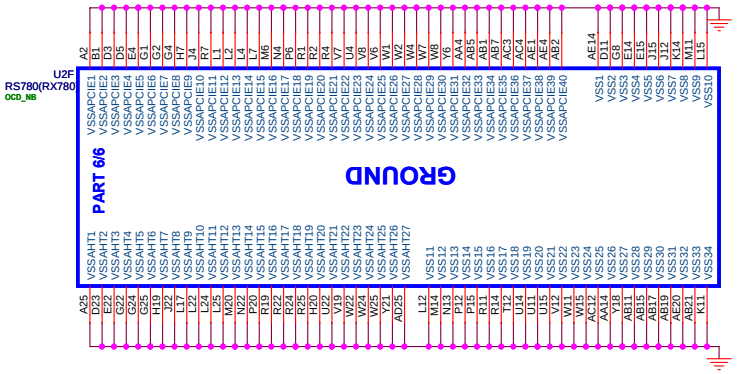
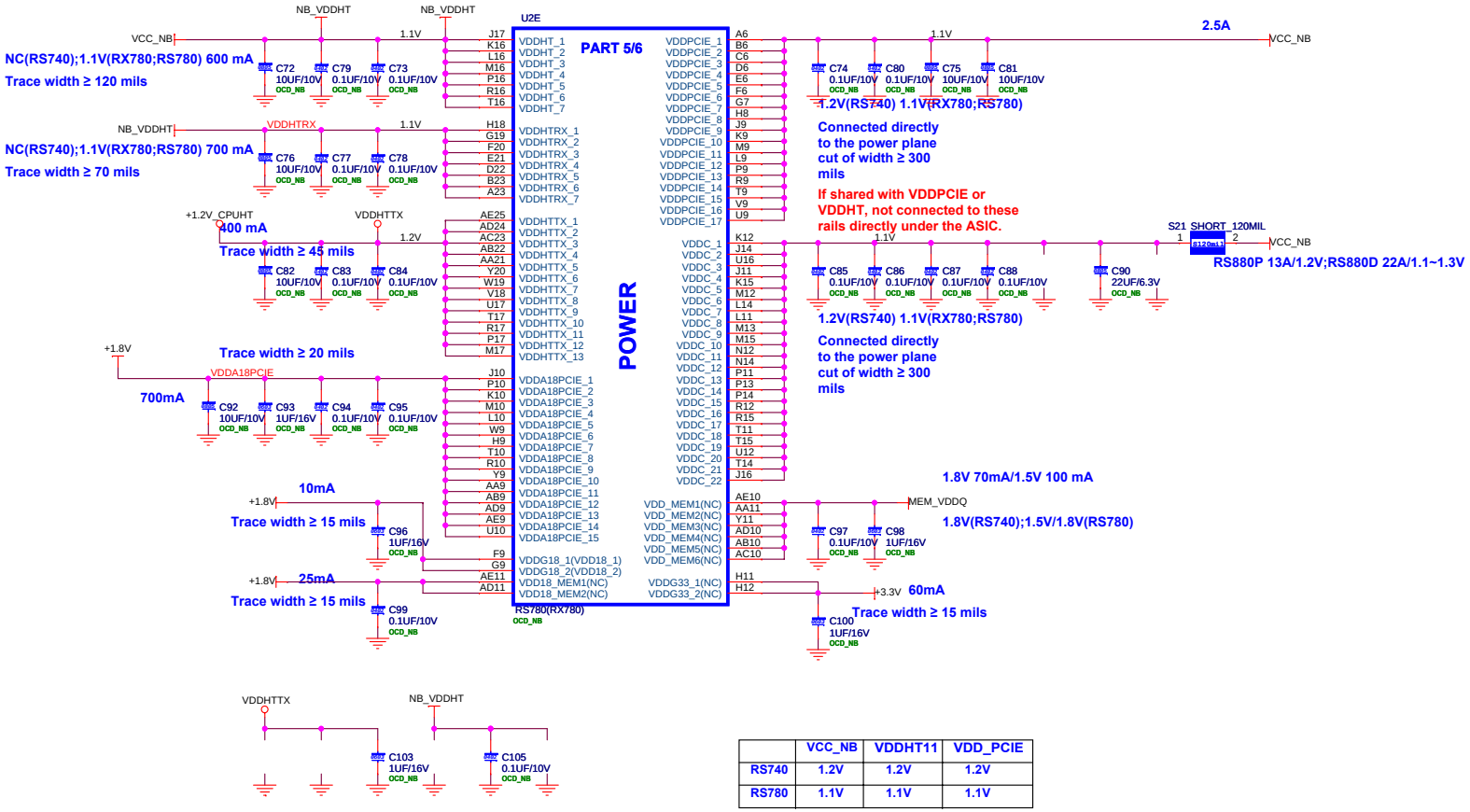


RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC



	VCC_NB	VDDHT11	VDD_PCIE
RS740	1.2V	1.2V	1.2V
RS780	1.1V	1.1V	1.1V

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Title: RS740/780 POWER

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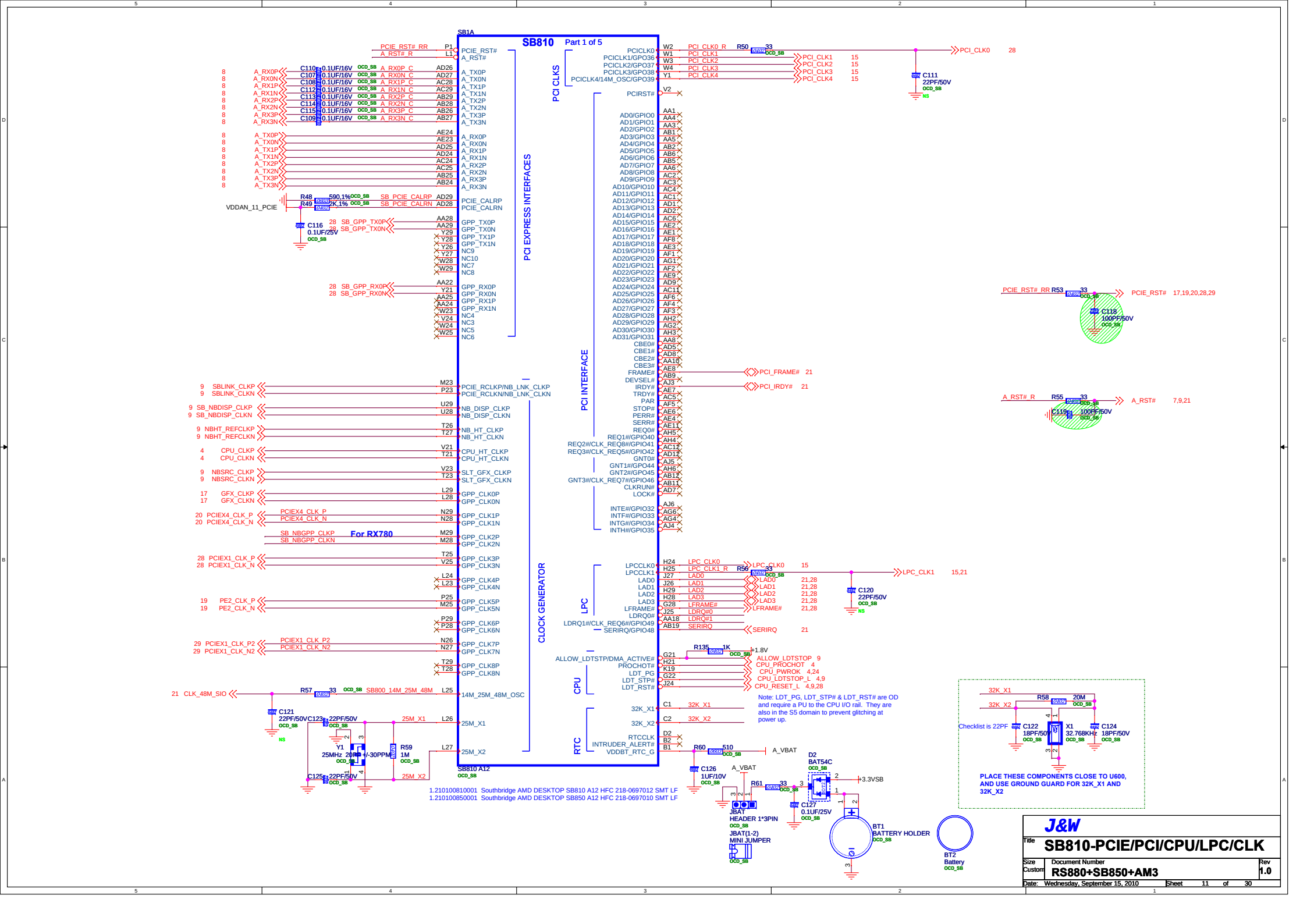
SB1A
SB810
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
PCIE_RST# R
A_RST# R
PCIE_RST#
A_RST#
A_RX0P C
A_RX0N C
A_RX1P C
A_RX1N C
A_RX2P C
A_RX2N C
A_RX3P C
A_RX3N C
A_TX0P
A_TX0N
A_TX1P
A_TX1N
A_TX2P
A_TX2N
A_TX3P
A_TX3N
A_RX0P
A_RX0N
A_RX1P
A_RX1N
A_RX2P
A_RX2N
A_RX3P
A_RX3N
R48 590,1%
R49 2K,1%
VDDAN_11_PCIE
SB_PCIE_CALRP
SB_PCIE_CALRN
PCIE_CALRP
PCIE_CALRN
C116 0.1UF/25V
SB_GPP_TX0P
SB_GPP_TX0N
GPP_TX0P
GPP_TX0N
GPP_TX1P
GPP_TX1N
SB_GPP_RX0P
SB_GPP_RX0N
GPP_RX0P
GPP_RX0N
GPP_RX1P
GPP_RX1N
PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN
NB_DISP_CLKP
NB_DISP_CLKN
NB_HT_CLKP
NB_HT_CLKN
CPU_HT_CLKP
CPU_HT_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
GPP_CLK4P
GPP_CLK4N
GPP_CLK5P
GPP_CLK5N
GPP_CLK6P
GPP_CLK6N
GPP_CLK7P
GPP_CLK7N
GPP_CLK8P
GPP_CLK8N
14M_25M_48M_OSC
25M_X1
25M_X2
SB810 A12
For RX780
PCIEX4_CLK_P
PCIEX4_CLK_N
PCIEX1_CLK_P2
PCIEX1_CLK_N2
SB_NBGPP_CLKP
SB_NBGPP_CLKN
CLK_48M_SIO
R57 33
SB800_14M_25M_48M
C121 22PF/50V
C123 22PF/50V
C125 22PF/50V
Y1 25MHz 20PPM +/-30PPM
R59 1M
PCICLK0
PCICLK1/GPO36
PCICLK2/GPO37
PCICLK3/GPO38
PCICLK4/14M_OSC/GPO39
PCI_CLK0_R
PCI_CLK1
PCI_CLK2
PCI_CLK3
PCI_CLK4
R50 33
C111 22PF/50V
PCIRST#
AD0/GPIO0
AD1/GPIO1
AD2/GPIO2
AD3/GPIO3
AD4/GPIO4
AD5/GPIO5
AD6/GPIO6
AD7/GPIO7
AD8/GPIO8
AD9/GPIO9
AD10/GPIO10
AD11/GPIO11
AD12/GPIO12
AD13/GPIO13
AD14/GPIO14
AD15/GPIO15
AD16/GPIO16
AD17/GPIO17
AD18/GPIO18
AD19/GPIO19
AD20/GPIO20
AD21/GPIO21
AD22/GPIO22
AD23/GPIO23
AD24/GPIO24
AD25/GPIO25
AD26/GPIO26
AD27/GPIO27
AD28/GPIO28
AD29/GPIO29
AD30/GPIO30
AD31/GPIO31
CBE0#
CBE1#
CBE2#
CBE3#
FRAME#
DEVSEL#
IRDY#
TRDY#
PAR
STOP#
PERR#
SERR#
REQ0#
REQ1#/GPIO40
REQ2#/CLK_REQ8#/GPIO41
REQ3#/CLK_REQ5#/GPIO42
GNT0#
GNT1#/GPO44
GNT2#/GPO45
GNT3#/CLK_REQ7#/GPIO46
CLKRUN#
LOCK#
INTE#/GPIO32
INTF#/GPIO33
INTG#/GPIO34
INTH#/GPIO35
PCI_FRAME#
PCI_IRDY#
LPCCLK0
LPCCLK1
LAD0
LAD1
LAD2
LAD3
LFRAME#
LDRQ0#
LDRQ1#/CLK_REQ6#/GPIO49
SERIRQ/GPIO48
LPC_CLK0
LPC_CLK1_R
R56 33
C120 22PF/50V
LPC_CLK1
SERIRQ
ALLOW_LDTSTP/DMA_ACTIVE#
PROCHOT#
LDT_PG
LDT_STP#
LDT_RST#
R135 1K
+1.8V
ALLOW_LDTSTOP 9
CPU_PROCHOT 4
CPU_PWROK 4,24
CPU_LDTSTOP_L 4,9
CPU_RESET_L 4,9,28
Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.
32K_X1
32K_X2
RTCCLK
INTRUDER_ALERT#
VDDBT_RTC_G
R60 510
A_VBAT
C126 1UF/10V
R61 33
D2 BAT54C
+3.3VSB
C127 0.1UF/25V
JBAT HEADER 1*3PIN
JBAT(1-2) MINI JUMPER
BT1 BATTERY HOLDER
BT2 Battery
PCIE_RST# RR
R53 33
PCIE_RST# 17,19,20,28,29
C118 100PF/50V
A_RST# R
R55 33
A_RST# 7,9,21
C119 100PF/50V
R58 20M
Checklist is 22PF
C122 18PF/50V
X1 32.768KHz
C124 18PF/50V
PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2
1.210100810001 Southbridge AMD DESKTOP SB810 A12 HFC 218-0697012 SMT LF
1.210100850001 Southbridge AMD DESKTOP SB850 A12 HFC 218-0697010 SMT LF
J&W
Title
SB810-PCIE/PCI/CPU/LPC/CLK
Size
Custom
Document Number
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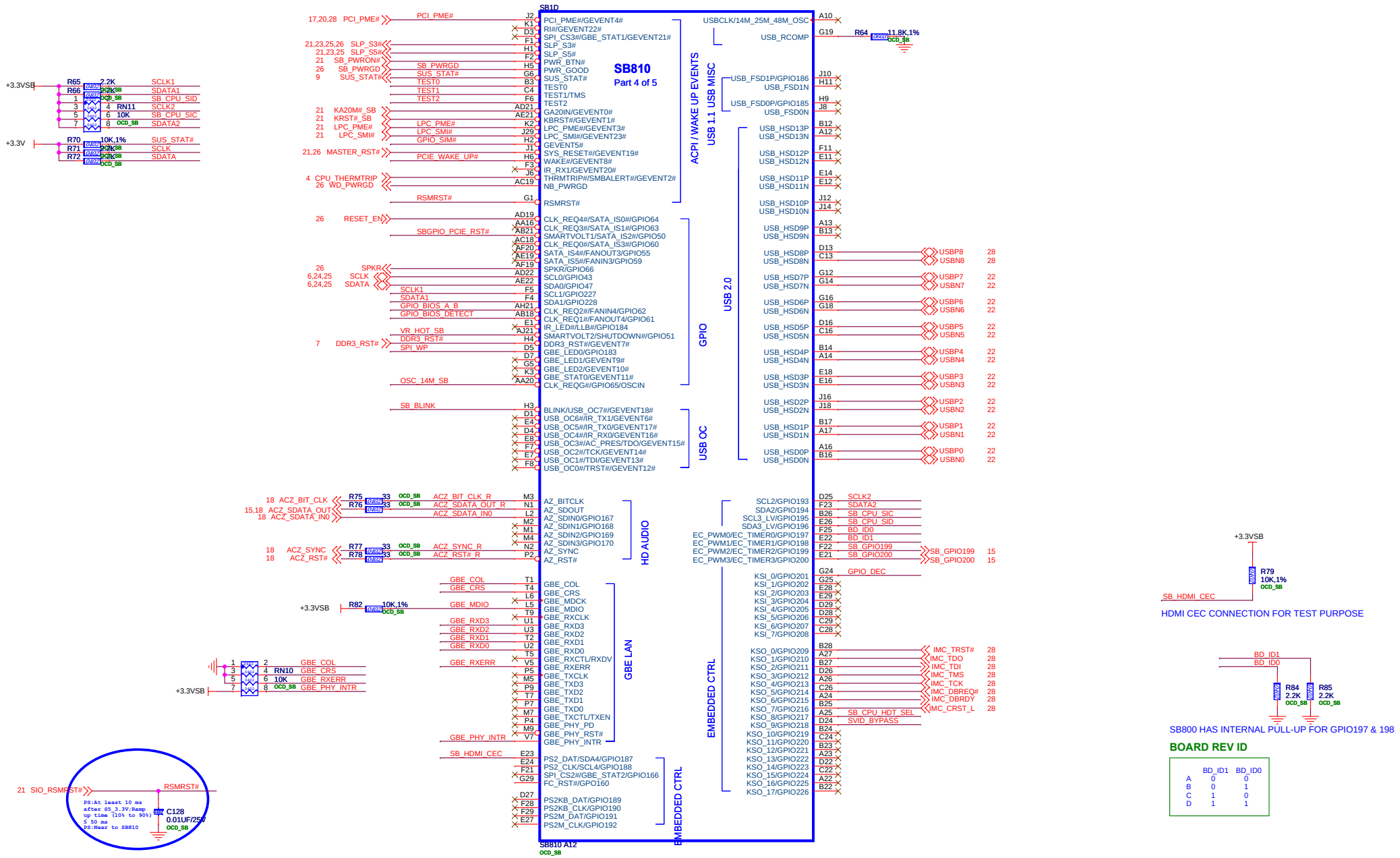

Title	SB810-ACPI/GPIO/USB/AUDIO
Size	Custom
Document Number	RS880+SB850+AM3
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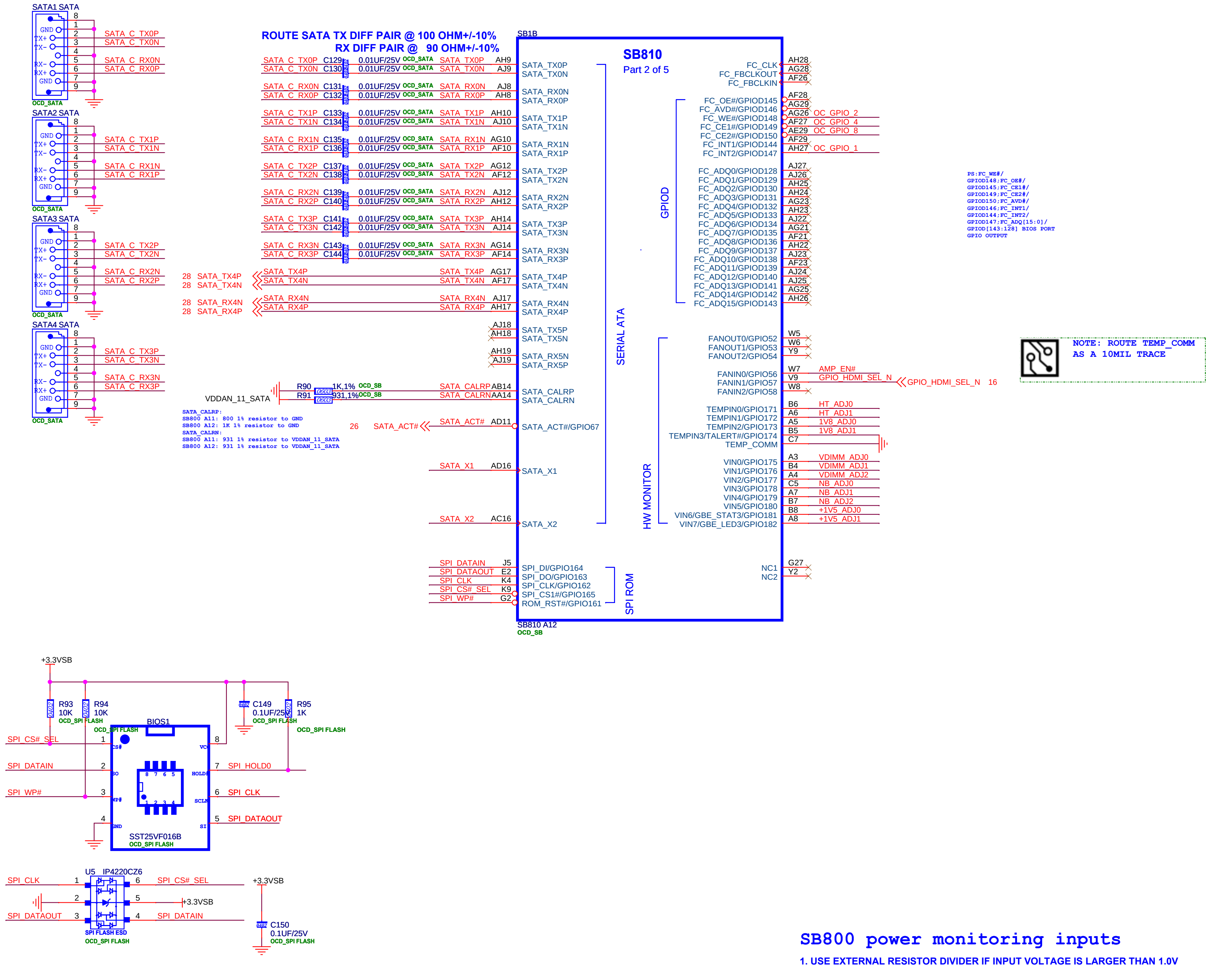

ROUTE SATA TX DIFF PAIR @ 100 OHM+/-10%
RX DIFF PAIR @ 90 OHM+/-10%
SATA1 SATA
SATA2 SATA
SATA3 SATA
SATA4 SATA
OCD_SATA
SB1B
SB810
Part 2 of 5
SERIAL ATA
GPIOD
HW MONITOR
SPI ROM
SB810 A12
OCD_SB
SATA_TX0P
SATA_TX0N
SATA_RX0N
SATA_RX0P
SATA_TX1P
SATA_TX1N
SATA_RX1N
SATA_RX1P
SATA_TX2P
SATA_TX2N
SATA_RX2N
SATA_RX2P
SATA_TX3P
SATA_TX3N
SATA_RX3N
SATA_RX3P
SATA_TX4P
SATA_TX4N
SATA_RX4N
SATA_RX4P
SATA_TX5P
SATA_TX5N
SATA_RX5N
SATA_RX5P
SATA_CALRP
SATA_CALRN
SATA_ACT#/GPIO67
SATA_X1
SATA_X2
SPI_DI/GPIO164
SPI_DO/GPIO163
SPI_CLK/GPIO162
SPI_CS1#/GPIO165
ROM_RST#/GPIO161
FC_CLK
FC_FBCLKOUT
FC_FBCLKIN
FC_OE#/GPIOD145
FC_AVD#/GPIOD146
FC_WE#/GPIOD148
FC_CE1#/GPIOD149
FC_CE2#/GPIOD150
FC_INT1/GPIOD144
FC_INT2/GPIOD147
FC_ADQ0/GPIOD128 … FC_ADQ15/GPIOD143
FANOUT0/GPIO52
FANOUT1/GPIO53
FANOUT2/GPIO54
FANIN0/GPIO56
FANIN1/GPIO57
FANIN2/GPIO58
TEMPIN0/GPIO171
TEMPIN1/GPIO172
TEMPIN2/GPIO173
TEMPIN3/TALERT#/GPIO174
TEMP_COMM
VIN0/GPIO175
VIN1/GPIO176
VIN2/GPIO177
VIN3/GPIO178
VIN4/GPIO179
VIN5/GPIO180
VIN6/GBE_STAT3/GPIO181
VIN7/GBE_LED3/GPIO182
NC1
NC2
OC_GPIO_2
OC_GPIO_4
OC_GPIO_8
OC_GPIO_1
AMP_EN#
GPIO_HDMI_SEL_N
HT_ADJ0
HT_ADJ1
1V8_ADJ0
1V8_ADJ1
VDIMM_ADJ0
VDIMM_ADJ1
VDIMM_ADJ2
NB_ADJ0
NB_ADJ1
NB_ADJ2
+1V5_ADJ0
+1V5_ADJ1
NOTE: ROUTE TEMP_COMM
AS A 10MIL TRACE
VDDAN_11_SATA
R90 1K,1%
R91 931,1%
SATA_CALRP:
SB800 A11: 800 1% resistor to GND
SB800 A12: 1K 1% resistor to GND
SATA_CALRN:
SB800 A11: 931 1% resistor to VDDAN_11_SATA
SB800 A12: 931 1% resistor to VDDAN_11_SATA
+3.3VSB
R93 10K
R94 10K
R95 1K
C149 0.1UF/25V
BIOS1
SST25VF016B
OCD_SPI FLASH
SPI_CS#_SEL
SPI_DATAIN
SPI_WP#
SPI_HOLD0
SPI_CLK
SPI_DATAOUT
U5 IP4220CZ6
SPI FLASH ESD
C150 0.1UF/25V

SB800 power monitoring inputs

1. USE EXTERNAL RESISTOR DIVIDER IF INPUT VOLTAGE IS LARGER THAN 1.0V
2. MAKE SURE THE CENTER VOLTAGE IS 0.9V IF USE EXTERNAL DIVIDER, IF THE RAIL ALLOWS OVERVOLTAGE, SET THE CENTER VOLTAGE TO 0.5V

J&W	
Title	SB810-SATA/HWM/SPI
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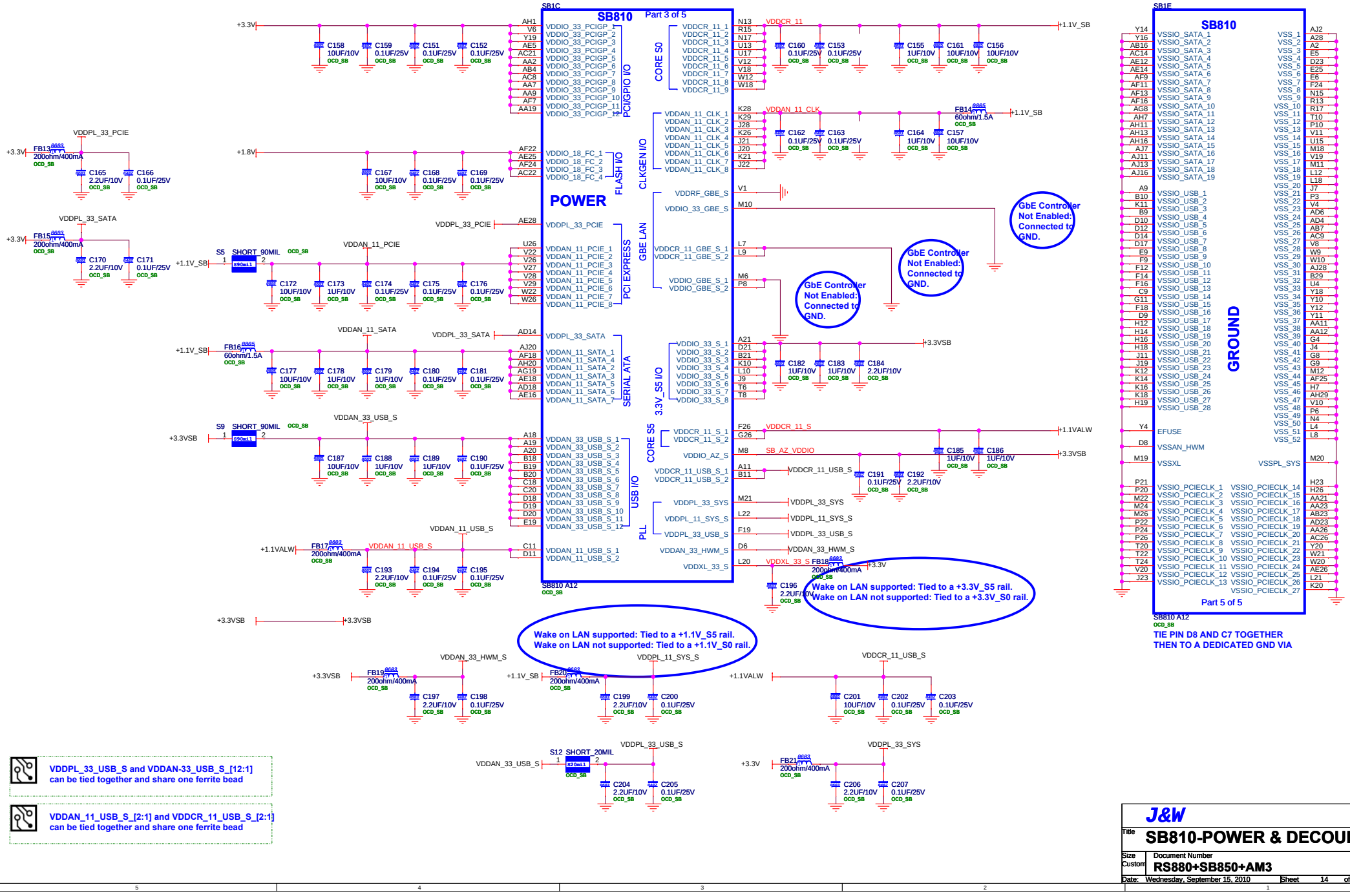
All Power Rails except VDDIO_33_S:
50 µs ≤ Power Rail Ramp time ≤ 40 ms.

VDDIO_33_S:
100 µs ≤ Power Rail Ramp time ≤ 40 ms.



VDDPL_33_USB_S and VDDAN-33_USB_S_[12:1] can be tied together and share one ferrite bead

VDDAN_11_USB_S_[2:1] and VDDCR_11_USB_S_[2:1] can be tied together and share one ferrite bead

J&W			
Title: SB810-POWER & DECOUPLING			
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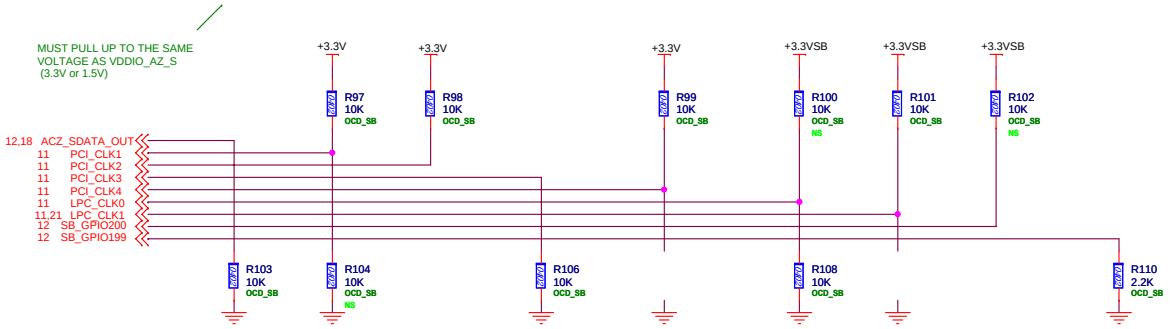
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

PLACE STRAP RESISTORS DIRECTLY ON CLK NETS (WITHOUT STUBS).

SB800 REQUIRED STRAPS



	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ON NB_PWRGD ENABLED DEFAULT	USE DEBUG STRAPS	NON-FUSION CPU CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED	ROM TYPE: H, H = Reserved	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER ON NB_PWRGD DISABLED	IGNORE DEBUG STRAPS DEFAULT	FUSION CPU CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	H, L = SPI ROM DEFAULT L, H = LPC ROM L, L = FWH ROM	

SB810/SB850:
Allow PCIe Gen2: 10-k 5% pull-up to +3.3V_S0.
Force PCIe Gen1: 10-k 5% pull-down.
SB820M: Only provision for pull-down is required, not installed by default.

LPCCLK0 : Embedded Controller (EC)
0V – Disabled
3.3V – Enabled
This strap has to be enabled to support enhanced hardware monitor features.

EC_PWM3, EC_PWM2:

ROMTYPE_1	ROMTYPE_0	ROM Type
3.3V	0V	SPI ROM
3.3V	3.3V	Reserved
0V	0V	Firmware Hub
0V	3.3V	LPC ROM (supports both LPC and PMC ROM types)

Configure these two strap pins to the corresponding state that matches the hardware ROM type installed.

LPCCLK1 : Defines clock generator.
0V – External clock mode: Use 100MHz PCIe clock as reference clock and generate internal clocks only.
3.3V – Integrated clock mode: Use 25MHz crystal clock and generate both internal and external clocks.

PCICLK1 : Set PCIe to Gen II mode.
0V – Force PCIe interface at Gen I mode.
3.3V – PCIe interfacce is at Gen II mode.

PCICLK2 : Watchdog function.
0V – Disable the boot fail timer function.
3.3V – Enable the boot fail timer function.

PCICLK3 : Default Debug Straps.
0V – Disable Debug Straps.
3.3V – Select external Debug Straps.

PCICLK4 : CPU/NB HT Clock Selection.
0V – Reserved
3.3V – Required setting for integrated clock mode
This strap is not used if the strap CLKGEN is configured for external clock generator mode.

AZ_SDOUT : Slow down core clock for low power platform.
0V – Performance mode.
3.3 V – Low Power mode.
This is required as the low power mode is not supported on the SB8xx.

SB800 DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

AD27 : Bypass PCI PLL (used in functional test at tester).
0V– Bypass internal PLL clock.
Use xSPciReqB_1_ as SPCI33 bypass clock.
Use xSPciReqB_2_as A-Link bypass clock.
Use xSPciGntB_1_as B-Link bypass clock.
Use xSPciGntB_0_ as B-Link266 bypass clock.
3.3V – Use internal PLL-generated PLL CLK.

AD26 : ILA auto run Enable.
0V – ILA auto run enable.
3.3V – ILA auto run disable.

AD25 : Bypass FC CLK.
0V – Bypass internal FC Clk (used in functional test at tester).
Use xSPciReqB_0_ as FC 1xClk bypass clock.
Use xSPciGntB_2_ as FC 2xClk bypass clock.
3.3V – Use internal PLL FC Clk.

AD24 : I2C ROM enable. Load the settings for A-Link Express/PLL/ misc control from I2C ROM.
0V – Getting the value from I2C EPROM.
I2C EPROM ADDRESS set to all zeroes.
Use REQ3# as SDA.
Use GNT3# as SCL.
3.3V – Disable I2C ROM

AD23 : Booting from PCI memory.
0V – Route ROM fetch to PCI bus on the very first boot. Use ROMTYPE to determine the ROM type on subsequent boots.
3.3V – Use ROMTYPE straps to determine the ROM type.

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Title: SB810-STRAPS

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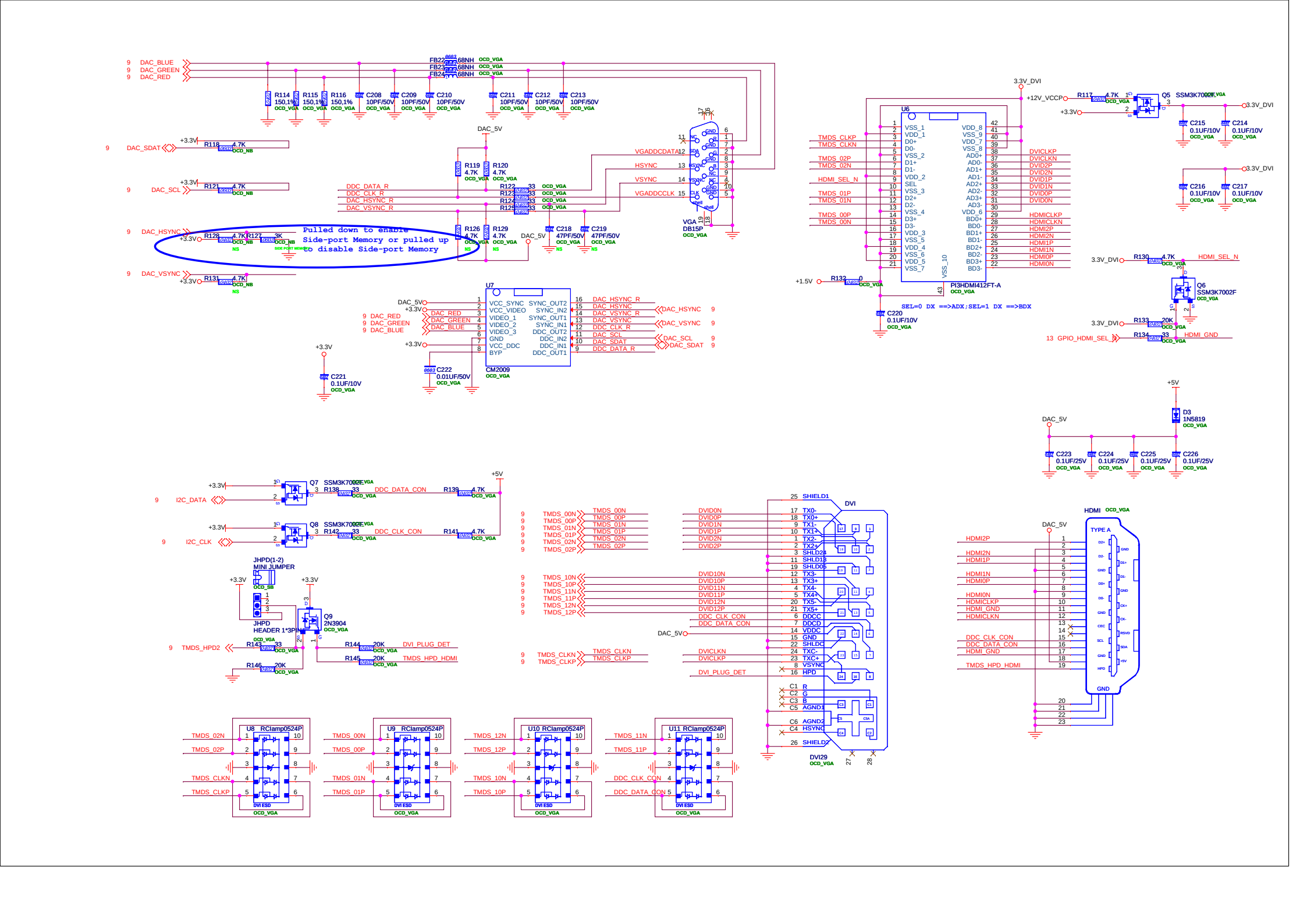
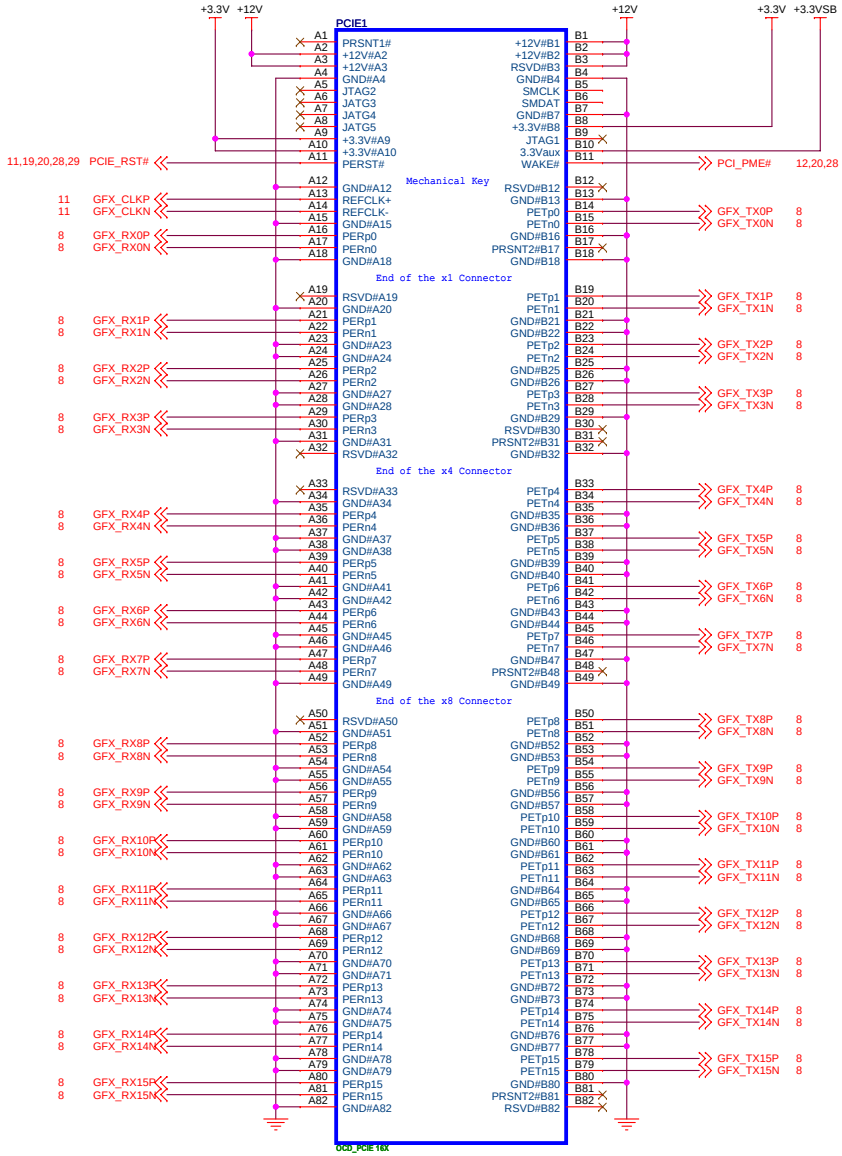
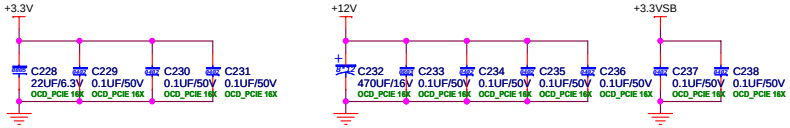

DAC_BLUE
DAC_GREEN
DAC_RED
FB22 68NH OCD_VGA
FB23 68NH OCD_VGA
FB24 68NH OCD_VGA
R114 150,1% OCD_VGA
R115 150,1% OCD_VGA
R116 150,1% OCD_VGA
C208 10PF/50V OCD_VGA
C209 10PF/50V OCD_VGA
C210 10PF/50V OCD_VGA
C211 10PF/50V OCD_VGA
C212 10PF/50V OCD_VGA
C213 10PF/50V OCD_VGA
DAC_5V
DAC_SDAT
R118 4.7K OCD_NB
DAC_SCL
R121 4.7K OCD_NB
R119 4.7K OCD_VGA
R120 4.7K OCD_VGA
DDC_DATA_R
DDC_CLK_R
DAC_HSYNC_R
DAC_VSYNC_R
R122 33 OCD_VGA
R123 33 OCD_VGA
R124 33 OCD_VGA
R125 33 OCD_VGA
VGADDCDATA
HSYNC
VSYNC
VGADDCCLK
VGA DB15P OCD_VGA
DAC_HSYNC
R128 4.7K OCD_NB NS
R127 3K OCD_NB SIDE PORT MEMORY
Pulled down to enable
Side-port Memory or pulled up
to disable Side-port Memory
R126 4.7K OCD_VGA NS
R129 4.7K OCD_VGA NS
C218 47PF/50V OCD_VGA NS
C219 47PF/50V OCD_VGA NS
DAC_VSYNC
R131 4.7K OCD_NB NS
U7
CM2009 OCD_VGA
DAC_HSYNC_R
DAC_VSYNC_R
DDC_CLK_R
DDC_DATA_R
C221 0.1UF/10V OCD_VGA
C222 0.01UF/50V OCD_VGA
3.3V_DVI
+12V_VCCP
R117 4.7K OCD_VGA
Q5 SSM3K7002F OCD_VGA
C215 0.1UF/10V OCD_VGA
C214 0.1UF/10V OCD_VGA
C216 0.1UF/10V OCD_VGA
C217 0.1UF/10V OCD_VGA
U6
PI3HDMI412FT-A OCD_VGA
TMDS_CLKP
TMDS_CLKN
TMDS_02P
TMDS_02N
HDMI_SEL_N
TMDS_01P
TMDS_01N
TMDS_00P
TMDS_00N
DVICLKP
DVICLKN
DVID2P
DVID2N
DVID1P
DVID1N
DVID0P
DVID0N
HDMICLKP
HDMICLKN
HDMI2P
HDMI2N
HDMI1P
HDMI1N
HDMI0P
HDMI0N
+1.5V
R132 0 OCD_VGA
SEL=0 DX ==>ADX;SEL=1 DX ==>BDX
C220 0.1UF/10V OCD_VGA
R130 4.7K OCD_VGA
Q6 SSM3K7002F OCD_VGA
R133 20K OCD_VGA
R134 33 OCD_VGA
GPIO_HDMI_SEL
HDMI_GND
DAC_5V
D3 1N5819 OCD_VGA
C223 0.1UF/25V OCD_VGA
C224 0.1UF/25V OCD_VGA
C225 0.1UF/25V OCD_VGA
C226 0.1UF/25V OCD_VGA
I2C_DATA
I2C_CLK
Q7 SSM3K7002F OCD_VGA
Q8 SSM3K7002F OCD_VGA
R138 33 OCD_VGA
R142 33 OCD_VGA
DDC_DATA_CON
DDC_CLK_CON
R139 4.7K OCD_VGA
R141 4.7K OCD_VGA
JHPD(1-2)
MINI JUMPER
OCD_SB
JHPD
HEADER 1*3P
Q9 2N3904 OCD_VGA
TMDS_HPD2
R143 33 OCD_VGA
R144 20K OCD_VGA
R145 20K OCD_VGA
R146 20K OCD_VGA
DVI_PLUG_DET
TMDS_HPD_HDMI
DVI
DVI29 OCD_VGA
DVID0N
DVID0P
DVID1N
DVID1P
DVID2N
DVID2P
DVID10N
DVID10P
DVID11N
DVID11P
DVID12N
DVID12P
DVID_CLK_CON
DVID_DATA_CON
DVICLKN
DVICLKP
DVI_PLUG_DET
HDMI OCD_VGA
TYPE A
U8 RClamp0524P
U9 RClamp0524P
U10 RClamp0524P
U11 RClamp0524P
DVI ESD OCD_VGA





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Title: PCIEX16 SLOT

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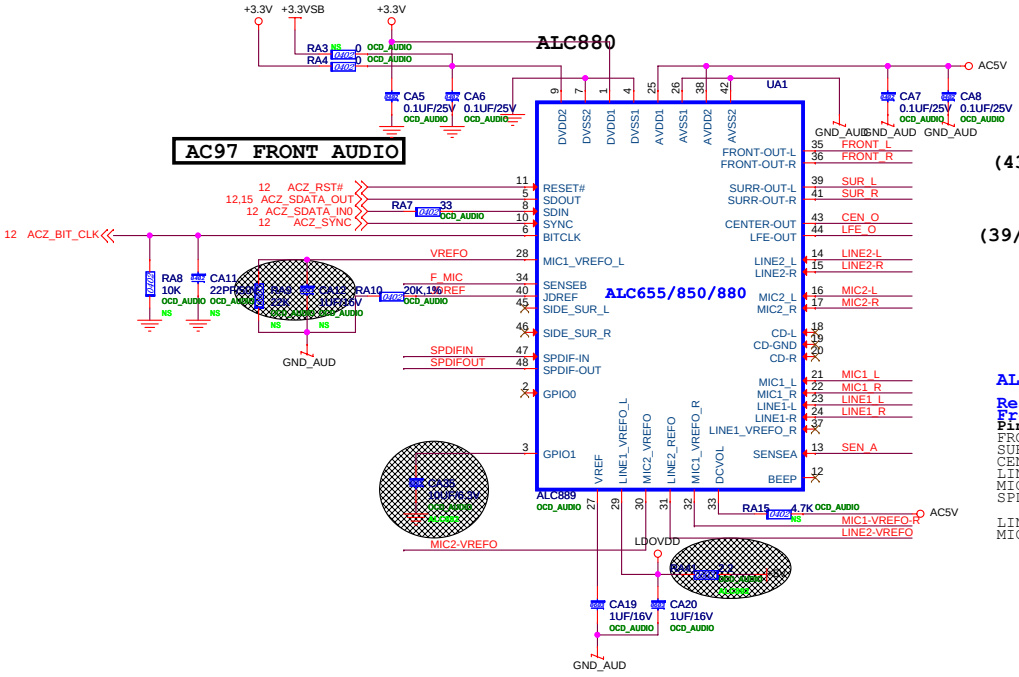
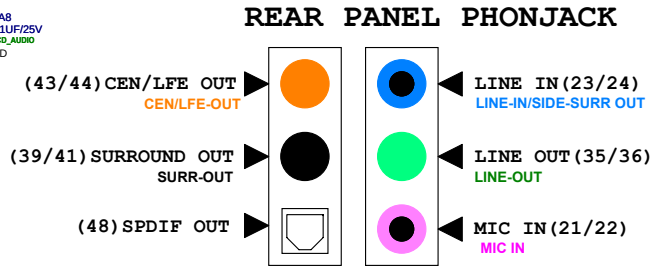
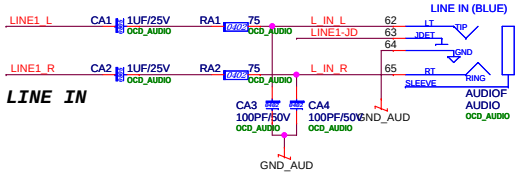


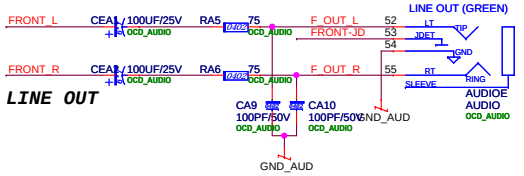


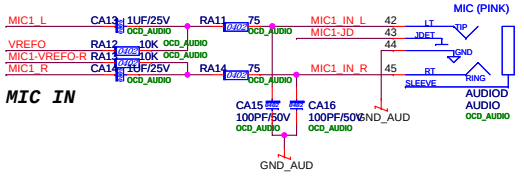
ALC885 Configuation (7.1 Channel)

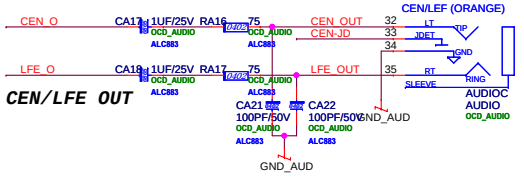
Rear Panel: 5 audio jacks + 1 SPDIF ouput
Front Panel: 2 re-tasking audio jacks

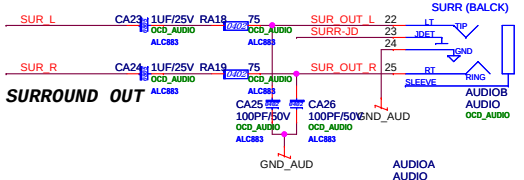
Pin Assignment	Location	Re-tasking
FRONT(pin-35,36)/Port-D	Rear Panel	Front-Out, HP-Out
SURR (pin-39,41)/Port-A	Rear Panel	Surr-Out
CEN/LFE (pin-43,44)/Port-G	Rear Panel	Cen/Lfe-Out
LINE1 (pin-23,24)/Port-C	Rear Panel	Line-In/Side-Surr Out
MIC1 (pin-21,22)/Port-B	Rear Panel	Mic-In
SPDIF OUT (pin-48)	Rear Panel	RCA / OPTICAL SPDIF OUT
LINE2 (pin-14,15)/Port-E	Front Panel	HP-Out, Line-In, Mic-In
MIC2 (pin-16,17)/Port-F	Front Panel	Mic-In, HP-Out, Line-In

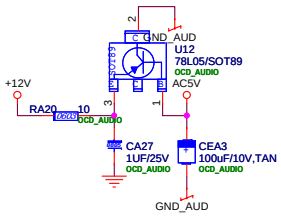


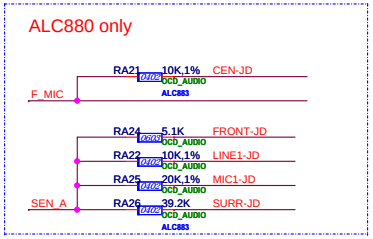


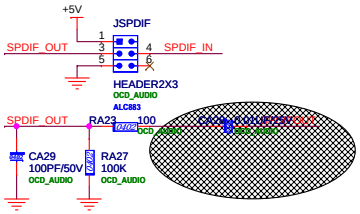


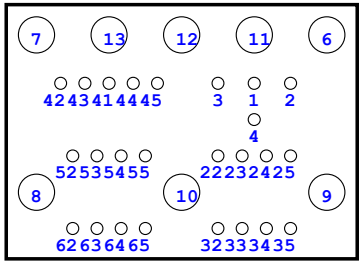


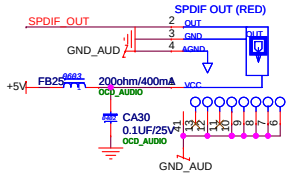


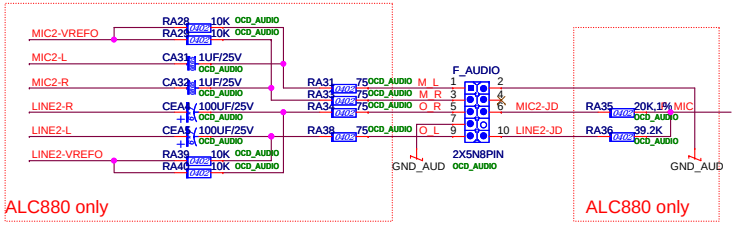


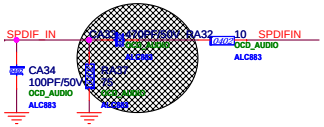


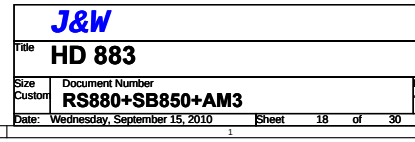












J&W		
Title	HD 883	
Size: Custom	Document Number: RS880+SB850+AM3	Rev: 1.0
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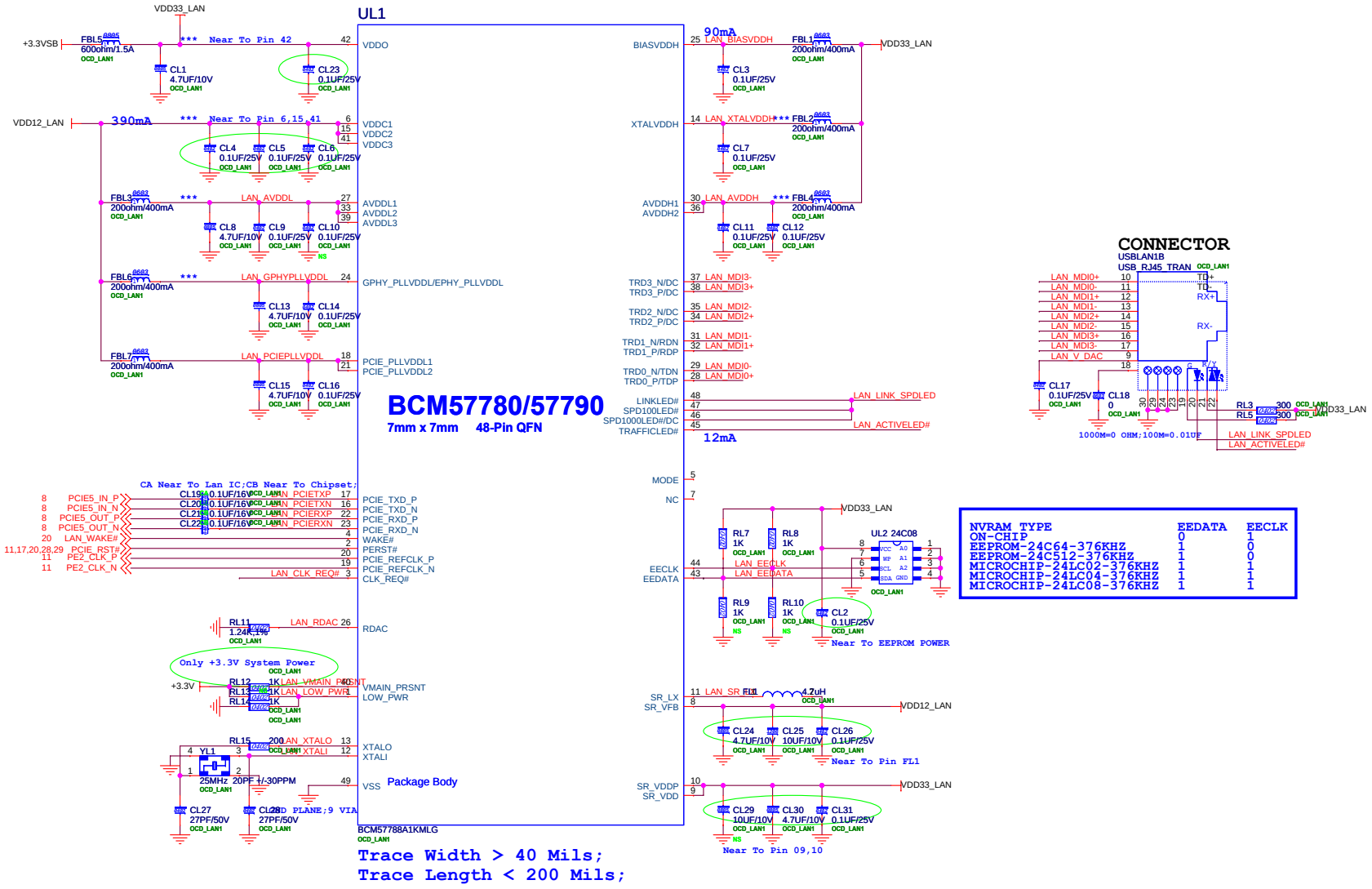
UL1
BCM57780/57790
7mm x 7mm 48-Pin QFN
BCM57788A1KMLG
Package Body
VDD33_LAN
VDD12_LAN
+3.3VSB
FBL5 600ohm/1.5A
*** Near To Pin 42
390mA
90mA
12mA
LAN_AVDDL
LAN_GPHYPLLVDDL
LAN_PCIEPLLVDDL
LAN_BIASVDDH
LAN_XTALVDDH
LAN_AVDDH
CA Near To Lan IC;CB Near To Chipset;
Only +3.3V System Power
Near To EEPROM POWER
Near To Pin FL1
Near To Pin 09,10
Trace Width > 40 Mils;
Trace Length < 200 Mils;
CONNECTOR
USBLAN1B
USB_RJ45_TRAN
1000M=0 OHM;100M=0.01UF
NVRAM_TYPE EEDATA EECLK
ON-CHIP 0 1
EEPROM-24C64-376KHZ 1 0
EEPROM-24C512-376KHZ 1 0
MICROCHIP-24LC02-376KHZ 1 1
MICROCHIP-24LC04-376KHZ 1 1
MICROCHIP-24LC08-376KHZ 1 1
J&W
BCM57780/57790 LAN
RS880+SB850+AM3
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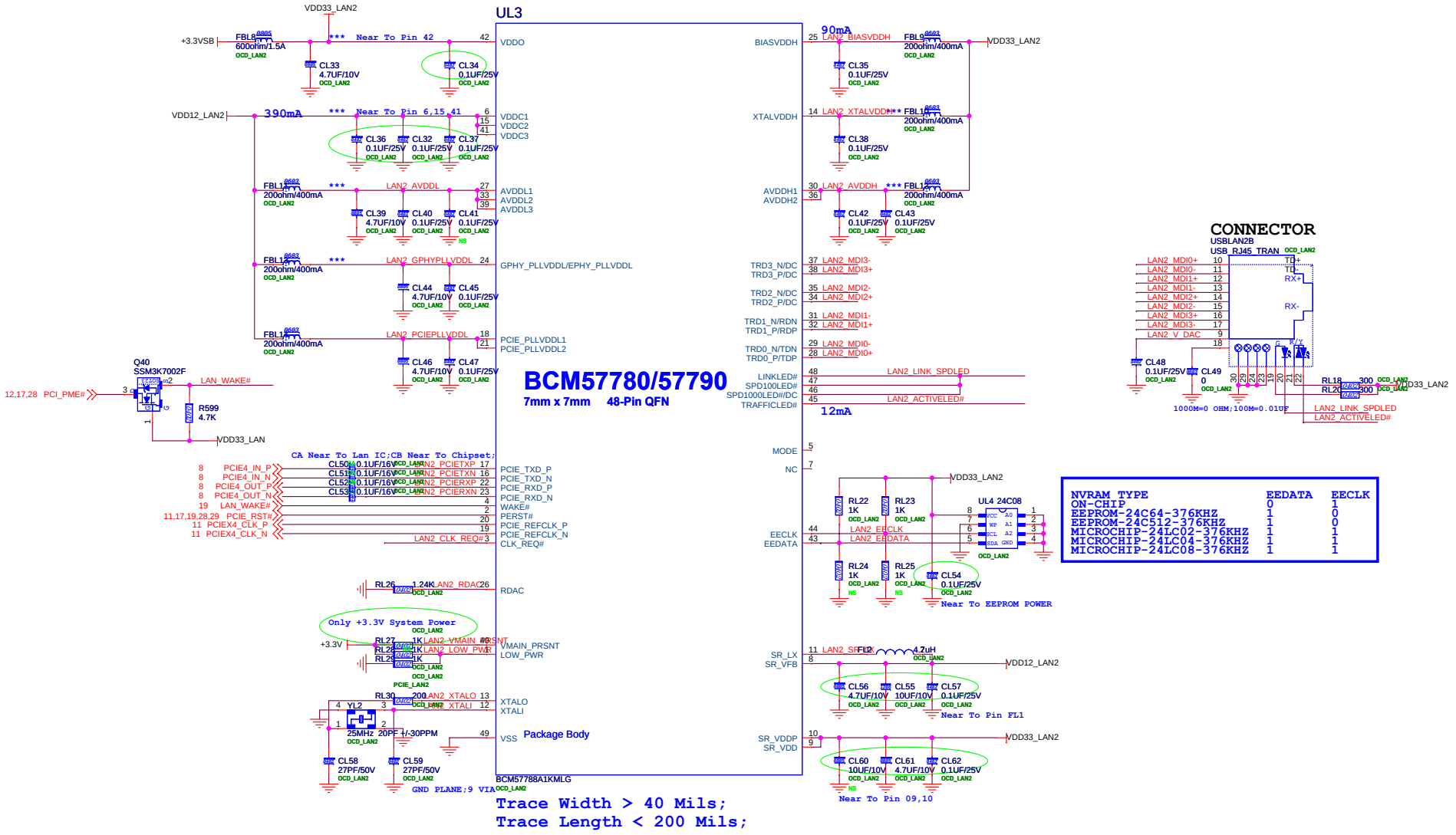

Title	BCM57780/57790 LAN	
Size: Custom	Document Number: RS880+SB850+AM3	Rev: 1.0
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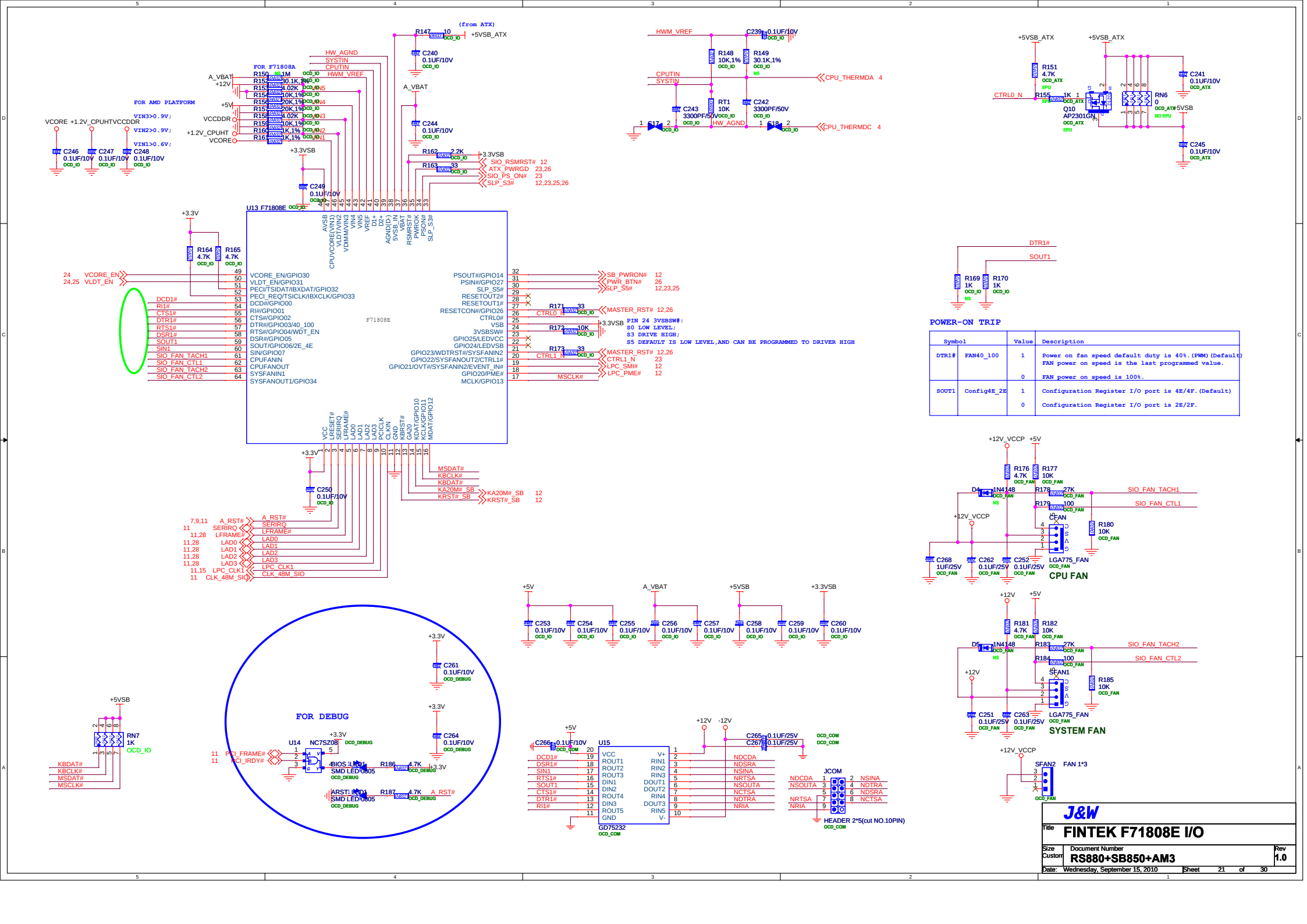

Symbol		Value	Description
DTR1#	FAN40_100	1	Power on fan speed default duty is 40%.(PWM)(Default) FAN power on speed is the last programmed value.
		0	FAN power on speed is 100%.
SOUT1	Config4E_2E	1	Configuration Register I/O port is 4E/4F.(Default)
		0	Configuration Register I/O port is 2E/2F.

Title	FINTEK F71808E I/O
Size	Custom
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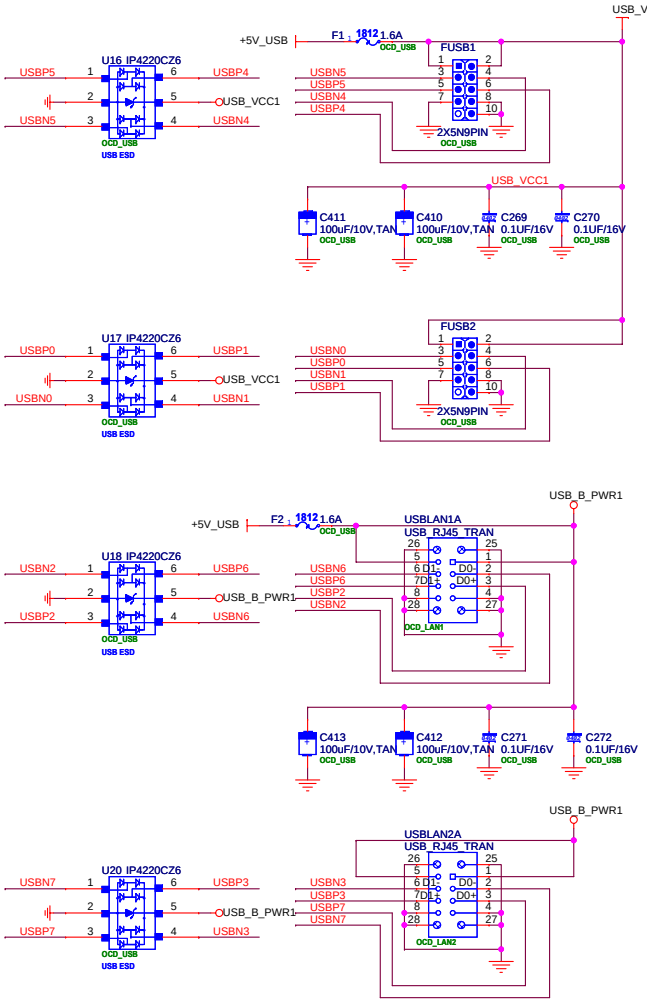

12 USBP0 USBP0
12 USBN0 USBN0
12 USBP1 USBP1
12 USBN1 USBN1

12 USBP2 USBP2
12 USBN2 USBN2
12 USBP3 USBP3
12 USBN3 USBN3

12 USBP4 USBP4
12 USBN4 USBN4
12 USBP5 USBP5
12 USBN5 USBN5

12 USBP6 USBP6
12 USBN6 USBN6
12 USBP7 USBP7
12 USBN7 USBN7

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Title: K/B, USB

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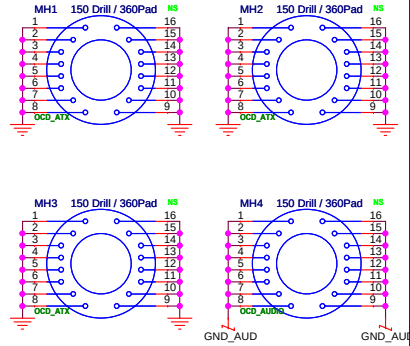

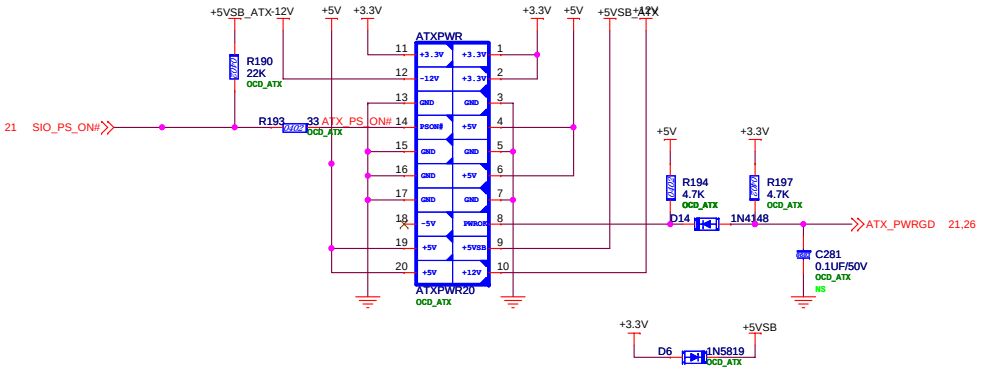

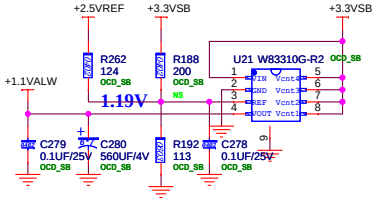

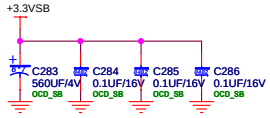

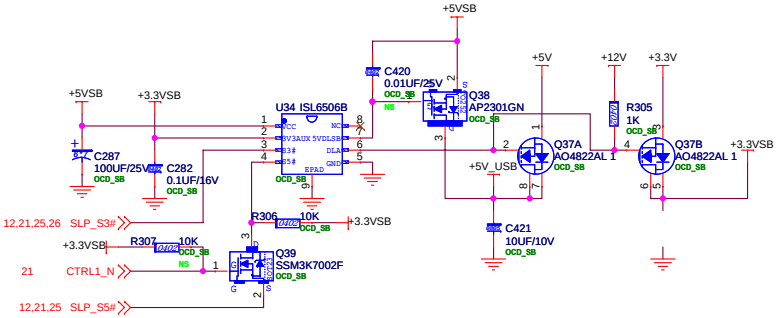

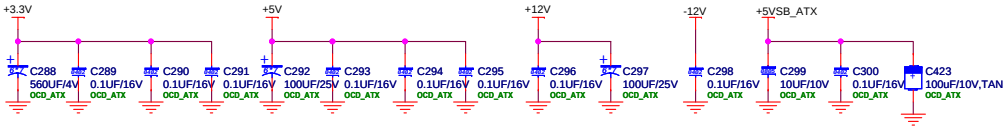

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Title	ATX CONNECTOR	
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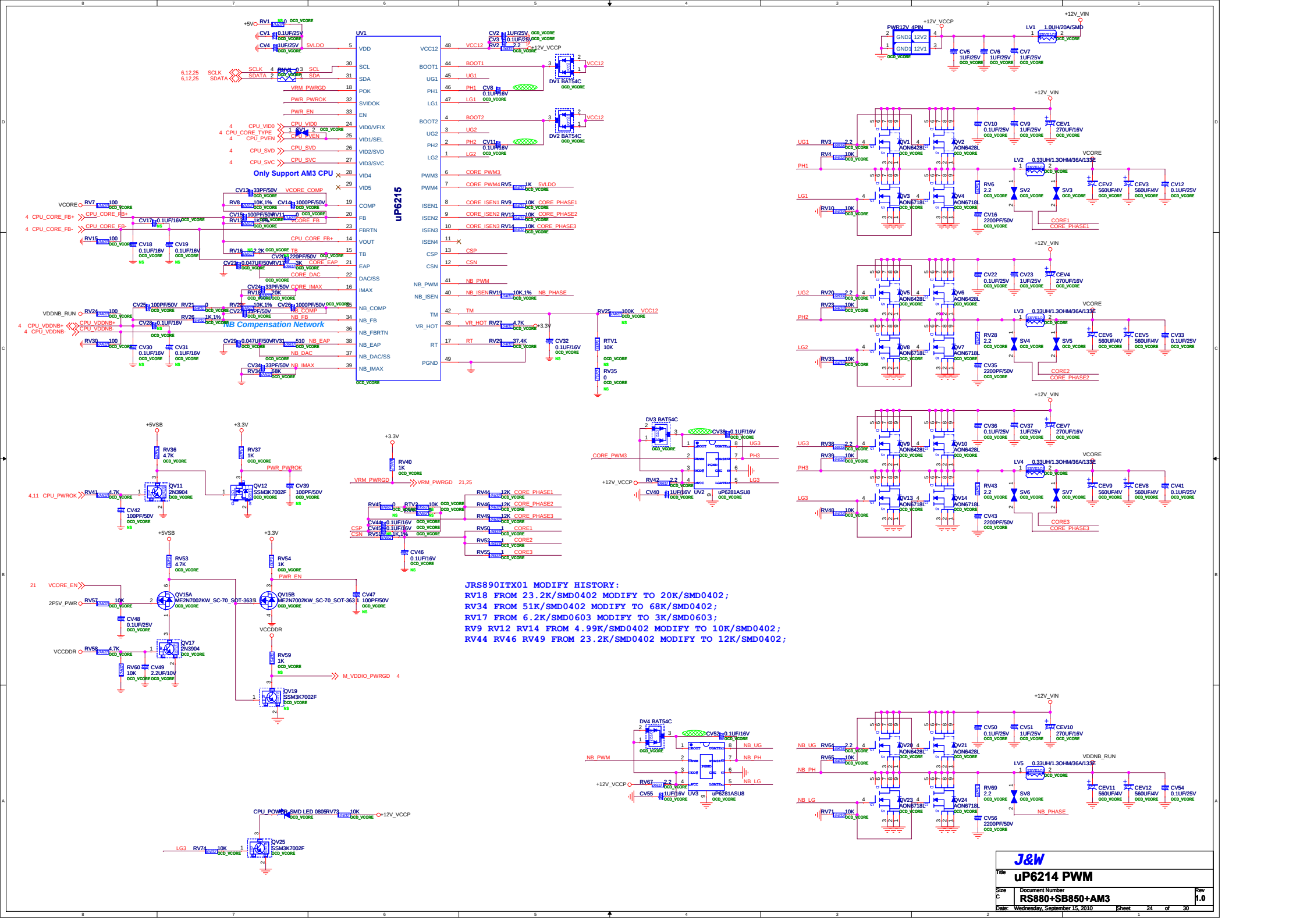
uP6215
Only Support AM3 CPU
NB Compensation Network
JRS890ITX01 MODIFY HISTORY:
RV18 FROM 23.2K/SMD0402 MODIFY TO 20K/SMD0402;
RV34 FROM 51K/SMD0402 MODIFY TO 68K/SMD0402;
RV17 FROM 6.2K/SMD0603 MODIFY TO 3K/SMD0603;
RV9 RV12 RV14 FROM 4.99K/SMD0402 MODIFY TO 10K/SMD0402;
RV44 RV46 RV49 FROM 23.2K/SMD0402 MODIFY TO 12K/SMD0402;
J&W
uP6214 PWM
RS880+SB850+AM3
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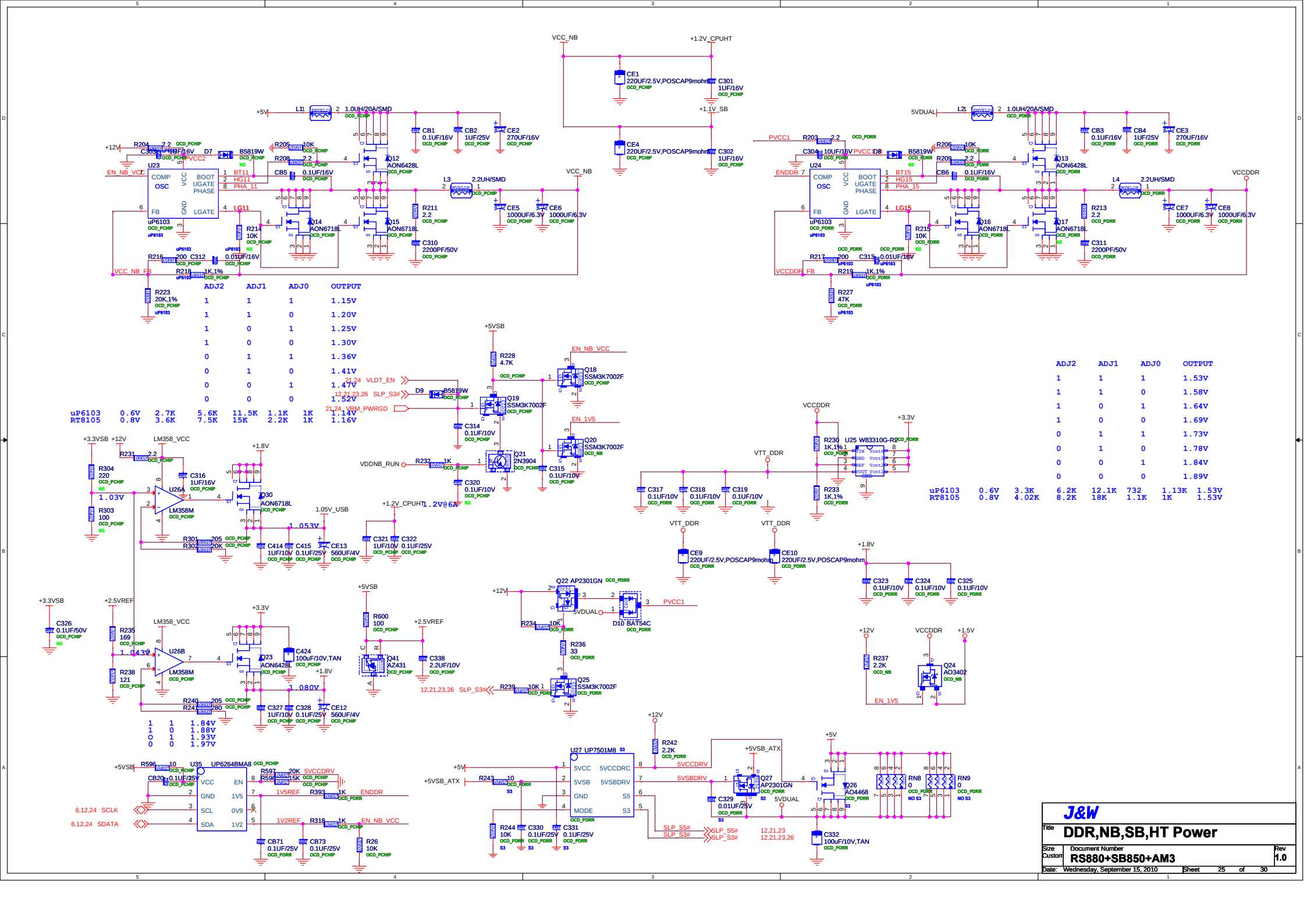

ADJ2	ADJ1	ADJ0	OUTPUT
1	1	1	1.15V
1	1	0	1.20V
1	0	1	1.25V
1	0	0	1.30V
0	1	1	1.36V
0	1	0	1.41V
0	0	1	1.47V
0	0	0	1.52V

uP6103	0.6V	2.7K	5.6K	11.5K	1.1K	1K	1.14V
RT8105	0.8V	3.6K	7.5K	15K	2.2K	1K	1.16V

uP6103	0.6V	3.3K	6.2K	12.1K	732	1.13K	1.53V
RT8105	0.8V	4.02K	8.2K	18K	1.1K	1K	1.53V

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Title: **DDR,NB,SB,HT Power**

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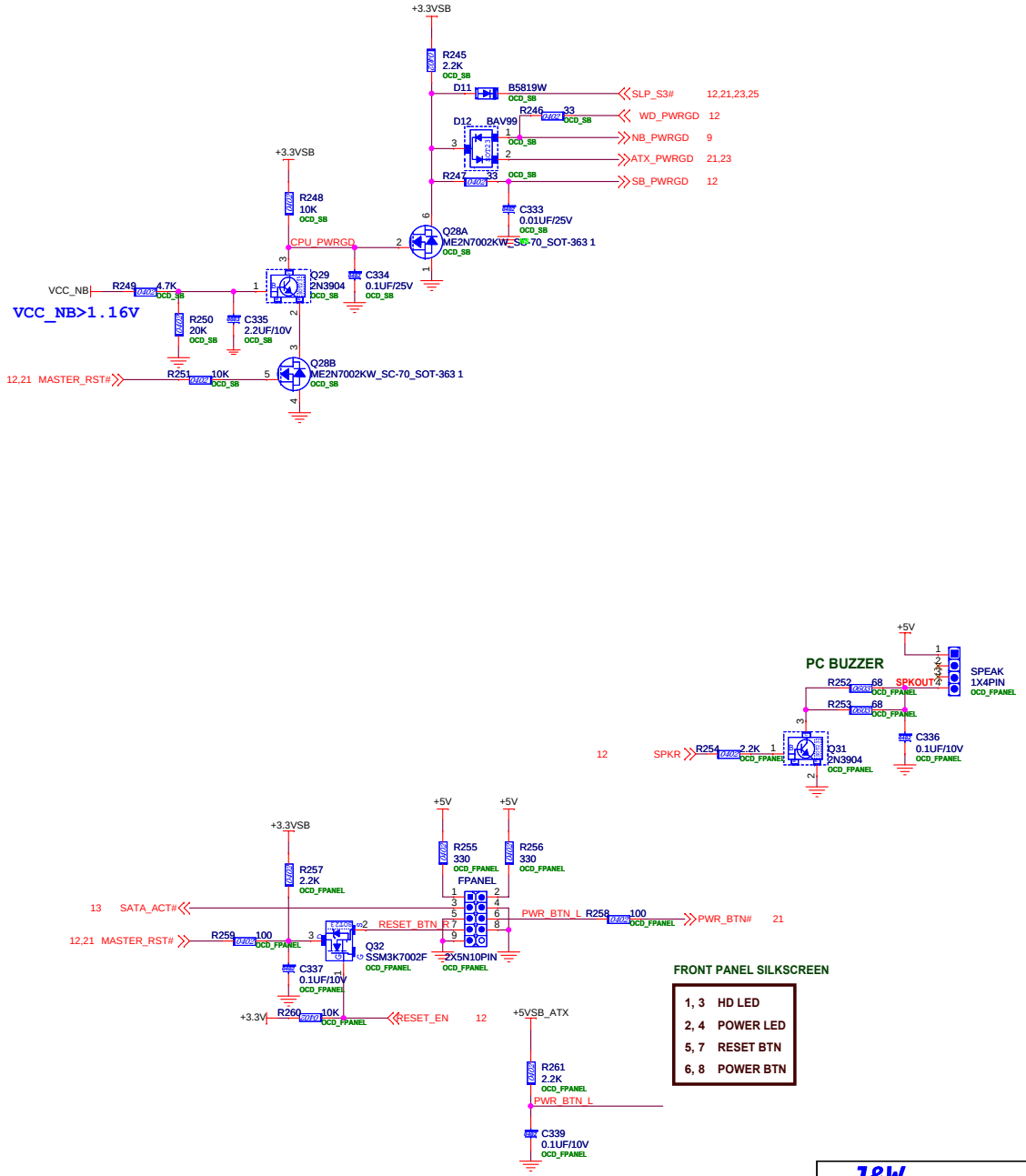

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Title: F_Panel, PWR_GD

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	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLCOK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLCOK

Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

FSB4	FSB3	FSB2	FSB1	FSB0	CPU	HTT(single) SEL_HTT=1	HTT(Differential) SEL_HTT=0	VCO	SRC	ATiG[3:0]	SB_SRC
0	1	1	1	1	200M	66M	100M	600M	100M	100M	100M

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases

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Title: RTM880N-790 CLOCK GEN

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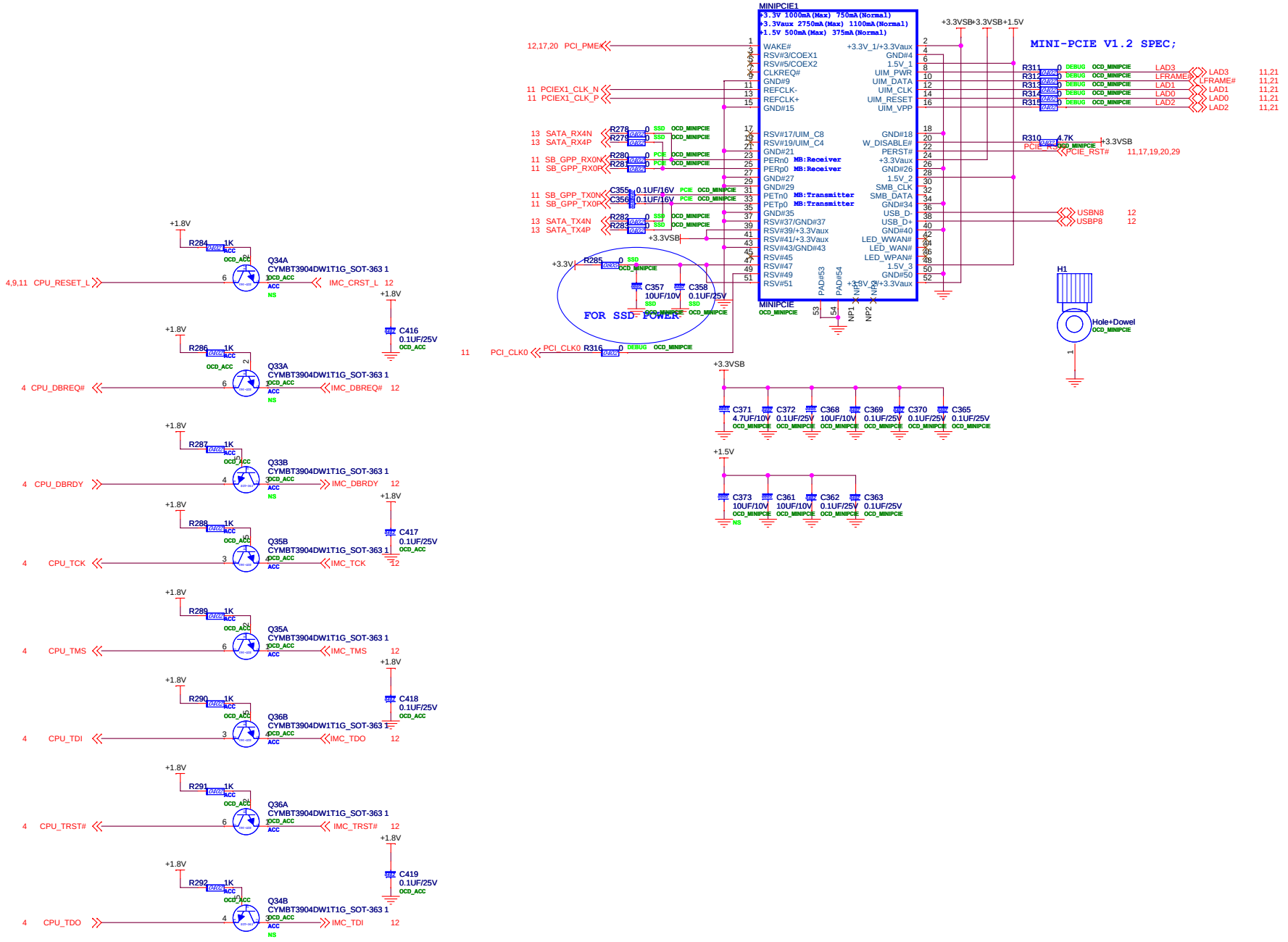

J&W		
Title: HDT		
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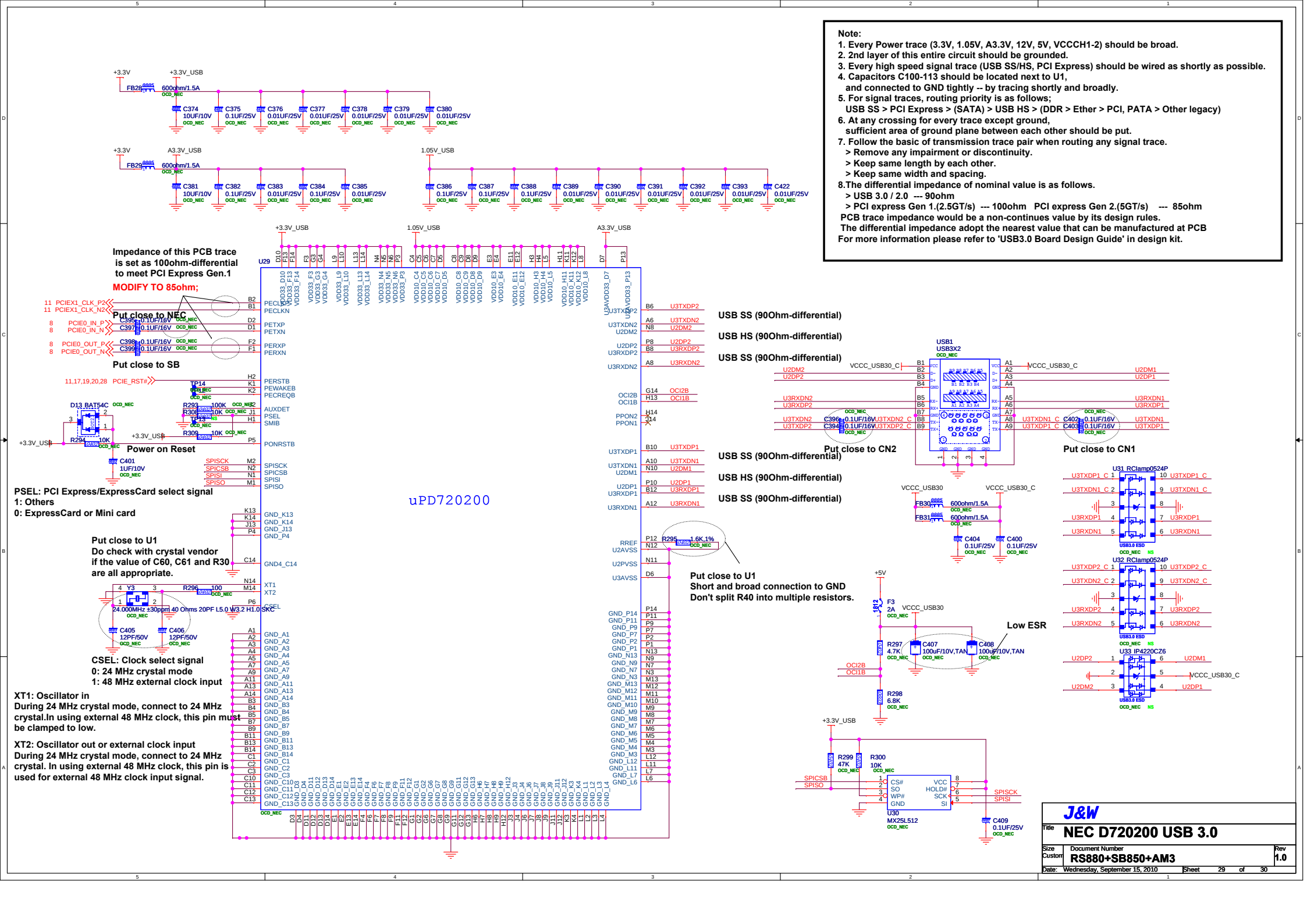
Note:
1. Every Power trace (3.3V, 1.05V, A3.3V, 12V, 5V, VCCCH1-2) should be broad.
2. 2nd layer of this entire circuit should be grounded.
3. Every high speed signal trace (USB SS/HS, PCI Express) should be wired as shortly as possible.
4. Capacitors C100-113 should be located next to U1,
and connected to GND tightly -- by tracing shortly and broadly.
5. For signal traces, routing priority is as follows;
USB SS > PCI Express > (SATA) > USB HS > (DDR > Ether > PCI, PATA > Other legacy)
6. At any crossing for every trace except ground,
sufficient area of ground plane between each other should be put.
7. Follow the basic of transmission trace pair when routing any signal trace.
> Remove any impairment or discontinuity.
> Keep same length by each other.
> Keep same width and spacing.
8.The differential impedance of nominal value is as follows.
> USB 3.0 / 2.0 --- 90ohm
> PCI express Gen 1.(2.5GT/s) --- 100ohm PCI express Gen 2.(5GT/s) --- 85ohm
PCB trace impedance would be a non-continues value by its design rules.
The differential impedance adopt the nearest value that can be manufactured at PCB
For more information please refer to 'USB3.0 Board Design Guide' in design kit.
+3.3V
+3.3V_USB
FB28 600ohm/1.5A
C374 10UF/10V
C375 0.1UF/25V
C376 0.01UF/25V
C377 0.01UF/25V
C378 0.01UF/25V
C379 0.01UF/25V
C380 0.01UF/25V
A3.3V_USB
FB29 600ohm/1.5A
C381 10UF/10V
C382 0.1UF/25V
C383 0.01UF/25V
C384 0.1UF/25V
C385 0.01UF/25V
1.05V_USB
C386 0.1UF/25V
C387 0.1UF/25V
C388 0.1UF/25V
C389 0.01UF/25V
C390 0.01UF/25V
C391 0.01UF/25V
C392 0.01UF/25V
C393 0.01UF/25V
C422 0.01UF/25V
Impedance of this PCB trace
is set as 100ohm-differential
to meet PCI Express Gen.1
MODIFY TO 85ohm;
Put close to NEC
Put close to SB
Power on Reset
PSEL: PCI Express/ExpressCard select signal
1: Others
0: ExpressCard or Mini card
Put close to U1
Do check with crystal vendor
if the value of C60, C61 and R30
are all appropriate.
Y3 24.000MHz ±30ppm 40 Ohms 20PF L5.0 W3.2 H1.0 SMD
C405 12PF/50V
C406 12PF/50V
CSEL: Clock select signal
0: 24 MHz crystal mode
1: 48 MHz external clock input
XT1: Oscillator in
During 24 MHz crystal mode, connect to 24 MHz crystal.In using external 48 MHz clock, this pin must be clamped to low.
XT2: Oscillator out or external clock input
During 24 MHz crystal mode, connect to 24 MHz crystal. In using external 48 MHz clock, this pin is used for external 48 MHz clock input signal.
uPD720200
USB SS (90Ohm-differential)
USB HS (90Ohm-differential)
USB SS (90Ohm-differential)
USB SS (90Ohm-differential)
USB HS (90Ohm-differential)
USB SS (90Ohm-differential)
USB1
USB3X2
Put close to CN2
Put close to CN1
U31 RClamp0524P
U32 RClamp0524P
U33 IP4220CZ6
R295 1.6K,1%
Put close to U1
Short and broad connection to GND
Don't split R40 into multiple resistors.
Low ESR
R297 4.7K
C407 100uF/10V,TAN
C408 100uF/10V,TAN
R298 6.8K
R299 47K
R300 10K
U30 MX25L512
C409 0.1UF/25V
J&W
NEC D720200 USB 3.0
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Title: HISTORY

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