SYNIC®
Intelligent Wireless

Data Sheet

Module name：IA9QH5 SY5-A24-F Module

Project Code：SMMSBRQHC58RH3

Version 1.5

Syncomm Technology Corp.

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1. Features

- 5.2GHz/5.8GHz ISM Band
- GFSK modulation
- Low BOM cost
- Long distance > 30m (Line of sight)
- Support 1-1 duplex mode or 1-N broadcasting mode
- Digital I2S audio interface
- Support no audio detection function
- Antenna diversity
- Short delay time variation
- Audio format 16/24bit , 32/44.1/48K/96KHz sampling rate
- Robust Packet error correction
- Low power consumption
- No RF induced audio noise
- Audio latency time < 20ms
  (Programmable according customized spec.)

2. Application

- Wireless HTiB Rear Speaker
- Wireless Outdoor Speaker
- Wireless TV theater
- Wireless Audio Sender
- Wireless Headphone
- Wireless Stereo Ear Microphone

3. RF Specification

Item	Min	Typ	Max	Unit	Note
Channel Range	5160	—	5240	MHz	
-20dB bandwidth	—	2.5	—	MHz	2M Mode
RF Output Power		11		dBm	Peak power at Antenna port
Sensitivity	—	-91	—	dBm	The smaller, the better

Table 1 5.2GHz RF Specification

Item	Min	Typ	Max	Unit	Note
Channel Range	5735	—	5840	MHz	
-20dB bandwidth	—	2.5	—	MHz	2M Mode
RF Output Power		11		dBm	Peak power at Antenna port
Sensitivity	—	-89	—-	dBm	The smaller, the better

Table 2 5.8GHz RF Specification

4. Audio Specification

2.1 CH						
	Item	Min	Typ	Max	Unit	Note
2.0 CH	SNR	90	94	—	dBr	@1kHz
	THD + N	—	-80	-75	dB	@1kHz, the smaller, the better
	Frequency Response	20	—	20k	Hz	@±1dB
	Dynamic range	90	94		dB	@1kHz
0.1 CH	SNR	90	94		dBr	@1kHz
	THD + N		-84	-80	dB	@1kHz, the smaller, the better
	Frequency Response	20		5k	Hz	@±3dB
	Dynamic range	90	94		dB	@1kHz

Note: Test condition is that using Card type EVB board with ADC: AK5357 at master mode and DAC: AK4386 at master mode.

Table 3 ADC to DAC

2.1 CH						
	Item	Min	Typ	Max	Unit	Note
2.0 CH	SNR	135	140		dBr	@1kHz
	THD + N		-100	-95	dB	@1kHz, the smaller, the better
	Frequency response	20		20k	Hz	@±1dB
	Dynamic range	95	100		dB	@1kHz
0.1 CH	SNR	130	135		dBr	@1kHz
	THD + N		-100	-95	dB	@1kHz, the smaller, the better
	Frequency response	20		5k	Hz	@±3dB
	Dynamic range	95	100		dB	@1kHz

Note: Test condition is that using sample rate 48 kHz, NFsCLK factor 512 and resolution 24.

Table 4 I2S to I2S

5. Electrical Specification

Item	Min	Typ	Max	Unit	Note
Power Supply Voltage	3.0	3.3	3.6	V	
Operating Temperature	0	25	55	℃	Operating temperature is ambient temperature that around module
2.1CH Audio Mode					
Consumption Current (TX_MODE)		210		mA	RF Power :11dBm No GPIO driving
Consumption Current (RX_MODE)		103		mA	
0.1CH Audio Mode					
Consumption Current (TX_MODE)		132		mA	RF Power :11dBm No GPIO driving
Consumption Current (RX_MODE)		91		mA	

Table 5

Item						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
V_{IH}	Input High Threshold	2.0	—	3.33	V	LDO_OUT=3V
V_{IL}	Input Low Threshold	-0.3	—	0.8	V	LDO_OUT=3V
V_{OH}	Output High Threshold	2.4	—	—	V	LDO_OUT=3V
V_{OL}	Output Low Threshold	—	—	0.4	V	LDO_OUT=3V

Table 6

◆ Power On Reset Characteristics

Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
Trst			10		mS	

Table 7

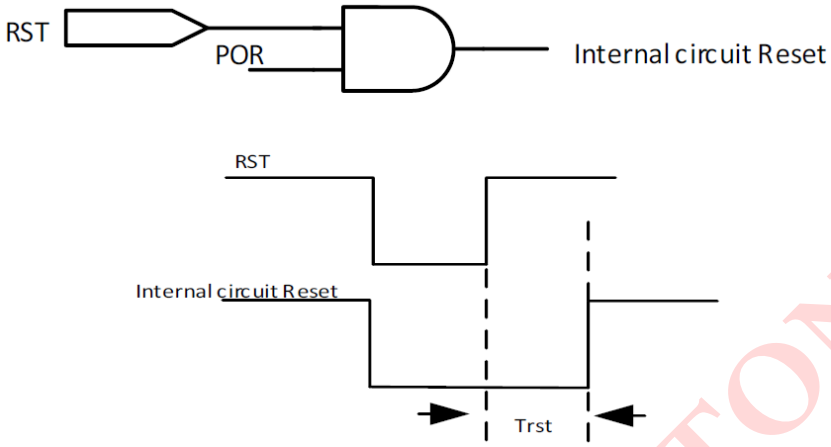


Fig 5.1 Power On Reset Timing Chart

6. Mechanical Specification

6.1 No Shielding Case

- Dimension：35 * 35 * 3 mm
- PCB 4 Layers

Mechanical Drawing：

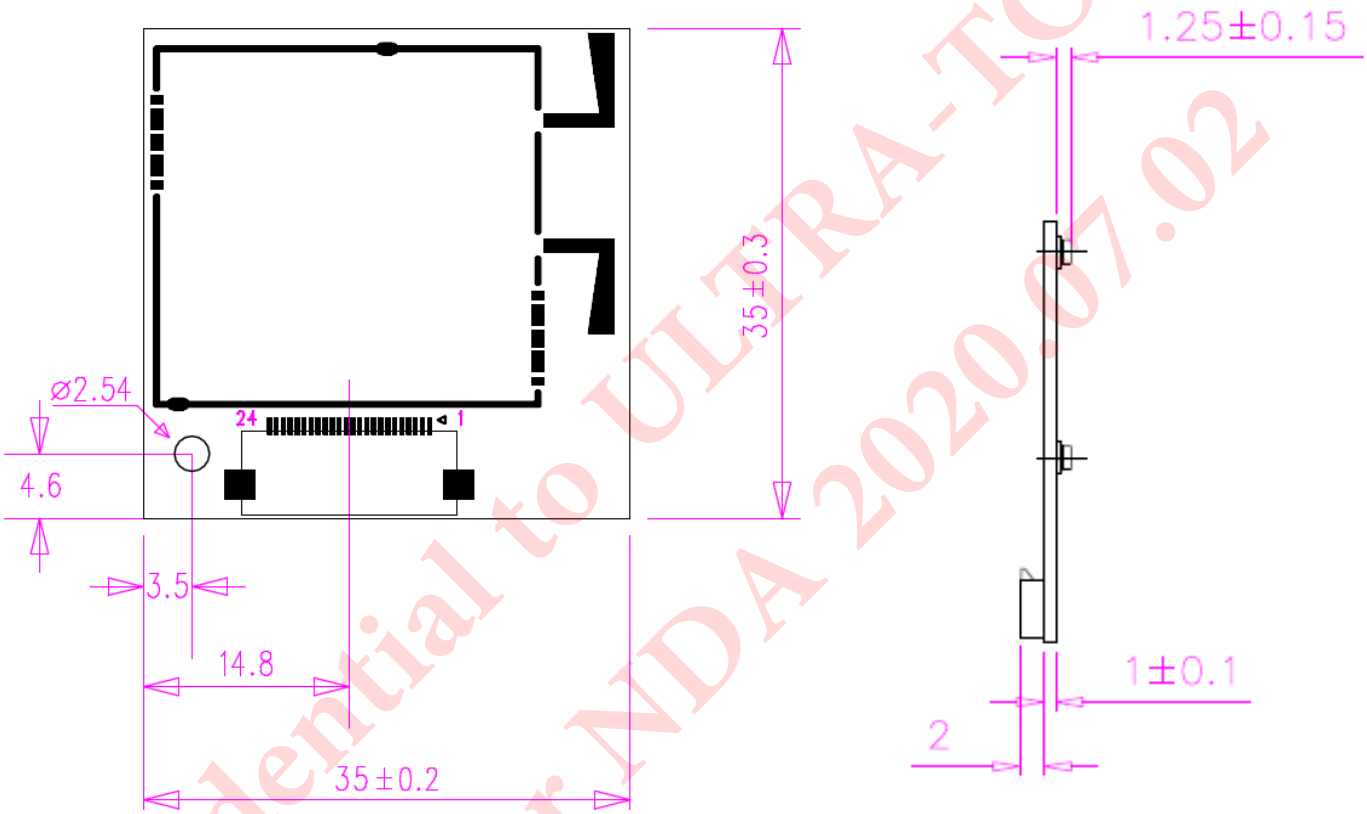


Fig 6.1 Mechanical Drawing of SY5-A24-F Module

◆ The length of FPC cable must be ≦ 10cm and use shielded type for EMI Test

6.2 With Shielding Case

- Dimension：35 * 35 * 3 mm
- PCB 4 Layers

Mechanical Drawing：

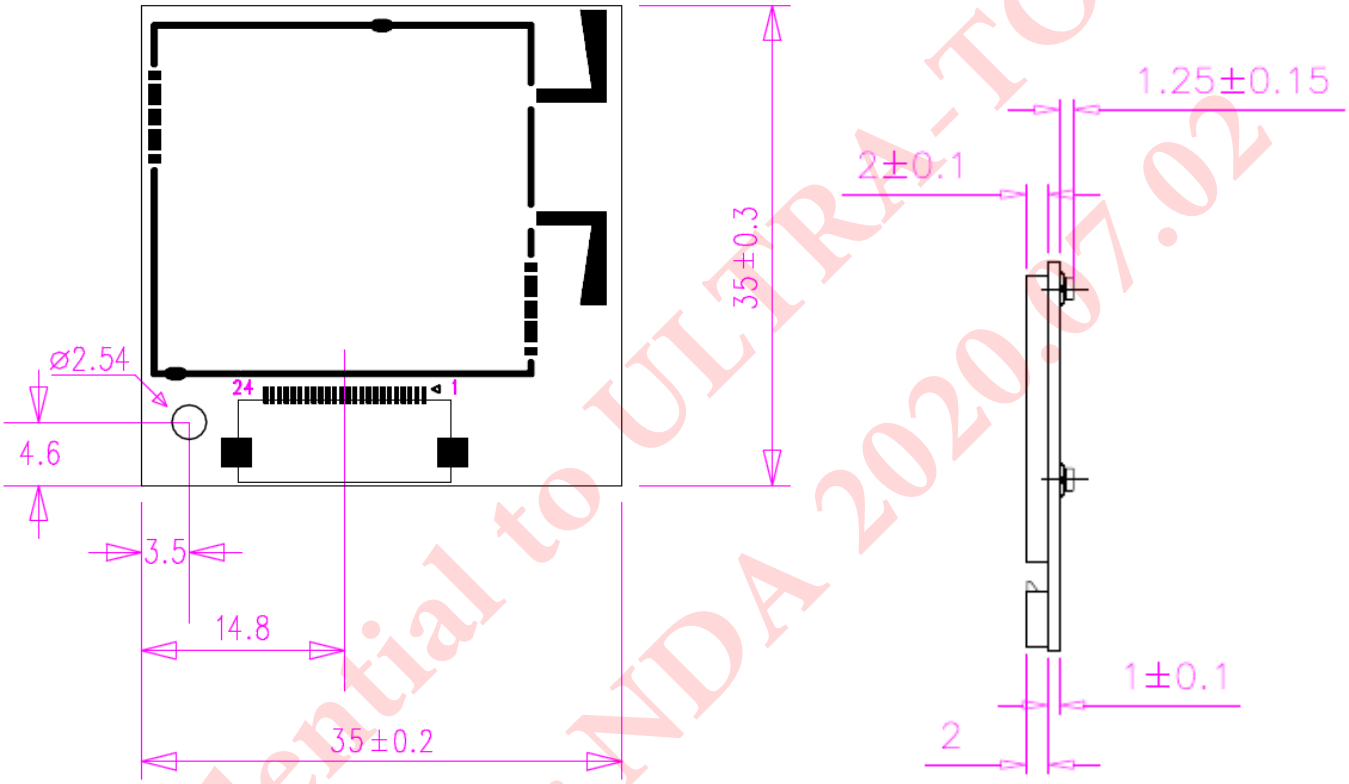


Fig 6.2 Mechanical Drawing of SY5-A24-F Module with shielding case

◆ The length of FPC cable must be ≦ 10cm and use shielded type for EMI Test

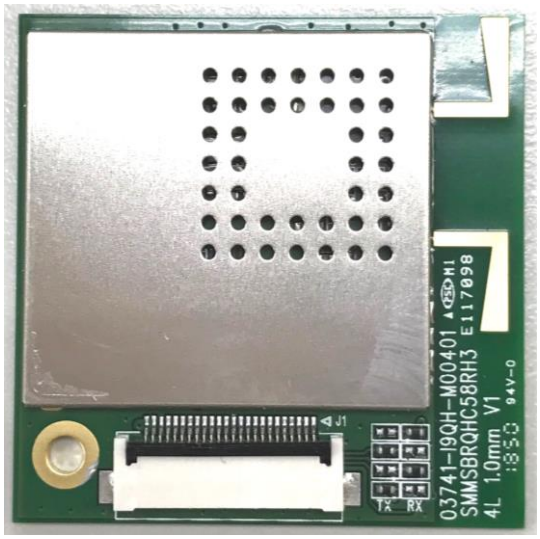


Fig 6.3 SY5-A24-F Module TX / RX with shielding case Top View

Part Number:
1. **1A5TI-I9QH-21T100 (TX)**
2. **1A5TI-I9QH-21T200 (RX)**
3. 1A5TI-I9QH-21T1PK (TX)
4. 1A5TI-I9QH-21T2PK (RX)

Fig 6.4 SY5-A24-F Module TX / RX without shielding case Top View

Part Number:
1. **1A5TI-I9QH-31T100 (TX)**
2. **1A5TI-I9QH-31T200 (RX)**
3. **1A5TI-I9QH-31T1PK(TX)**
4. **1A5TI-I9QH-31T2PK(RX)**

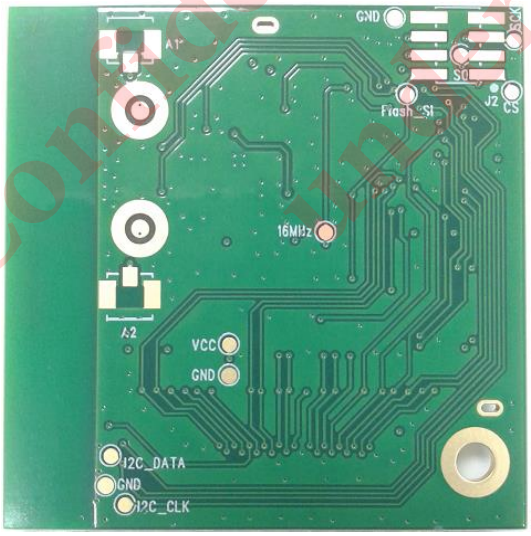
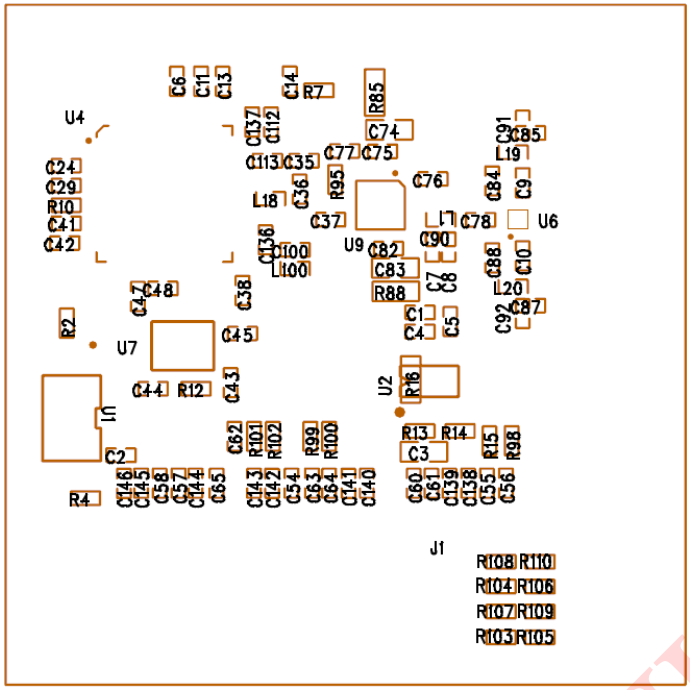
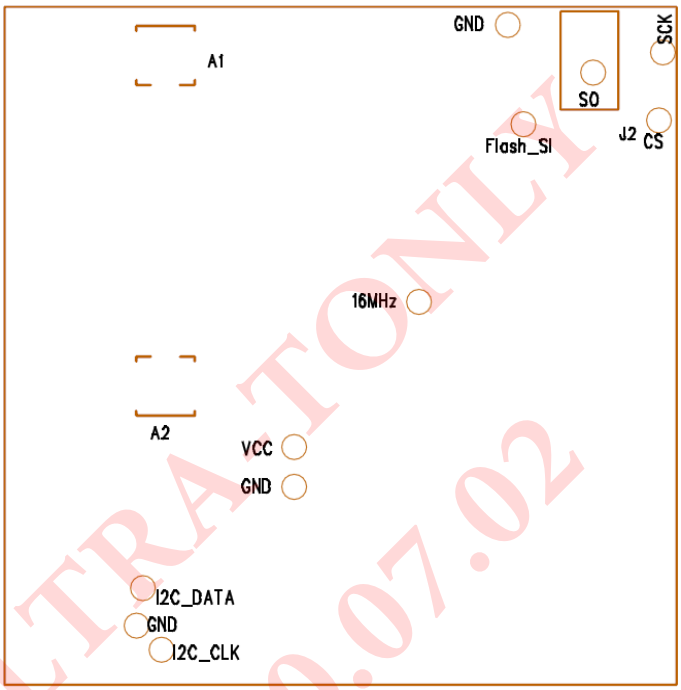


Fig 6.5 SY5-A24-F Module TX / RX Button View

Part Number:
1. **1A5TI-I9QH-21T100 (TX)**
2. **1A5TI-I9QH-31T100 (TX)**
3. **1A5TI-I9QH-21T200 (RX)**
4. **1A5TI-I9QH-31T200 (RX)**
5. 1A5TI-I9QH-21T1PK (TX)
6. 1A5TI-I9QH-21T2PK (RX)
7. **1A5TI-I9QH-31T1PK(TX)**
8. **1A5TI-I9QH-31T2PK(RX)**





7. Block Diagram

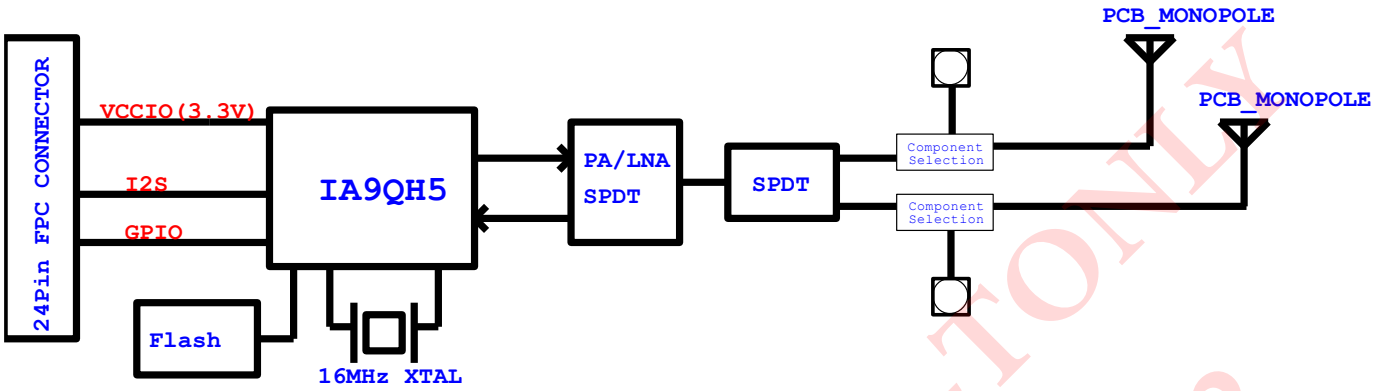


Fig 7.1 Block Diagram of IA9QH5 SY5-A24-F Module

8. Interface

Fig 8.1 Pin sequence of SY5-A24-F Module

Pin	Name	I/O	Pin Function Define
1	GPIO0	I/O	GPIO
2	GPIO15	I/O	GPIO
3	I2C_DATA	I/O	I2C Master/Slave data signal , must be connected to VCC via a pull high resistor
4	I2C_CLK	I/O	I2C Master/Slave clock signal , must be connected to VCC via a pull high resistor
5	GPIO26	I/O	GPIO
6	GPIO27	I/O	GPIO
7	GPIO 32	I/O	GPIO
8	GPIO 13	I/O	GPIO
9	SPB_I2S_BCK	I/O	SPB I2S audio BCK
10	SPB_I2S_LRCK	I/O	SPB I2S audio LRCK
11	SPB_I2S_MCLK	I/O	SPB I2S audio MCLK
12	DGND	P	Digital GND
13	SPA_I2S_BCK	I/O	SPA I2S audio BCK
14	SPA_I2S_LRCK	I/O	SPA I2S audio LRCK
15	SPA_I2S_DATA	I/O	I2S DATA 0
16	SPB_I2S_DATA	I/O	SPB I2S audio Data
17	GPIO 21	I/O	GPIO
18	GPIO 30	I/O	GPIO
19	GPIO 16	I/O	GPIO
20	GPIO 17	I/O	GPIO
21	GPIO 14	I/O	GPIO
22	DGND	P	Digital GND
23	VCCIO	P	DC 3.3V IN
24	VCCIO	P	DC 3.3V IN

Table 8 IO Function Define

9. Design Reference

*. ADC/DAC Reference Design

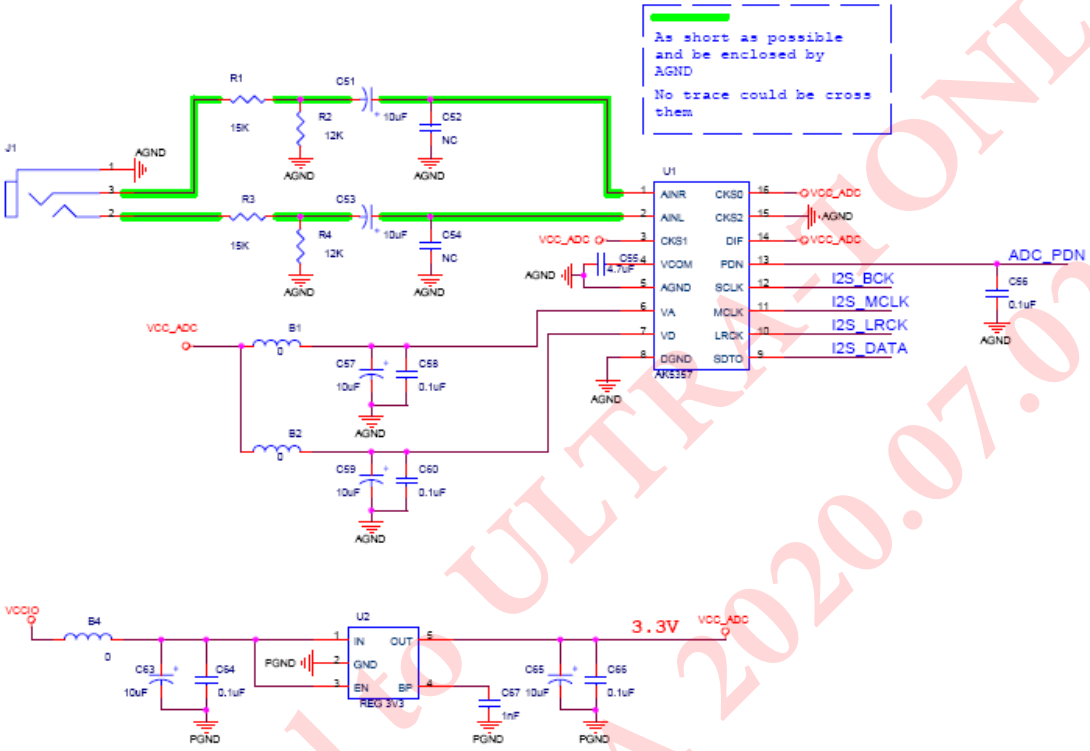


Fig 9.1 ADC reference design circuit

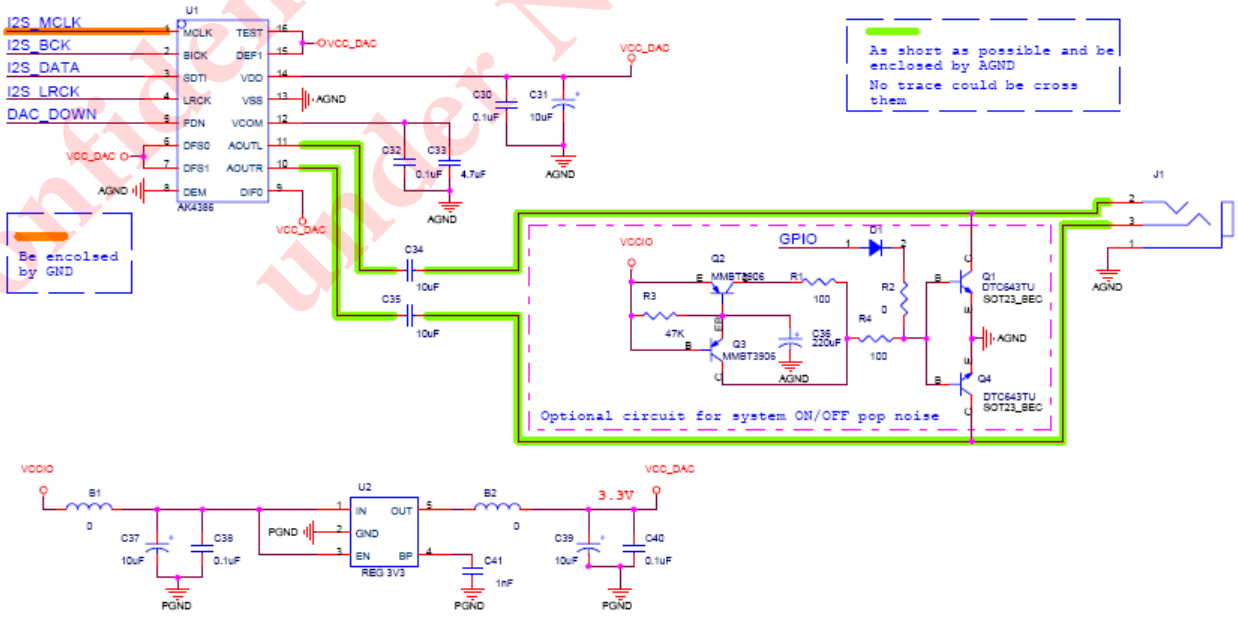


Fig 9.2 DAC reference design circuit

10. I²S Interface

I²S interface is supported by pin Sound Port A&B (SPA&SPB). Sound Port A (SPA), including SPA0, SPA1, SPA2 and SPA3, are defined as I2S_MCLK, BCK, LRCK, and I2S_DATA respectively. Sound Port B (SPB), including SPB0, SPB1, SPB2, and SPB3, are also defined as I2S_MCLK, BCK, LRCK, and I2S_DATA respectively.

IA9QH5 I²S audio interface can work for master and slave mode.

In master mode, **IA9QH5** generate I2S_MCLK/LRCK/BCK for external audio codec. In slave mode, **IA9QH5** accept external LRCK/BCK signal. **IA9QH5** will synchronize with external audio clock. Mono channel data can feed through left channel (Lch) pr right channel (Rch) as Figure 10.1

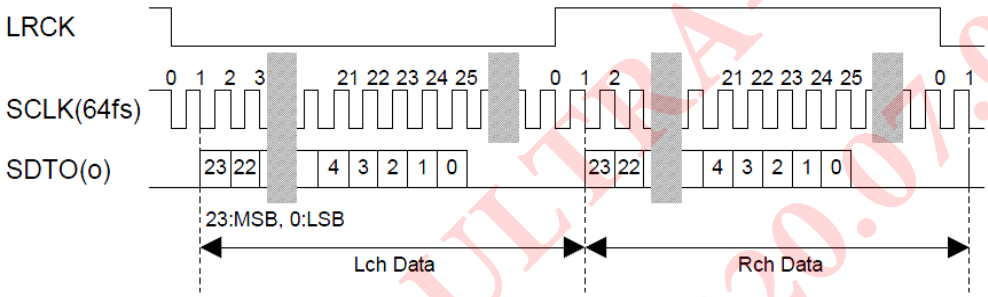


Figure 10.1 I²S Signal

I²S timing chart is shown Figure 10.2 and Table 9

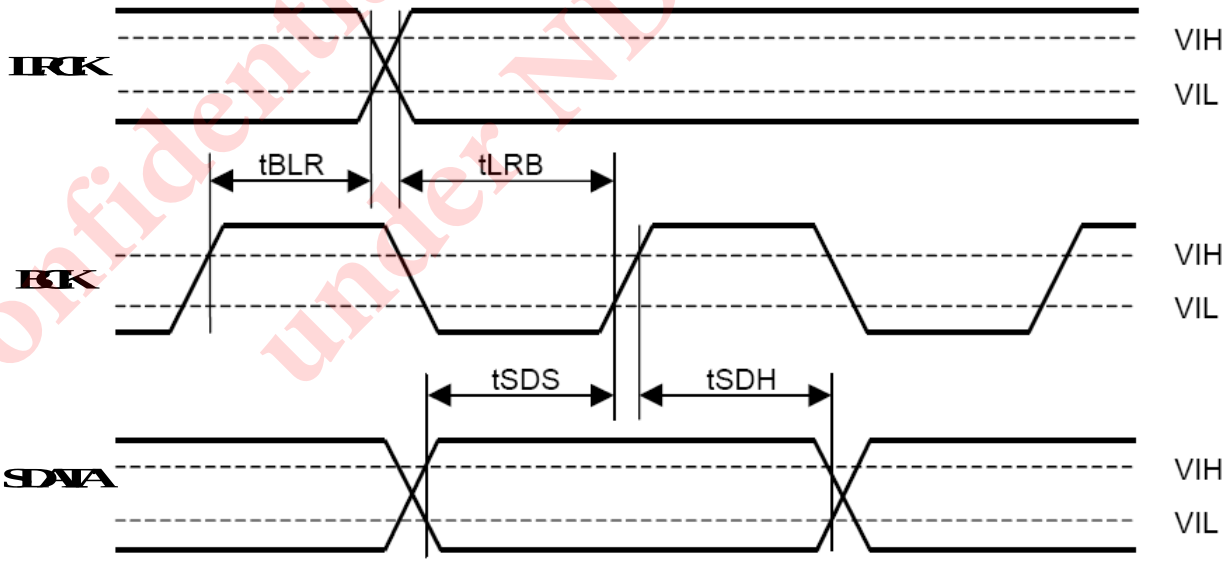


Fig 10.2 I2S timing chart

Symbol	Parameter	Min	Typ	Max	Unit
tBLR	BCK rising to LRCK edge	60			ns
tLRB	LRCK edge to BCK rise	60			ns
tSDS	SDATA setup time	60			ns
tSDH	SDATA hold time	60			ns

Table 9

Audio output clock jitter is shown Table 10

Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
ΔI2S_MCLK	Locking range vs nominal I2S_MCLK frequency	-800		+800	ppm	256Fs

Table 10 Audio Output clock Jitter

11. DC Power Supply

11.1 Power-On Timing

On Board Flash power on timing is shown Figure 11.1 and Table 11

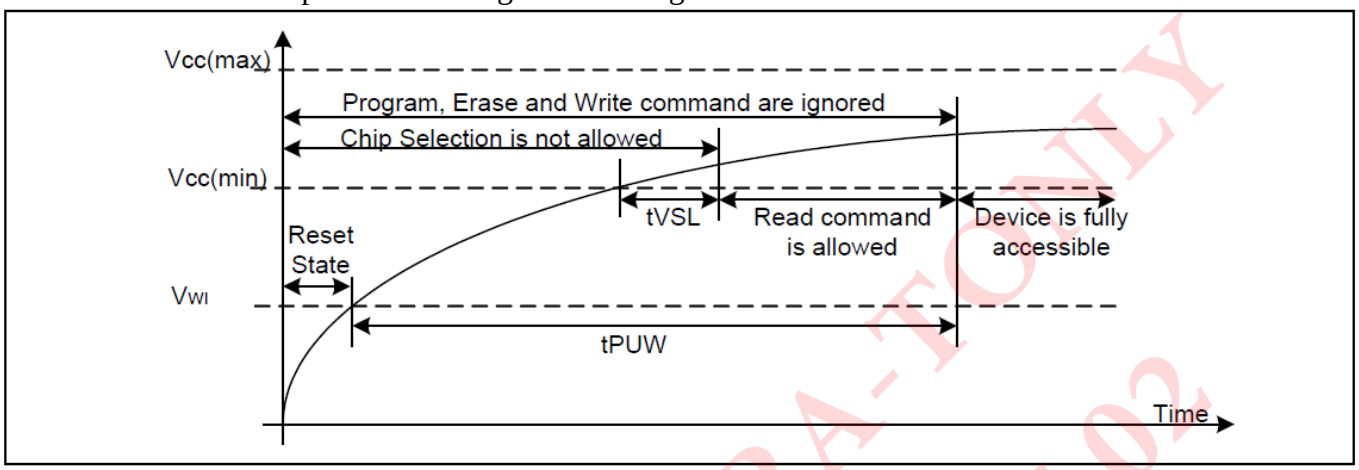


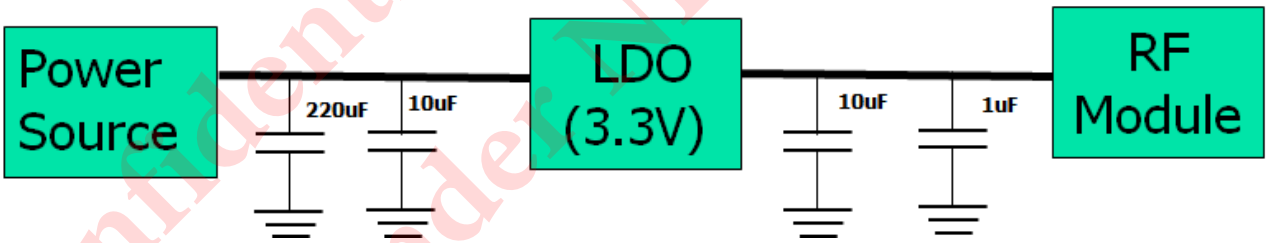
Fig 11.1 On Board Flash Power On Timing

Symbol	Parameter	Min	Max	Unit
tVSL	VCC(min) To CS# Low	10		us
tPUW	Time Delay From VCC(min) To Write Instruction	1	10	ms
VWI	Write Inhibit Voltage VCC(min)	1	2.5	V

Table 11

11.2 DC Power

Recommend system DC power supply for IA9QH5 SY5-A24-F Module as below :



Long power supply lines on the PCB should be avoided. VCC connections and VCC bypass capacitors must be connected as close as possible to SY5-A24-F module. Power supply ripple of module side must be below 150mVpp to ensure RF normal operation.

LDO Spec.:

- ⇨ **High PSRR Low Dropout Voltage Linear Regulators**
- ⇨ **Iout ≧ 500mA**
- ⇨ **PSRR ≧ 65dB**

12. Antenna Application

12.1 Suggested Clear Area

The recommended antenna clearance for embedded PCB antennas are shown below. Note that this clearance should be maintained when mounting the module on a motherboard.

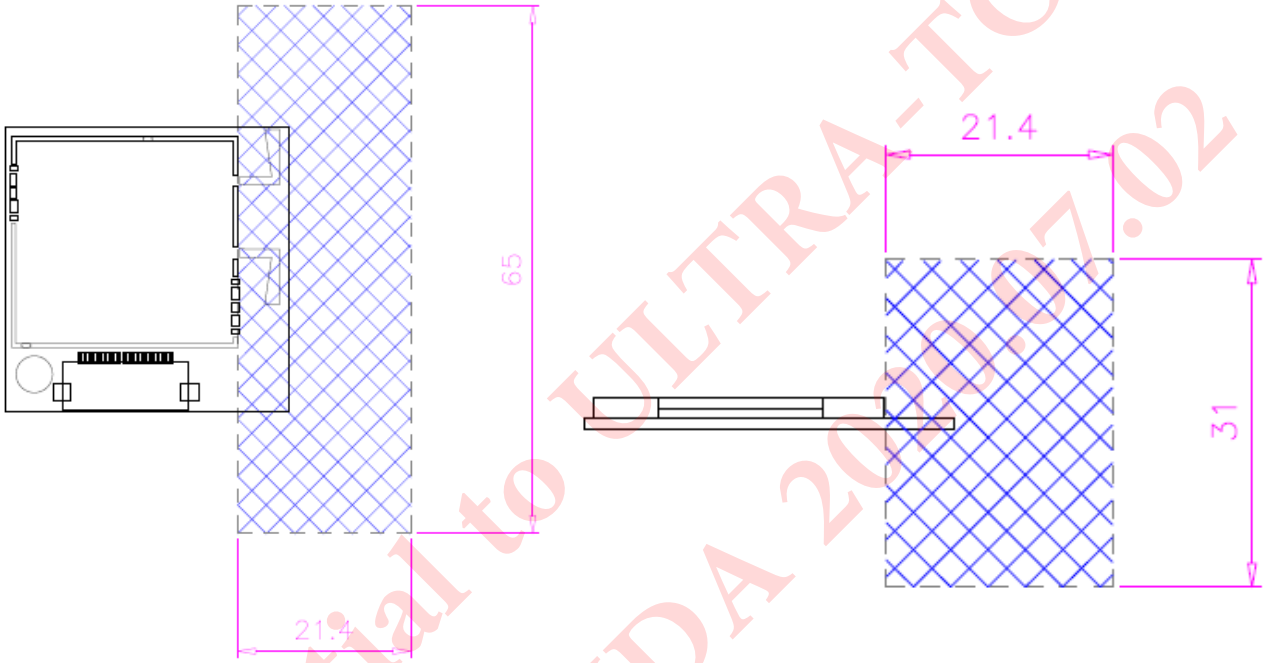
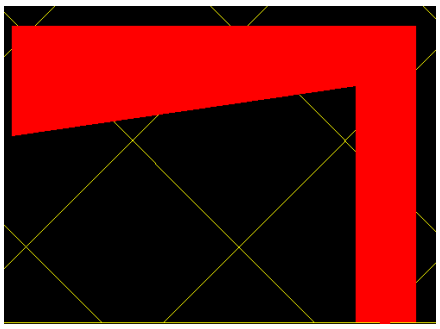


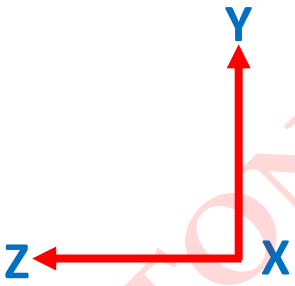
Fig 10.1 Antenna Clearance Recommendations from Top and Side View

Do not place any copper, metal or even PCB in the area marked with cross lines.

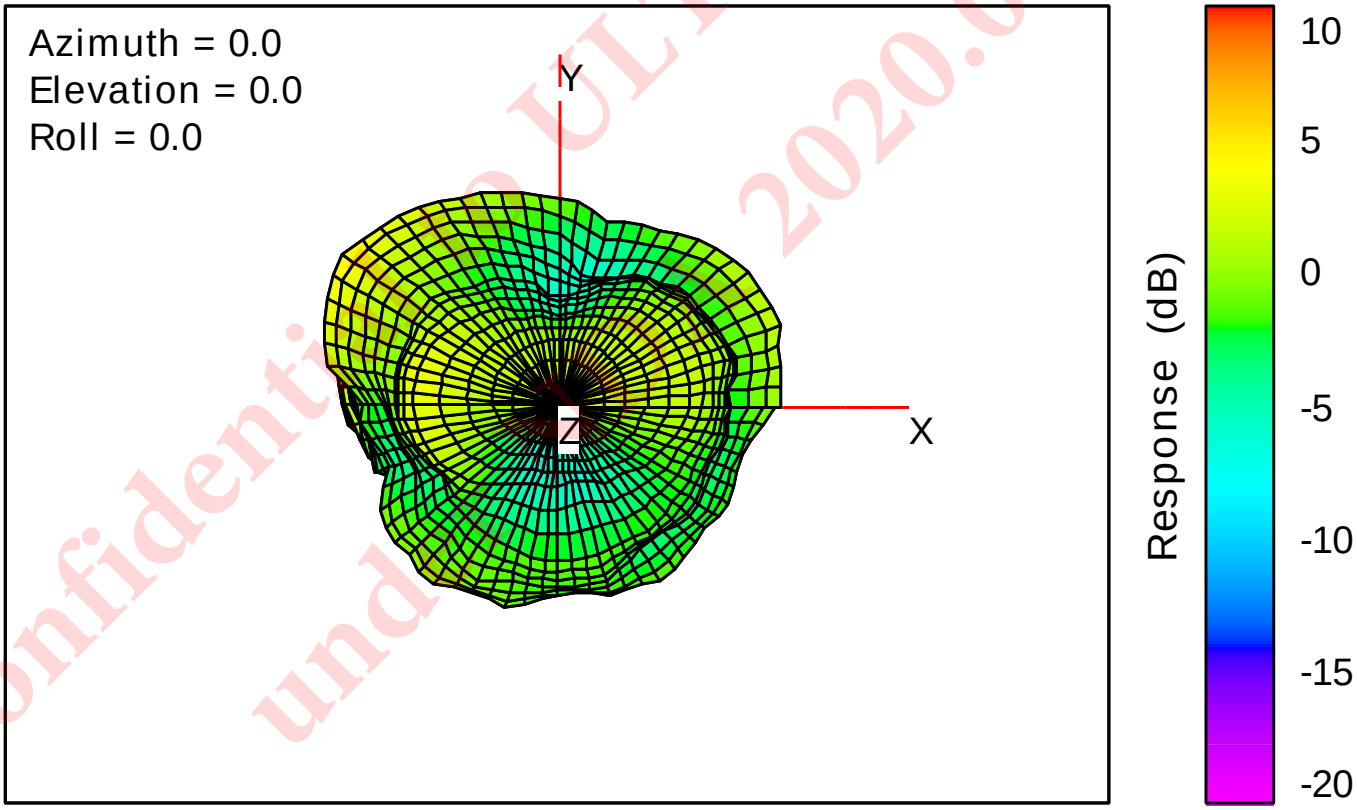
Unit : mm

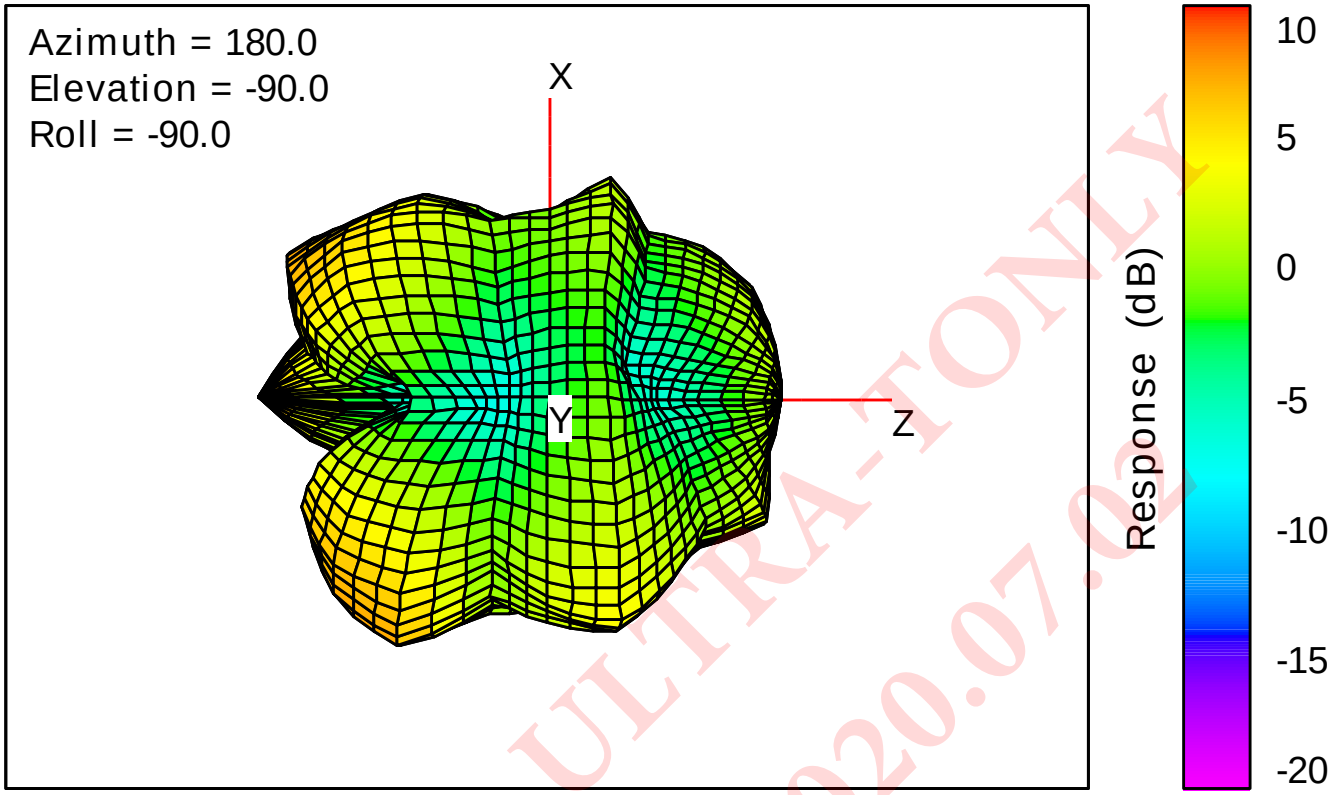
12.2 Antenna Pattern

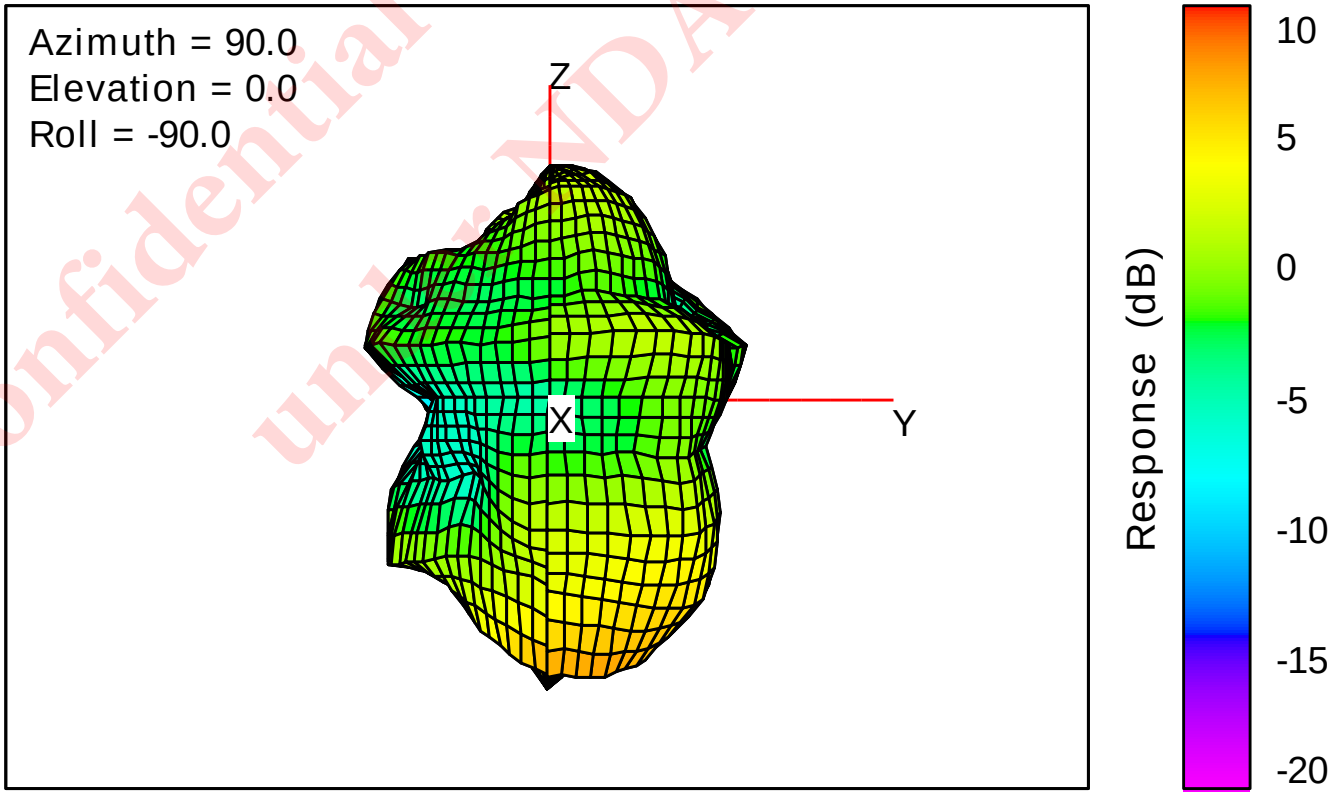




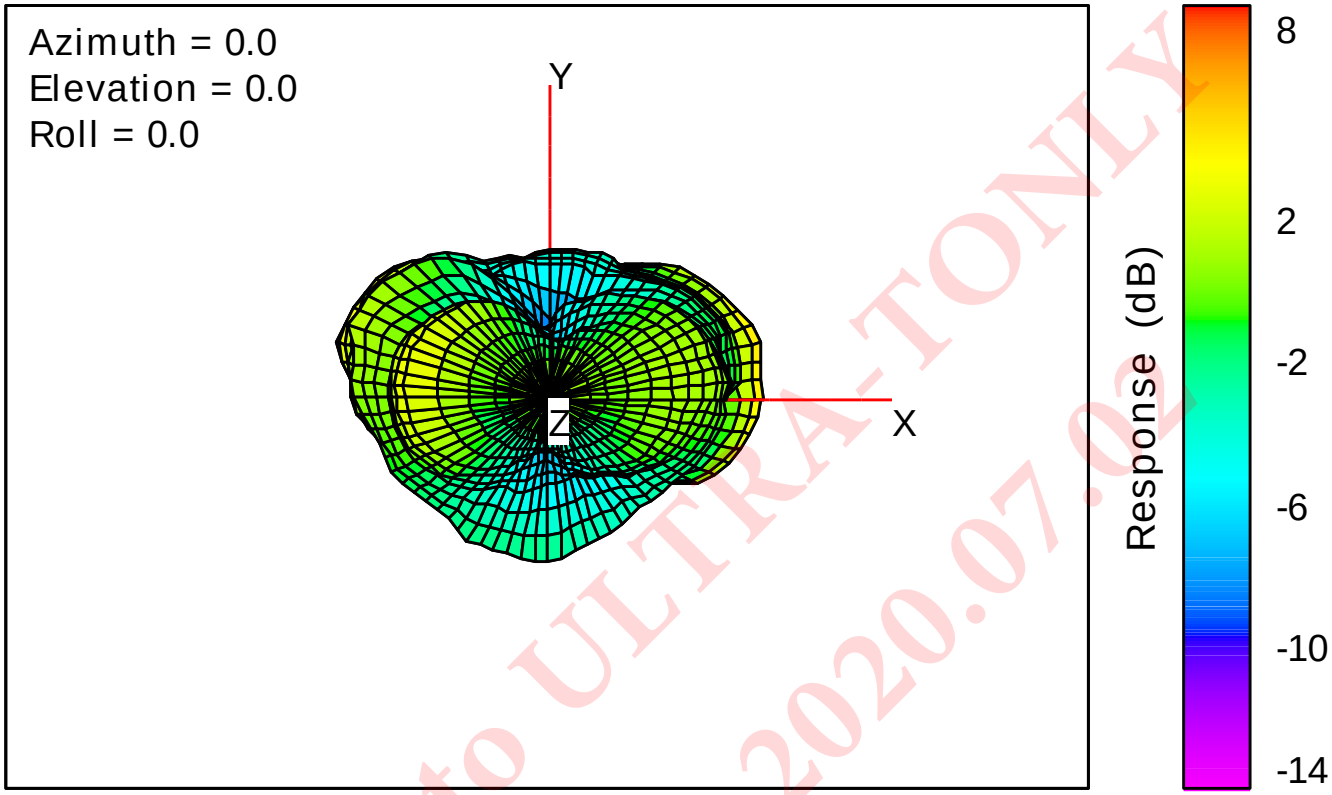
Frequency: 5805 MHz

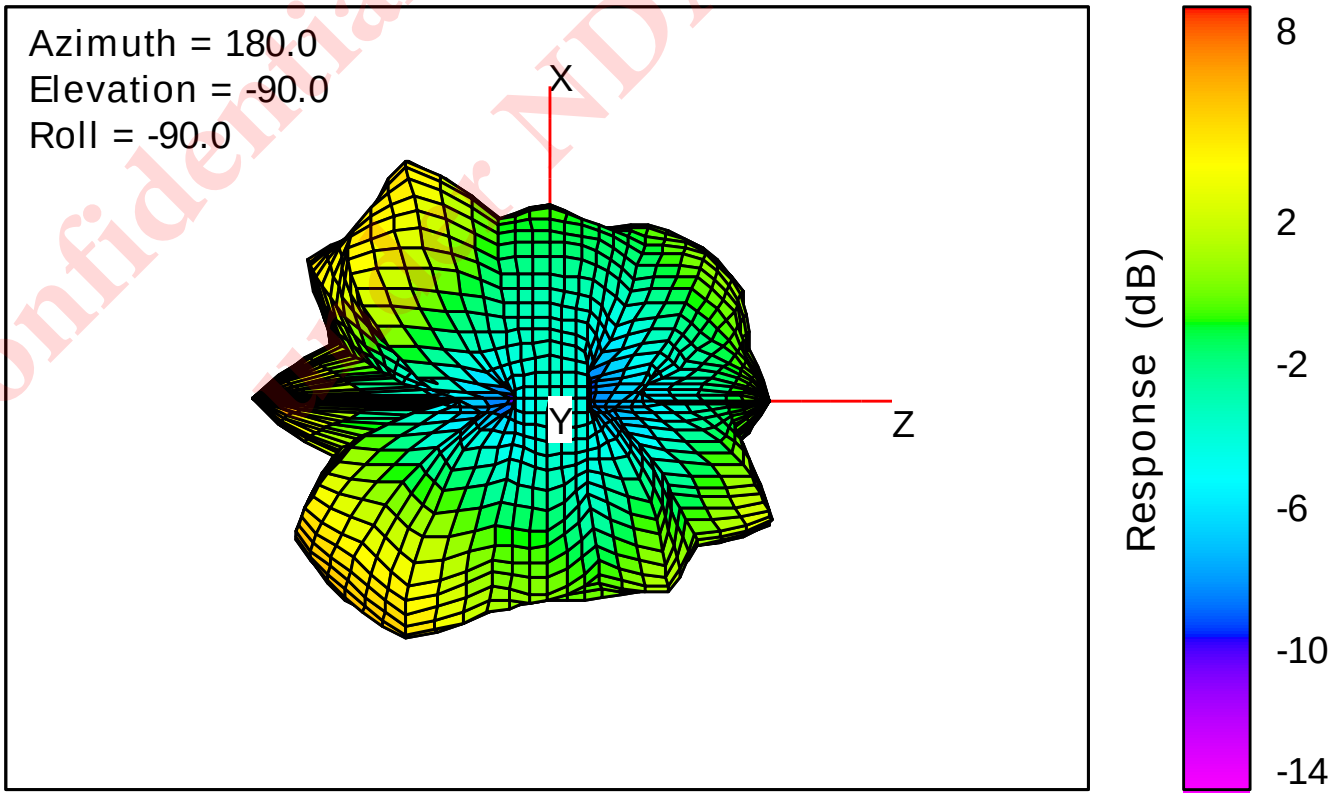


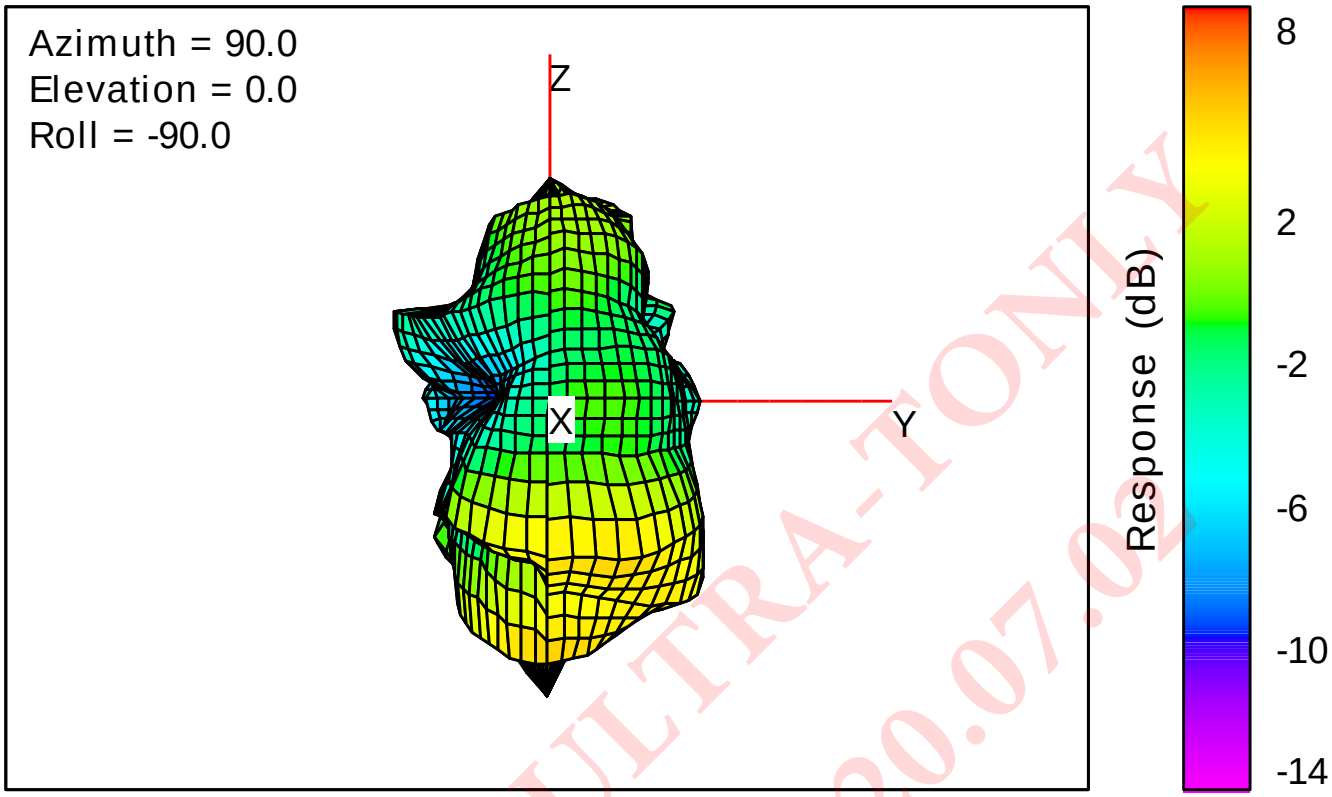




Frequency: 5205 MHz







Max Antenna Gain：2.5 dBi

13. Ordering Information

TX Part Number	Description	Notes
1A5TI-I9QH-21T100	IA9QH5 SY5-A24-F Module_FPS	Non MHF + shielding
1A5TI-I9QH-21T1PK	IA9QH5 SY5-A24-F Module_FPS	Non MHF + shielding
1A5TI-I9QH-31T100	IA9QH5 SY5-A24-F Module_FP	Non MHF + Non shielding
1A5TI-I9QH-31T1PK	IA9QH5 SY5-A24-F Module_FP	Non MHF + Non shielding

RX Part Number	Description	Notes
1A5TI-I9QH-21T200	IA9QH5 SY5-A24-F Module_FPS	Non MHF + shielding
1A5TI-I9QH-21T2PK	IA9QH5 SY5-A24-F Module_FPS	Non MHF + shielding
1A5TI-I9QH-31T200	IA9QH5 SY5-A24-F Module_FP	Non MHF + Non shielding
1A5TI-I9QH-31T2PK	IA9QH5 SY5-A24-F Module_FP	Non MHF + Non shielding

Table 12

14. Revision History

Date	Revision	Descriptions
2018/11/08	0.1	First release
2018/12/24	0.2	Modify interface pin description
2019/10/24	1.0	Add ordering information
2019/12/06	1.1	Add Module with shielding case photo
2020/02/10	1.2	Add I2S Jitter and DC Power spec.
2020/03/12	1.3	Change Module with MHF connector photo
2020/04/09	1.4	Change ordering information and antenna pattern
2020/04/09	1.5	Change ordering information

Table 13