OV550-B49 Camera Bridge Processor

General Description

The OV550 Camera Bridge Processor is a low cost, enhanced single-chip processor for USB 2.0 PC camera applications, capable of supporting up to 5.0 Megapixel sensors for game console applications. When combined with an OmniVision VGA, 1.3 Mpixel, 2.0 Mpixel, 3.2 Mpixel, or 5.0 Mpixel digital CAMERACHIP™, the OV550 comprises an integrated USB 2.0 camera system, with no additional USB transceiver or DRAM required. The OV550 also supports full video operation.

Note: The OV550-B49 is available in a lead-free package.

Features

General Features

- Low cost, low powered image processor that supports up to 5.0 Megapixel sensors
- Maximum pixel clock running at 48 MHz: 30 fps for 1.3MP Raw mode, 15 fps for 1.3MP YUV mode
- Supports USB Video Class with uncompressed format
- Serial Camera Control Bus (SCCB) Master Controllers

CAMERACHIP Interfaces

- Up to 5 Megapixel
- 10-bit RGB interface
- 8-bit YUV interface

Host Interface - USB 2.0

- Supports USB Video Class with uncompressed format
- Supports both isochronous and bulk endpoint for video transfer

Embedded 8-bit Microcontroller

- Embedded 512-Byte data memory
- Embedded 12KB program memory

Miscellaneous

- Embedded 3.3V to 1.8V regulators
- Embedded PLL
- Optional external serial EEPROM
- General Purpose I/O (GPIO)
- Power-down control

Ordering Information

Product	Package
OV0550-LB30	BGA-49 (Lead-free)

Applications

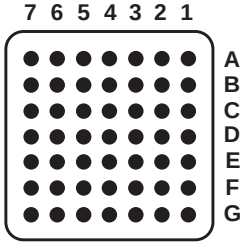
- USB 2.0 applications combined with the following OmniVision CAMERACHIP families:
  - OV56xx (5.0 MegaPixel)
  - OV36xx (3.2 MegaPixel)
  - OV26xx (2.0 MegaPixel)
  - OV96xx (1.3 MegaPixel)
  - OV86xx (SVGA)
  - OV76xx (VGA)
  - OV66xx (CIF)

NOTE: The OV550 supports digital image sensors up to 5.0 Megapixel resolution. However, it will not support analog image sensors (OVx9xx or OVx4xx products)

Key Specifications

Power Supply	**Core**	1.8 V
	I/O	3.3V
	Regulator Input	3.3V
Power Requirements	**Active**	TBD
	Standby	TBD
Temperature Range		TBD
Package Dimensions		6.00 mm x 6.00 mm

Figure 1 OV550-B49 Pin Diagram



	7	6	5	4	3	2	1
A	IO_VDD2	OSCEN	TM	GPIO1	GPIO0	SIO_C	SIO_D
B	RESET_	GPIO4	IO_VSS2	IO_VDD1	Y[1]	Y[0]	GPIO2
C	XIN	XOUT	CORE_VSS2	Y[4]	Y[3]	Y[2]	IO_VSS1
D	USB_VSSA2	VRES	CORE_VDD2	PCLK	CORE_VSS1	CCLK	Y[5]
E	USB_VDDL	USB_VSSL	USB_VDDA2	Y[8]	Y[7]	Y[6]	CORE_VDD1
F	DM	USB_VSSA1	USB_VDDD	SPWDN	VSYNC	HREF	Y[9]
G	DP	RPU	USB_VDDA1	ROUT_VDD1	REG_VSS18	RIN_VDD18	GPIO3

Functional Description

Figure 2 shows the functional block diagram of the OV550 processor. The OV550 includes:

- Camera Interface
- USB Converter
- Host Controller
- SCCB Master Controller
- Microcontroller
- System Controller

Camera Interface

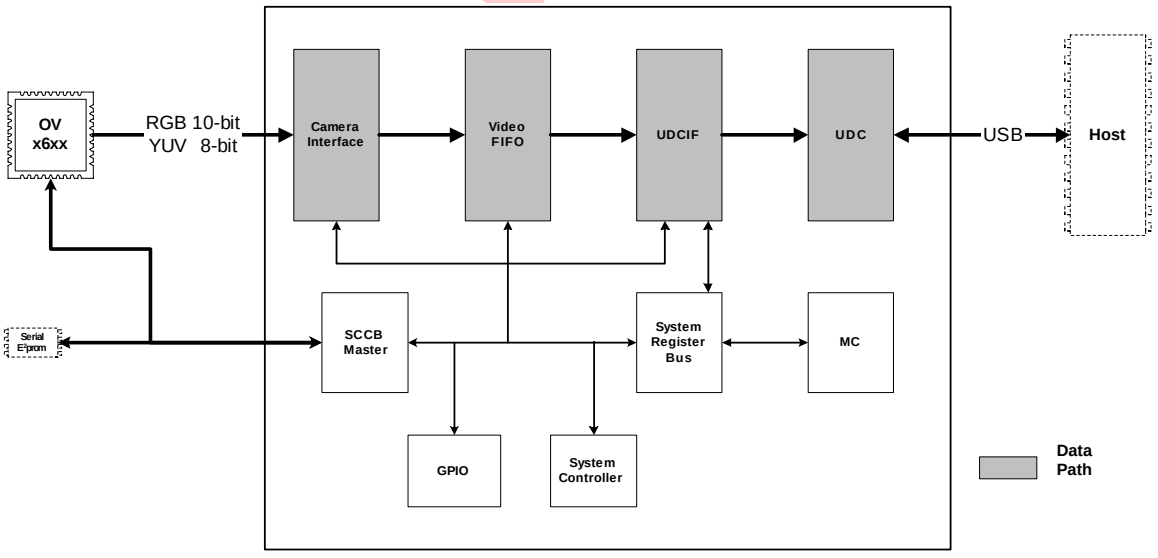
The Camera Interface takes either 10-bit RGB raw data or 8-bit YUV data from a maximum 5 Megapixels image sensor. The maximum pixel clock runs at 48MHz to support 30 fps for 1.3 Megapixel RAW mode or 15 fps for 1.3 Megapixel YUV mode.

The Camera Interface can interface with the image sensor CCIR656 and CCIR601 modes.

Host Controller

The OV550 uses USB2.0 to communicate with the Host Controller and supports USB video class with uncompressed format.

Figure 2 Functional Block Diagram



SCCB Master Controller

The SCCB Master Controller controls sensor registers. It is possible for the SCCB Master Controller to interface with an optional external EEPROM for downloading firmware to the program memory of the Microcontroller when the system is powered up.

Microcontroller

The OV550 is embedded with an 8-bit microcontroller with 512-Byte data memory and 12KB program memory. It provides the flexibility of decoding protocol commands from the host for controlling the system, as well as fine-tuning image qualities.

System Controller

The System Controller provides some system functions, such as GPIO and power down functions.

Pin Description

Table 1 Pin Description by Function

Ball Number	Name	Pin Type	Function/Description
System Control			
F4	SPWDN	I/O	Sensor Power Down General Purpose I/O Default: Output 1
A3	GPIO0	I/O	General Purpose I/O Audio interface synchronization signal Default: Output 0
A4	GPIO1	I/O	General Purpose I/O Audio interface clock signal Default: Output 1
B1	GPIO2	I/O	General Purpose I/O Default: Input
G1	GPIO3	I/O	General Purpose I/O Default: Input
B6	GPIO4	I/O	General Purpose I/O Default: Input
B7	RESET_	Input	Power On Reset 0: Reset
C6	XOUT	Output	Crystal Output
C7	XIN	Input	Crystal Input
A5	TM	Input	Test Mode Enable
A6	OSCEN	Output	Crystal Enable
Camera Interface			
B2	Y[0]	I/O	Sensor Data Y[0] General Purpose I/O Default: Input of sensor data Y[0]
B3	Y[1]	I/O	Sensor Data Y[1] General Purpose I/O Default: Input of sensor data Y[1]
C2	Y[2]	I/O	Sensor Data Y[2] General Purpose I/O Default: Input of sensor data Y[2]
C3	Y[3]	I/O	Sensor Data Y[3] General Purpose I/O Default: Input of sensor data Y[3]

Table 1 Pin Description by Function (Continued)

Ball Number	Name	Pin Type	Function/Description
C4	Y[4]	I/O	Sensor Data Y[4] General Purpose I/O Default: Input of sensor data Y[4]
D1	Y[5]	I/O	Sensor Data Y[5] General Purpose I/O Default: Input of sensor data Y[5]
E2	Y[6]	I/O	Sensor Data Y[6] General Purpose I/O Default: Input of sensor data Y[6]
E3	Y[7]	I/O	Sensor Data Y[7] General Purpose I/O Default: Input of sensor data Y[7]
E4	Y[8]	I/O	Sensor Data Y[8] General Purpose I/O Default: Input of sensor data Y[8]
F1	Y[9]	I/O	Sensor Data Y[9] General Purpose I/O Default: Input of sensor data Y[9]
D2	CCLK	I/O	Camera Clock to Sensor General Purpose I/O Default: Output of camera clock
D4	PCLK	I/O	Pixel Clock from Sensor General Purpose I/O Default: Input of pixel clock
F2	HREF	I/O	Horizontal Reference/Sync from Sensor General Purpose I/O Default: Input of sensor HREF
F3	VSYNC	I/O	Vertical Sync from Sensor General Purpose I/O Default: Input of sensor VSYNC
A1	SIO_D	I/O	Master SCCB Data Default: Input
A2	SIO_C	I/O	Master SCCB Clock Default: Input
USB 2.0 Interface			
D6	VRES	Input	USB Bias
G6	RPU	Input	USB Bias
G7	DP	I/O	USB DP
F7	DM	I/O	USB DM

Table 1 Pin Description by Function (Continued)

Ball Number	Name	Pin Type	Function/Description
Power and Ground			
B4	IO_VDD1	Power	3.3V I/O Power
C1	IO_VSS1	Ground	I/O Ground
E1	CORE_VDD1	Power	1.8V Core Power
D3	CORE_VSS1	Ground	1.8V Core Ground
G2	RIN_VDD18	Power	3.3V to 1.8V Regulator Input
G3	REG_VSS18	Ground	3.3V to 1.8V Regulator Ground
G4	ROUT_VDD1	Power	3.3V to 1.8V Regulator Output
A7	IO_VDD2	Power	I/O Power
B5	IO_VSS2	Ground	I/O Ground
D5	CORE_VDD2	Power	1.8V Core Power
C5	CORE_VSS2	Ground	1.8V Core Ground
D7	USB_VSSA2	Ground	USB Analog Ground
E5	USB_VDDA2	Power	3.3V USB Analog Power
E6	USB_VSSL	Ground	USB Digital Ground
E7	USB_VDDL	Power	1.8V USB Core Power
F5	USB_VDDD	Power	3.3V USB Digital Power
F6	USB_VSSA1	Ground	USB Analog Ground
G5	USB_VDDA1	Power	3.3V USB Analog Power

Electrical Characteristics

Table 2 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_{STG}	Ambient storage temperature	TBD	TBD	°C
V_{SUP}	All I/O supply voltage	TBD	TBD	V
V_{ESD}	ESD rating (HBM)	TBD	TBD	V
T_{JUNC}	Junction Temperature	TBD	TBD	°C
R_{THM}	Thermal resistance	TBD	TBD	C/W

Table 3 DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input voltage HIGH	V_{DD_IO} = 3.3V ± 10%	TBD	TBD	–	V
V_{IL}	Input voltage LOW	V_{DD_IO} = 3.3V ± 10%	–	TBD	TBD	V
V_{OH}	Output voltage HIGH	V_{DD_IO} = 3.3V ± 10%	TBD	TBD	–	V
V_{OL}	Output voltage LOW	V_{DD_IO} = 3.3V ± 10%	–	TBD	TBD	V
V_{OHX1}	Output current HIGH[a]	V_{DD_IO} = 3.3V	–	TBD	–	mA
I_{OHX2}	Output current HIGH[b]	V_{DD_IO} = 3.3V	–	TBD	–	mA
I_{OLX1}	Output current LOW[c]	V_{DD_IO} = 3.3V	–	TBD	–	mA
I_{OLX2}	Output current LOW[d]	V_{DD_IO} = 3.3V	–	TBD	–	mA
I_S	Suspend current	V_{DD_CORE} = 1.8V ± 10%, clock toggling V_{DD_CORE} = 1.8V ± 10%, clock static	–	TBD TBD	–	µA
I_{DDA}	Operating current	V_{DD_IO} = 3.3V, QVGA 30 fps V_{DD_IO} = 3.3V, 1.3MP 15 fps V_{DD_IO} = 3.3V, 2.0MP 10 fps	–	TBD TBD TBD	–	mA

a. 1x drive strength, C_L=15pf, output HIGH voltage threshold at V_{DD_IO} x 90%
b. 2x drive strength, C_L=15pf, output HIGH voltage threshold at V_{DD_IO} x 90%
c. 1x drive strength, C_L=15pf, output LOW voltage threshold at V_{DD_IO} x 10%
d. 2x drive strength, C_L=15pf, output LOW voltage threshold at V_{DD_IO} x 10%

Table 4 1.8V Regulator Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OUT}	Output voltage	I_{OUT} = 0mA, 2.2V<V_{IN}<3.6V, Typ=2.8V I_{OUT} = 25mA, 2.2V<V_{IN}<3.6V, Typ=2.8V I_{OUT} = 50mA, 2.2V<V_{IN}<3.6V, Typ=2.8V I_{OUT} = 100mA, 2.2V<V_{IN}<3.6V, Typ=2.8V	TBD TBD TBD TBD	TBD TBD TBD TBD	TBD TBD TBD TBD	V
ΔV_{LINE}	Line regulation	I_{OUT} = 100mA, 2.2V<V_{IN}<3.6V	–	–	TBD	mV
ΔV_{LOAD}	Load regulation	V_{IN} = 2.8V, 0mA<I_{OUT} <150mA	–	–	TBD	mV
V_{DROP}	Dropout voltage	1.9V<V_{IN} < 2.2V, 0mA<I_{OUT} <150mA	–	TBD	TBD	mV
I_{LIMIT}	Current limit		–	–	TBD	mA
I_{MIN}	Min current load	V_{OUT} maintains at 1.8V	TBD	–	–	µA
I_{OPER}	Operating current	I_{OUT} = 100mA	–	TBD	–	mA
I_{QUIE}	Quiescent current	I_{OUT} = 0mA	–	TBD	–	mA
I_{SUSP}	Suspend current		–	–	TBD	µA
V_{NOISE}	RMS output noise	% of V_{OUT}	–	TBD	–	%
I_{PUL}	Max power-up load				TBD	mA

Timing Specifications

SCCB Timing Specifications

Master SCCB Timing

The master SCCB is a two-wire SCCB bus, including SIO_D and SIO_C.

Figure 3 Master SCCB Timing Diagram

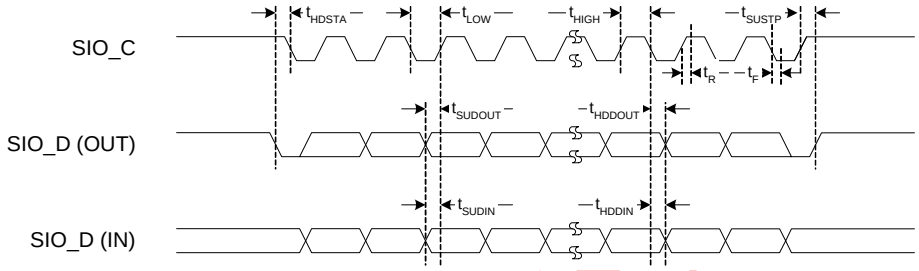


Table 5 Master SCCB Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{SIO_C}	SIO_C clock frequency	–	TBD	–	KHz
t_{HIGH}	SIO_C high clock time	–	TBD	–	µs
t_{LOW}	SIO_C low clock time	–	TBD	–	µs
t_{HDSTA}	Start of transmission hold time	–	TBD	–	µs
t_{SUSTP}	Stop of transmission setup time	–	TBD	–	µs
t_{SUDOUT}	Output data transmission setup time	–	TBD	–	µs
t_{HDDOUT}	Output data transmission hold time	–	TBD	–	µs
t_R	SIO_C clock rising time	–	TBD	–	µs
t_F	SIO_C clock falling time	–	TBD	–	µs
t_{SUDIN}	Input data setup time	TBD	–	–	µs
t_{HDDIN}	Input data hold time	TBD	–	–	µs

GPIO Timing Specifications

There is no direct relationship between GPIOs and clocks. The following tables describe GPIO rising/falling timings under different drive strengths, loadings, and supply voltages.

1x Drive Strength

Table 6 GPIO Rising/Falling Time — 1x Drive Strength with C_L = 15 pf, R_L = Open

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{GPR_1X0}	GPIO rising time	V_{DD_IO} = 3.3V	–	TBD	–	ns
t_{GPF_1X0}	GPIO falling time	V_{DD_IO} = 3.3V	–	TBD	–	ns

Table 7 GPIO Rising/Falling Time — 1x Drive Strength with C_L = 15 pf, R_L = 10 KΩ

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{GPR_1X1}	GPIO rising time	V_{DD_IO} = 3.3V	–	TBD	–	ns
t_{GPF_1X1}	GPIO falling time	V_{DD_IO} = 3.3V	–	TBD	–	ns

Table 8 GPIO Rising/Falling Time — 1x Drive Strength with C_L = 15 pf, R_L = 1.5 KΩ

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{GPR_1X2}	GPIO rising time	V_{DD_IO} = 3.3V	–	TBD	–	ns
t_{GPF_1X2}	GPIO falling time	V_{DD_IO} = 3.3V	–	TBD	–	ns

2x Drive Strength

Table 9 GPIO Rising/Falling Time — 2x Drive Strength with C_L = 15 pf, R_L = Open

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{GPR_2X0}	GPIO rising time	V_{DD_IO} = 3.3V	–	TBD	–	ns
t_{GPF_2X0}	GPIO falling time	V_{DD_IO} = 3.3V	–	TBD	–	ns

Table 10 GPIO Rising/Falling Time — 2x Drive Strength with C_L = 15 pf, R_L = 10 KΩ

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{GPR_2X1}	GPIO rising time	V_{DD_IO} = 3.3V	–	TBD	–	ns
t_{GPF_2X1}	GPIO falling time	V_{DD_IO} = 3.3V	–	TBD	–	ns

Table 11 GPIO Rising/Falling Time — 2x Drive Strength with C_L = 15 pf, R_L = 1.5 KΩ

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{GPR_2X2}	GPIO rising time	V_{DD_IO} = 3.3V	–	TBD	–	ns
t_{GPF_2X2}	GPIO falling time	V_{DD_IO} = 3.3V	–	TBD	–	ns

Clock Timing Specifications

Table 12 Input Clock X_IN Timing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{X_IN}	Input clock frequency		TBD	TBD	TBD	MHz
$t_{X\_IN\_DCY}$	Input clock duty cycle	See Note [a]	TBD	TBD	TBD	%
$f_{X\_IN\_TLN}$	Input frequency tolerance		–	–	TBD	%

a. Embedded PLL is not sensitive to input clock duty cycle

Table 13 Input Clock PCLK Timing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PCK}	Input clock frequency		–	–	TBD	MHz
t_{PCK_DCY}	Input clock duty cycle		TBD	TBD	TBD	%
f_{PCK_TLN}	Input frequency tolerance		–	–	TBD	%

Table 14 Output Clock CCLK Timing Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{CCK}	Output clock frequency		–	–	TBD	MHz
t_{CCK_DCY}	Output clock duty cycle		TBD	TBD	TBD	%
t_{CCK_JT}	Output clock jitter		–	–	TBD	ps

Register Set

Table 15 provides a list and description of the Device Control registers contained in the OV550.

Table 15 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
SCCB and Microcontroller				
F0	MS_SP	TBD	RW	SCCB Master Speed
F1	MS_ID	TBD	RW	SCCB Master ID
F2	MS_ADDRESS	TBD	RW	SCCB Master Address
F3	MS_DO	TBD	RW	SCCB Master Data Out
F4	MS_DI		R	SCCB Master Data In
F5	MS_CTRL	TBD	RW	SCCB Master Command Control Bit[7]: Send NAK/ACK in acknowledge phase of data in cycle Bit[6]: Use read ID (bit[0] of MS_ID: 1) Bit[5]: Launch stop bit cycle Bit[4]: Launch start bit cycle Bit[3]: Launch data in cycle Bit[2]: Launch data out cycle Bit[1]: Launch address cycle Bit[0]: Launch ID cycle 8'h37: 3-byte write 8'h33: 2-byte write 8'hF9: 2-byte read Burst write: 8'h13: Launch start-id-address cycle 8'h04: Launch data out cycle, n times 8'h20: Launch stop bit cycle Burst read: 8'h33: Launch 2-byte write for address 8'h51: Launch start-id with read ID 8'h08: Launch data in cycle with ACK 8'hA4: Launch last data in cycle with NAK, then stop bit
F6	MS_STATUS		R	Status of SCCB Master Bit[7:3]: Reserved Bit[2]: Slave status 0: ACK 1: NAK Bit[1]: Cycle completed for burst mode Bit[0]: Command busy
F7-F8	RSVD	XX	–	Reserved

Table 15 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
F9	MC_BIST		RW	Bit[7]: Microcontroller reset Bit[6]: Boot ROM select Bit[5]: R/W 1 error for 12K-byte memory Bit[4]: R/W 0 error for 12K-byte memory Bit[3]: R/W 1 error for 512-byte memory Bit[2]: R/W 0 error for 512-byte memory Bit[1]: BIST busy bit for read; One-shot reset of microcontroller for write Bit[0]: Launch BIST
FA	MC_AL		RW	Program Memory Pointer Address Low Byte
FB	MC_AH		RW	Program Memory Pointer Address High Byte
FC	MC_D	TBD	RW	Program Memory Pointer Access Address
Auto Timing Generator				
18	RPN	TBD	RW	Bit[7]: Auto mode enable 0: Manual mode 1: Auto mode Bit[6:0]: Pixel clock period
19	RH0	TBD	RW	Line Period 1 Bit[7:0]: RH[7:0]
1A	RH1	TBD	RW	Line Period 2 Bit[7:0]: RH[15:8]
1B	RH2	TBD	RW	Line Period 3 Bit[7:0]: RH[23:16]
System Controller				
E0	RESET0	TBD	RW	Reset Bit[7]: SCCB Bit[6:4]: Reserved Bit[3]: VFIFO Bit[2:1]: Reserved Bit[0]: CIF
E1	RESET1	TBD	RW	Clock Enable Bit[7:3]: Reserved Bit[2]: UDCIF Bit[1]: UDC Bit[0]: Microcontroller
E2	CLOCK0	TBD	RW	Clock Control (1: OFF, 0: ON) Bit[7]: SCCB Bit[6:4]: Reserved Bit[3]: VFIFO Bit[2:1]: Reserved Bit[0]: CIF

Table 15 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
E3	CLOCK1	TBD	RW	Clock Control (1: OFF, 0: ON) Bit[7:4]: Reserved Bit[3]: Sensor power down in suspend mode enable Bit[2]: Reserved Bit[1]: PLL disable Bit[0]: Microcontroller
E4	RSVD	XX	–	Reserved
E5	CAMERA_CLK	TBD	RW	Bit[7]: Drive 0 to SRAM output 0: Normal 1: Driver 0 Bit[6]: SRAM input force to 0 0: Normal mode 1: Force to 0 Bit[5]: SRAM CEN Bit[4:0]: Camera clock select
E6	USER		RW	User defined
E7	SYS_CTRL	TBD	RW	System Control Bit[7]: Launch suspend Bit[6]: Launch register reset Bit[5]: Reserved Bit[4]: Microcontroller wakeup reset enable Bit[3]: Reserved Bit[2]: Wakeup enable Bit[1]: Suspend enable Bit[0]: Camera power ON/OFF 0: Power ON camera 1: Power down camera
EC	IRQ_M0			Interrupt Mask Bit[7]: UDC Bit[6]: USB enumeration done Bit[5]: USB suspend Bit[4]: USB early suspend Bit[3]: USB SOF Bit[2]: UDCIF interrupt Bit[1:0]: Reserved
ED	IRQ_M1			Interrupt Mask Bit[7]: Line interrupt Bit[6:3]: Reserved Bit[2]: VSYNC Bit[1:0]: Reserved

Table 15 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
EE	IRQ0			Interrupt Status Bit[7]: UDC Bit[6]: USB enumeration done Bit[5]: USB suspend Bit[4]: USB early suspend Bit[3]: USB SOF Bit[2]: UDCIF interrupt Bit[1:0]: Reserved
EF	IRQ1			Interrupt Status Bit[7]: Line interrupt Bit[6:3]: Reserved Bit[2]: VSYNC Bit[1:0]: Reserved
35	DIF	TBD	RW	Bit[7:3]: Reserved Bit[2]: Select RGB mode Bit[1:0]: Reserved
3B	CIF_FRAME	TBD	RW	Bit[7:6]: Number of frame for output Bit[5]: Enable/disable CIF output after (Bit[3:0]) frames Bit[4]: Enable CIF output Bit[3:0]: Number of frames for CIF output
3D	PHY_BIST0	TBD	RW	Bit[7:0]: BIST data
3E	PHY_BIST1	TBD	RW	Bit[15:8]: BIST data
3F	PHY_BIST2		RW	Bit[7]: BIST transceiver select Bit[6]: BIST termination select Bit[5:4]: BIST OP mode Bit[3]: BIST suspendm Bit[2]: BIST on Bit[1]: BIST txvalidh Bit[0]: BIST txvalid
GPIO				
20	GPIO_N0	TBD	RW	PHY Control Bit[7:6]: PHY input clock reference Bit[5]: PHY data bus 16/8 select Bit[4:0]: Reserved
21	GPIO_C0	TBD	RW	I/O Pad In/Out Control 0: Input 1: Output
22	GPIO_I0		R	I/O Pad Input
23	GPIO_V0	TBD	RW	I/O Pad Output

Table 15 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
24	GPIO_N1	TBD	RW	I/O Pad (1: Normal mode, 0: Register control) Bit[7:5]: Reserved Bit[4]: SIO_C Bit[3]: SIO_D Bit[2:0]: Reserved
25	GPIO_C1	TBD	RW	I/O Pad In/Out Control Bit[7]: Reserved Bit[6]: OSCEN Bit[5]: Reserved Bit[4]: SIO_C Bit[3]: SIO_D Bit[2:0]: GPIO[10:8]
26	GPIO_I1	TBD	R	I/O Pad Input Bit[7]: Reserved Bit[6]: OSCEN Bit[5:4]: Reserved Bit[3]: PHY BIST fail Bit[2:0]: GPIO[10:8]
27	GPIO_V1	TBD	RW	I/O Pad Output Bit[7]: Reserved Bit[6]: OSCEN Bit[5]: Reserved Bit[4]: SIO_C Bit[3]: SIO_D Bit[2:0]: GPIO[10:8]
28	SENSOR_S1	TBD	RW	I/O Pad Driving Strength Bit[7]: Y[7] Bit[6]: Y[6] Bit[5]: Y[5] Bit[4]: Y[4] Bit[3]: Y[3] Bit[2]: Y[2] Bit[1]: Y[1] Bit[0]: Y[0]
29	SENSOR_C1	TBD	RW	I/O Pad Output Bit[7]: Y[7] Bit[6]: Y[6] Bit[5]: Y[5] Bit[4]: Y[4] Bit[3]: Y[3] Bit[2]: Y[2] Bit[1]: Y[1] Bit[0]: Y[0]

Table 15 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
2A	SENSOR_I1	TBD	RW	I/O Pad In/Out Control Bit[7]: Y[7] Bit[6]: Y[6] Bit[5]: Y[5] Bit[4]: Y[4] Bit[3]: Y[3] Bit[2]: Y[2] Bit[1]: Y[1] Bit[0]: Y[0]
2B	SENSOR_V1	TBD	RW	I/O Pad Output Bit[7]: Y[7] Bit[6]: Y[6] Bit[5]: Y[5] Bit[4]: Y[4] Bit[3]: Y[3] Bit[2]: Y[2] Bit[1]: Y[1] Bit[0]: Y[0]
2C	SENSOR_S0	TBD	RW	I/O Pad Driving Strength Bit[7]: Reserved Bit[6]: CCLK Bit[5]: SPWDN Bit[4]: HREF Bit[3]: VSYNC Bit[2]: PCLK Bit[1]: Y[9] Bit[0]: Y[8]
2D	SENSOR_C0	TBD	RW	I/O Pad In/Out Control Bit[7]: Reserved Bit[6]: CCLK Bit[5]: SPWDN Bit[4]: HREF Bit[3]: VSYNC Bit[2]: PCLK Bit[1]: Y[9] Bit[0]: Y[8]
2E	SENSOR_I0		R	I/O Pad Input Bit[7]: Reserved Bit[6]: CCLK Bit[5]: SPWDN Bit[4]: HREF Bit[3]: VSYNC Bit[2]: PCLK Bit[1]: Y[9] Bit[0]: Y[8]

Table 15 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
2F	SENSOR_V0	TBD	RW	I/O Pad Output Bit[7]: Reserved Bit[6]: CCLK Bit[5]: SPWDN Bit[4]: HREF Bit[3]: VSYNC Bit[2]: PCLK Bit[1]: Y[9] Bit[0]: Y[8]
30	REGULATOR_C	TBD	RW	1.8V Regulator Control Bit[7:0]: Reserved
31	GPIO_P	TBD	RW	GPIO Pulse Detect (1: Pulse detected, write 0 to clear) Bit[7:4]: Reserved Bit[3]: GPIO3, positive pulse Bit[2]: GPIO2, positive pulse Bit[1]: GPIO1, positive pulse Bit[0]: GPIO0, positive pulse
39	GPIO_S0	TBD	RW	I/O Pad Driving Strength Bit[7:0]: P_GPIO[7:0]
3A	GPIO_S1	TBD	RW	I/O Pad (1: Normal mode, 0: Register control) Bit[7]: Reserved Bit[6]: OSCEN Bit[5]: RESET_ Bit[4]: SIO_C Bit[3]: SIO_D Bit[2:0]: Reserved
UDC Control				
0E	UDC_PTR	TBD	RW	UDC Control Register Pointer
0F	UDC_DAT	TBD	RW	UDC Control Register Data
0x0F-00	UDC_APP0	TBD	RW	Bit[7]: UDC scale down for test mode Bit[6]: CSR programming support Bit[5]: RAM interface support Bit[4]: Device remote wakeup support Bit[3]: Set descriptor command support Bit[2]: SYNC command support Bit[1]: Self power Bit[0]: PHY 8/16 bit select
0x0F-01	UDC_APP1	TBD	RW	Bit[7]: Stall Bit[6]: Stall clear endpoint 0 halt Bit[5]: Non-zero length packet stall all Bit[4]: Non-zero length packet stall Bit[3]: Enable erratic error Bit[2]: Device soft disconnect Bit[1:0]: Exp speed

Table 15 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0x0F-02	UDC_APP2	TBD	RW	Bit[7]: Reserved Bit[6:4]: Full speed time out calibration Bit[3]: Reserved Bit[2:0]: High speed time out calibration
0x0F-03	UDC_APP3	TBD	RW	USB Control Interrupt Enable Bit[7:4]: Reserved Bit[3]: USB set interface interrupt Bit[2]: USB set configuration interrupt Bit[1]: USB set CSR interrupt Bit[0]: USB set erratic error interrupt
0x0F-04	UDC_R0		R	Bit[7:6]: PHY XVER select Bit[5:4]: PHY OP mode Bit[3:2]: PHY mode Bit[1:0]: USB enumeration speed
0x0F-05	UDC_R1		R	UDC micro frame number
0x0F-06	UDC_R2		R	Timestamp[7:0]
0x0F-07	UDC_R3		R	Bit[7:4]: Interface Bit[3:0]: Alternate setting
0x0F-08	UDC_R4		R	Bit[7:4]: Configuration Bit[3]: USB set interface interrupt Bit[2]: USB set configuration interrupt Bit[1]: USB set CSR interrupt Bit[0]: USB set erratic error interrupt
UDCIF Control				
0x00	EPIRQ_PTR	TBD	RW	Interrupt endpoint buffer pointer
0x01	EPIRQ_DATA	TBD	RW	Interrupt endpoint buffer access
0x02	EPIRQ_CTRL	TBD	RW	Interrupt endpoint control Bit[7:5]: Reserved Bit[4]: Interrupt for INTERRUPT IN enable Bit[3]: Interrupt for INTERRUPT IN Bit[2]: Send STALL for next interrupt IN Bit[1]: Send ACK for next interrupt IN Bit[0]: Send ACK for all Interrupt IN
0x03	EPCTRL_CFG	TBD	RW	Bit[7:5]: Reserved Bit[4]: Setup indicator Bit[3]: Last transfer RwL (0: write; 1 read) Bit[2]: External audio interface enable Bit[1]: Debug interface enable Bit[0]: Descriptor decoder enable
0x04	EPCTRL_PTR	TBD	R	Control endpoint buffer pointer
0x05	EPCTRL_DATA	TBD	R	Control endpoint buffer data access

Table 15 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0x06	EPCTRL_CTRL	TBD	RW	Control endpoint control Bit[7]: Status interrupt enable Bit[6]: Status read indicator Bit[5]: High speed indicator Bit[4]: Send ACK for all control DATA Bit[3]: Send STALL for next control STATUS Bit[2]: Send ACK for control STATUS Bit[1]: Send STALL for next control DATA Bit[0]: Send ACK for next control DATA
0x07	EPCTRL_CNT	TBD	RW	Number of byte transferred
0x08	CSR_PTR	TBD	R	CSR register address
0x09	CSR_D0	TBD	RW	CSR data[7:0]
0x0a	CSR_D1	TBD	RW	CSR data[15:8]
0x0b	CSR_D2	TBD	RW	CSR data[23:16]
0x0c	CSR_D3	TBD	RW	CSR data[31:24]
0x0d	CSR_CTRL		RW	CSR control Bit[7]: Microsoft ID enable (read only) Bit[6]: SONY ID enable (read only) Bit[5]: High speed ISO transfer enable Bit[4]: Enumeration interrupt Bit[3]: CSR valid Bit[2]: CSR done Bit[1]: CSR Read (1) / Write (0) Bit[0]: Use default configuration
Video Data[a]				
00	V_FMT	TBD	RW	Bit[7]: Swap even byte and odd byte Bit[6:5]: Video Format 0: RAW8 1: RAW10 2: RAW16 3: Reserved 4: YUV422 5: YUV411, first line is YYYY, second line is YUYV 6: YUV411, first line is YUYV, second line is YYYY 7: YUV411, first line is UYY, second line is VYY Bit[3]: Transfer select 0: BULK transfer 1: ISO transfer Bit[2]: Still image header for USB video class Bit[1:0]: Reserved
01	PLOAD_H	TBD	RW	Bit[15:8]: Of pay load size, divided by 4
02	PLOAD_L	TBD	RW	Bit[7:0]: Of pay load size, divided by 4

Table 15 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
03	FRAME_H	TBD	RW	Bit[23:16]:Of frame size, divided by 4
04	FRAME_M	TBD	RW	Bit[15:8]: Of frame size, divided by 4
05	FRAME_L	TBD	RW	Bit[7:0]: Of frame size, divided by 4
0A	V_CNTL0	TBD	RW	Bit[7]: Reserved Bit[6]: Internal video RAM BIST enable Bit[5:2]: Reserved Bit[1]: Header End for USB video class Bit[0]: Header Reserved for USB video class
0B	V_CNTL1	TBD	RW	Bit[7]: Internal video RAM BIST OK Bit[6]: Internal video RAM BIST ERR Bit[5:4]: Reserved Bit[3]: Auto Frame size Bit[2:0]: Reserved
0C-0F	RSVD	XX	–	Reserved

a. The video data registers are indirectly control by 0x1C and 0x1D registers.

Package Specifications

The OV550-B49 uses a 49-pin BGA package. Refer to Figure 4 for package information.

Figure 4 OV550-B49 Package Specifications

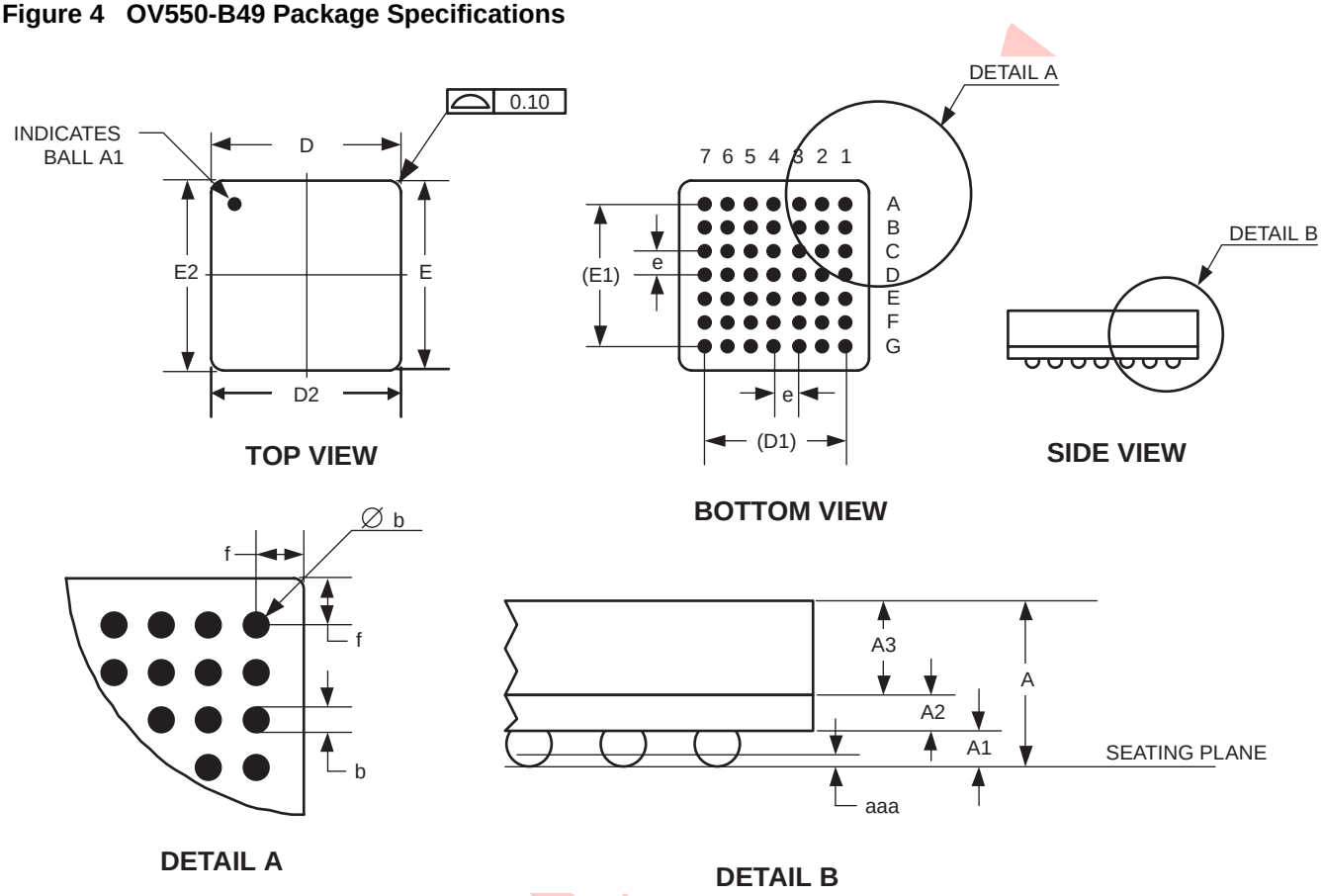


Table 16 49-Pin BGA Package Dimensions

Dimension Reference	Minimum	Nominal	Maximum
A	1.1		1.3
A1	0.25		0.35
A2		0.26 REF	
A3		0.7 REF	
b	0.35		0.45
D		6.00 BSC	
E		6.00 BSC	
e		0.80 BSC	
D1		4.80 BSC	
E1		4.80 BSC	
D2		6.00 BSC	
E2		6.00 BSC	
aaa		0.10 BSC	
f		0.60 BSC	

NOTE: All dimensions are in millimeters.

IR Reflow Ramp Rate Requirements

OV550-B49 Lead-Free Packaged Devices

Note: For lead-free OVT devices, parts will be marked with part numbers ending with a "G" (i.e., OV550)

Figure 5 IR Reflow Ramp Rate Requirements

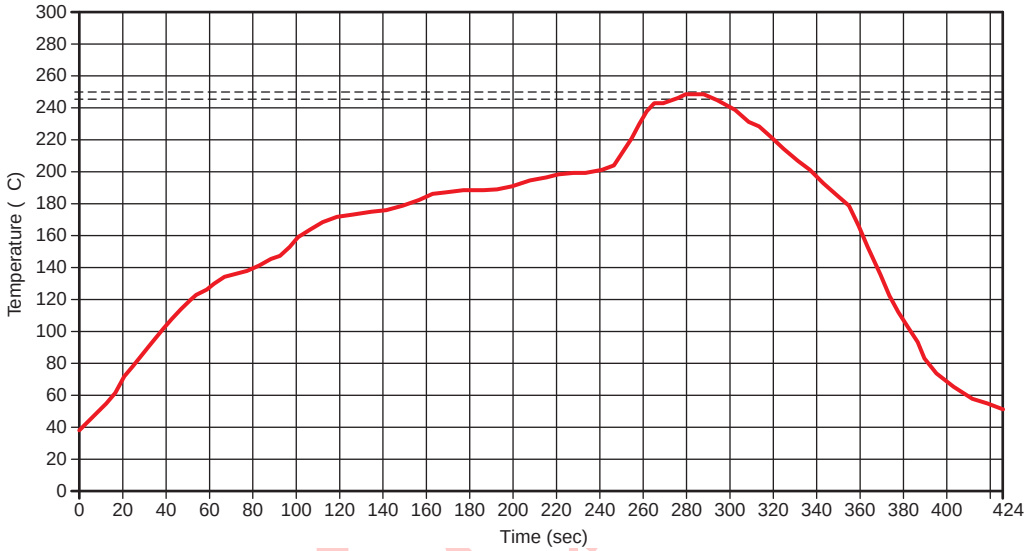


Table 17 Heat Zone Temperature Setup

Zone	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Set Temperature (°C) (upper)	180	180	190	200	260	0	0	0	0	0	0	0	0	0	0	0
Set Temperature (°C) (lower)	180	180	190	200	260	0	0	0	0	0	0	0	0	0	0	0

Maximum Temperature (°C)	Time (sec)	Time Above 245°C (sec)	Time Above 217°C (sec)
248.5	284.0	20.1	69.8

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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REVISION CHANGE LIST

Document Title: OV550-B49 Datasheet **Version:** 1.0

DESCRIPTION OF CHANGES

- Intial Release

REVISION CHANGE LIST

Document Title: OV550-B49 Datasheet **Version:** 1.1

DESCRIPTION OF CHANGES

The following changes were made to version 1.0:

- Added Lead-free symbol and Note on page 1
- Under Ordering Information on page 1, changed part number from “OV0550-BB30” to “OV0550-LB30” and added “(Lead-free)” under Package description column