General Description

The CYBT-343052-02 is a fully integrated Bluetooth® Smart Ready wireless module. The CYBT-343052-02 includes an onboard crystal oscillator, passive components, flash memory, and the Cypress CYW20735 silicon device. Refer to the CYW20735 datasheet for additional details on the capabilities of the silicon device used in this module.

The CYBT-343052-02 supports peripheral functions (ADC and PWM), UART, I²C, and SPI communication, and a PCM/I²S audio interface. The CYBT-343052-02 includes a royalty-free Bluetooth stack compatible with Bluetooth 5.0 in a 13.3 × 22.4 × 1.95 mm package.

The CYBT-343052-02 includes 512 KB of onboard serial flash memory and is designed for standalone operation. The CYBT-343052-02 uses an integrated power amplifier to achieve Class I or Class II output power capability.

The CYBT-343052-02 is fully qualified by Bluetooth SIG and is targeted at applications requiring cost-optimized Bluetooth wireless connectivity.

Module Description

- Module size: 13.3 mm × 22.4 mm × 1.95 mm
- Bluetooth 5.0 Qualified Smart Ready module
  - ❒ QDID: TBD
  - ❒ Declaration ID: TBD
- Certified to FCC, ISED, MIC, and CE regulations
- Castelated solder pad connections for ease-of-use
- 512-KB on-module serial flash memory
- Up to 24 GPIOs
- Temperature range: –30 °C to +85 °C
- Cortex-M4 32-bit processor
- Maximum TX output power
  - ❒ +10 dbm for Bluetooth Classic
  - ❒ +12 dBm for Bluetooth Low Energy
    - BLE connection range of up to 250 meters at 12 dBm[1]
- RX receive sensitivity:
  - ❒ Bluetooth Classic: –91.5 dBm
  - ❒ –94.5 dBm for Bluetooth Low Energy

Power Consumption

- BLE Current Consumption
  - ❒ RX current: 8 mA
  - ❒ TX current: 18 mA @ 12 dBm
  - ❒ Interval BLE ADV average current consumption: 30 µA
  - ❒ HIDOFF (Deep Sleep): 1 µA

Functional Capabilities

- 1x MIPI DMI-C interface
- 6x 16-bit PWMs
- Programmable key-scan matrix interface, up to 8x20 key scanning matrix
- Quadrature decoder
- Watchdog timer (WDT)
- 1x peripheral UART, 1x UART for programming and HCI
- 1x SPI (master or slave mode)
- 1x I2C master
- One ADC (10-ENoB for DC measurement and 12-ENOB for Audio measurement)
- Hardware security engine

Benefits

CYBT-343052-02 provides all necessary components required to operate BLE and/or BR communication standards.

- Proven ready-to-use hardware design
- Dual-mode operation eliminates the need for multiple modules
- Cost optimized for applications without space constraints
- Nonvolatile memory for self-sufficient operation and over-the-air updates
- Bluetooth SIG listed with QDID and Declaration ID
- Fully certified module eliminates the time needed for design, development, and certification processes
- WICED® Studio provides an easy-to-use integrated design environment (IDE) to configure, develop, and program a Bluetooth application

Note
1. Connection range tested module-to-module in full line-of-sight environment, free of obstacles or interference sources with output power of +12.0 dBm. Actual range will vary based on end product design, environment, receive sensitivity, and transmit output power of the central device.

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

References

- Overview: EZ-BLE/BT Module Portfolio, Module Roadmap
- CYW20735 BT Silicon Datasheet
- Development Kits:
  - CYBT-343052-EVAL, CYBT-343052-02 Evaluation Board
- Test and Debug Tools:
  - CYSmart, Bluetooth® LE Test and Debug Tool (Windows)
  - CYSmart Mobile, Bluetooth® LE Test and Debug Tool (Android/iOS Mobile App)

- Knowledge Base Article
  - KBA97095 - EZ-BLE™ Module Placement
  - TBD - TBD
  - KBA213976 - FAQ for BLE and Regulatory Certifications with EZ-BLE modules
  - KBA210802 - Queries on BLE Qualification and Declaration Processes
  - KBA218122 - 3D Model Files for EZ-BLE/EZ-BT Modules
  - TBD - Platform Files for CYBT-343026-EVAL
  - KBA223428 - Programming an EZ-BT WICED Module

Development Environments

Wireless Connectivity for Embedded Devices (WICED) Studio Software Development Kit (SDK)

Cypress' WICED® is a full-featured platform with proven Software Development Kits (SDKs) and turnkey hardware solutions from partners to readily enable Wi-Fi and Bluetooth® connectivity in system design.

WICED Studio is the only SDK for the Internet of Things (IoT) that combines Wi-Fi and Bluetooth into a single integrated development environment. In addition to providing WICED APIs and an application framework designed to abstract complexity, WICED Studio also leverages many common industry standards.

Technical Support

- Cypress Community: Whether you are a customer, partner, or a developer interested in the latest Cypress innovations, the Cypress Developer Community offers you a place to learn, share, and engage with both Cypress experts and other embedded engineers around the world.

- Frequently Asked Questions (FAQs): Learn more about our Bluetooth ecosystem.

- Visit our support page and create a technical support case or contact a local sales representatives. If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 2 at the prompt.
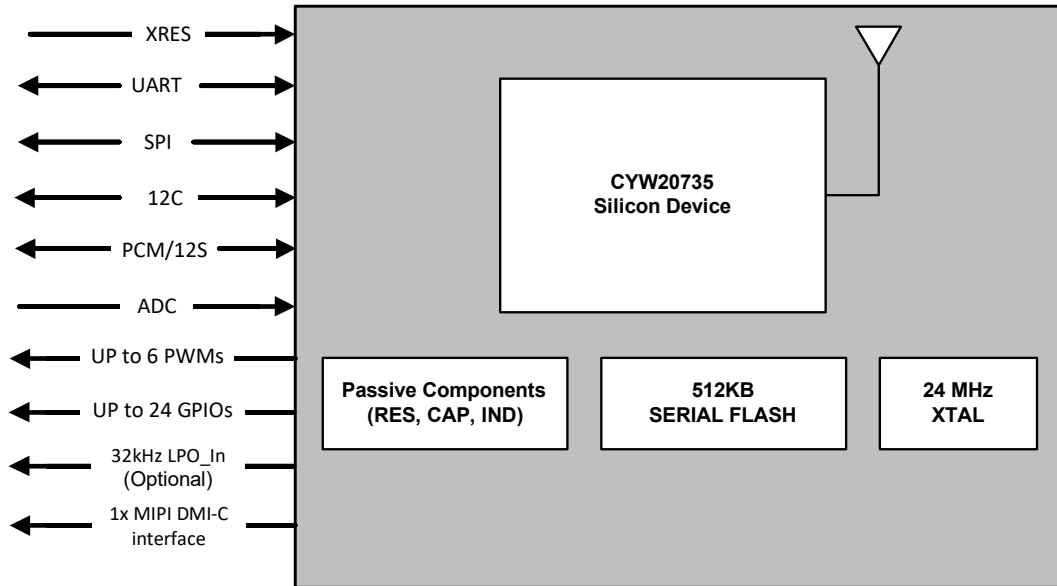
Contents

Overview

Functional Block Diagram

Figure 1 illustrates the CYBT-343052-02 functional block diagram.

Figure 1. Functional Block Diagram (GPIOs)

Module Description

The CYBT-343052-02 module is a complete module designed to be soldered to the application's main board.

Module Dimensions and Drawing

Cypress reserves the right to select components from various vendors to achieve the Bluetooth module functionality. Such selections will still guarantee that all mechanical specifications and module certifications are maintained. Designs should be held within the physical dimensions shown in the mechanical drawings in Figure 2 on page 5. All dimensions are in millimeters (mm).

Table 1. Module Design Dimensions

Dimension Item		Specification
Module dimensions	Length (X)	13.31 ± 0.15 mm
	Width (Y)	22.40 ± 0.15 mm
Antenna connection location dimensions	Length (X)	13.31 mm
	Width (Y)	7.42 mm
PCB thickness	Height (H)	0.50 ± 0.05 mm
Shield height	Height (H)	1.45-mm typical
Maximum component height	Height (H)	1.45-mm typical
Total module thickness (bottom of module to highest component)	Height (H)	1.95-mm typical

See Figure 2 for the mechanical reference drawing for CYBT-343052-02.

Figure 2. Module Mechanical Drawing

Top View (Seen from Top)

Side View

Bottom View
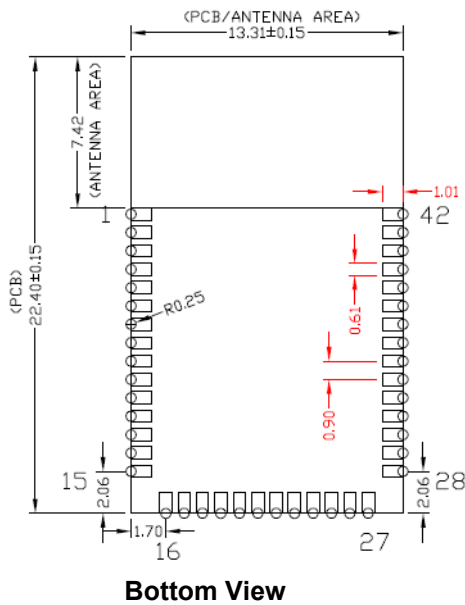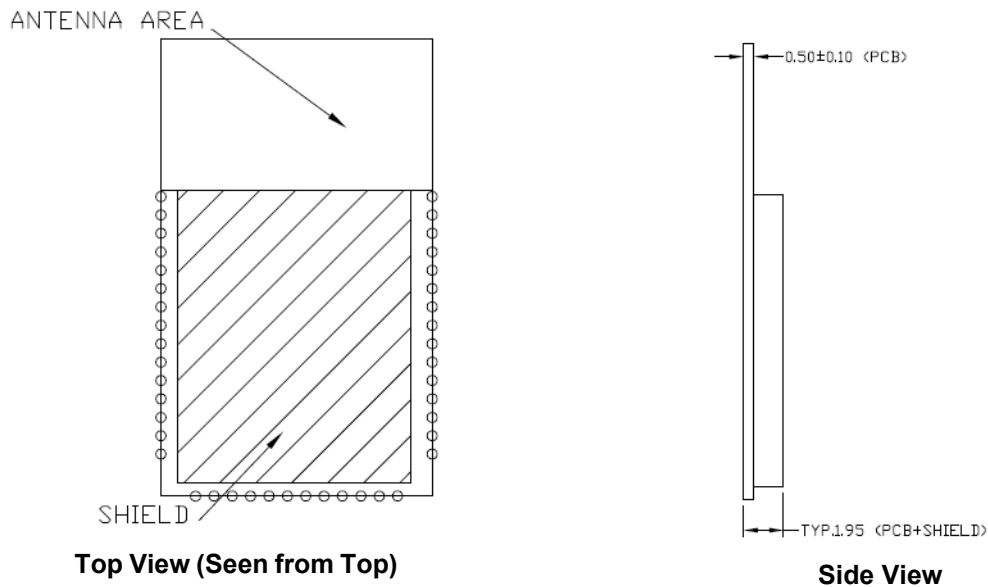
PAD1:GND	PAD32:SPI_MOSI
PAD2:VDD	PAD33:P2
PAD3:XRES	PAD34:P3
PAD4:P32	PAD35:HOST_WAKE
PAD5:P27	PAD36:P4
PAD6:P26	PAD37:P5
PAD7:P38	PAD38:P6
PAD8:P34	PAD39:P7
PAD9:P1	PAD40:P8
PAD10:P0	PAD41:P14
PAD11:P29	PAD42:GND
PAD12:P28	
PAD13:P13	
PAD14:P12	
PAD15:P11	
PAD16:P10	
PAD17:P9	
PAD18:GND	
PAD19:P15/XTALI_32K	
PAD20:XTALO_32K	
PAD21:GND	
PAD22:GND_A	
PAD23:MIC_AVDD	
PAD24:MIC_N	
PAD25:MIC_P	
PAD26:MIC_BIAS	
PAD27:GND_A	
PAD28:UART_CTS_N	
PAD29:UART_RTS_N	
PAD30:UART_TXD	
PAD31:UART_RXD	

Notes
2. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see "Recommended Host PCB Layout" on page 7.
3. The CYBT-343052-02 includes castellated pad connections, denoted as the circular openings at the pad location above.

Pad Connection Interface

As shown in the bottom view of Figure 2 on page 5, the CYBT-343052-02 connects to the host board via solder pads on the backside of the module. Table 2 and Figure 3 detail the solder pad length, width, and pitch dimensions of the CYBT-343052-02 module.

Table 2. Connection Description

Name	Connections	Connection Type	Pad Length Dimension	Pad Width Dimension	Pad Pitch
SP	42	Solder Pads	1.01 mm	0.61 mm	0.90 mm

Figure 3. Solder Pad Dimensions (Seen from Bottom)
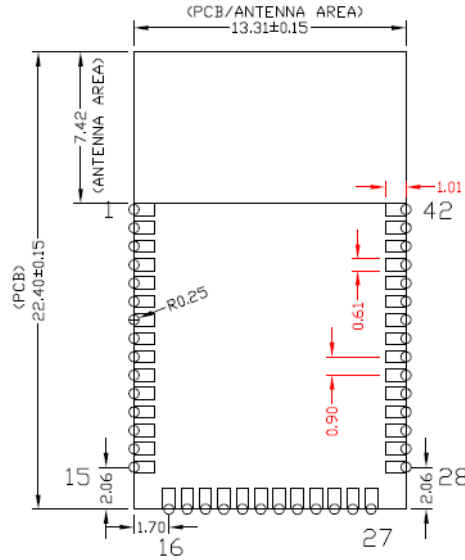
To maximize RF performance, the host layout should follow these recommendations:

1. Antenna Area Keepout: The host board directly below the antenna area of the Cypress module (see Figure 2 on page 5) must not contain ground or signal traces. This keepout area requirement applies to all layers of the host board.

2. Module Placement: The ideal placement of the Cypress Bluetooth module is in a corner of the host board with the PCB trace antenna located at the far corner. This placement minimizes the additional recommended keepout area stated in item 2. Refer to AN96841 for module placement best practices.

Figure 4. Recommended Host PCB Keepout Area Around the CYBT-343052-02 Antenna
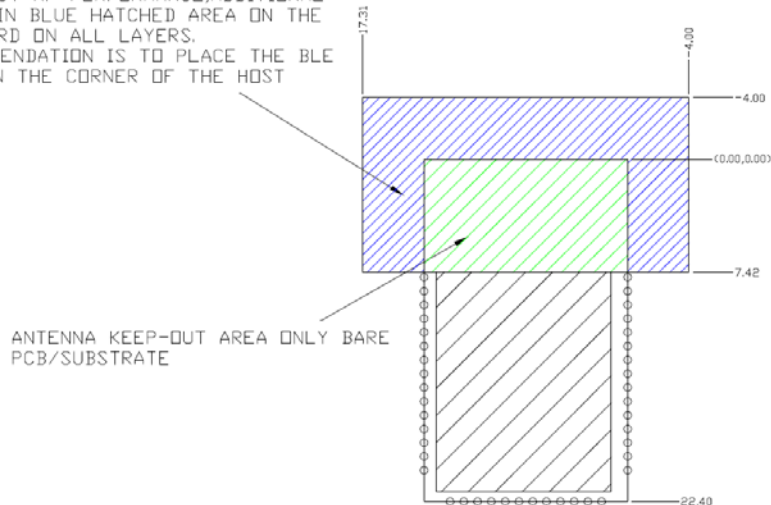
Recommended Host PCB Layout

Figure 5, Figure 6, Figure , and Table provide details that can be used for the recommended host PCB layout pattern for the CYBT-343052-02. Dimensions are in millimeters unless otherwise noted. Pad length of 1.27 mm (0.635 mm from center of the pad on either side) shown in Figure is the minimum recommended host pad length. The host PCB layout pattern can be completed using either Figure 5, Figure 6, or Figure . It is not necessary to use all figures to complete the host PCB layout pattern.

Figure 5. CYBT-343052-02 Host Layout (Dimensioned)

Top View (Seen on Host PCB)

Figure 6. CYBT-343052-02 Host Layout (Relative to Origin)
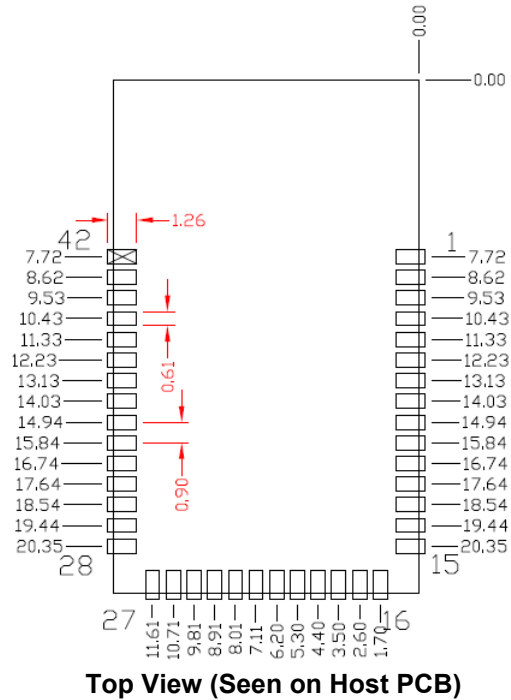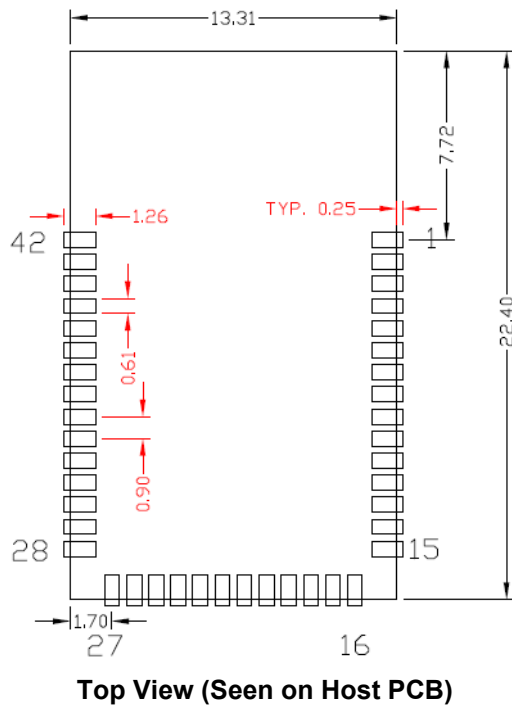

Top View (Seen on Host PCB)

Table 3 provides the center location for each solder pad on the CYBT-343052-02. All dimensions are referenced to the center of the solder pad. Refer to Figure for the location of each module solder pad.

Table 3. Module Solder Pad Location

Solder Pad (Center of Pad)	Location (X,Y) from Orign (mm)	Dimension from Orign (mils)
1	(0.38, 7.72)	(14.96, 303.94)
2	(0.38, 8.62)	(14.96, 339.37)
3	(0.38, 9.53)	(14.96, 375.20)
4	(0.38, 10.43)	(14.96, 410.63)
5	(0.38, 11.33)	(14.96, 446.06)
6	(0.38, 12.23)	(14.96, 481.50)
7	(0.38, 13.13)	(14.96, 516.93)
8	(0.38, 14.03)	(14.96, 552.36)
9	(0.38, 14.94)	(14.96, 588.19)
10	(0.38, 15.84)	(14.96, 623.62)
11	(0.38, 16.74)	(14.96, 659.05)
12	(0.38, 17.64)	(14.96, 694.49)
13	(0.38, 18.54)	(14.96, 729.92)
14	(0.38, 19.44)	(14.96, 765.35)
15	(0.38, 20.35)	(14.96, 801.18)
16	(1.70, 22.02)	(66.93, 866.93)
17	(2.60, 22.02)	(102.36, 866.93)
18	(3.50, 22.02)	(137.80, 866.93)
19	(4.40, 22.02)	(173.23, 866.93)
20	(5.30, 22.02)	(208.66, 866.93)
21	(6.20, 22.02)	(244.09, 866.93)
22	(7.11, 22.02)	(279.92, 866.93)
23	(8.01, 22.02)	(315.35, 866.93)
24	(8.91, 22.02)	(350.79, 866.93)
25	(9.81, 22.02)	(386.22, 866.93)
26	(10.71, 22.02)	(421.65, 866.93)
27	(11.61, 22.02)	(457.09, 866.93)
28	(12.93, 20.35)	(509.05, 801.18)
29	(12.93, 19.44)	(509.05, 765.35)
30	(12.93, 18.54)	(509.05, 729.92)
31	(12.93, 17.64)	(509.05, 694.49)
32	(12.93, 16.74)	(509.05, 659.05)
33	(12.93, 15.84)	(509.05, 623.62)
34	(12.93, 14.94)	(509.05, 588.19)
35	(12.93, 14.03)	(509.05, 552.36)
36	(12.93, 13.13)	(509.05, 516.93)
37	(12.93, 12.23)	(509.05, 481.50)
38	(12.93, 11.33)	(509.05, 446.06)
39	(12.93, 10.43)	(509.05, 410.63)

Table 3. Module Solder Pad Location

Solder Pad (Center of Pad)	Location (X,Y) from Orign (mm)	Dimension from Orign (mils)
40	(12.93, 9.53)	(509.05, 375.20)
41	(12.93, 8.62)	(509.05, 339.37)
42	(12.93, 7.72)	(509.05, 303.94)

Figure 7. Solder Pad Reference Location
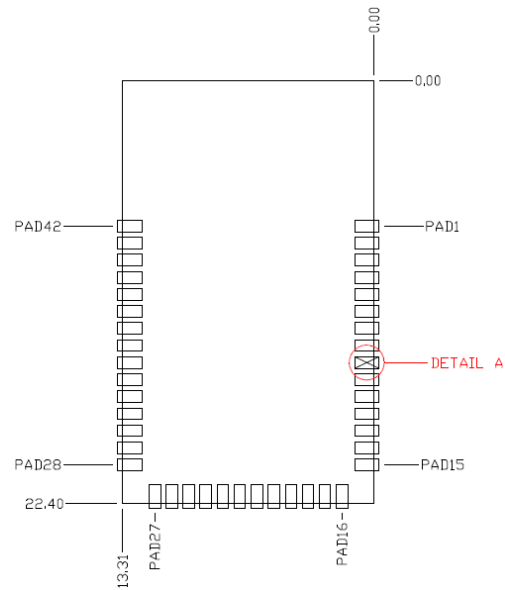
Top View (Seen on Host PCB)
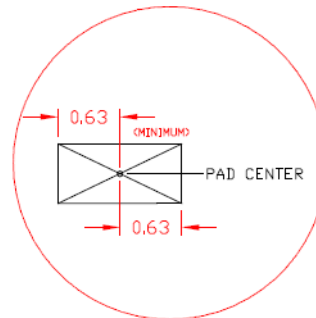
Module Connections

Table 4 details the solder pad connection definitions and available functions for the pad connections for the CYBT-343052-02 module. Table 4 lists the solder pads on the CYBT-343052-02 module, the silicon device pin, and denotes what functions are available for each solder pad.

Table 4.

Module Pad Name	Pad Number	Silicon Pin Name	I/O	Power Domain	Description
Microphone		**Microphone**			
MIC_AVDD	23	MIC_AVDD	I	MIC_AVDD	Microphone supply
MIC_BIAS	26	MICBIAS	O	MIC_AVDD	Microphone bias supply
MIC_N	24	MICN	I	MIC_AVDD	Microphone negative input
MIC_P	25	MICP	I	MIC_AVDD	Microphone positive input
GND_A	22 27	Analog ground for microphone			
Power Supply					
VDD	2	2.5V~3.6V			
Ground Pins		**Ground Pins**			
GND	1 18 21 42	HS-VSS	I	VSS	Digital ground
UART		**UART**			
UART_CTS_N	28	UART_CTS_N	I, PU	VDDO	CTS for HCI UART interface: NC if unused.
UART_RTS_N	29	UART_RTS_N	O, PU	VDDO	RTS for HCI UART interface. NC if unused.
UART_RXD	31	UART_RXD	I	VDDO	UART serial input. Serial data input for the HCI
					UART interface.
UART_TXD	30	UART_TXD	O, PU	VDDO	UART serial input. Serial data input for the HCI
					UART interface.
Interface		**Serial Peripheral Interface**			
NA	NA	SPI_MISO	I	VDDO	SPI Master In Slave Out
SPI_MOSI	32	SPI_MOSI	O	VDDO	SPI Master Out Slave In
NA	NA	SPI_CSN	O	VDDO	SPI Chip Select
NA	NA	SPI_CLK	O	VDDO	SPI Clock
Crystal		**Crystal**			
NA	NA	BT_XTALI	I	PLLVDD1P2	Crystal oscillator input: see "Crystal Oscillator" on page 12 for options
NA	NA	BT_XTALO	O	PLLVDD1P2	Crystal oscillator output
XTALI_32K	19	XTALI_32K	I	VDDO	Low-power oscillator input
XTALO_32K	20	XTALO_32K	O	VDDO	Low-power oscillator output
Others		**Others**			
NA	NA	DEFAULT_STRAP	I	VDDO	Connect to VDDO

Table 4. (continued)

Module Pad Name	Pad Number	Silicon Pin Name	I/O	Power Domain	Description
HOST_WAKE	35	BT_HOST_WAKE	O	VDDO	Host wake-up. This is a signal from the Bluetooth device to the host indicating that the Bluetooth device requires attention. ■ Asserted: Host device must wake up or remain awake ■ Deasserted: Host device may sleep when sleep awake criteria is met. The polarity of this signal is software configurable and can be asserted high or low.
NA	NA	BT_RF	I/O	PAVDD2P5	RF antenna port
NA	NA	JTAG_SEL	–	–	ARM JTAG debug mode control: connect to GND for all applications
XRES	3	RST_N	I	VDDO	Active-low system reset with open-drain output and internal pull-up resistor

Table 5.

Module pad Name	Pad Number	Silicon Pin Name	Direction Default	POR State	Power Domain	Default Alternate Function Description
P0	10	P0	Input	Floating	VDDO	GPIO: P0
						A/D converter input 29 **Note** Not available during TM1 = 1.
P1	9	P1	Input	Floating	VDDO	GPIO: P1
						A/D converter input 28
P2	33	P2	Input	Floating	VDDO	GPIO: P2
P3	34	P3	Input	Floating	VDDO	GPIO: P3
P4	36	P4	Input	Floating	VDDO	GPIO: P4
P5	37	P5	Input	Floating	VDDO	GPIO: P5
P6	38	P6	Input	Floating	VDDO	GPIO: P6
P7	39	P7	Input	Floating	VDDO	GPIO: P7
P8	40	P8	Input	Floating	VDDO	GPIO: P8
						A/D converter input 27
P9	17	P9	Input	Floating	VDDO	GPIO: P9
						A/D converter input 26
P10	16	P10	Input	Floating	VDDO	GPIO: P10
						A/D converter input 25
P11	15	P11	Input	Floating	VDDO	GPIO: P11
						A/D converter input 24
P12	14	P12	Input	Floating	VDDO	GPIO: P12
						A/D converter input 23
P13	13	P13	Input	Floating	VDDO	GPIO: P13
						A/D converter input 22
P14	41	P14	Input	Floating	VDDO	GPIO: P14
						A/D converter input 21

Table 5. (continued)

Module pad Name	Pad Number	Silicon Pin Name	Direction Default	POR State	Power Domain	Default Alternate Function Description
P15	19	P15	Input	Floating	VDDO	GPIO: P15
						A/D converter input 20
NA	NA	P16	Input	Floating	VDDO	GPIO: P16
						A/D converter input 19
P26	6	P26	Input	Floating	VDDO	GPIO: P26
		PWM0				Current: 16 mA sink
P27	5	P27	Input	Floating	VDDO	GPIO: P27
		PWM1				Current: 16 mA sink
P28	12	P28	Input	Floating	VDDO	GPIO: P28
		PWM2				A/D converter input 11
						Current: 16 mA sink
P29	11	P29	Input	Floating	VDDO	GPIO: P29
		PWM3				A/D converter input 10
						Current: 16 mA sink
P32	4	P32	Input	Floating	VDDO	GPIO: P32
						A/D converter input 7
P34	8	P34	Input	Floating	VDDO	GPIO: P34
						A/D converter input 5
P38	7	P38	Input	Floating	VDDO	GPIO: P38
						A/D converter input 1
NA	NA	P39	Input	Floating	VDDO	Reserved for system use. Leave this GPIO unconnected

Notes
4. The CYBT-343052-02 contains a single SPI (SPI1) peripheral supporting both master or slave configurations. SPI2 is used for on-module serial memory interface.
5. In Master mode, any available GPIO can be configured as SPI1_CS. This function is not explicitly shown in Table .

Connections and Optional External Components

Power Connections (VDDIN)

The CYBT-343052-02 contains one power supply connection, VDDIN, which accepts a supply input range of 2.3 V to 3.6 V for CYBT-343052-02. Table 12 provides this specification. The maximum power supply ripple for this power connection is 100 mV, as shown in Table 12.

It is not required to place any power supply decoupling or noise reduction circuitry on the host PCB. If desired, an external ferrite bead between the supply and the module connection can be included, but is not necessary. If used, the ferrite bead should be positioned as close as possible to the module pin connection and the recommended ferrite bead value is 330 Ω, 100 MHz.

*Considerations and Optional Components for Brown Out (BO) Conditions*

Power supply design must be completed to ensure that the CYBT-343052-02 module does not encounter a Brown Out condition, which can lead to unexpected functionality, or module lock up. A Brown Out condition may be met if power supply provided to the module during power up or reset is in the following range:

$$V_{IL} \leq VDDIN \leq V_{IH}$$

Refer to Table 13 for the V_{IL} and V_{IH} specifications.

System design should ensure that the condition above is not encountered when power is removed from the system. In the event that this cannot be guaranteed (that is, battery installation, high-value power capacitors with slow discharge), it is recommended that an external voltage detection device be used to prevent the Brown Out voltage range from occurring during power removal. Refer to Figure 8 for the recommended circuit design when using an external voltage detection IC.

Figure 8. Reference Circuit Block Diagram for External Voltage Detection IC
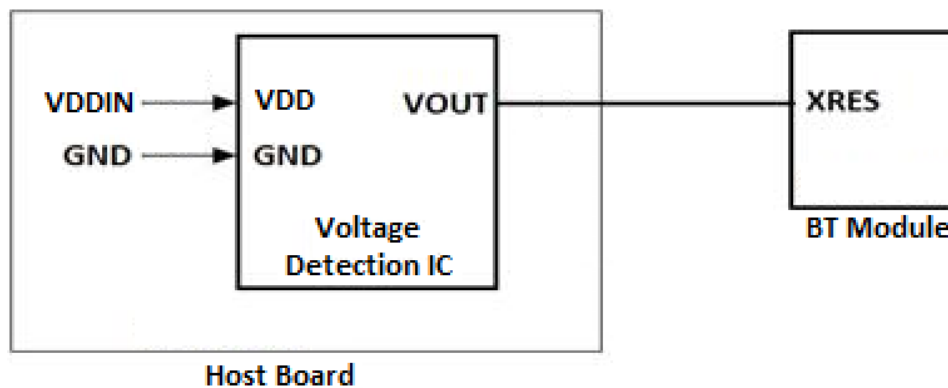
In the event that the module does encounter a Brown Out condition, and is operating erratically or is not responsive, power cycling the module will correct this issue and once reset, the module should operate correctly. Brown Out conditions can potentially cause issues that cannot be corrected, but in general, a power-on-reset operation will correct a Brown Out condition.

External Reset (XRES)

The CYBT-343052-02 has an integrated power-on reset circuit, which completely resets all circuits to a known power-on state. This action can also be evoked by an external reset signal, forcing it into a power-on reset state. The XRES signal is an active-low signal, which is an input to the CYBT-343052-02 module (solder pad 3). The CYBT-343052-02 module does not require an external pull-up resistor on the XRES input

During power-on operation, the XRES connection to the CYBT-343052-02 is required to be held low 50 ms after the VDD power supply input to the module is stable. This can be accomplished in the following ways:

■ The host device should connect a GPIO to the XRES of the Cypress CYBT-343052-02 module and pull XRES low until VDD is stable. XRES is recommended to be released 50 ms after VDDIN is stable.

■ If the XRES connection of the CYBT-343052-02 module is not used in the application, a 10-µF capacitor may be connected to the XRES solder pad of the CYBT-343052-02 to delay the XRES release. The capacitor value for this recommended implementation is approximate, and the exact value may differ depending on the VDDIN power supply ramp time of the system. The capacitor value should result in an XRES release timing of 50 ms after VDDIN stability.

■ The XRES release timing may be controlled by an external voltage detection IC. XRES should be released 50 ms after VDD is stable.

Refer to Figure on page 18 for XRES operating and timing requirements during power-on events.

Multiple-Bonded GPIO Connections

The CYBT-343052-02 contains GPIOs, which are multiple-bonded at the silicon level. If any of these dual-bonded GPIOs are used, only the functionality and features for one of these port pins may be used. The desired port pin should be configured in the WICED Studio SDK. For details on the features and functions that each of these multiple-bonded GPIOs provide, refer to Table .

The following list details the multiple-bonded GPIOs available on the CYBT-343052-02 module:

- PAD 1 P0/34: I2S_WS_PCM_SYNC/P0/P34 (triple bonded; only one of four is available)

- PAD 2 I2C_SCL: I2S_PCM_OUT/P3/P29/P35 (quadruple bonded; only one of four is available)

- PAD 4 I2C_SDA: I2S_PCM_IN/P12 (dual bonded; only one of two is available)

- PAD 5 P2/P37/P28: I2S_PCM_CLK/P2/P28/P37 (quadruple bonded; only one of four is available)

- PAD 11 GPIO_0: GPIO_0/P36/P38 (triple bonded; only one of three is available)

- PAD 12 GPIO_1: GPIO_1/P25/P32 (triple bonded; only one of three is available)

- PAD 14 GPIO_4: GPIO_4/LPO_IN/P6/P31 (quadruple bonded; only of four is available)

- PAD 15 P4/P24: BT_CLK_REQ/P4/P24 (triple bonded; only one of three is available)

- PAD 19 GPIO_7: GPIO_7/P30 (Dual bonded; only one of two is available)

- PAD 22 GPIO_3: GPIO_3/P27/P33 (triple bonded; only one of three is available)

- PAD 23 GPIO_6: GPIO_6/P11/P26 (triple bonded; only one of three is available)

Figure 9 illustrates the CYBT-343052-02 schematic.

Figure 9. CYBT-343052-02 Schematic Diagram
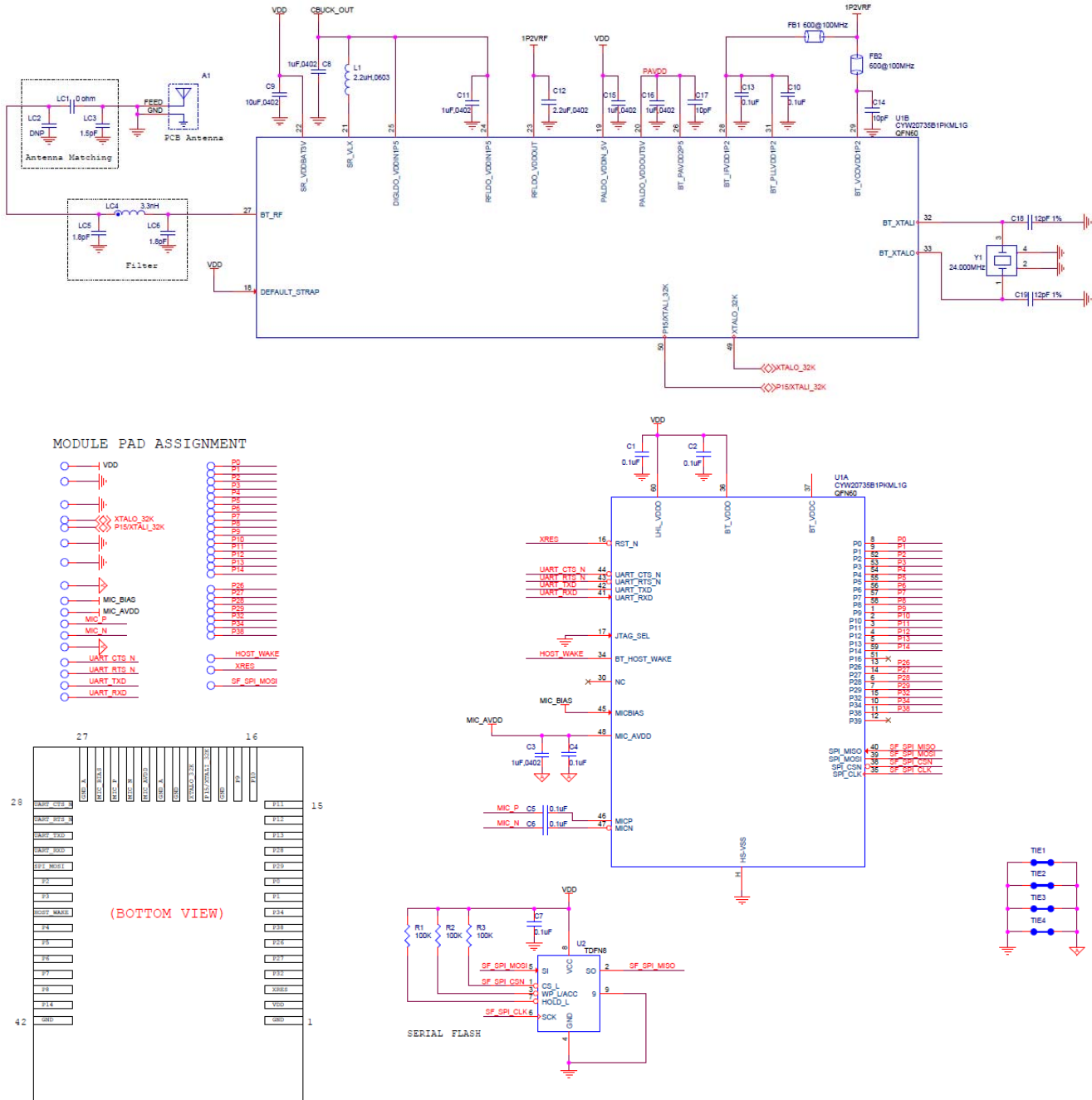
Critical Components List

Table 6 details the critical components used in the CYBT-343052-02 module.

Table 6. Critical Component List

Component	Reference Designator	Description
Silicon	U1	60-pin QFN BT/BLE Silicon Device - CYW20735
Silicon	U2	8-pin TDF8N, 512K Serial Flash
Crystal	Y1	24.000 MHz, 12PF

Antenna Design

Table 7 details trace antenna used in the CYBT-343052-02 module. For more information, see Table 7.

Table 7. Trace Antenna Specifications

Item	Description
Frequency Range	2400–2500 MHz
Peak Gain	0 dBi typical
Return Loss	10-dB minimum

Functional Description

Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules ACL and TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

Table 8. Bluetooth Features

Bluetooth 1.0	Bluetooth 1.2	Bluetooth 2.0
Basic Rate	Interlaced Scans	--
SCO	Adaptive Frequency Hopping	–
Paging and Inquiry	–	–
Page and Inquiry Scan	–	–
Sniff	–	–
Bluetooth 2.1	**Bluetooth 3.0**	**Bluetooth 4.0**
Secure Simple Pairing	Unicast Connectionless Data	Bluetooth Low Energy
Enhanced Inquiry Response	Enhanced Power Control	–
Sniff Subrating	–	–
Bluetooth 4.1	**Bluetooth 4.2**	**Bluetooth 5.0**
Low Duty Cycle Advertising	Data Packet Length Extension	LE 2Mbps
Dual Mode	LE Secure Connection	–
LE Link Layer Topology	Link Layer Privacy	–

Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task is performed in a different state or substate in the Bluetooth Link Controller.

■ BLE states:
  ❒ Advertising
  ❒ Scanning
  ❒ Connection

■ Major states:
  ❒ Standby
  ❒ Connection

■ Substates:
  ❒ Page
  ❒ Page Scan
  ❒ Inquiry
  ❒ Inquiry Scan
  ❒ Sniff

Test Mode Support

The CYBT-343052-02 fully supports the Bluetooth Test mode as described in Part I:1 of the Specification of the Bluetooth System Version 3.0. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the CYBT-343052-02 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

■ Fixed frequency carrier wave (unmodulated) transmission
  ❏ Simplifies some type-approval measurements (Japan)
  ❏ Aids in transmitter performance analysis

■ Fixed frequency constant receiver mode
  ❏ Receiver output directed to I/O pin
  ❏ Allows for direct BER measurements using standard RF test equipment
  ❏ Facilitates spurious emissions testing for receive mode

■ Fixed frequency constant transmission
  ❏ 8-bit fixed pattern or PRBS-9
  ❏ Enables modulated signal measurements with standard RF test equipment.

Frequency Hopping Generator

The frequency hopping sequence generator selects the correct hopping channel number based on the link controller state, Bluetooth clock, and device address.

Microcontroller Unit

The CYW20735B1 microprocessor unit runs software from the link control (LC) layer up to the host controller interface (HCI). The microprocessor is a Cortex-M4 32-bit RISC processor with embedded ICE-RT debug and serial wire debug (SWD) interface units.

The microprocessor also includes 2 MB of ROM memory for program storage and 384 KB of RAM for data scratch-pad. The internal ROM provides flexibility during power-on reset to enable the same device to be used in various configurations. At powerup, the lower-layer protocol stack is executed from internal ROM.

External patches can be applied to the ROM-based firmware to provide flexibility for bug fixes and feature additions. The device also supports the integration of user applications and profiles.

Floating Point Unit

CYW20735B1 includes the CM4 single precision IEEE-754 compliant floating point unit. For details, see the Cortex-M4 manual.

OTP Memory

The CYW20735B1 includes 2 KB of one-time programmable memory that can be used by the factory to store product-specific information.

Note Use of OTP requires that a 3V supply be present at all times.

NVRAM Configuration Data and Storage

NVRAM contains configuration information about the customer application, including the following:

■ Fractional-N information

■ BD_ADDR

■ UART baud rate

■ SDP service record

■ File system information used for code, code patches, or data. The CYW20735B1 uses SPI Serial Flash for NVRAM storage.
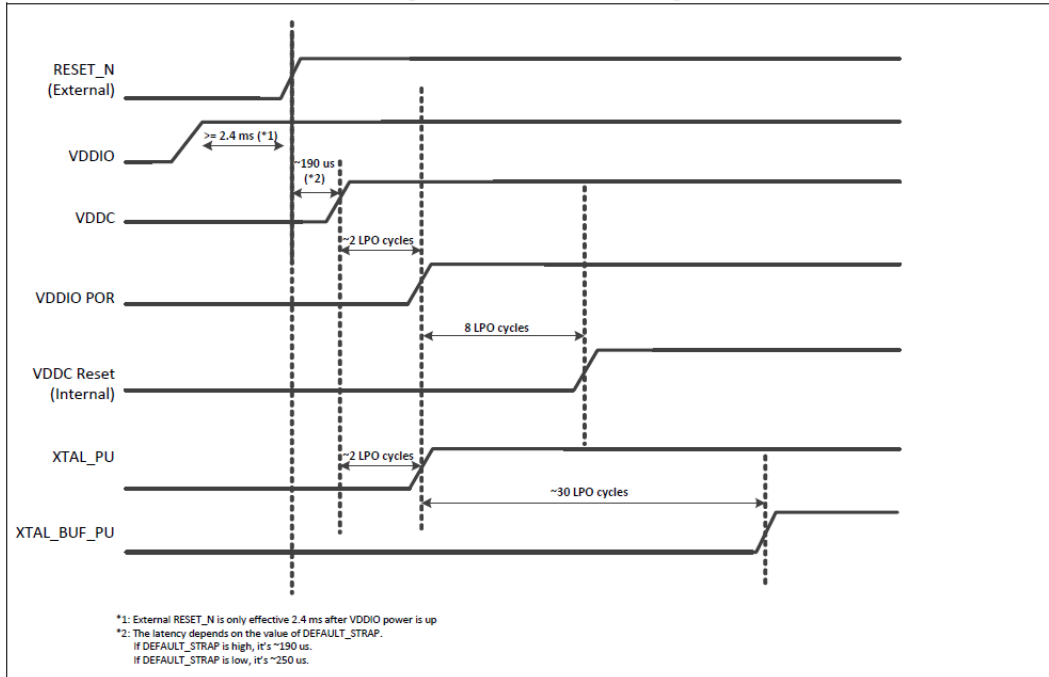
Power-On Reset (POR)

The CYW20735B1 includes POR logic to allow the part to initialize correctly when power is applied. Figure 10 shows the sequence used by the CYW20735B1 during initialization. An small external cap may be used on RESET_N to add delay as VDDIO ramps up.

External Reset (XRES)

The CYBT-343052-02 has an integrated power-on reset circuit that completely resets all circuits to a known power-on state. An external active low reset signal, XRES, can be used to put the CYBT-343052-02 in the reset state. The XRES pin has an internal pull-up resistor and, in most applications, it does not require anything to be connected to it.

Figure 10. Power-On Reset Timing

*1: External RESET_N is only effective 2.4 ms after VDDIO power is up
*2: The latency depends on the value of DEFAULT_STRAP.
    If DEFAULT_STRAP is high, it's ~190 us.
    If DEFAULT_STRAP is low, it's ~250 us.

Brownout Detection

An external voltage detector reset IC may be used if brownout detection is required. The reset IC should release RESET_N only after the VDDO supply voltage level has been at or above a minimum operating voltage for 50 ms or longer.

Integrated Radio Transceiver

The CYBT-343052-02 has an integrated radio transceiver that has been optimized for use in 2.4-GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4-GHz unlicensed ISM band. The CYBT-343052-02 is fully compliant with the Bluetooth Radio Specification and enhanced data rate (EDR) specification and meets or exceeds the requirements to provide the highest communication link quality of service.

Transmitter Path

The CYBT-343052-02 features a fully integrated transmitter. The baseband transmit data is GFSK modulated in the 2.4 GHz ISM band.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal.

Power Amplifier

The CYW20735B1 has an integrated power amplifier (PA) that can transmit up to +10 dBm for class 1 operations.

Receiver Path

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the CYBT-343052-02 to be used in most applications with minimal off-chip filtering.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the CYBT-343052-02 provides a receiver signal strength indicator (RSSI) to the baseband. This enables the controller to take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

Local Oscillator Generation

The local oscillator (LO) provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation sub-block employs an architecture for high immunity to LO pulling during PA operation. The CYBT-343052-02 uses an internal loop filter.

Calibration

The CYBT-343052-02 radio transceiver features an automated calibration scheme that is fully self-contained in the radio. No user interaction is required during normal operation or during manufacturing to provide optimal performance. Calibration tunes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops, and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

Peripheral and Communication Interfaces

I²C Communication Interface

The CYBT-343052-02 provides a 2-pin master I²C interface, which can be used to retrieve configuration information from an external EEPROM or to communicate with peripherals such as track-ball or touch-pad modules, and motion tracking ICs used in mouse devices. This interface is compatible with I²C slave devices. I²C does not support multimaster capability or flexible wait-state insertion by either master or slave devices.

The following transfer clock rates are supported by the I²C:

■ 100 kHz

■ 400 kHz

■ 800 kHz (not a standard I²C-compatible speed.)

■ 1 MHz (Compatibility with high-speed I²C-compatible devices is not guaranteed.)

The following transfer types are supported by the I²C:

■ Read (Up to 8 bytes can be read)

■ Write (Up to 8 bytes can be written)

■ Read-then-Write (Up to 8 bytes can be read and up to 8 bytes can be written)

■ Write-then-Read (Up to 8 bytes can be written and up to 8 bytes can be read)

Hardware controls the transfers, requiring minimal firmware setup and supervision.

The clock pad (I2C_SCL) and data pad 2 (I2C_SDA) are both open-drain I/O pins. Pull-up resistors, external to the CYBT-343052-02, are required on both the SCL and SDA pad for proper operation.

HCI UART Interface

The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 57600 bps to 6 Mbps. During initial boot, UART speeds may be limited to 750 kbps. The baud rate may be selected via a vendor-specific UART HCI command. The CYBT-343052-02 has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

The UART clock default setting is 24 MHz, and can be configured to run as high as 48 MHz to support up to 6 Mbps. The baud rate of the CYBT-343052-02UART is controlled by two values. The first is a UART clock divisor (set in the DLBR register) that divides the UART clock by an integer multiple of 16. The second is a baud rate adjustment (set in the DHBR register) that is used to specify a number of UART clock cycles to stuff in the first or second half of each bit time. Up to eight UART cycles can be inserted into the first half of each bit time, and up to eight UART clock cycles can be inserted into the end of each bit time.

Table 9 contains example values to generate common baud rates with a 24 MHz UART clock.

Table 9. Common Baud Rate Examples, 24 MHz Clock

Baud Rate (bps)	Baud Rate Adjustment		Mode	Error (%)
	High Nibble	Low Nibble		
3M	0xFF	0xF8	High rate	0.00
2M	0XFF	0XF4	High rate	0.00
1M	0X44	0XFF	Normal	0.00
921600	0x05	0x05	Normal	0.16
460800	0x02	0x02	Normal	0.16
230400	0x04	0x04	Normal	0.16
115200	0x00	0x00	Normal	0.16
57600	0x00	0x00	Normal	0.16
38400	0x01	0x00	Normal	0.00

Table 10 contains example values to generate common baud rates with a 48 MHz UART clock.

Table 10. Common Baud Rate Examples, 48 MHz Clock

Baud Rate (bps)	High Rate	Low Rate	Mode	Error (%)
6M	0xFF	0xF8	High rate	0
4M	0xFF	0xF4	High rate	0
3M	0x0	0xFF	Normal	0
2M	0x44	0xFF	Normal	0
1.5M	0x0	0xFE	Normal	0
1M	0x0	0xFD	Normal	0
921600	0x22	0xFD	Normal	0.16
230400	0x0	0xF3	Normal	0.16
115200	0x1	0xE6	Normal	−0.08
57600	0x1	0xCC	Normal	0.04

Normally, the UART baud rate is set by a configuration record downloaded after reset. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

The CYBT-343052-02 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Triac Control

The CYBT-343052-02 includes hardware support for zero-crossing detection and trigger control for up to four triacs. The CYBT-343052-02 detects zero-crossing on the AC zero detection line and uses that to provide a pulse that is offset from the zero crossing. This allows the CYBT-343052-02to be used in dimmer applications, as well as any other applications that require a control signal that is offset from an input event.

The zero-crossing hardware includes an option to suppress glitches.

Peripheral UART Interface

The CYBT-343052-02 has a second UART that may be used to interface to peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each functional pin. The CYBT-343052-02 can map the peripheral UART to any LHL GPIO. The peripheral UART clock is fixed at 24 MHz. Both TX and RX have a 256-byte FIFO (see Table 4 on page 9).

Serial Peripheral Interface

The CYBT-343052-02 has two independent SPI interfaces, both of which support single, dual, and quad mode SPI operations. Either interface can be a master or a slave. Each interface has a 64-byte transmit buffer and a 64-byte receive buffer. To support more flexibility for user applications, the CYBT-343052-02 has optional I/O ports that can be configured individually and separately for each functional pin. The CYBT-343052-02 acts as an SPI master device that supports 1.8V or 3.3V SPI slaves. The CYBT-343052-02 can also act as an SPI slave device that supports a 1.8V or 3.3V SPI master.

Note SPI voltage depends on VDDO/VDDM; therefore, it defines the type of devices that can be supported.

Infrared Modulator

The CYBT-343052-02 includes hardware support for infrared TX. The hardware can transmit both modulated and unmodulated waveforms. For modulated waveforms, hardware inserts the desired carrier frequency into all IR transmissions. IR TX can be sourced from firmware-supplied descriptors, a programmable bit, or the peripheral UART transmitter.

If descriptors are used, they include IR on/off state and the duration between 1–32767/μsec. The CYBT-343052-02 IR TX firmware driver inserts this information in a hardware FIFO and makes sure that all descriptors are played out without a glitch due to underrun (see Figure 11).

Figure 11. Infrared TX
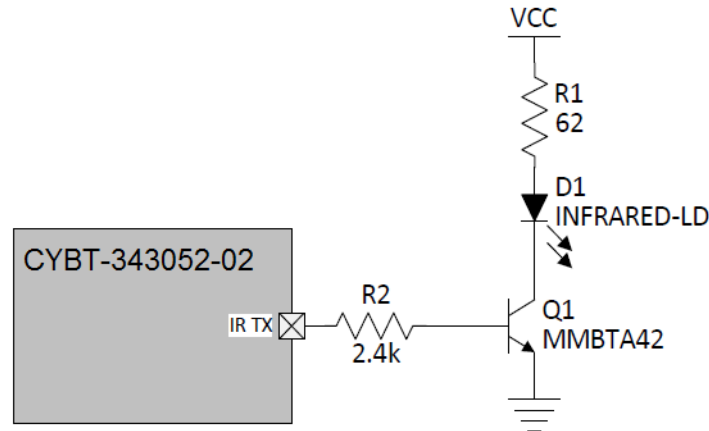
PDM Microphone

The CYBT-343052-02 accepts a $\Sigma\Delta$-based one-bit pulse density modulation (PDM) input stream and outputs filtered samples at either 8 kHz or 16 kHz sampling rates. The PDM signal derives from an external kit that can process analog microphone signals and generate digital signals. The digital signal passes through the chip IO and MUX inputs using an auxADC signal. The PDM shares the filter path with the aux ADC.

Two types of data rates can be supported:

■ 8 kHz

■ 16 kHz

The external digital microphone accepts a 2.4 MHz clock generated by the CYBT-343052-02 and outputs a PDM signal which is registered by the PDM interface with either the rising or falling edge of the 2.4 MHz clock selectable through a programmable control bit. The design can accommodate two simultaneous PDM input channels, so stereo voice is possible.

Security Engine

The CYBT-343052-02 includes a hardware security accelerator that greatly decreases the time required to perform typical security operations. These functions include:

■ Public key acceleration (PKA) cryptography

■ AES-CTR/CBC-MAC/CCM acceleration

■ SHA2 message hash and HMAC acceleration

■ RSA encryption and decryption of modulus sizes up to 2048 bits

■ Elliptic curve Diffie-Hellman in prime field GF(p)

■ Generic modular math functions

Keyboard Scanner

The keyboard scanner is designed to autonomously sample keys and store them into buffer registers without the need for the host microcontroller to intervene. The scanner has the following features:

■ Ability to turn off its clock if no keys are pressed.

■ Sequential scanning of up to 160 keys in an 8 × 20 matrix.

■ Programmable number of columns from 1 to 20.

■ Programmable number of rows from 1 to 8.

■ 16-byte key code buffer (can be augmented by firmware).

■ 128 kHz clock that allows scanning of full 160-key matrix in about 1.2 ms.

■ N-key rollover with selective 2-key lockout if ghost is detected.

■ Keys are buffered until host microcontroller has a chance to read it, or until overflow occurs.

■ Hardware debouncing and noise/glitch filtering.

■ Low-power consumption. Single-digit μA-level sleep current.

Theory of Operation

The key scan block is controlled by a state machine with the following states: Idle, Scan, Scan End.

Idle

The state machine begins in the idle state. In this state, all column outputs are driven high. If any key is pressed, a transition occurs on one of the row inputs. This transition causes the 128 kHz clock to be enabled (if it is not already enabled by another peripheral) and the state machine to enter the scan state. Also in this state, an 8-bit row-hit register and an 8-bit key-index counter is reset to 0.

Scan

In the scan state, a row counter counts from 0 up to a programmable number of rows minus 1. After the last row is reached, the row counter is reset and the column counter is incremented. This cycle repeats until the row and column counters are both at their respective terminal count values. At that point, the state machine moves into the Scan-End state.

As the keys are being scanned, the key-index counter is incremented. This counter value is compared to the modifier key codes stored in RAM, or in the key code buffer if the key is not a modifier key. It can be used by the microprocessor as an index into a lookup table of usage codes.

Also, as the nth row is scanned, the row-hit register is ORed with the current 8-bit row input values if the current column contains two or more row hits. During the scan of any column, if a key is detected at the current row, and the row-hit register indicates that a hit was detected in that same row on a previous column, then a ghost condition may have occurred, and a bit in the status register is set to indicate this.

Scan End

This state determines whether any keys were detected while in the scan state. If yes, the state machine returns to the scan state. If no, the state machine returns to the idle state, and the 128 kHz clock request signal is made inactive.

Note The microcontroller can poll the key status register.

Mouse Quadrature Signal Decoder

The mouse signal decoder is designed to autonomously sample two quadrature signals commonly generated by an optomechanical mouse. The decoder has the following features:

■ Three pairs of inputs for X, Y, and Z (typical scroll wheel) axis signals. Each axis has two options:
  ❏ For the X axis, choose P2 or P32 as X0 and P3 or P33 as X1.
  ❏ For the Y axis, choose P4 or P34 as Y0 and P5 or P35 as Y1.
  ❏ For the Z axis, choose P6 or P36 as Z0 and P7 or P37 as Z1.

■ Control of up to four external high-current GPIOs to power external optoelectronics:
  ❏ Turn-on and turn-off time can be staggered for each HC-GPIO to avoid simultaneous switching of high currents and having multiple high-current devices on at the same time.
  ❏ Sample time can be staggered for each axis.
  ❏ Sense of the control signal can be active high or active low.
  ❏ Control signal can be tristated for off condition or driven high or low, as appropriate.

Theory of Operation

The mouse decoder block has four 10-bit PWMs for controlling external quadrature devices and sampling the quadrature inputs at its core.

The GPIO signals may be used to control such items as LEDs, external ICs that may emulate quadrature signals, photodiodes, and photodetectors.

ADC Port

The ADC block is a single switched-cap $\Sigma\text{-}\Delta$ ADC core for audio and DC measurement. It operates at the 12 MHz clock rate and has 32 DC input channels, including 28 GPIO inputs. The internal bandgap reference has ±5% accuracy without calibration. Different calibration and digital correction schemes can be applied to reduce ADC absolute error and improve measurement accuracy in DC mode.

Clock Frequencies

The CYBT-343052-02 has an integrated 24-MHz crystal on the module. There is no need to add an additional crystal oscillator.

GPIO Port

GPIO ports for this device is shown in Table 4-2 on page 9. The CYBT-343052-02 uses 39 general-purpose I/Os (GPIOs). All GPIOs support programmable pull-ups and are capable of driving up to 8 mA at 3.3V or 4 mA at 1.8V, except P26, P27, P28, and P29, which are capable of driving up to 16 mA at 3.3V or 8 mA at 1.8V.

P0, P1, P8-P15, P17, P18, P21-23, P28-P38: all of these pins can be programmed as ADC inputs.

Port 26-Port 29: All four of these pins are capable of sinking up to 16 mA for LEDs. These pins also have the PWM function, which can be used for LED dimming.

PWM

The CYBT-343052-02 has four PWMs. The PWM module consists of the following:

- PWM0-5. Each of the six PWM channels contains the following registers:
  - 16-bit initial value register (read/write)
  - 16-bit toggle register (read/write)
  - 16-bit PWM counter value register (read)
- PWM configuration register shared among PWM0-5 (read/write). This 18-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

Figure 12 shows the structure of one PWM.

Figure 12. PWM Block Diagram
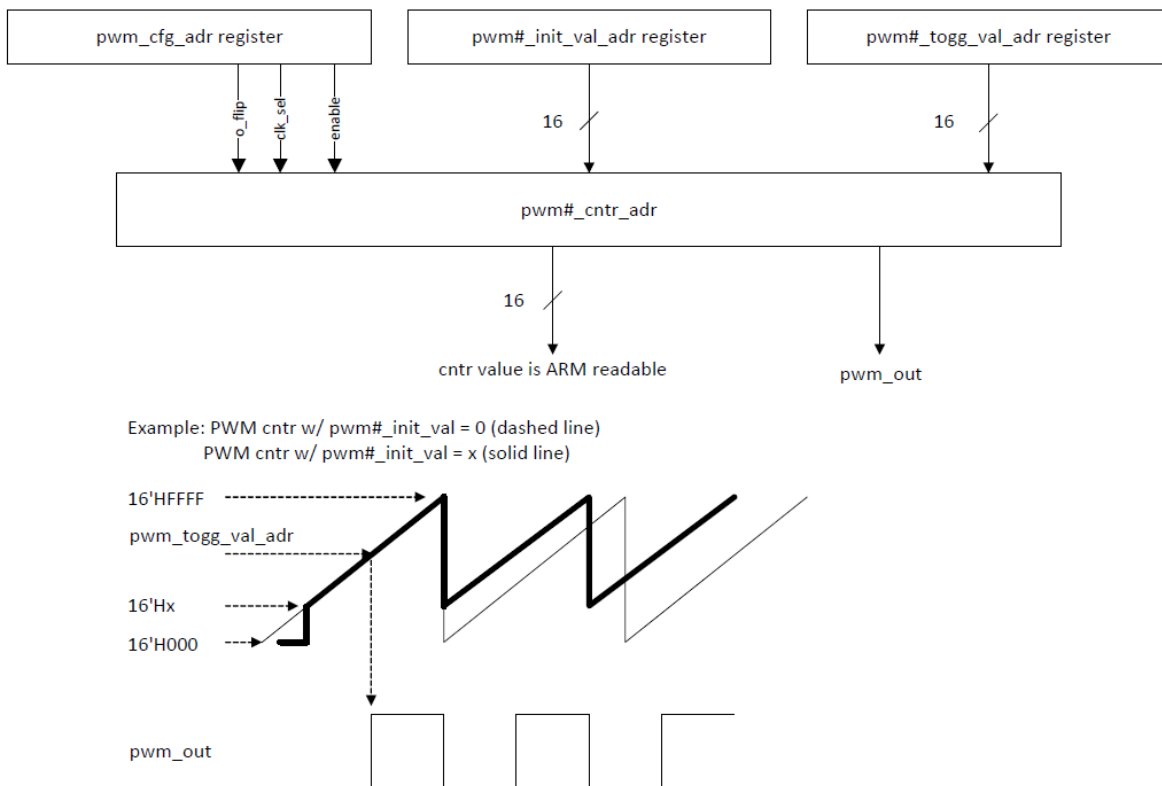
Power Management Unit

The Power Management Unit (PMU) provides power management features that can be invoked by software through power management registers or packet-handling in the baseband core.

RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4-GHz transceiver, which then processes the power-down functions accordingly.

Host Controller Power Management

Power is automatically managed by the firmware based on input device activity. As a power-saving task, the firmware controls the disabling of the on-chip regulator when in Deep Sleep (HIDOFF) mode.

BBC Power Management

There are several low-power operations for the BBC:

■ Physical layer packet handling turns RF on and off dynamically within packet TX and RX.

■ Bluetooth-specified low-power connection mode. While in these low-power connection modes, the CYBT-343052-02 runs on the Low Power Oscillator and wakes up after a predefined time period.

The CYBT-343052-02 automatically adjusts its power dissipation based on user activity. The following power modes are supported:

■ Active mode

■ Idle mode

■ Sleep mode

■ HIDOFF (Deep Sleep) mode

The CYBT-343052-02 transitions to the next lower state after a programmable period of user inactivity. Busy mode is immediately entered when user activity resumes.

In HIDOFF (Deep Sleep) mode, the CYBT-343052-02 baseband and core are powered off by disabling power to VDDC_OUT and PAVDD. The VDDO domain remains powered up and will turn the remainder of the chip on when it detects user events. This mode minimizes chip power consumption and is intended for long periods of inactivity.

Electrical Characteristics

Table 11 shows the maximum electrical rating for voltages referenced to VDDIN pad.

Table 11. Maximum Electrical Rating

Rating	Symbol	Value	Unit
V_{DDIN}	–	3.795	V
Voltage on input or output pin	–	V_{SS} – 0.3 to V_{DD} + 0.3	
Operating ambient temperature range	T_{opr}	–30 to +85	°C
Storage temperature range	T_{stg}	–40 to +85	

Table 12 shows the power supply characteristics for the range T_J = 0 to 125 °C.

Table 12. Power Supply

Parameter	Description	Min[6]	Typ	Max[6]	Unit
V_{DDIN}	Power Supply Input (CYBT-343052-02)	2.5	–	3.6	V
V_{DDIN_RIPPLE}	Maximum Power Supply Ripple for V_{DDIN} input voltage	–	–	100	mV

Table 13 shows the specifications for the digital voltage levels.

Table 13. Digital Voltage Levels

Characteristics	Symbol	Min	Typ	Max	Unit
Input low voltage	V_{IL}	–	–	0.8	V
Input high voltage	V_{IH}	2.0	–	–	
Output low voltage	V_{OL}	–	–	0.4	
Output high voltage	V_{OH}	V_{DDIN} – 0.4	–	–	
Input capacitance (V_{DDMEM} domain)	C_{IN}	–	–	0.4	pF

Table 14 shows the current consumption measurements

Table 14. BLE Current Consumption

Operational Mode	Conditions	Typ	Unit
Receiving	Receiver and baseband are both operating, 100% ON.	8	mA
Transmitting@12 dBm	Transmitter and baseband are both operating, 100% ON.	18	
Advertising	1.28s direct advertising in low power idle mode	30	µA
Scanning	TBD	TBD	mA
Connecting	1-second connection interval in low power idle mode	25	µA
HIDOFF (Deep Sleep)	–	1	

Note
6. Overall performance degrades beyond minimum and maximum supply voltages.The voltage range specified is determined by the minimum and maximum operating voltage of the SPI Serial Flash included on the module.

Chipset RF Specifications

All specifications in Table 15 are for industrial temperatures and are single-ended. Unused inputs are left open.

Table 15. Receiver RF Specifications

Parameter	Conditions	Min	Typ[1]	Max	Unit
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity [2]	–	–	–91.5	–	–
Maximum input	GFSK, 1 Mbps	–	–	–20	dBm
Interference Performance					
TBD					
Out-of-Band Blocking Performance (CW)[3]					
30 MHz–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	
2498–3000 MHz	0.1% BER	–	–27	–	
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	
Intermodulation Performance[4]					
BT, Df = 4 MHz	–	–39.0	–	–	dBm
Spurious Emissions[5]					
30 MHz to 1 GHz	–	–	–	–62	dBm
1 GHz to 12.75 GHz	–	–	–	–47	
65 MHz to 108 MHz	FM RX	–	–147	–	dBm/Hz
746 MHz to 764 MHz	CDMA	–	–147	–	
851–894 MHz	CDMA	–	–147	–	
925–960 MHz	EDGE/GSM	–	–147	–	
1805–1880 MHz	EDGE/GSM	–	–147	–	
1930–1990 MHz	PCS	–	–147	–	
2110–2170 MHz	WCDMA	–	–147	–	

1. Typical operating conditions are 1.22V operating voltage and 25°C ambient temperature.
2. The receiver sensitivity is measured at BER of 0.1% on the device interface.
3. Meets this specification using front-end band pass filter.
4. f0 = –64 dBm Bluetooth-modulated signal, f1 = –39 dBm sine wave, f2 = –39 dBm Bluetooth-modulated signal, f0 = 2f1 – f2, and |f2 – f1| = n*1 MHz, where n is 3, 4, or 5. For the typical case, n = 4.
5. Includes baseband radiated emissions.

Notes
7. Typical operating conditions are 1.22-V operating voltage and 25°C ambient temperature.
8. The receiver sensitivity is measured at BER of 0.1% on the device interface.
9. Meets this specification using front-end band pass filter.

Table 16. Transmitter RF Specifications (TBD)

Parameter	Conditions	Min	Typ	Max	Unit
General					
Frequency range	–	2402	–	2480	MHz
Class 1: GFSK TX power	–	–	10	–	dBm
Power control step	–	2	4	8	dB
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0[10]	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0[11]	
1.8 GHz to 1.9 GHz	–	–	–	–47.0	
5.15 GHz to 5.3 GHz	–	–	–	–47.0	

Notes
10. Maximum value is the value required for Bluetooth qualification.
11. Meets this spec using a front-end band-pass filter.

Table 17. BLE RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	N/A	2402	–	2480	MHz
RX sense[1]	GFSK, 0.1% BER, 1 Mbps	–	–94.5	–	dBm
TX power	N/A	–	12	–	
Mod Char: Delta F1 average	N/A	225	255	275	kHz
Mod Char: Delta F2 max[2]	N/A	99.9	–	–	%
Mod Char: Ratio	N/A	0.8	0.95	–	

1. Dirty TX is OFF.
2. At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

Timing and AC Characteristics

In this section, use the numbers listed in the **Reference** column of each table to interpret the following timing diagrams.

UART Timing

Table 18. UART Timing Specifications

Reference	Characteristics	Min	Max	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	1.50	
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	0.67	Baud periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	1.33	

Figure 13. UART Timing
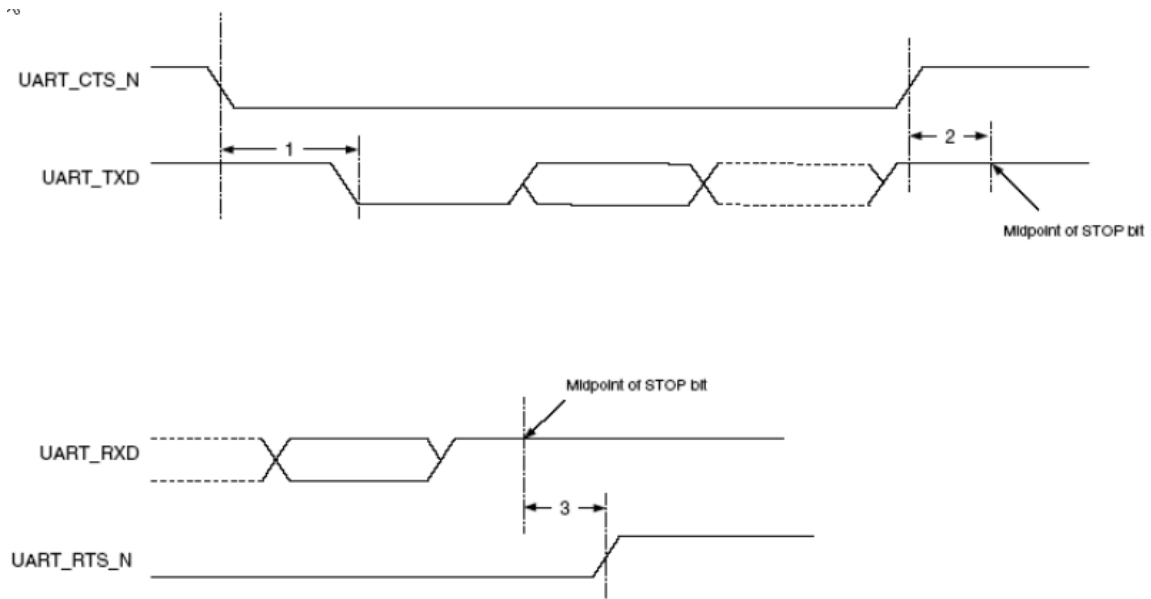
SPI Timing

The SPI interface supports clock speeds up to 12 MHz

Table 19 and Figure 14 show the timing requirements when operating in SPI Mode 0 and 2, and SPI Mode 1 and 3, respectively.

Table 19. SPI Mode 0 and 2

Reference	Characteristics	Min	Max	Unit
1	Time from slave assert SPI_INT to master assert SPI_CSN (DirectRead)	0	∞	ns
2	Time from master assert SPI_CSN to slave assert SPI_INT (DirectWrite)	0	∞	
3	Time from master assert SPI_CSN to first clock edge	20	∞	
4	Setup time for MOSI data lines	8	½ SCK	
5	Hold time for MOSI data lines	8	½ SCK	
6	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	
7	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	∞	
8	Idle time between subsequent SPI transactions	1 SCK	∞	

Figure 14. SPI Timing – Mode 0 and 2
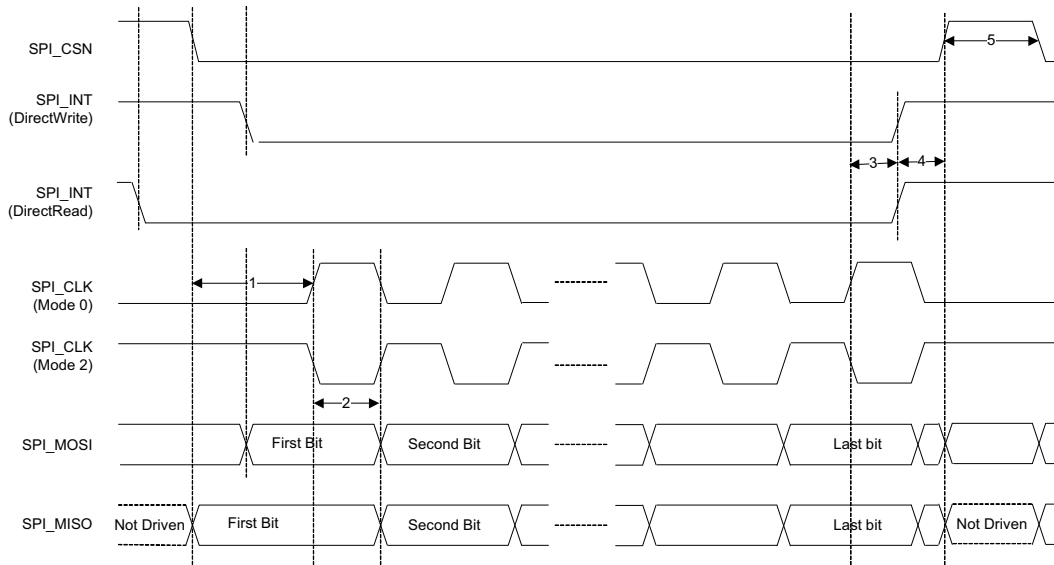
Table 20 and Figure 15 show the timing requirements when operating in SPI Mode 1 and 3.

Table 20. SPI Mode 1 and 3

Reference	Characteristics	Min	Max	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	
2	Hold time for MOSI data lines	12	½ SCK	
3	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
4	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	–	
5	Idle time between subsequent SPI transactions	1 SCK	–	

Figure 15. SPI Timing – Mode 1 and 3
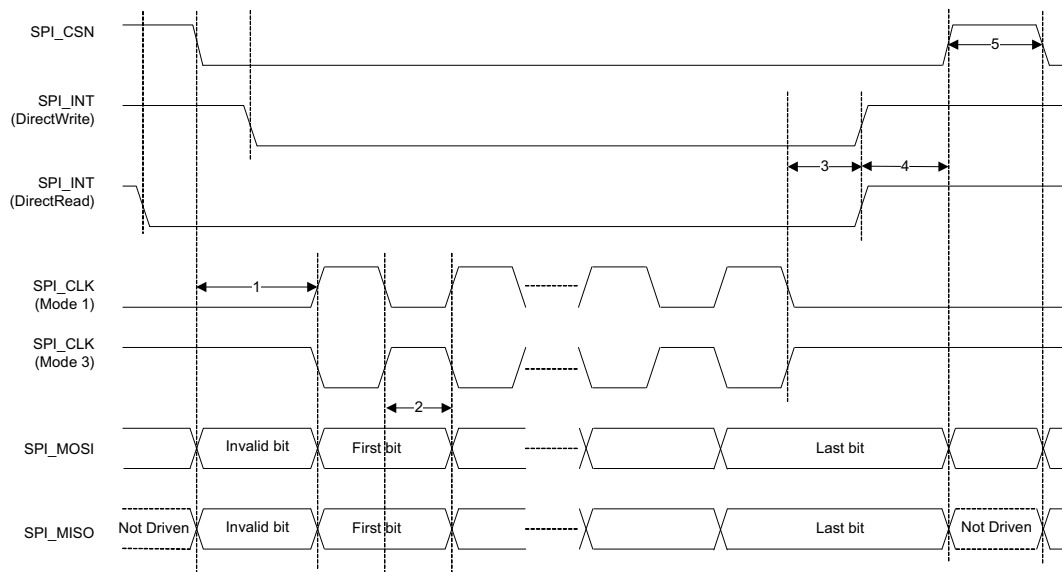
I^{2}C Interface Timing

Table 21. I^{2}C Interface Timing Specifications

Reference	Characteristics	Min	Max	Unit
1	Clock frequency	–	100	kHz
			400	
			800	
			1000	
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	
4	Clock low time	650	–	
5	Clock high time	280	–	
6	Data input hold time[12]	0	–	
7	Data input setup time	100	–	
8	STOP condition setup time	280	–	
9	Output valid from clock	–	400	
10	Bus free time[13]	650	–	

Notes
12. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
13. Time that the bus must be free before a new transaction can start.

Figure 16. I^{2}C Interface Timing Diagram
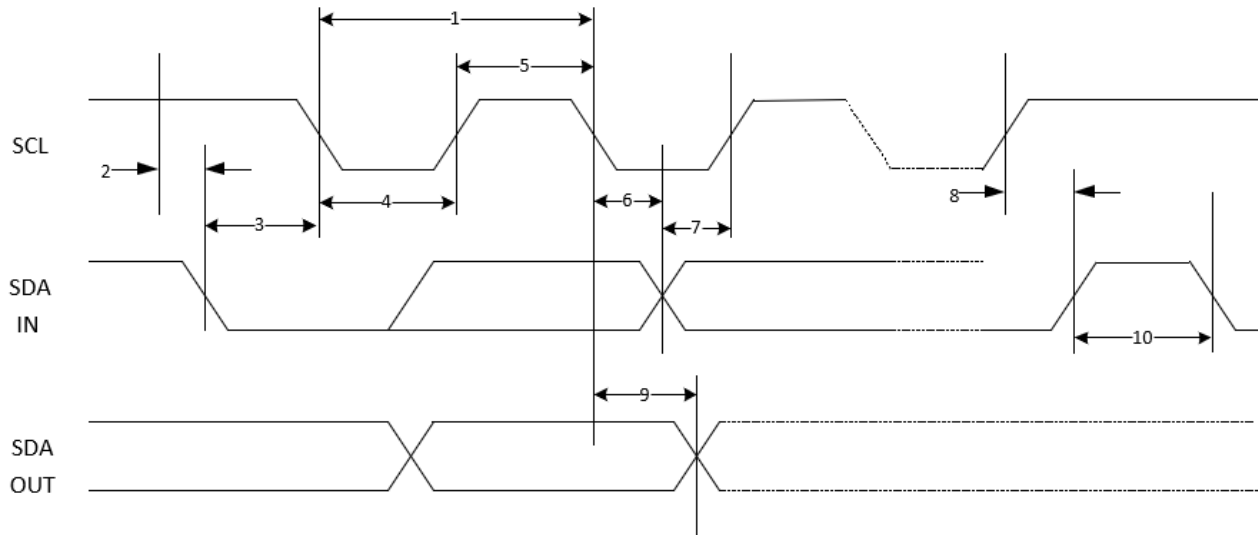
Table 22. Timing for I^{2}S Transmitters and Receivers

	Transmitter				Receiver				Notes
	Lower LImit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	14
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	15
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	15
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	16
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	16
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	17
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	18
Hold time t_{htr}	0	–	–	–	–	–	–	–	17
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	19
Hold time t_{hr}	–	–	–	–	–	0	–	–	18

Notes

14. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
15. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
16. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
17. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
18. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
19. The data setup and hold time must not be less than the specified receiver setup and hold time.

Note The time periods specified in Figure 17 and Figure 18 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Figure 17. I²S Transmitter Timing
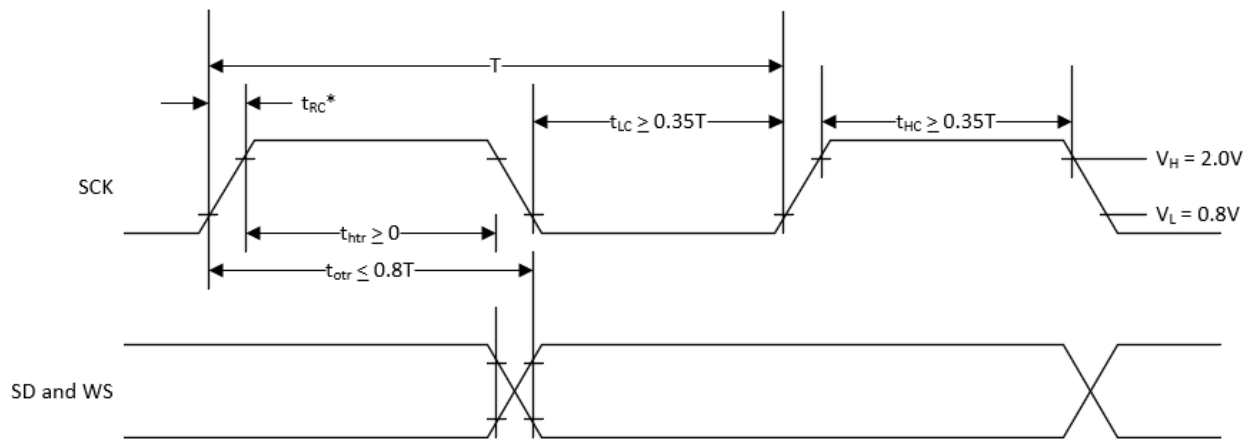
T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

Figure 18. I²S Receiver Timing
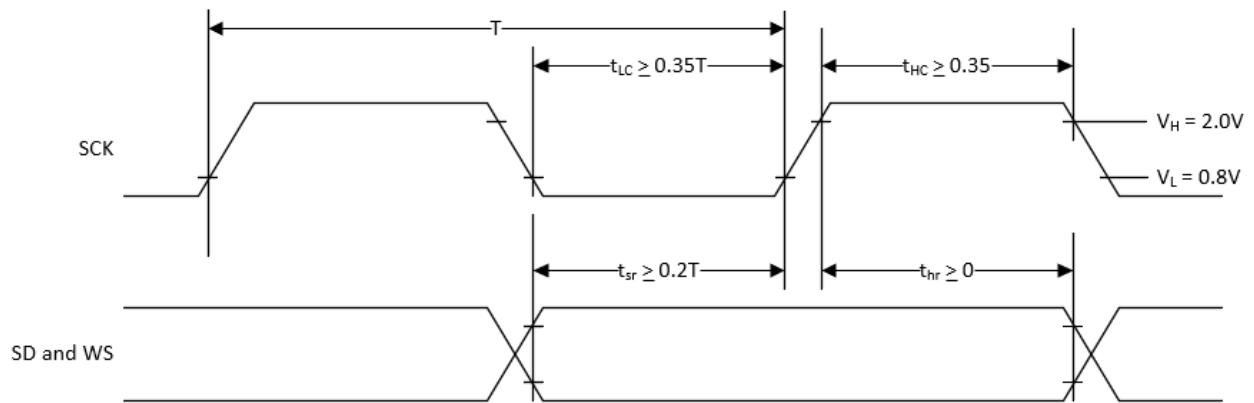
T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

Environmental Specifications

Environmental Compliance

This CYBT-343052-02 BLE module is produced in compliance with the Restriction of Hazardous Substances (RoHS) and Halogen-Free (HF) directives. The Cypress module and components used to produce this module are RoHS and HF compliant.

RF Certification

The CYBT-343052-02 module will be certified under the following RF certification standards at production release.

■ FCC: WAP3052

■ CE

■ IC: 7922A-3052

■ MIC: TBD

Safety Certification

The CYBT-343052-02 module complies with the following safety regulations:

■ Underwriters Laboratories, Inc. (UL): Filing E331901

■ CSA

■ TUV

Environmental Conditions

Table 23 describes the operating and storage conditions for the Cypress BLE module.

Table 23. Environmental Conditions for CYBT-343052-02

Description	Minimum Specification	Maximum Specification
Operating temperature	–30 °C	85 °C
Operating humidity (relative, non-condensation)	5%	85%
Thermal ramp rate	–	3 °C/minute
Storage temperature	–40 °C	85 °C
Storage temperature and humidity	–	85 °C at 85%
ESD: Module integrated into end system Components[20]	–	15 kV Air 2.0 kV Contact

Note
20. This does not apply to the RF pins (ANT).

ESD and EMI Protection

Exposed components require special attention to ESD and electromagnetic interference (EMI).

A grounded conductive layer inside the device enclosure is suggested for EMI and ESD performance. Any openings in the enclosure near the module should be surrounded by a grounded conductive layer to provide ESD protection and a low-impedance path to ground.

Device Handling: Proper ESD protocol must be followed in manufacturing to ensure component reliability.

Regulatory Information

FCC

FCC NOTICE:

The device CYBT-343052-02 complies with Part 15 of the FCC Rules. The device meets the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407.transmitter Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

CAUTION:

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Cypress Semiconductor may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that FCC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor FCC identifier for this product as well as the FCC Notice above. The FCC identifier is FCC ID: WAP3052.

In any case the end product must be labeled exterior with "Contains FCC ID: WAP3052"

ANTENNA WARNING:

This device is tested with a standard SMA connector and with the antenna listed in Table 7 on page 15. When integrated in the OEMs product, these fixed antennas require installation preventing end-users from replacing them with non-approved antennas. Any antenna not in the following table must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions.

RF EXPOSURE:

To comply with FCC RF Exposure requirements, the Original Equipment Manufacturer (OEM) must ensure to install the approved antenna in the previous.

The preceding statement must be included as a CAUTION statement in manuals, for products operating with the approved antenna in Table 7, to alert users on FCC RF Exposure compliance. Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of CYBT-343052-02 with the trace antenna is far below the FCC radio frequency exposure limits. Nevertheless, use CYBT-343052-02 in such a manner that minimizes the potential for human contact during normal operation.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

This module is only FCC authorized for the specific rule FCC 15.247 listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification, final host product requires Part 15 Subpart B compliance testing with the modular transmitter installed.

ISED

Innovation, Science and Economic Development Canada (ISED) Certification

CYBT-343052-02 is licensed to meet the regulatory requirements of Innovation, Science and Economic Development Canada (ISED),

License: IC: 7922A-3052

Manufacturers of mobile, fixed, or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from www.ic.gc.ca.

This device has been designed to operate with the antennas listed in Table 7 on page 15, having a maximum gain of 0 dBi. Antennas not included in this list or having a gain greater than 0 dBi   are strictly prohibited for use with this device. The require d antenna impedance is 50 ohms. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

ISED NOTICE:

The device CYBT-343052-02 including the built-in trace antenna complies with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-GEN. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

L'appareil CYBT-343052-02, y compris l'antenne intégrée, est conforme aux Règles RSS-GEN de Canada. L'appareil répond aux exigences d'approbation de l'émetteur modulaire tel que décrit dans RSS-GEN. L'opération est soumise aux deux conditions suivantes: (1) Cet appareil ne doit pas causer d'interférences nuisibles, et (2) Cet appareil doit accepter toute interférence reçue, y compris les interférences pouvant entraîner un fonctionnement indésirable.

ISED INTERFERENCE STATEMENT FOR CANADA

This device complies with Innovation, Science and Economic Development (ISED) Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil est conforme à la norme sur l'innovation, la science et le développement économique (ISED) norme RSS exempte de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

ISED RADIATION EXPOSURE STATEMENT FOR CANADA

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 15 mm between the radiator and your body.

Cet équipement est conforme aux limites d'exposition aux radiations ISED prévues pour un environnement incontrôlé. Cet équipement doit être installé et utilisé avec un minimum de 15 mm de distance entre la source de rayonnement et votre corps.

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that ISED labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor IC identifier for this product as well as the ISED Notices above. The IC identifier is 7922A-3052. In any case, the end product must be labeled in its exterior with "Contains IC: 7922A-3052"

European Declaration of Conformity

Hereby, Cypress Semiconductor declares that the Bluetooth module CYBT-343052-02 complies with the essential requirements and other relevant provisions of Directive 2014. As a result of the conformity assessment procedure described in Annex III of the Directive 2014, the end-customer equipment should be labeled as follows:

$$CE$$

All versions of the CYBT-343052-02 in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

MIC Japan

CYBT-343052-02 is certified as a module with certification number TBD. End products that integrate CYBT-343052-02 do not need additional MIC Japan certification for the end product.

End product can display the certification label of the embedded module.

Figure 19. MIC Label

TBD

Packaging

Table 24. Solder Reflow Peak Temperature

Module Part Number	Package	Maximum Peak Temperature	Maximum Time at Peak Temperature	No. of Cycles
CYBT-343052-02	42-pad SMT	260 °C	30 seconds	2

Table 25. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Module Part Number	Package	MSL
CYBT-343052-02	24-pad SMT	MSL 3

The CYBT-343052-02 is offered in tape and reel packaging. Figure 20 details the tape dimensions used for the CYBT-343052-02.

Figure 20. CYBT-343052-02 Tape Dimensions

Item	W	A_0	B_0	K_0	P_1	F	E	D_0	D_1	P_0	P_2	T
Measurement	$24.0^{+0.30}_{-0.30}$	$12.40^{+0.10}_{-0.10}$	$15.90^{+0.10}_{-0.10}$	$2.35^{+0.10}_{-0.10}$	$20.0^{+0.10}_{-0.10}$	$11.5^{+0.10}_{-0.10}$	$1.75^{+0.10}_{-0.10}$	$1.50^{+0.10}_{-0.00}$	$1.50^{+0.10}_{-0.10}$	$4.00^{+0.10}_{-0.10}$	$2.00^{+0.10}_{-0.10}$	$0.30^{+0.05}_{-0.05}$
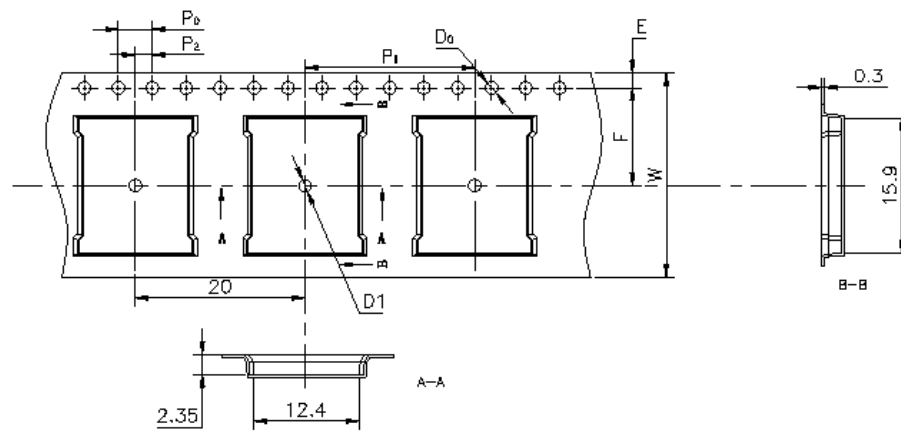
Figure 21 details the orientation of the CYBT-343052-02 in the tape as well as the direction for unreeling.

Figure 21. Component Orientation in Tape and Unreeling Direction
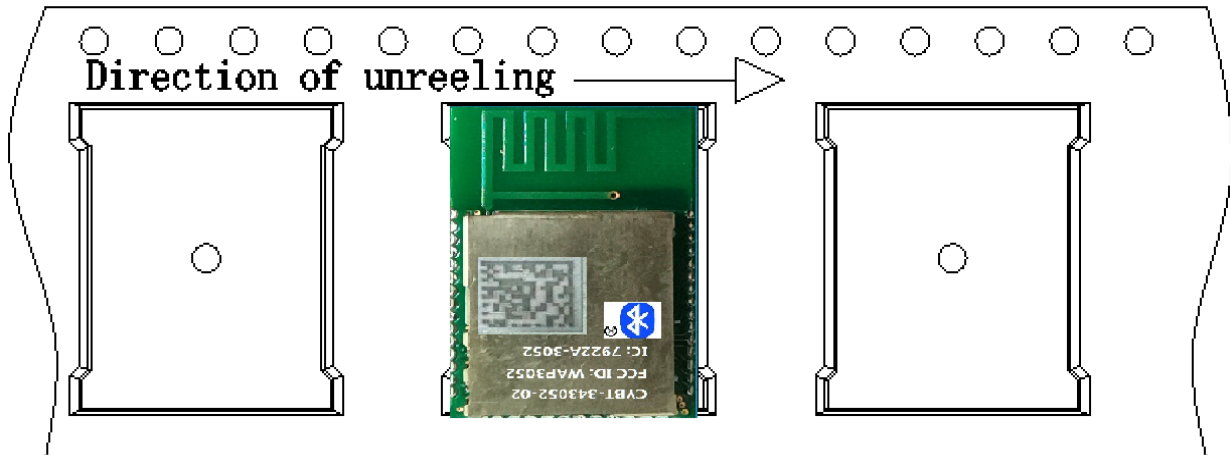
Figure 22 details reel dimensions used for the CYBT-343052-02.

Figure 22. Reel Dimensions

Index	NOTE	Dimension	Tolerance	
A	Inside Width	24.4	+2.0mm	−0.0mm
B	Reel Diameter	254.00	+2.0mm	−2.0mm
C	Outer Axis Diameter	100.00	+2.0mm	−2.0mm
D	Inner Axis Diameter	13.20	+0.3mm	−0.2mm
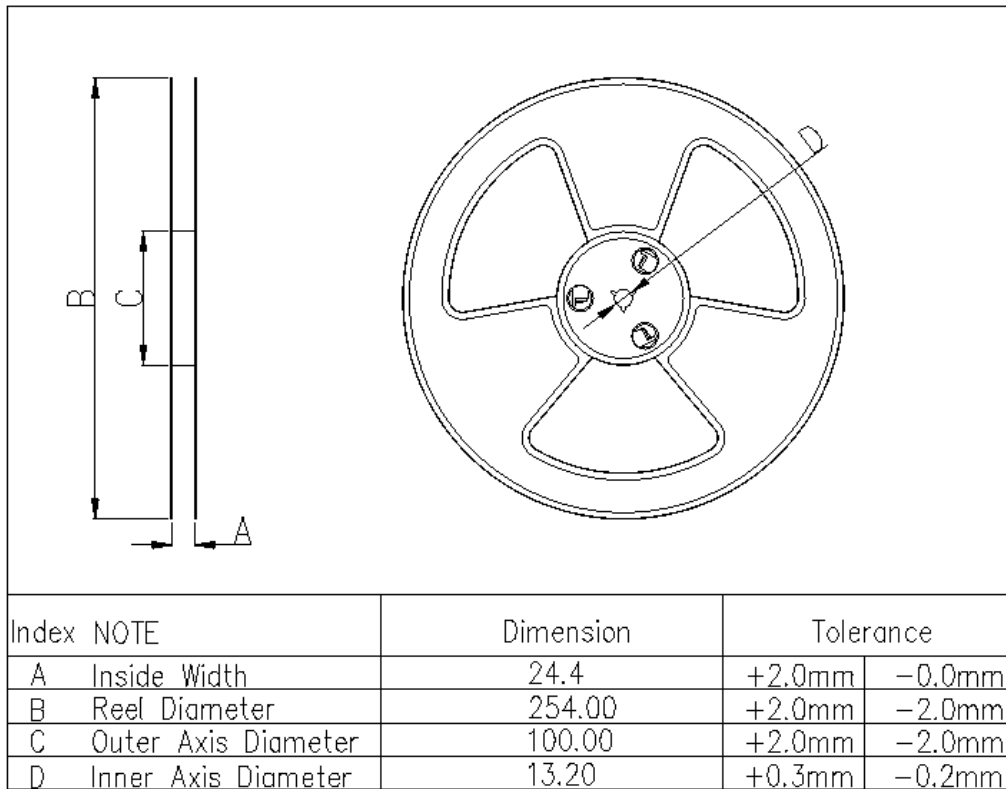
The CYBT-343052-02 is designed to be used with pick-and-place equipment in an SMT manufacturing environment. The center-of-mass for the CYBT-343052-02 is detailed in Figure 23.

Figure 23. CYBT-343052-02 Center of Mass
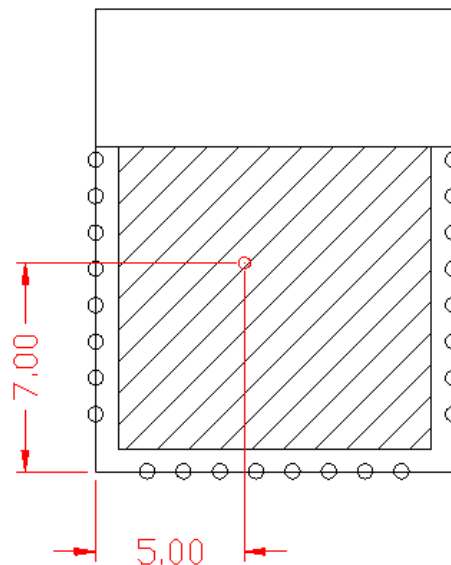
Ordering Information

Table 26 lists the CYBT-343052-02 part number and features. Table 27 lists the reel shipment quantities for the CYBT-343052-02.

Table 26. Ordering Information

Part Number	CPU Speed (MHz)	Flash Size (KB)	RAM Size (KB)	UART	I^{2}C (BSC)	PWM	Package	Packaging
CYBT-343052-02	96	512	384	Yes	Yes	6	42-SMT	Tape and Reel

Table 27. Tape and Reel Package Quantity and Minimum Order Amount

Description	Minimum Reel Quantity	Maximum Reel Quantity	Comments
Reel Quantity	500	500	Ships in 500 unit reel quantities.
Minimum Order Quantity (MOQ)	500	–	–
Order Increment (OI)	500	–	–

The CYBT-343052-02 is offered in tape and reel packaging. The CYBT-343052-02 ships in a reel size of 500.

For additional information and a complete list of Cypress Semiconductor Wireless products, contact your local Cypress sales representative. To locate the nearest Cypress office, visit our website.

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Acronyms

Table 28. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
ARM®	advanced RISC machine, a CPU architecture
BLE	Bluetooth Low Energy
Bluetooth SIG	Bluetooth Special Interest Group
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CE	European Conformity
CSA	Canadian Standards Association
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
ESD	electrostatic discharge
FCC	Federal Communications Commission
FET	field-effect transistor
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HCI	host controller interface
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC

Acronym	Description
IDE	integrated development environment
I^{2}C, or IIC	Inter-Integrated Circuit, a communications protocol
IC	Industry Canada
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
KC	Korea Certification
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LNA	low noise amplifier
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MIC	Ministry of Internal Affairs and Communications (Japan)
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
Opamp	operational amplifier
PA	power amplifier

Table 28. Acronyms Used in this Document (continued)

Acronym	Description		Acronym	Description
PAL	programmable array logic, see also PLD		SOF	start of frame
PC	program counter		S/H	sample and hold
PCB	printed circuit board		SINAD	signal to noise and distortion ratio
PGA	programmable gain amplifier		SIO	special input/output, GPIO with advanced features. See GPIO.
PHUB	peripheral hub		SMT	surface-mount technology; a method for producing electronic circuitry in which the components are placed directly onto the surface of PCBs
PHY	physical layer		SPI	Serial Peripheral Interface, a communications protocol
PICU	port interrupt control unit		SR	slew rate
PLA	programmable logic array		SRAM	static random access memory
PLD	programmable logic device, see also PAL		SRES	software reset
PLL	phase-locked loop		STN	super twisted nematic
PMDD	package material declaration data sheet		SWD	serial wire debug, a test protocol
POR	power-on reset		SWV	single-wire viewer
PRES	precise power-on reset		TD	transaction descriptor, see also DMA
PRS	pseudo random sequence		THD	total harmonic distortion
PS	port read data register		TIA	transimpedance amplifier
PSoC®	Programmable System-on-Chip™		TN	twisted nematic
PSRR	power supply rejection ratio		TRM	technical reference manual
PWM	pulse-width modulator		TTL	transistor-transistor logic
QDID	qualification design ID		TUV	Germany: Technischer Überwachungs-Verein (Technical Inspection Association)
RAM	random-access memory		TX	transmit
RISC	reduced-instruction-set computing		UART	Universal Asynchronous Transmitter Receiver, a communications protocol
RMS	root-mean-square		UDB	universal digital block
RTC	real-time clock		USB	Universal Serial Bus
RTL	register transfer language		USBIO	USB input/output, PSoC pins used to connect to a USB port
RTR	remote transmission request		VDAC	voltage DAC, see also DAC, IDAC
RX	receive		WDT	watchdog timer
SAR	successive approximation register		WOL	write once latch, see also NVL
SC/CT	switched capacitor/continuous time		WRES	watchdog timer reset
SCL	I^2C serial clock		XRES	external reset I/O pin
SDA	I^2C serial data		XTAL	crystal
SOC	start of conversion			

Document Conventions

Units of Measure

Table 29. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
dBm	decibel-milliwatts
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Document History Page

Document Title: CYBT-343052-02, EZ-BT WICED Module Document Number: 002-28053			
Revision	ECN	Submission Date	Description of Change
**		08/23/2019	Preliminary datasheet for CYBT-343052-02 module.

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