PRELIMINARY

CYBLE-222005-00

EZ-BLE™ PRoC™ Module

General Description

The Cypress CYBLE-222005-00 is a fully certified and qualified module supporting Bluetooth® Low Energy (BLE) wireless communication. The CYBLE-222005-00 is a turnkey solution and includes onboard crystal oscillators, chip antenna, passive components, and Cypress PRoC™ BLE.

The CYBLE-222005-00 supports a number of peripheral functions (ADC, timers, counters, PWM) and serial communication protocols (I^2C, UART, SPI) through its programmable architecture. The CYBLE-222005-00 includes a royalty-free BLE stack compatible with Bluetooth 4.1 and provides up to 16 GPIOs in a small 10 × 10 × 1.80 mm package.

The CYBLE-222005-00 is a complete solution and an ideal fit for applications requiring BLE wireless connectivity.

Module Description

- Module size: 10.0 mm ×10.0 mm × 1.80 mm (with shield)
- Drop-in compatible with CYBLE-022001-00 and includes additional V_{REF} input
- Bluetooth 4.1 single-mode module
- Industrial temperature range: –40 °C to +85 °C
- 32-bit processor (0.9 DMIPS/MHz) with single-cycle 32-bit multiply, operating at up to 48 MHz
- 256-KB flash memory
- 32-KB SRAM memory
- Watchdog timer with dedicated internal low-speed oscillator (ILO)
- Two-pin SWD for programming
- Up to 16 GPIOs configurable as open drain high/low, pull-up/pull-down, HI-Z analog, HI-Z digial, or strong output
- Certified to FCC, CE MIC, KC, and IC regulations
- Bluetooth SIG 4.1 qualified

Power Consumption

- TX output power: –18 dbm to +3 dbm
- Received signal strength indicator (RSSI) with 1-dB resolution
- TX current consumption of 15.6 mA (radio only, 0 dbm)
- RX current consumption of 16.4 mA (radio only)
- Low power mode support
  - Deep Sleep: 1.3 µA with watch crystal oscillator (WCO) on
  - Hibernate: 150 nA with SRAM retention
  - Stop: 60 nA with XRES wakeup

Functional Capabilities

- Up to 15 capacitive sensors for buttons or sliders with best-in-class signal-to-noise ration (SNR) and liquid tolerance
- 12-bit, 1-Msps SAR ADC with internal reference, sample-and-hold (S/H), and channel sequencer
- Two serial communication blocks (SCBs) supporting I^2C (master/slave), SPI (master/slave), or UART
- Four dedicated 16-bit timer, counter, or PWM blocks (TCPWMs)
- Programmable low voltage detect (LVD) from 1.8 V to 4.5 V
- I^2S master interface
- Bluetooth Low Energy protocol stack supporting generic access profile (GAP) Central, Peripheral, Observer, or Broadcaster roles
- Switches between Central and Peripheral roles on-the-go
- Standard Bluetooth Low Energy profiles and services for interoperability
- Custom profile and service for specific use cases

Benefits

The CYBLE-222005-00 module is provided as a turnkey solution, including all necessary hardware required to use BLE communication standards.

- Proven, qualified, and certified hardware design ready to use
- Small footprint (10 × 10 mm × 1.80 mm), perfect for space constrained applications
- Reprogrammable architecture
- Fully certified module eliminates the time needed for design, development and certification processes
- Bluetooth SIG qualified with QDID and Declaration ID
- Flexible communication protocol support
- PSoC Creator™ provides an easy-to-use integrated design environment (IDE) to configure, develop, program, and test a BLE application

Contents

Overview

Module Description

The CYBLE-222005-00 module is a complete module designed to be soldered to the applications main board.

Module Dimensions and Drawing

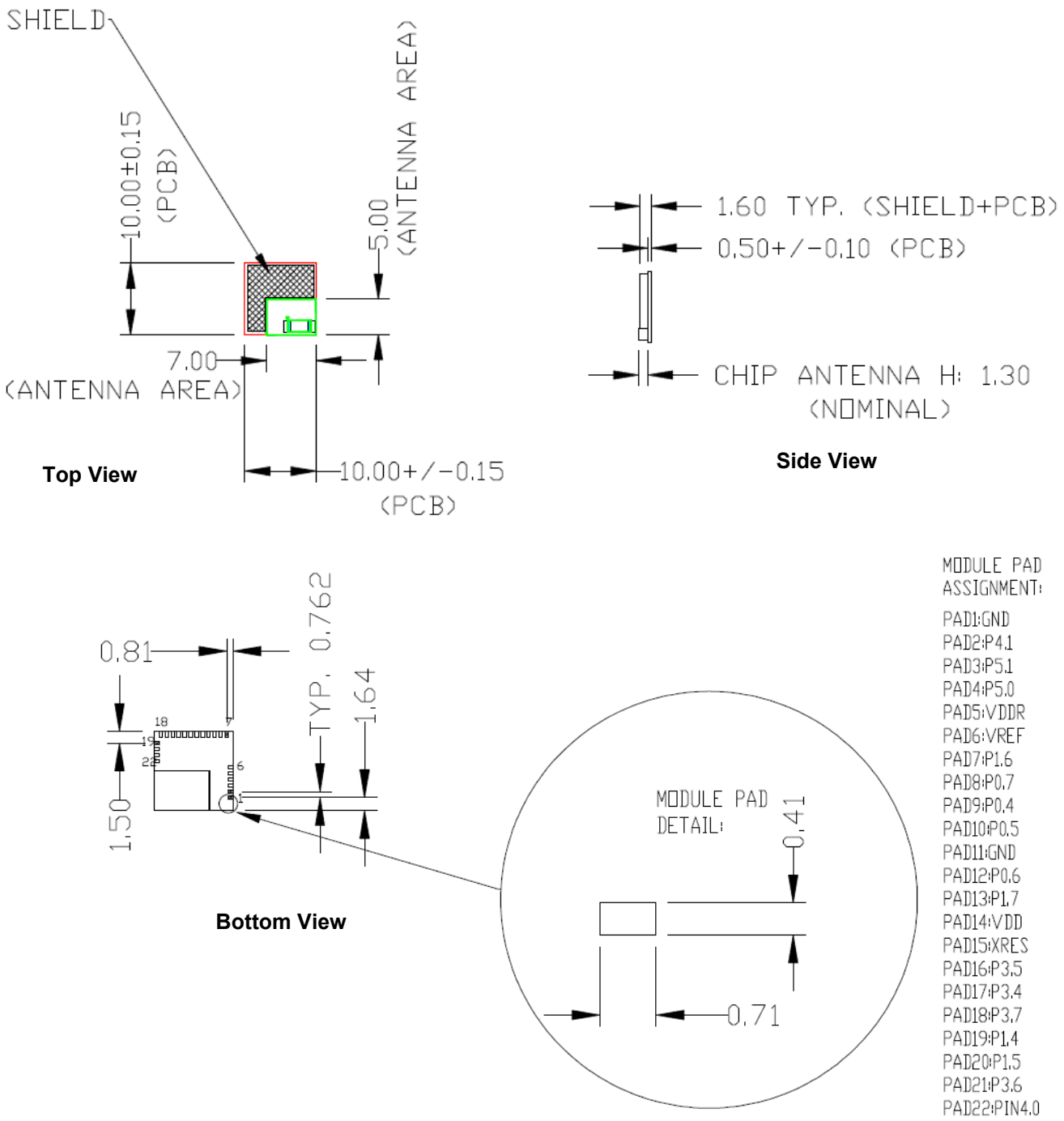
Cypress reserves the right to select components (including the appropriate BLE device) from various vendors to achieve the BLE module functionality. Such selections will still guarantee that all height restrictions of the component area are maintained. Designs should be held within the physical dimensions shown in the mechanical drawings in Figure 1. All dimensions are in millimeters (mm).

Table 1. Module Design Dimensions

Dimension Item		Specification
Module dimensions	Length (X)	10.00 ± 0.15 mm
	Width (Y)	10.00 ± 0.15 mm
Antenna location dimensions	Length (X)	7.00 ± 0.15 mm
	Width (Y)	5.00 ± 0.15 mm
PCB thickness	Height (H)	0.50 ± 0.10 mm
Shield height	Height (H)	1.10 ± 0.10 mm
Maximum component height	Height (H)	1.30 mm typical (chip antenna)
Total module thickness (bottom of module to highest component)	Height (H)	1.80 mm typical

See Figure 1 on page 4 for the mechanical reference drawing for CYBLE-222005-00.

Figure 1. Module Mechanical Drawing



Note
1. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see Figure 3 and Figure 4 on page 6.

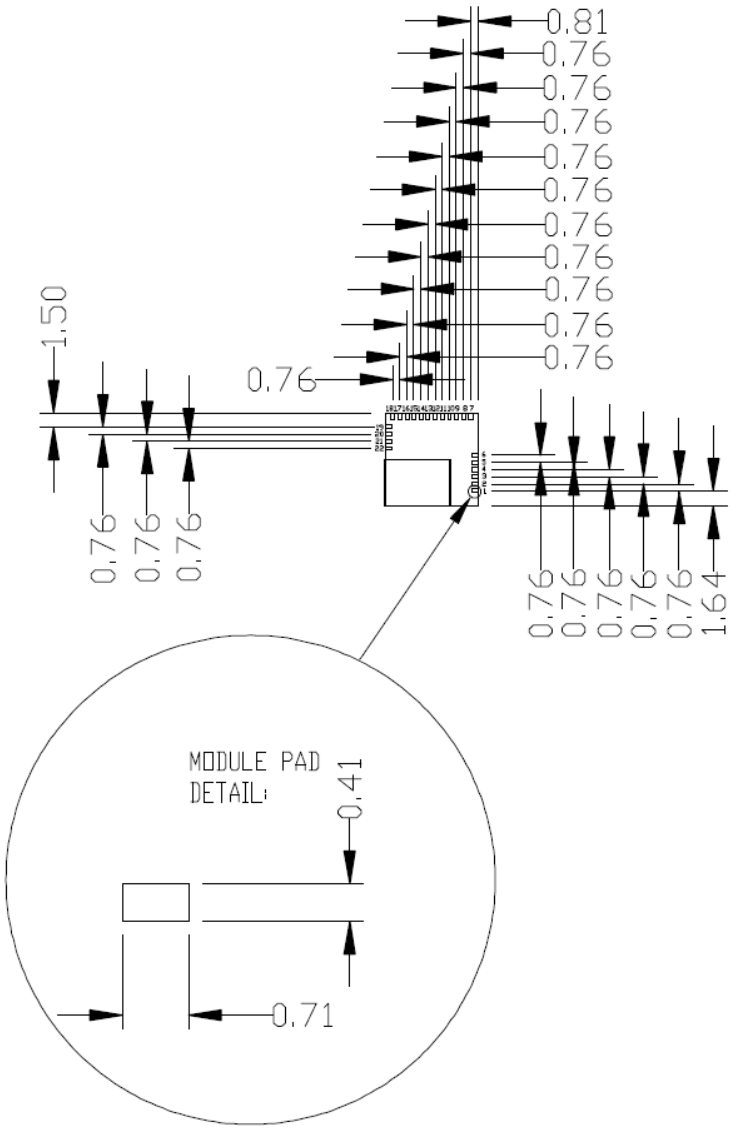
Pad Connection Interface

As shown in the bottom view of Figure 1 on page 4, the CYBLE-222005-00 connects to the host board via solder pads on the back of the module. Table 2 and Figure 2 detail the solder pad length, width, and pitch dimensions of the CYBLE-222005-00 module.

Table 2. Solder Pad Connection Description

Name	Connections	Connection Type	Pad Length Dimension	Pad Width Dimension	Pad Pitch
SP	22	Solder Pads	0.71 mm	0.41 mm	0.76 mm

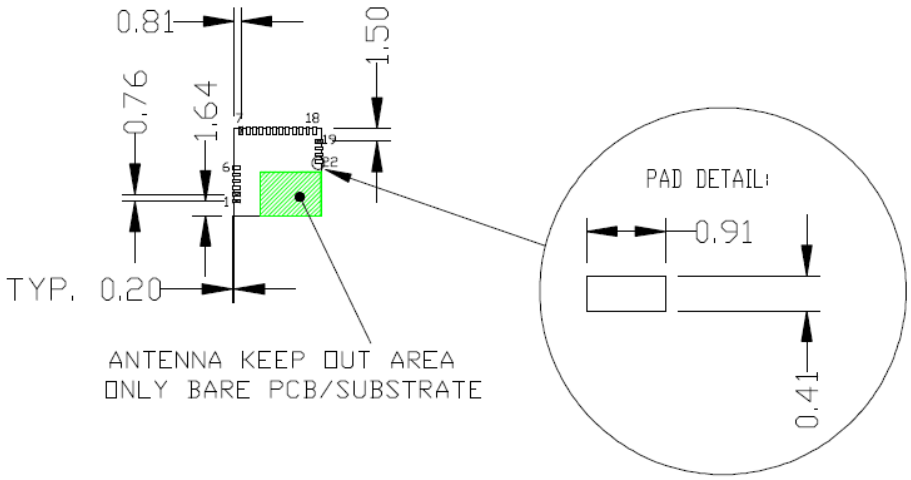
Figure 2. Solder Pad Dimensions



Recommended Host PCB Layout

Figure 3 details the recommended PCB layout pattern for the host PCB. Dimensions are in mm.

Figure 3. Recommended PCB Layout Pattern for CYBLE-222005-00

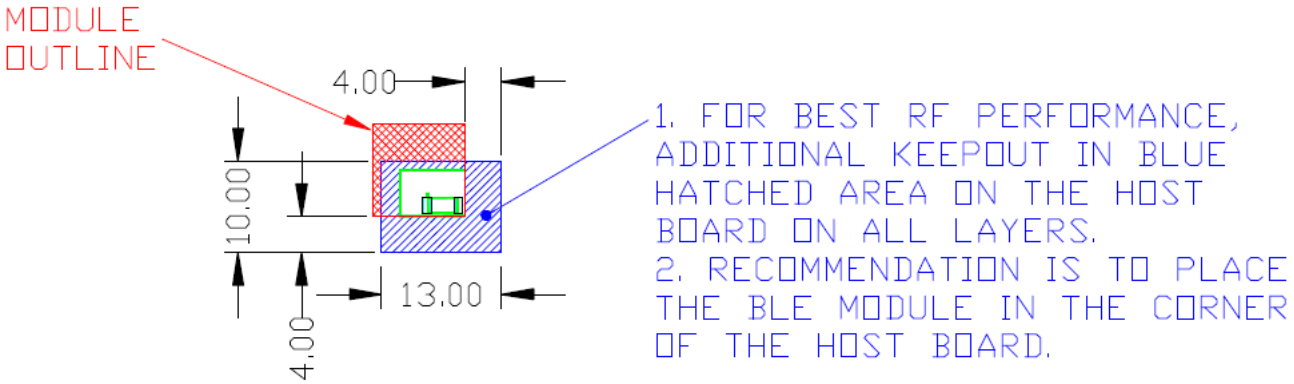


Top View (On Host PCB)

To maximize RF performance, the host layout should follow these recommendations:

1. The ideal placement of the Cypress BLE module is in a corner of the host board with the chip antenna located at the far corner. This placement minimizes the additional recommended keep out area stated in item 2.
2. It is recommended that the area around the Cypress BLE module chip antenna should contain an additional keep out area, where no grounding or signal trace are contained. The keep out area applies to all layers of the host board. The recommended dimensions of the host PCB keep out area are shown in Figure 4 (dimensions are in mm).

Figure 4. Recommended Host PCB Keep Out Area Around the CYBLE-222005-00 Chip Antenna



Host PCB Keep Out Area Around Chip Antenna

Table 3 details the solder pad pitch (center-to-center) for each of the neighboring connections.

Table 3. Module Solder Pad Connection Dimensions

Pad X	Pad Y	Pad Pitch (Pad X - Pad Y)	Comments
Bottom Right Corner	1	1.64 mm	Distance from bottom right corner to Pad 1 center
1	2	0.76 mm	Distance from Pad 1 center to Pad 2 center
2	3	0.76 mm	Distance from Pad 2 center to Pad 3 center
3	4	0.76 mm	Distance from Pad 3 center to Pad 4 center
4	5	0.76 mm	Distance from Pad 4 center to Pad 5 center
5	6	0.76 mm	Distance from Pad 5 center to Pad 6 center
Top Right Corner	7	0.81 mm	Distance from top right corner to Pad 7 center
7	8	0.76 mm	Distance from Pad 7 center to Pad 8 center
8	9	0.76 mm	Distance from Pad 8 center to Pad 9 center
9	10	0.76 mm	Distance from Pad 9 center to Pad 10 center
10	11	0.76 mm	Distance from Pad 10 center to Pad 11 center
11	12	0.76 mm	Distance from Pad 11 center to Pad 12 center
12	13	0.76 mm	Distance from Pad 12 center to Pad 13 center
13	14	0.76 mm	Distance from Pad 13 center to Pad 14 center
14	15	0.76 mm	Distance from Pad 14 center to Pad 15 center
15	16	0.76 mm	Distance from Pad 15 center to Pad 16 center
16	17	0.76 mm	Distance from Pad 16 center to Pad 17 center
17	18	0.76 mm	Distance from Pad 17 center to Pad 18 center
Top Left Corner	19	1.50 mm	Distance from top left corner to Pad 19 center
19	20	0.76 mm	Distance from Pad 19 center to Pad 20 center
20	21	0.76 mm	Distance from Pad 20 center to Pad 21 center
21	22	0.76 mm	Distance from Pad 21 center to Pad 22 center

Table 4 details the solder pad connection definitions and available functions for each connection pad. Table 4 lists the solder pads on CYBLE-222005-00, the BLE device port-pin, and denotes whether the function shown is available for each solder pad. Each connection is configurable for a single option shown with a ✓.

Table 4. Solder Pad Connection Definitions

Solder Pad Number	Device Port Pin	UART	SPI	I²C	TCPWM[2]	CapSense	WCO Out	ECO_OUT	LCD	SWD	GPIO
1	GND[3]	Ground Connection									
2	P4.1[4]	✓(CTS)	✓(MISO)		✓	✓(Sensor / C_{TANK})			✓		✓
3	P5.1	✓(TX)	✓(SCLK)	✓(SCL)	✓	✓(Sensor)		✓	✓		✓
4	P5.0	✓(RX)	✓(SS)	✓(SDA)	✓	✓(Sensor)			✓		✓
5	V_{DDR}	Radio Power Supply (1.9V to 5.5V)									
6	V_{REF}[5]	Voltage Reference Input (Optional)									
7	P1.6	✓(RTS)	✓(SS)		✓	✓(Sensor)			✓		✓
8	P0.7	✓(CTS)	✓(SCLK)		✓	✓(Sensor)			✓	✓(SWDCLK)	✓
9	P0.4	✓(RX)	✓(MOSI)	✓(SDA)	✓	✓(Sensor)		✓	✓		✓
10	P0.5	✓(TX)	✓(MISO)	✓(SCL)	✓	✓(Sensor)			✓		✓
11	GND	Ground Connection									
12	P0.6	✓(RTS)	✓(SS)		✓	✓(Sensor)			✓	✓(SWDIO)	✓
13	P1.7	✓(CTS)	✓(SCLK)		✓	✓(Sensor)			✓		✓
14	V_{DD}	Digital Power Supply Input (1.71 to 5.5V)									
15	XRES	External Reset Hardware Connection Input									
16	P3.5	✓(TX)		✓(SCL)	✓	✓(Sensor)			✓		✓
17	P3.4	✓(RX)		✓(SDA)	✓	✓(Sensor)			✓		✓
18	P3.7	✓(CTS)	✓(MISO)			✓(Sensor)	✓		✓		✓
19	P1.4	✓(RX)	✓(MOSI)	✓(SDA)	✓	✓(Sensor)			✓		✓
20	P1.5	✓(TX)	✓(MISO)	✓(SCL)	✓	✓(Sensor)			✓		✓
21	P3.6	✓(RTS)			✓	✓(Sensor)			✓		✓
22	P4.0[6]	✓(RTS)	✓(MOSI)		✓	✓(C_{MOD})			✓		✓

Notes
2. TCPWM stands for timer, counter, and PWM. If supported, the pad can be configured to any of these peripheral functions.
3. The main board needs to connect both GND connections (Pad 1 and Pad 10) on the module to the common ground of the system.
4. When using the capacitive sensing functionality, Pad 2 (P4.1) can be connected to a C_{TANK} capacitor (located off of Cypress BLE Module). C_{Tank} should be used if implementing a shield layer on the capacitive sensor. If used, this capacitor should be placed as close to the module as possible.
5. Analog block functionality is augmented for the user with the external V_{REF} input. The internal bandgap may be bypassed with a 1-µF to 10-µF capacitor.
6. When using the capacitive sensing functionality, Pad 22 (P4.0) must be connected to a C_{MOD} capacitor (located off of Cypress BLE Module). The value of this capacitor is 2.2 nF and should be placed as close to the module as possible.
7. If the I²S feature is used in the design, the I²S pins shall be dynamically routed to the appropriate available GPIO by PSoC Creator

Power Supply Connections and Recommended External Components

Power Connections

The CYBLE-222005-00 contains two power supply connections, VDD and VDDR. The VDD connection supplies power for both digital and analog device operation. The VDDR connection supplies power for the device radio.

VDD accepts a supply range of 1.8 V to 5.5 V. VDDR accepts a supply range of 1.9 V to 5.5 V. These specifications can be found in Table 9. The maximum power supply ripple for both power connections on the module is 100 mV, as shown in Table 7.

The power supply ramp rate of VDD must be equal to or greater than that of VDDR.

Connection Options

Two connection options are available for any application:

1. Single supply: Connect VDD and VDDR to the same supply.
2. Independent supply: Power VDD and VDDR separately.

External Component Recommendation

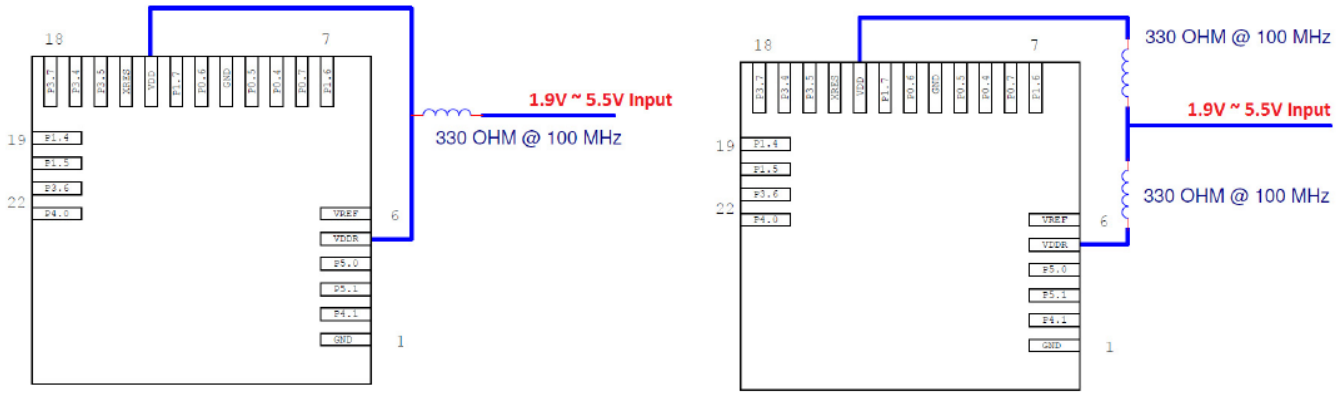
In either connection scenario, it is recommended to place an external ferrite bead between the supply and the module connection. The ferrite bead should be positioned as close as possible to the module pin connection.

Figure 5 details the recommended host schematic options for a single supply scenario. The use of one or two ferrite beads will depend on the specific application and configuration of the CYBLE-222005-00.

Figure 6 details the recommended host schematic for an independent supply scenario.

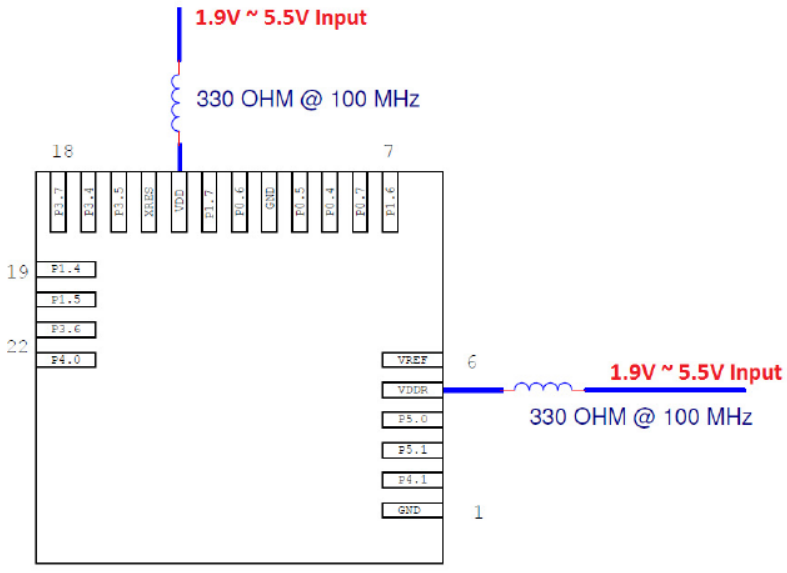
The recommended ferrite bead value is 330 Ω, 100 MHz. (Murata BLM21PG331SN1D).

Figure 5. Recommended Host Schematic Options for a Single Supply Option



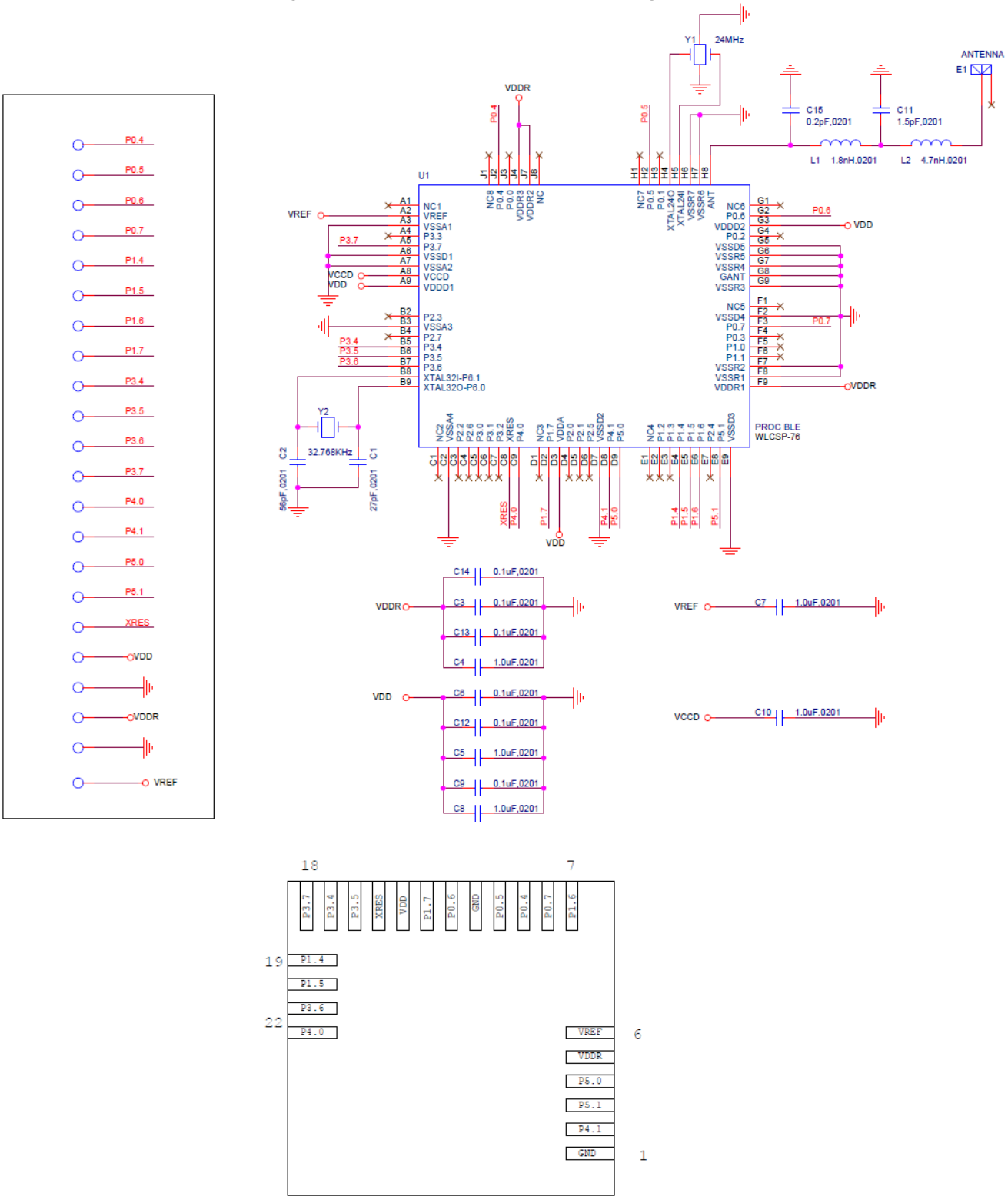
Single Ferrite Bead Option **Two Ferrite Bead Option**

Figure 6. Recommended Host Schematic for an Independent Supply Option



The CYBLE-222005-00 schematic is shown in Figure 7.

Figure 7. CYBLE-222005-00 Schematic Diagram



Critical Components List

Table 5 details the critical components used in the CYBLE-222005-00 module.

Table 5. Critical Component List

Component	Reference Designator	Description
Silicon	U1	68-pin WLCSP Programmable Radio-on-Chip (PRoC) with BLE
Crystal	Y1	24.000 MHz, 10PF
Crystal	Y2	32.768 kHz, 12.5PF
Antenna	E1	2.4 – 2.5 GHz chip antenna

Antenna Design

Table 6 details the chip antenna used in the CYBLE-222005-00 module. The specifications listed are according to the vendor's datasheet. The Cypress module performance improves many of these characteristics. For more information, see Table 8.

Table 6. Chip Antenna Specifications

Item	Description
Chip Antenna Manufacturer	Johanson Technology Inc.
Chip Antenna Part Number	2450AT18B100
Frequency Range	2400 – 2500 MHz
Peak Gain	0.5 dBi typical
Average Gain	-0.5 dBi typical
Return Loss	9.5 dB minimum

Electrical Specification

Table 7 details the absolute maximum electrical characteristics for the Cypress BLE module.

Table 7. CYBLE-222005-00 Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{DDD_ABS}	Analog, digital, or radio supply relative to V_{SS} ($V_{SSD} = V_{SSA}$)	–0.5	–	6	V	Absolute maximum
V_{CCD_ABS}	Direct digital core voltage input relative to V_{SSD}	–0.5	–	1.95	V	Absolute maximum
V_{DDD_RIPPLE}	Maximum power supply ripple for V_{DD} and V_{DDR} input voltage	–	–	100	mV	3.0V supply Ripple frequency of 100 kHz to 750 kHz
V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD} +0.5	V	Absolute maximum
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	Absolute maximum
$I_{GPIO\_injection}$	GPIO injection current: Maximum for $V_{IH} > V_{DD}$ and minimum for $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	Absolute maximum current injected per pin
LU	Pin current for latch up	–200		200	mA	–

Table 8 details the RF characteristics for the Cypress BLE module.

Table 8. CYBLE-222005-00 RF Performance Characteristics

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
RF_O	RF output power on ANT	–18	0	3	dBm	Configurable via register settings
RX_S	RF receive sensitivity on ANT	–	–91	–	dBm	Guaranteed by design simulation; High Gain Mode
F_R	Module frequency range	2400	–	2480	MHz	–
G_P	Peak gain	–	0.5	–	dBi	–
G_{Avg}	Average gain	–	–0.5	–	dBi	–
RL	Return loss	–	–10.5	–	dB	–

Table 9 through Table 47 list the module level electrical characteristics for the CYBLE-222005-00. All specifications are valid for –40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 9. CYBLE-222005-00 DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{DD1}	Power supply input voltage	1.8	–	5.5	V	With regulator enabled
V_{DD2}	Power supply input voltage unregulated	1.71	1.8	1.89	V	Internally unregulated supply
V_{DDR1}	Radio supply voltage (radio on)	1.9	–	5.5	V	–
V_{DDR2}	Radio supply voltage (radio off)	1.71	–	5.5	V	–
Active Mode, V_{DD} = 1.71 V to 5.5 V						
I_{DD3}	Execute from flash; CPU at 3 MHz	–	1.7	–	mA	T = 25 °C, V_{DD} = 3.3 V
I_{DD4}	Execute from flash; CPU at 3 MHz	–	–	–	mA	T = –40 °C to 85 °C
I_{DD5}	Execute from flash; CPU at 6 MHz	–	2.5	–	mA	T = 25 °C, V_{DD} = 3.3 V
I_{DD6}	Execute from flash; CPU at 6 MHz	–	–	–	mA	T = –40 °C to 85 °C
I_{DD7}	Execute from flash; CPU at 12 MHz	–	4	–	mA	T = 25 °C, V_{DD} = 3.3 V

Table 9. CYBLE-222005-00 DC Specifications (continued)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{DD8}	Execute from flash; CPU at 12 MHz	–	–	–	mA	T = –40 °C to 85 °C
I_{DD9}	Execute from flash; CPU at 24 MHz	–	7.1	–	mA	T = 25 °C, V_{DD} = 3.3 V
I_{DD10}	Execute from flash; CPU at 24 MHz	–	–	–	mA	T = –40 °C to 85 °C
I_{DD11}	Execute from flash; CPU at 48 MHz	–	13.4	–	mA	T = 25 °C, V_{DD} = 3.3 V
I_{DD12}	Execute from flash; CPU at 48 MHz	–	–	–	mA	T = –40 °C to 85 °C
Sleep Mode, V_{DD} = 1.8 to 5.5 V						
I_{DD13}	IMO on	–	–	–	mA	T = 25 °C, V_{DD} = 3.3 V, SYSCLK = 3 MHz
Sleep Mode, V_{DD} and V_{DDR} = 1.9 to 5.5 V						
I_{DD14}	ECO on	–	–	–	mA	T = 25 °C, V_{DD} = 3.3 V, SYSCLK = 3 MHz
Deep-Sleep Mode, V_{DD} = 1.8 to 3.6 V						
I_{DD15}	WDT with WCO on	–	1.5	–	µA	T = 25 °C, V_{DD} = 3.3 V
I_{DD16}	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
I_{DD17}	WDT with WCO on	–	–	–	µA	T = 25 °C, V_{DD} = 5 V
I_{DD18}	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
Deep-Sleep Mode, V_{DD} = 1.71 to 1.89 V (Regulator Bypassed)						
I_{DD19}	WDT with WCO on	–	–	–	µA	T = 25 °C
I_{DD20}	WDT with WCO on	–	–	–	µA	T = –40 °C to 85 °C
Hibernate Mode, V_{DD} = 1.8 to 3.6 V						
I_{DD27}	GPIO and reset active	–	150	–	nA	T = 25 °C, V_{DD} = 3.3 V
I_{DD28}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Hibernate Mode, V_{DD} = 3.6 to 5.5 V						
I_{DD29}	GPIO and reset active	–	–	–	nA	T = 25 °C, V_{DD} = 5 V
I_{DD30}	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
Stop Mode, V_{DD} = 1.8 to 3.6 V						
I_{DD33}	Stop-mode current (V_{DD})	–	20	–	nA	T = 25 °C, V_{DD} = 3.3 V
I_{DD34}	Stop-mode current (V_{DDR})	–	40	–-	nA	T = 25 °C, V_{DDR} = 3.3 V
I_{DD35}	Stop-mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C
I_{DD36}	Stop-mode current (V_{DDR})	–	–	–	nA	T = –40 °C to 85 °C, V_{DDR} = 1.9 V to 3.6 V
Stop Mode, V_{DD} = 3.6 to 5.5 V						
I_{DD37}	Stop-mode current (V_{DD})	–	–	–	nA	T = 25 °C, V_{DD} = 5 V
I_{DD38}	Stop-mode current (V_{DDR})	–	–	–	nA	T = 25 °C, V_{DDR} = 5 V
I_{DD39}	Stop-mode current (V_{DD})	–	–	–	nA	T = –40 °C to 85 °C
I_{DD40}	Stop-mode current (V_{DDR})	–	–	–	nA	T = –40 °C to 85 °C

Table 10. AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{CPU}	CPU frequency	DC	–	48	MHz	1.71 V ≤ V_{DD} ≤ 5.5 V
T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	Guaranteed by characterization
$T_{DEEPSLEEP}$	Wakeup from Deep-Sleep mode	–	–	25	µs	24-MHz IMO. Guaranteed by characterization
$T_{HIBERNATE}$	Wakeup from Hibernate mode	–	–	2	ms	Guaranteed by characterization
T_{STOP}	Wakeup from Stop mode	–	–	2	ms	XRES wakeup

GPIO

Table 11. GPIO DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}[8]	Input voltage HIGH threshold	0.7 × V_{DD}	–	–	V	CMOS input
	LVTTL input, V_{DD} < 2.7 V	0.7 × V_{DD}	–	–	V	–
	LVTTL input, V_{DD} >= 2.7 V	2.0	–	–	V	–
V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DD}	V	CMOS input
	LVTTL input, V_{DD} < 2.7 V	–	–	0.3× V_{DD}	V	–
	LVTTL input, V_{DD} >= 2.7 V	–	–	0.8	V	–
V_{OH}	Output voltage HIGH level	V_{DD} –0.6	–	–	V	I_{OH} = 4 mA at 3.3-V V_{DD}
	Output voltage HIGH level	V_{DD} –0.5	–	–	V	I_{OH} = 1 mA at 1.8-V V_{DD}
V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 8 mA at 3.3-V V_{DD}
	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8-V V_{DD}
	Output voltage LOW level	–	–	0.4	V	I_{OL} = 3 mA at 3.3-V V_{DD}
R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DD} = 3.3 V
I_{IL_CTBM}	Input leakage on CTBm input pins	–	–	4	nA	–
C_{IN}	Input capacitance	–	–	7	pF	–
V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	V_{DD} > 2.7 V
$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DD}	–	–	1	–
I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Note
8. V_{IH} must not exceed V_{DD} + 0.2 V.

Table 12. GPIO AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_{RISEF}	Rise time in Fast-Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{LOAD} = 25 pF
T_{FALLF}	Fall time in Fast-Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{LOAD} = 25 pF
T_{RISES}	Rise time in Slow-Strong mode	10	–	60	ns	3.3-V V_{DDD}, C_{LOAD} = 25 pF
T_{FALLS}	Fall time in Slow-Strong mode	10	–	60	ns	3.3-V V_{DDD}, C_{LOAD} = 25 pF
$F_{GPIOUT1}$	GPIO Fout; 3.3 V ≤ V_{DD} ≤ 5.5 V Fast-Strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOUT2}$	GPIO Fout; 1.7 V≤ V_{DD} ≤ 3.3 V Fast-Strong mode	–	–	16.7	MHz	90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOUT3}$	GPIO Fout; 3.3 V ≤ V_{DD} ≤ 5.5 V Slow-Strong mode	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOUT4}$	GPIO Fout; 1.7 V ≤ V_{DD} ≤ 3.3 V Slow-Strong mode	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
F_{GPIOIN}	GPIO input operating frequency 1.71 V ≤ V_{DD} ≤ 5.5 V	–	–	48	MHz	90/10% V_{IO}

Table 13. OVT GPIO DC Specifications (P5_0 and P5_1 Only)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{IL}	Input leakage (absolute value). V_{IH} > V_{DD}	–	–	10	µA	25°C, V_{DD} = 0 V, V_{IH} = 3.0 V
V_{OL}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 20 mA, V_{DD} > 2.9 V

Table 14. OVT GPIO AC Specifications (P5_0 and P5_1 Only)

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_{RISE_OVFS}	Output rise time in Fast-Strong mode	1.5	–	12	ns	25-pF load, 10%–90%, V_{DD}=3.3 V
T_{FALL_OVFS}	Output fall time in Fast-Strong mode	1.5	–	12	ns	25-pF load, 10%–90%, V_{DD}=3.3 V
T_{RISESS}	Output rise time in Slow-Strong mode	10	–	60	ns	25 pF load, 10%-90%, V_{DD} = 3.3 V
T_{FALLSS}	Output fall time in Slow-Strong mode	10	–	60	ns	25 pF load, 10%-90%, V_{DD} = 3.3 V
$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V ≤ V_{DD} ≤ 5.5 V Fast-Strong mode	–	–	24	MHz	90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOUT2}$	GPIO F_{OUT}; 1.71 V ≤ V_{DD} ≤ 3.3 V Fast-Strong mode	–	–	16	MHz	90/10%, 25 pF load, 60/40 duty cycle

XRES

Table 15. XRES DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS input
V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	CMOS input
R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
C_{IN}	Input capacitance	–	3	–	pF	–
$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	–
I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–

Table 16. XRES AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	–

SAR ADC

Table 17. SAR ADC DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
A_RES	Resolution	–	–	12	bits	
A_CHNIS_S	Number of channels - single-ended	–	–	8		8 full-speed
A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
A-MONO	Monotonicity	–	–	–		Yes
A_GAINERR	Gain error	–	–	±0.1	%	With external reference
A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V_{REF}
A_ISAR	Current consumption	–	–	1	mA	
A_VINS	Input voltage range - single-ended	V_{SS}	–	V_{DDA}	V	
A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	
A_INRES	Input resistance	–	–	2.2	kΩ	
A_INCAP	Input capacitance	–	–	10	pF	
VREFSAR	Trimmed internal reference to SAR	–1	–	1	%	Percentage of Vbg (1.024 V)

Table 18. SAR ADC AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
A_PSRR	Power-supply rejection ratio	70	–	–	dB	Measured at 1-V reference
A_CMRR	Common-mode rejection ratio	66	–	–	dB	
A_SAMP	Sample rate	–	–	1	Msps	806 Ksps for More Part Numbers devices
Fsarintref	SAR operating speed without external ref. bypass	–	–	100	Ksps	12-bit resolution
A_SNR	Signal-to-noise ratio (SNR)	65	–	–	dB	F_{IN} = 10 kHz
A_BW	Input bandwidth without aliasing	–	–	A_SAMP/2	kHz	
A_INL	Integral nonlinearity. V_{DD} = 1.71 V to 5.5 V, 1 Msps	–1.7	–	2	LSB	V_{REF} = 1 V to V_{DD}
A_INL	Integral nonlinearity. V_{DDD} = 1.71 V to 3.6 V, 1 Msps	–1.5	–	1.7	LSB	V_{REF} = 1.71 V to V_{DD}
A_INL	Integral nonlinearity. V_{DD} = 1.71 V to 5.5 V, 500 Ksps	–1.5	–	1.7	LSB	V_{REF} = 1 V to V_{DD}
A_dnl	Differential nonlinearity. V_{DD} = 1.71 V to 5.5 V, 1 Msps	–1	–	2.2	LSB	V_{REF} = 1 V to V_{DD}
A_DNL	Differential nonlinearity. V_{DD} = 1.71 V to 3.6 V, 1 Msps	–1	–	2	LSB	V_{REF} = 1.71 V to V_{DD}
A_DNL	Differential nonlinearity. V_{DD} = 1.71 V to 5.5 V, 500 Ksps	–1	–	2.2	LSB	V_{REF} = 1 V to V_{DD}

Table 18. SAR ADC AC Specifications (continued)

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
A_THD	Total harmonic distortion	–	–	–65	dB	F_{IN} = 10 kHz

CSD

CSD Block Specifications

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
V_{CSD}	Voltage range of operation	1.71	–	5.5	V	
IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	
IDAC1	INL for 8-bit resolution	–3	–	3	LSB	
IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	
IDAC2	INL for 7-bit resolution	–3	–	3	LSB	
SNR	Ratio of counts of finger to noise	5	–	–	Ratio	Capacitance range of 9 pF to 35 pF, 0.1-pF sensitivity. Radio is not operating during the scan
I_{DAC1_CRT1}	Output current of IDAC1 (8 bits) in High range	–	612	–	µA	
I_{DAC1_CRT2}	Output current of IDAC1 (8 bits) in Low range	–	306	–	µA	
I_{DAC2_CRT1}	Output current of IDAC2 (7 bits) in High range	–	305	–	µA	
I_{DAC2_CRT2}	Output current of IDAC2 (7 bits) in Low range	–	153	–	µA	

Digital Peripherals

Timer

Table 19. Timer DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{TIM1}	Block current consumption at 3 MHz	–	–	42	µA	16-bit timer
I_{TIM2}	Block current consumption at 12 MHz	–	–	130	µA	16-bit timer
I_{TIM3}	Block current consumption at 48 MHz	–	–	535	µA	16-bit timer

Table 20. Timer AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{TIMFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	
$T_{CAPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{CAPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
T_{TIMRES}	Timer resolution	T_{CLK}	–	–	ns	
$T_{TENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{TENWIDEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
$T_{TIMRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{TIMRESEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	

Counter

Table 21. Counter DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{CTR1}	Block current consumption at 3 MHz	–	–	42	µA	16-bit counter
I_{CTR2}	Block current consumption at 12 MHz	–	–	130	µA	16-bit counter
I_{CTR3}	Block current consumption at 48 MHz	–	–	535	µA	16-bit counter

Table 22. Counter AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{CTRFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	
$T_{CTRPWINT}$	Capture pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{CTRPWEXT}$	Capture pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
T_{CTRES}	Counter Resolution	T_{CLK}	–	–	ns	
$T_{CENWIDINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{CENWIDEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
$T_{CTRRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{CTRRESWEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	

Pulse Width Modulation (PWM)

Table 23. PWM DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{PWM1}	Block current consumption at 3 MHz	–	–	42	µA	16-bit PWM
I_{PWM2}	Block current consumption at 12 MHz	–	–	130	µA	16-bit PWM
I_{PWM3}	Block current consumption at 48 MHz	–	–	535	µA	16-bit PWM

Table 24. PWM AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{PWMFREQ}$	Operating frequency	F_{CLK}	–	48	MHz	
$T_{PWMPWINT}$	Pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
T_{PWMEXT}	Pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
$T_{PWMKILLINT}$	Kill pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{PWMKILLEXT}$	Kill pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
$T_{PWMEINT}$	Enable pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{PWMENEXT}$	Enable pulse width (external)	$2 \times T_{CLK}$	–	–	ns	
$T_{PWMRESWINT}$	Reset pulse width (internal)	$2 \times T_{CLK}$	–	–	ns	
$T_{PWMRESWEXT}$	Reset pulse width (external)	$2 \times T_{CLK}$	–	–	ns	

LCD Direct Drive

Table 25. LCD Direct Drive DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID228	I_{LCDLOW}	Operating current in low-power mode	–	17.5	–	µA	16 × 4 small segment display at 50 Hz
SID229	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	
SID230	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	
SID231	I_{LCDOP1}	LCD system operating current V_{BIAS} = 5 V	–	2	–	mA	32 × 4 segments. 50 Hz at 25 °C
SID232	I_{LCDOP2}	LCD system operating current V_{BIAS} = 3.3 V	–	2	–	mA	32 × 4 segments 50 Hz at 25 °C

Table 26. LCD Direct Drive AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID233	F_{LCD}	LCD frame rate	10	50	150	Hz	

Serial Communication

Table 27. Fixed I²C DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	–
I_{I2C2}	Block current consumption at 400 kHz	–	–	155	µA	–
I_{I2C3}	Block current consumption at 1 Mbps	–	–	390	µA	–
I_{I2C4}	I²C enabled in Deep-Sleep mode	–	–	1.4	µA	–

Table 28. Fixed I²C AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{I2C1}	Bit rate	–	–	400	kHz	

Table 29. Fixed UART DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{UART1}	Block current consumption at 100 kbps	–	–	55	µA	–
I_{UART2}	Block current consumption at 1000 kbps	–	–	312	µA	–

Table 30. Fixed UART AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{UART}	Bit rate	–	–	1	Mbps	–

Table 31. Fixed SPI DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{SPI1}	Block current consumption at 1 Mbps	–	–	360	µA	–
I_{SPI2}	Block current consumption at 4 Mbps	–	–	560	µA	–
I_{SPI3}	Block current consumption at 8 Mbps	–	–	600	µA	–

Table 32. Fixed SPI AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{SPI}	SPI operating frequency (master; 6x over sampling)	–	–	8	MHz	–

Table 33. Fixed SPI Master Mode AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_{DMO}	MOSI valid after SCLK driving edge	–	–	18	ns	–
T_{DSI}	MISO valid before SCLK capturing edge Full clock, late MISO sampling used	20	–	–	ns	Full clock, late MISO sampling
T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge

Table 34. Fixed SPI Slave Mode AC Specifications

Parameter	Description	Min	Typ	Max	Units
T_{DMI}	MOSI valid before SCLK capturing edge	40	–	–	ns
T_{DSO}	MISO valid after SCLK driving edge	–	–	$42 + 3 \times T_{CPU}$	ns
T_{DSO_ext}	MISO Valid after SCLK driving edge in external clock mode. $V_{DD} < 3.0$ V	–	–	50	ns
T_{HSO}	Previous MISO data hold time	0	–	–	ns
$T_{SSELSCK}$	SSEL valid to first SCK valid edge	100	–	–	ns

Memory

Table 35. Flash DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{PE}	Erase and program voltage	1.71	–	5.5	V	–
T_{WS48}	Number of Wait states at 32–48 MHz	2	–	–		CPU execution from flash
T_{WS32}	Number of Wait states at 16–32 MHz	1	–	–		CPU execution from flash
T_{WS16}	Number of Wait states for 0–16 MHz	0	–	–		CPU execution from flash

Table 36. Flash AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{ROWWRITE}$[9]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
$T_{ROWERASE}$[9]	Row erase time	–	–	13	ms	–
$T_{ROWPROGRAM}$[9]	Row program time after erase	–	–	7	ms	–
$T_{BULKERASE}$[9]	Bulk erase time (128 KB)	–	–	35	ms	–
$T_{DEVPROG}$[9]	Total device program time	–	–	25	seconds	–
F_{END}	Flash endurance	100 K	–	–	cycles	–
F_{RET}	Flash retention. $T_A \le 55$ °C, 100 K P/E cycles	20	–	–	years	–
F_{RET2}	Flash retention. $T_A \le 85$ °C, 10 K P/E cycles	10	–	–	years	–

System Resources

Power-on-Reset (POR)

Table 37. POR DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.45	V	–
$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.40	V	–
$V_{IPORHYST}$	Hysteresis	15	–	200	mV	–

Table 38. POR AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_{PPOR_TR}	Precision power-on reset (PPOR) response time in Active and Sleep modes	–	–	1	µs	–

Table 39. Brown-Out Detect

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$V_{FALLPPOR}$	BOD trip voltage in Active and Sleep modes	1.64	–	–	V	–
$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.4	–	–	V	–

Table 40. Hibernate Reset

Parameter	Description	Min	Typ	Max	Units	Details/Conditions

Note

9. It can take as much as 20 ms to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

Table 40. Hibernate Reset

$V_{HBRTRIP}$	BOD trip voltage in Hibernate	1.1	–	–	V	–

Voltage Monitors (LVD)

Table 41. Voltage Monitor DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{LVI1}	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	–
V_{LVI2}	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	–
V_{LVI3}	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	–
V_{LVI4}	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	–
V_{LVI5}	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	–
V_{LVI6}	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	–
V_{LVI7}	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	–
V_{LVI8}	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	–
V_{LVI9}	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	–
V_{LVI10}	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	–
V_{LVI11}	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	–
V_{LVI12}	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	–
V_{LVI13}	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	–
V_{LVI14}	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	–
V_{LVI15}	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	–
V_{LVI16}	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	–
LVI_IDD	Block current	–	–	100	µA	–

Table 42. Voltage Monitor AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{MONTRIP}$	Voltage monitor trip time	–	–	1	µs	–

SWD Interface

Table 43. SWD Interface Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 × T	ns	–
T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	–

Internal Main Oscillator

Table 44. IMO DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	–
I_{IMO2}	IMO operating current at 24 MHz	–	–	325	µA	–
I_{IMO3}	IMO operating current at 12 MHz	–	–	225	µA	–
I_{IMO4}	IMO operating current at 6 MHz	–	–	180	µA	–
I_{IMO5}	IMO operating current at 3 MHz	–	–	150	µA	–

Table 45. IMO AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$F_{IMOTOL3}$	Frequency variation from 3 to 48 MHz	–	–	±2	%	With API-called calibration
$F_{IMOTOL3}$	IMO startup time	–	12	–	µs	–

Internal Low-Speed Oscillator

Table 46. ILO DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I_{ILO2}	ILO operating current at 32 kHz	–	0.3	1.05	µA	–

Table 47. ILO AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{STARTILO1}$	ILO startup time	–	–	2	ms	–
$F_{ILOTRIM1}$	32-kHz trimmed frequency	15	32	50	kHz	–

Table 48. ECO Trim Value Specification

Parameter	Description	Value	Details/Conditions
ECO_{TRIM}	24-MHz trim value (firmware configuration)	0x00003FFA	Optimum trim value that needs to be loaded to register CY_SYS_XTAL_BLERD_BB_XO_CAPTRIM_REG

Environmental Specifications

Environmental Compliance

This Cypress BLE module is built in compliance with the Restriction of Hazardous Substances (RoHS) and Halogen Free (HF) directives. The Cypress module and components used to produce this module are RoHS and HF compliant.

RF Certification

The CYBLE-222005-00 module is certified under the following RF certification standards:

- FCC
- CE
- IC
- MIC
- KC

Environmental Conditions

Table 49 describes the operating and storage conditions for the Cypress BLE module.

Table 49. Environmental Conditions for CYBLE-222005-00

Description	Minimum Specification	Maximum Specification
Operating temperature	-40 °C	85 °C
Operating humidity (relative, non-condensation)	5%	85%
Thermal ramp rate	–	3 °C/minute
Storage temperature	–40 °C	85 °C
Storage temperature and humidity	–	85 ° C at 85%
ESD: Module integrated into system Components[10]	–	15 kV Air 2.2 kV Contact

ESD and EMI Protection

Exposed components require special attention to ESD and electromagnetic interference (EMI).

A grounded conductive layer inside the device enclosure is suggested for EMI and ESD performance. Any openings in the enclosure near the module should be surrounded by a grounded conductive layer to provide ESD protection and a low-impedance path to ground.

Device Handling: Proper ESD protocol must be followed in manufacturing to ensure component reliability.

Note
10. This does not apply to the RF pins (ANT, XTALI, and XTALO). RF pins (ANT, XTALI, and XTALO) are tested for 500-V HBM.

Regulatory Information

FCC

FCC NOTICE:

The device CYBLE-222005-00, including the antenna 2450AT18B100 from Johanson Technology, complies with Part 15 of the FCC Rules. The device meets the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407.transmitter Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

CAUTION:

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Cypress Semiconductor may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions,ê may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that FCC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor FCC identifier for this product as well as the FCC Notice above. The FCC identifier is FCC ID: **TBD**.

In any case the end product must be labeled exterior with "Contains FCC ID: **TBD**"

ANTENNA WARNING:

This device is tested with a standard SMA connector and with the antennas listed below. When integrated in the OEMs product, these fixed antennas require installation preventing end-users from replacing them with non-approved antennas. Any antenna not in the following table must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions.

RF EXPOSURE:

To comply with FCC RF Exposure requirements, the Original Equipment Manufacturer (OEM) must ensure to install the approved antenna in the previous.

The preceding statement must be included as a CAUTION statement in manuals, for products operating with the approved antennas in Table 6 on page 11, to alert users on FCC RF Exposure compliance. Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of CYBLE-222005-00 with the chip antenna mounted (FCC ID: **TBD**) is far below the FCC radio frequency exposure limits. Nevertheless, use CYBLE-222005-00 in such a manner that minimizes the potential for human contact during normal operation.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

Industry Canada (IC) Certification

CYBLE-222005-00 is licensed to meet the regulatory requirements of Industry Canada (IC), License: IC: **TBD**

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from www.ic.gc.ca.

This device has been designed to operate with the antennas listed in Table 6 on page 11, having a maximum gain of 0.5 dBi. Antennas not included in this list or having a gain greater than 0.5 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

IC NOTICE:

The device CYBLE-222005-00 including the antenna 2450AT18B100 from Johanson technology, complies with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-GEN. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that IC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor IC identifier for this product as well as the IC Notice above. The IC identifier is **TBD**. In any case, the end product must be labeled in its exterior with "Contains IC: **TBD**"

European R&TTE Declaration of Conformity

Hereby, Cypress Semiconductor declares that the Bluetooth module CYBLE-222005-00 complies with the essential requirements and other relevant provisions of Directive 1999/5/EC. As a result of the conformity assessment procedure described in Annex III of the Directive 1999/5/EC, the end-customer equipment should be labeled as follows:

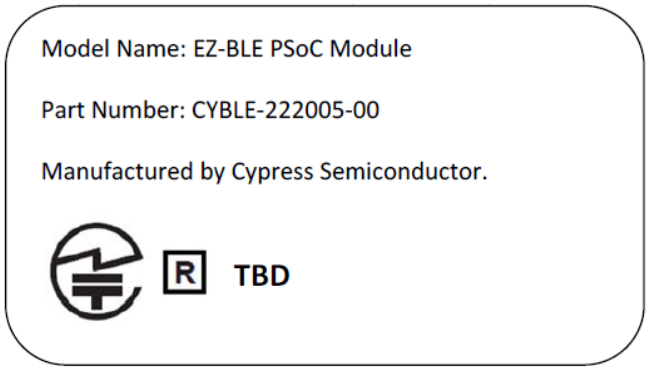
CE

All versions of the CYBLE-222005-00 in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

MIC Japan

CYBLE-222005-00 is certified as a module with type certification number TBD. End products that integrate CYBLE-222005-00 do not need additional MIC Japan certification for the end product.

End product can display the certification label of the embedded module.



KC Korea

CYBLE-222005-00 is certified for use in Korea with certificate number TBD.

한국 인증 세부정보:

해당 무선설비는 전파혼신 가능성이 있으므로 인명안전과 관련된 서비스는 할 수 없습니다.

Packaging

The CYBLE-222005-00 is offered in tape and reel pacakging. Figure 8 details the tape dimensions used for the CYBLE-222005-00.

Figure 8. CYBLE-222005-00 Tape Dimensions

Item	W	A_0	B_0	K_0	K_1	P_1	F	E	D_0	D_1	P_0	P_2	T
Measurement	$24.0^{+0.30}_{-0.30}$	$10.26^{+0.10}_{-0.10}$	$10.26^{+0.10}_{-0.10}$	$2.00^{+0.10}_{-0.10}$	$^{+0.10}_{-0.10}$	$16.0^{+0.10}_{-0.10}$	$11.5^{+0.10}_{-0.10}$	$1.75^{+0.10}_{-0.10}$	$1.50^{+0.10}_{-0.00}$	$1.50^{+0.10}_{-0.10}$	$4.00^{+0.10}_{-0.10}$	$2.00^{+0.10}_{-0.10}$	$0.30^{+0.05}_{-0.05}$

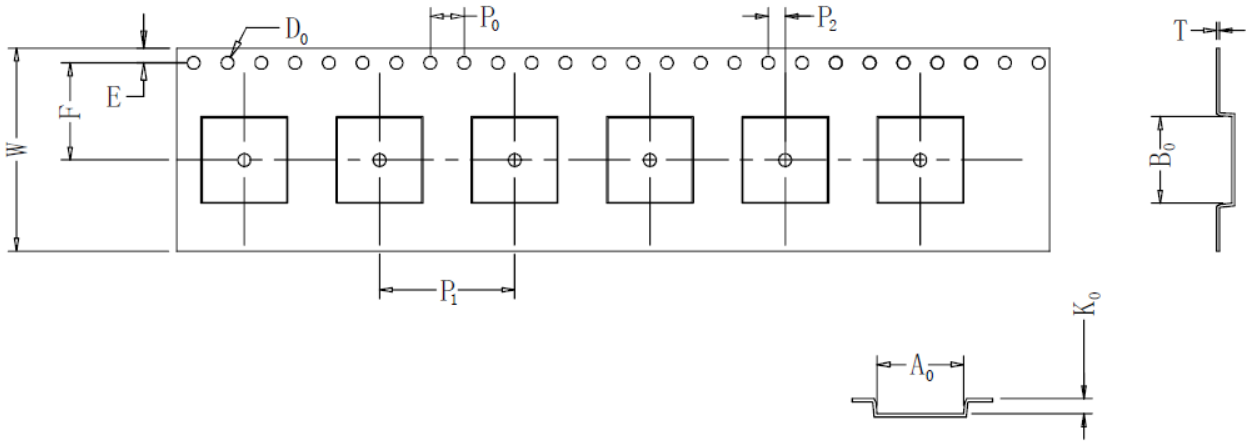


Figure 9 details the orientation of the CYBLE-222005-00 in the tape as well as the direction for unreeling.

Figure 9. Component Orientation in Tape and Unreeling Direction

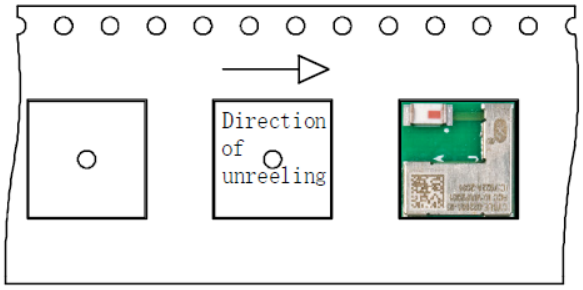
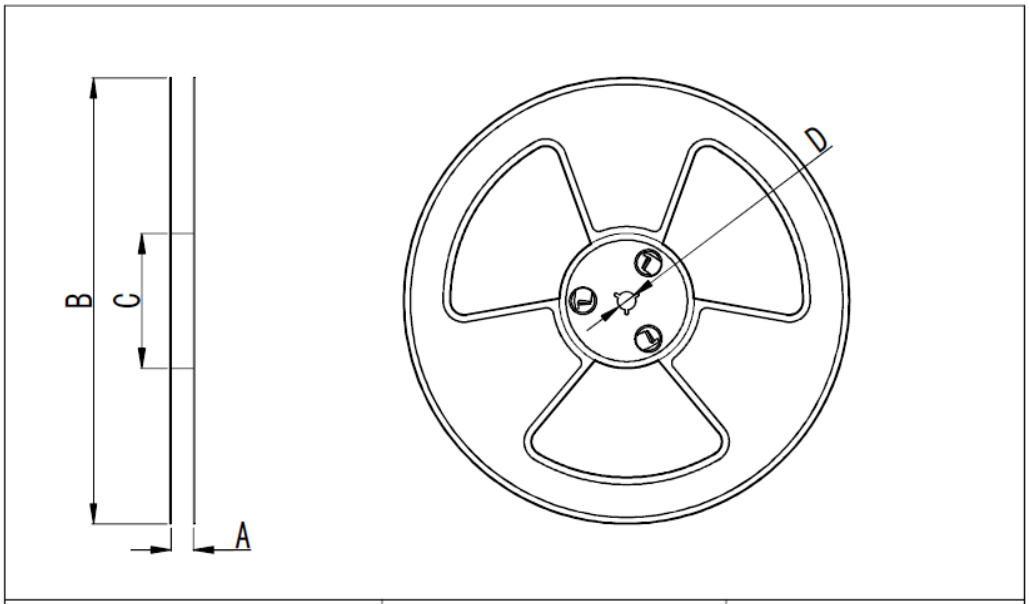


Figure 10 details reel dimensions used for the CYBLE-222005-00.

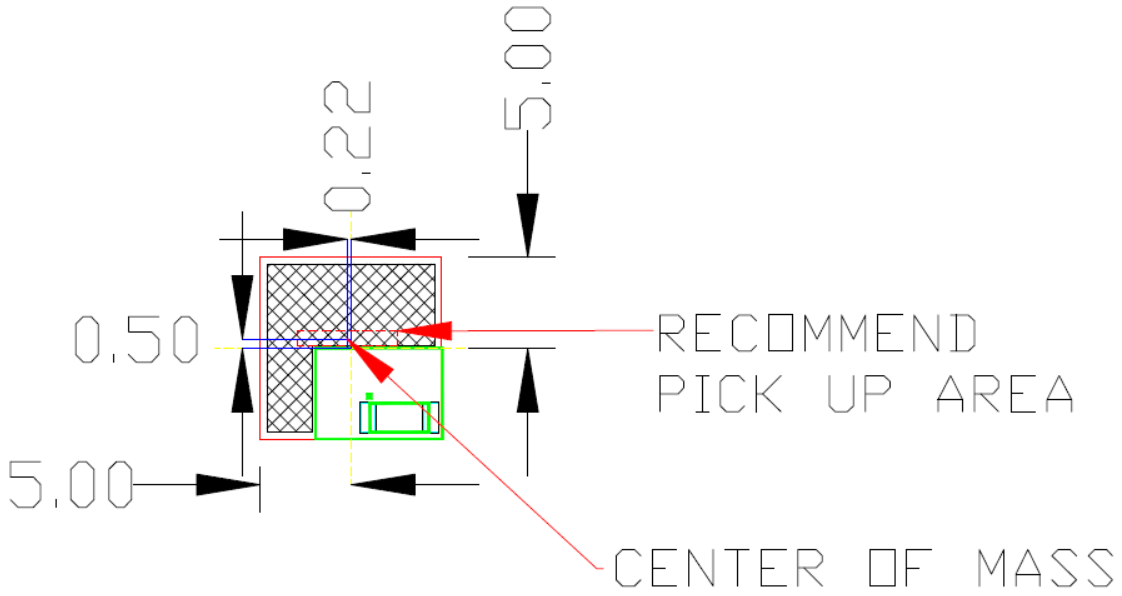
Figure 10. Reel Dimensions



Index	NOTE	Dimension	Tolerance	
A	Inside Width	24.5	+0.50mm	-0.50mm
B	Reel Diameter	330.00	+1.5mm	-1.5mm
C	Outer Axis Diameter	100.00	+1.5mm	-1.5mm
D	Inner Axis Diameter	13.00	+0.50mm	-0.50mm

The CYBLE-222005-00 is designed to be used with pick-and-place equipment in an SMT manufacturing environment. The center-of-mass for the CYBLE-222005-00 is detailed in Figure 11.

Figure 11. CYBLE-222005-00 Center of Mass



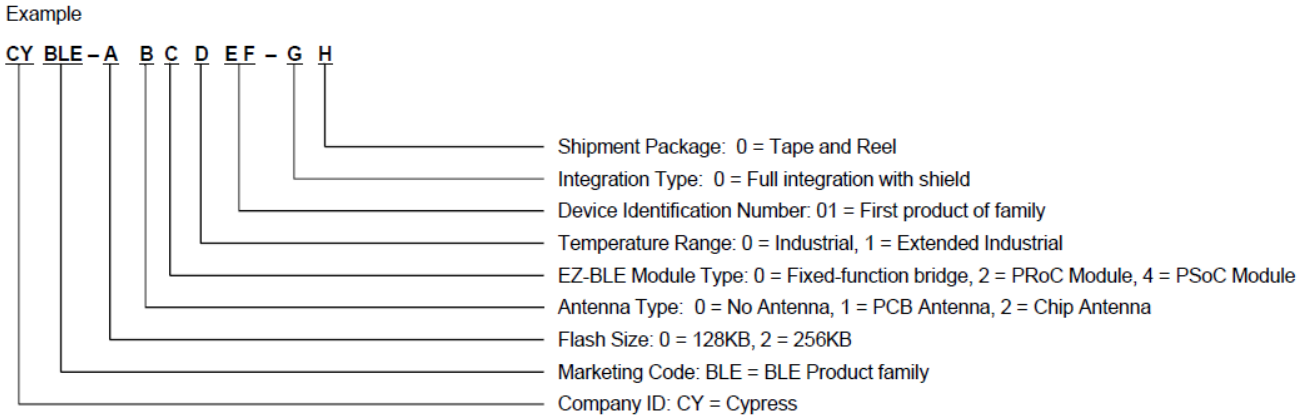
Ordering Information

The CYBLE-222005-00 part number and features are listed in the following table.

Part Number	CPU Speed (MHz)	Flash Size (KB)	CapSense	SCB	TCPWM	12-Bit SAR ADC	I^2S	LCD	Package	Packing
CYBLE-222005-00	48	256	Yes	2	4	1 Msps	Yes	Yes	22-SMT	Tape and Reel

Part Numbering Convention

The part numbers are of the form CYBLE-ABCDEF-GH where the fields are defined as follows.



For additional information and a complete list of Cypress Semiconductor BLE products, contact your local Cypress sales representative. To locate the nearest Cypress office, visit our website.

U.S. Cypress Headquarters Address	198 Champion Court, San Jose, CA 95134
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Cypress website address	http://www.cypress.com

Acronyms

Acronym	Description
BLE	Bluetooth Low Energy
Bluetooth SIG	Bluetooth Special Interest Group
CE	European Conformity
CSA	Canadian Standards Association
EMI	electromagnetic interference
ESD	electrostatic discharge
FCC	Federal Communications Commission
GPIO	general-purpose input/output
IC	Industry Canada
IDE	integrated design environment
KC	Korea Certification
MIC	Ministry of Internal Affairs and Communications (Japan)
PCB	printed circuit board
RX	receive
QDID	qualification design ID
SMT	surface-mount technology; a method for producing electronic circuitry in which the components are placed directly onto the surface of PCBs
TCPWM	timer, counter, pulse width modulator (PWM)
TUV	Germany: Technischer Überwachungs-Verein (Technical Inspection Association)
TX	transmit

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kV	kilovolt
mA	milliamperes
mm	millimeters
mV	millivolt
µA	microamperes
µm	micrometers
MHz	megahertz
GHz	gigahertz
V	volt

Document History Page

Document Title: CYBLE-222005-00 Bluetooth® Low Energy (BLE) Module Document Number: 002-00214				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	PRELIM-INARY	DSO	09/10/2015	Preliminary datasheet for CYBLE-222005-00 module.

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