

CY8CKIT-062-BLE PSoC 6 BLE Pioneer Board

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Drawing Numbers

PCBA	121-60367-01
PCB	600-60380-01
FAB DRW	610-60337-01
ASSY DRW	620-60345-01
SCH DRW	630-60357-01



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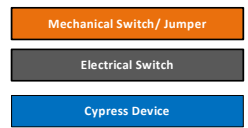
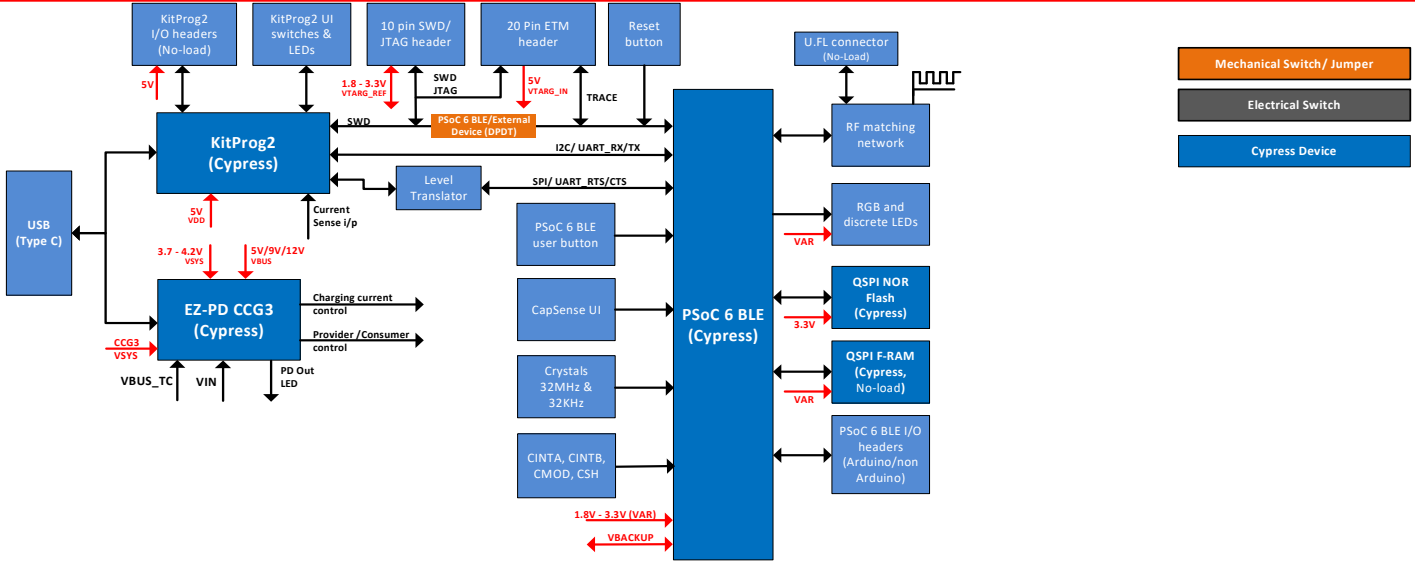
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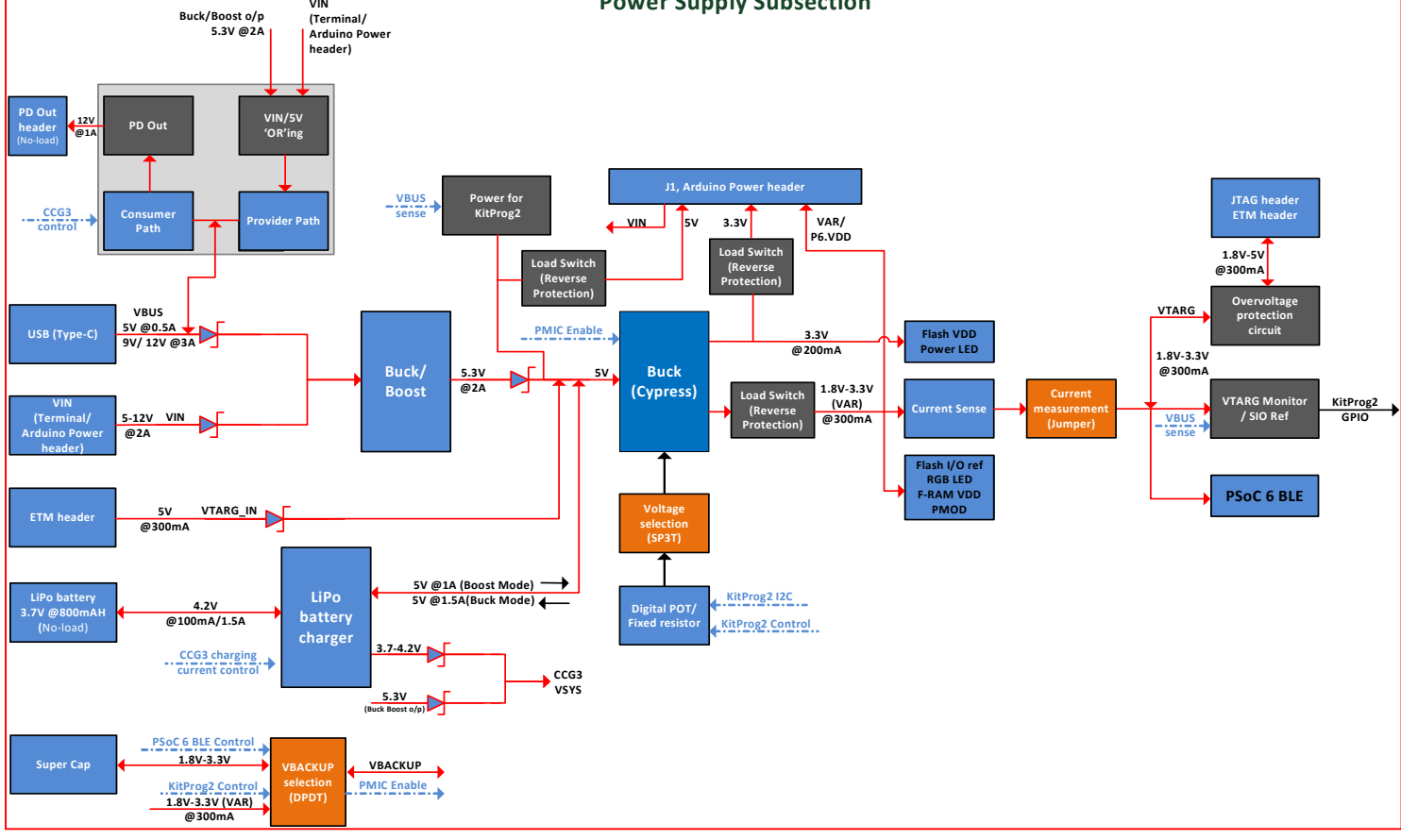
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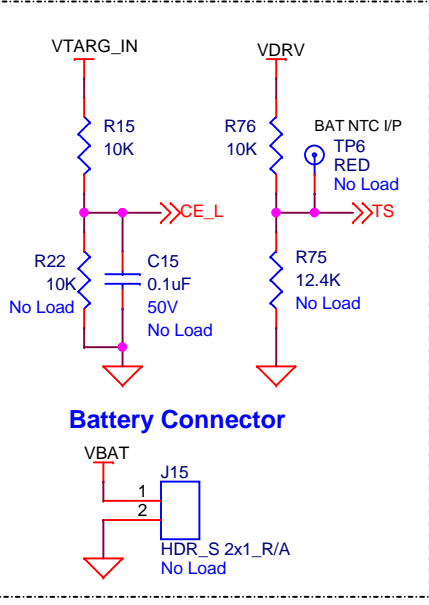
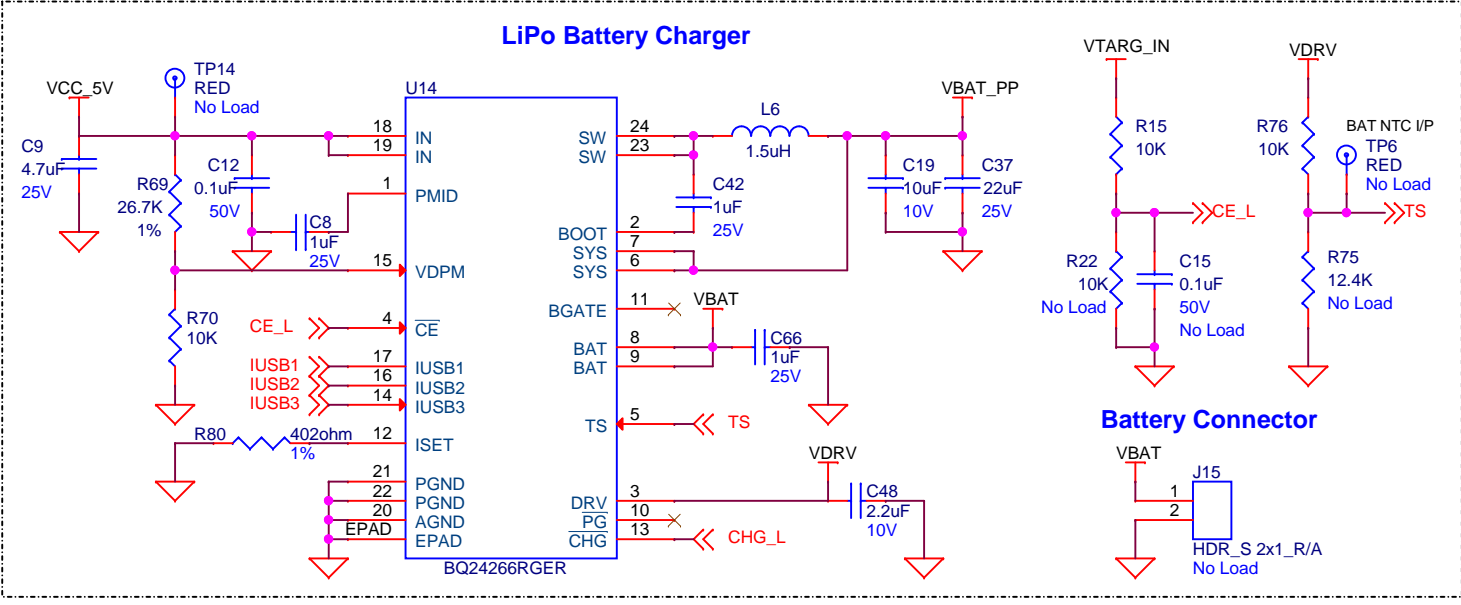
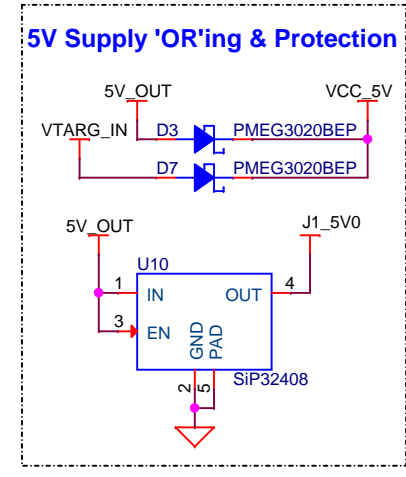
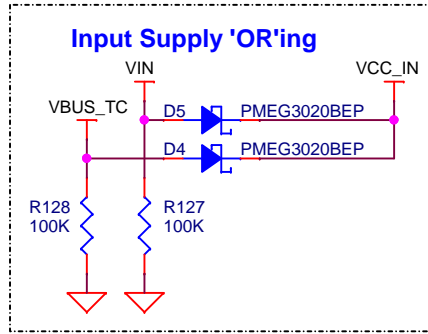
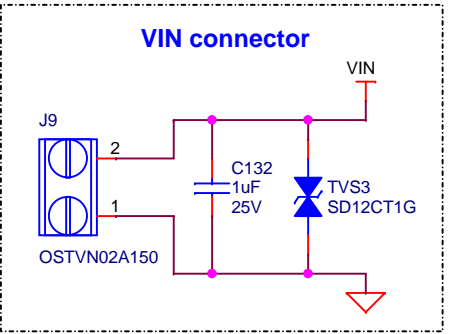
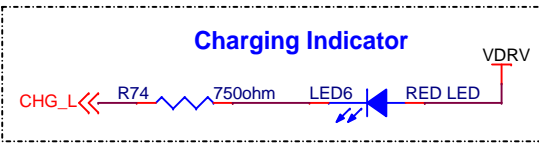
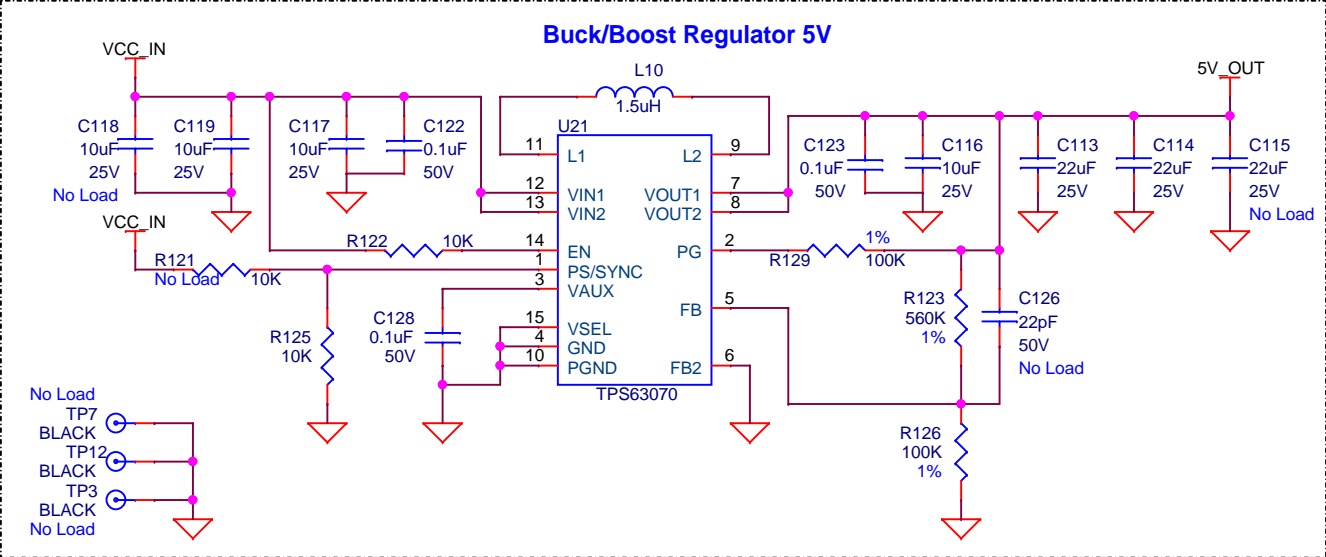
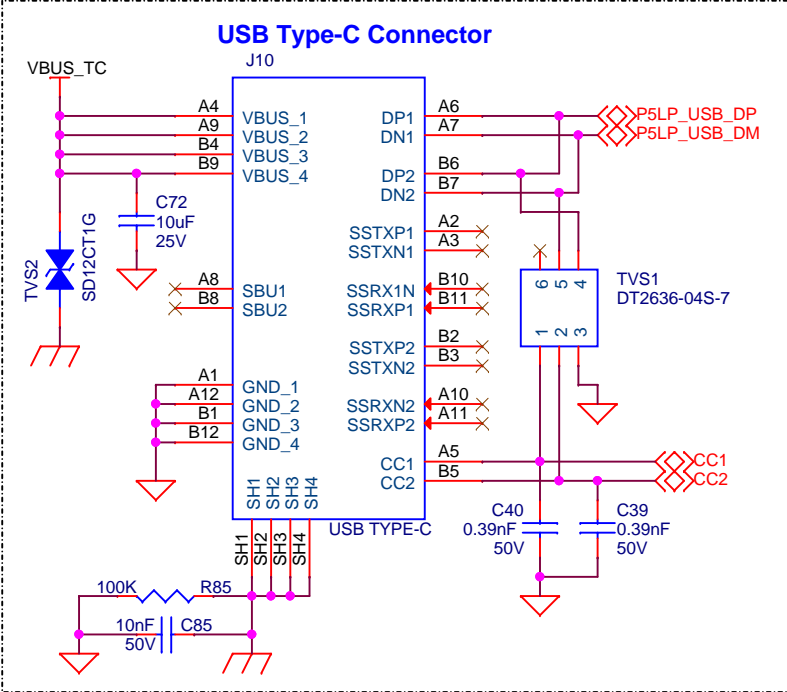
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Power Supply Subsection

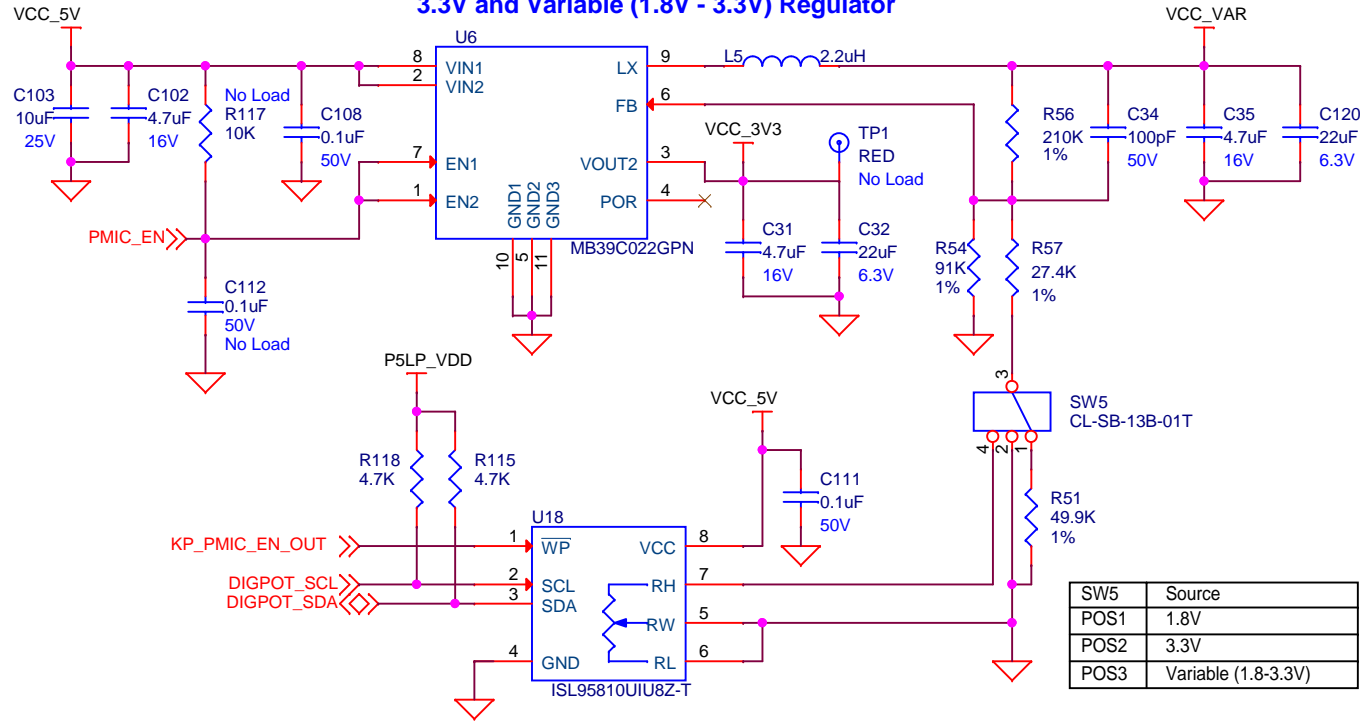


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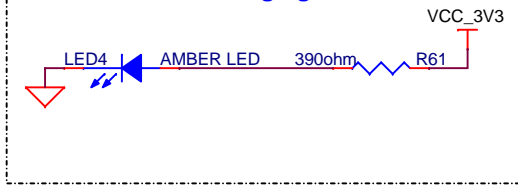


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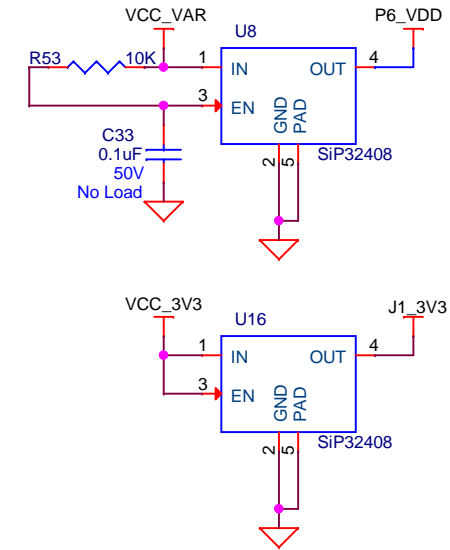
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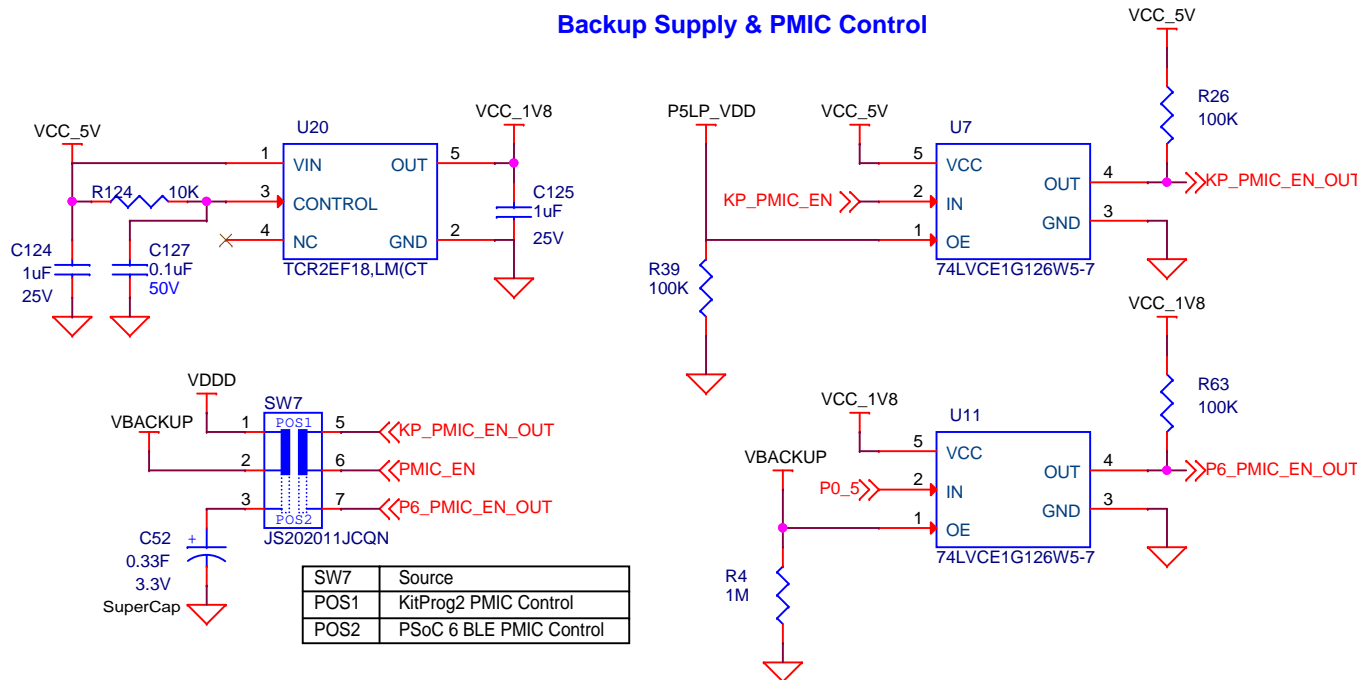
Power & Charging LED



Reverse protection



Backup Supply & PMIC Control



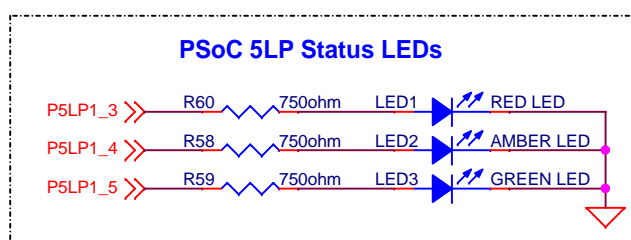
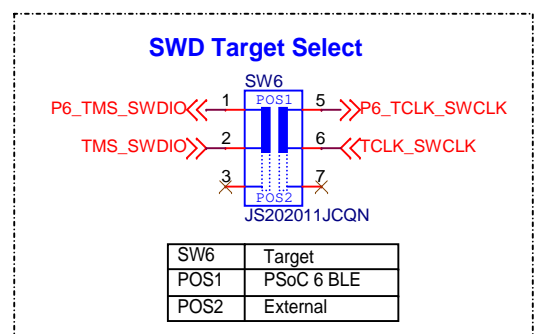
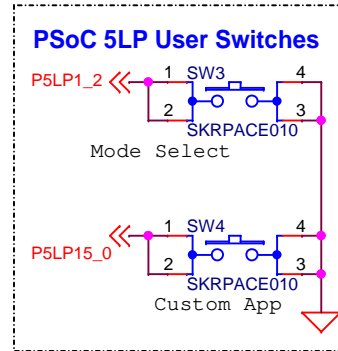
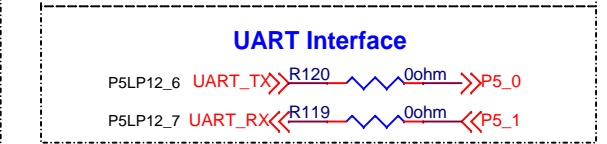
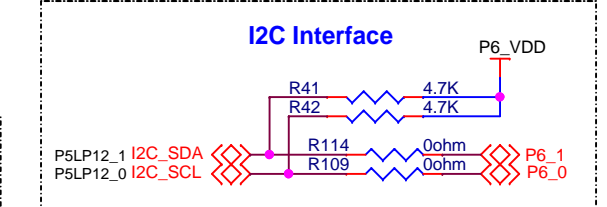
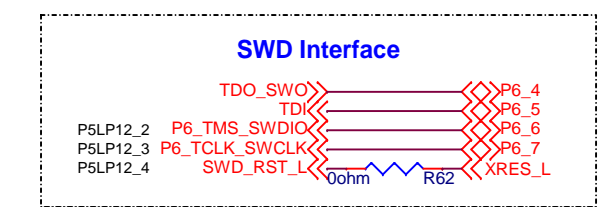
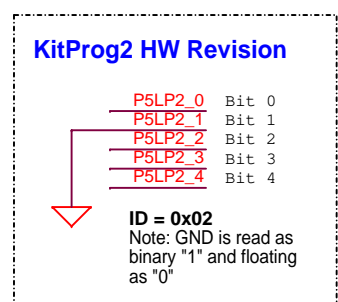
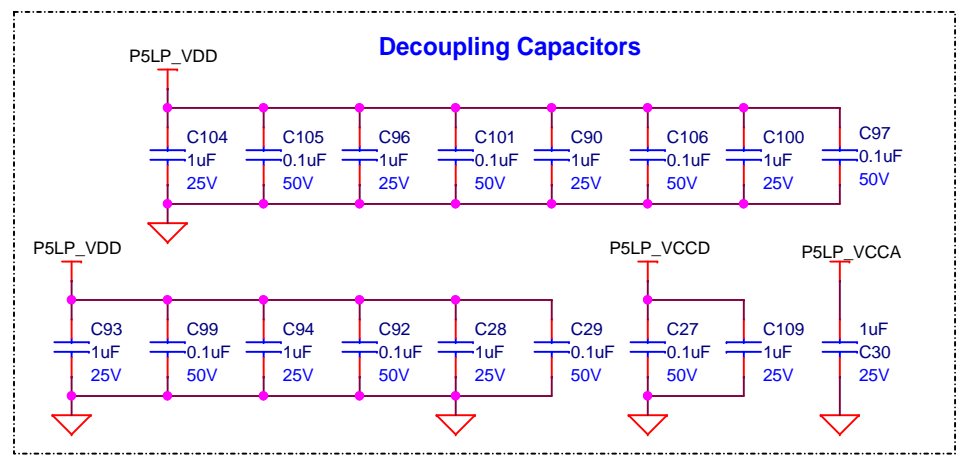
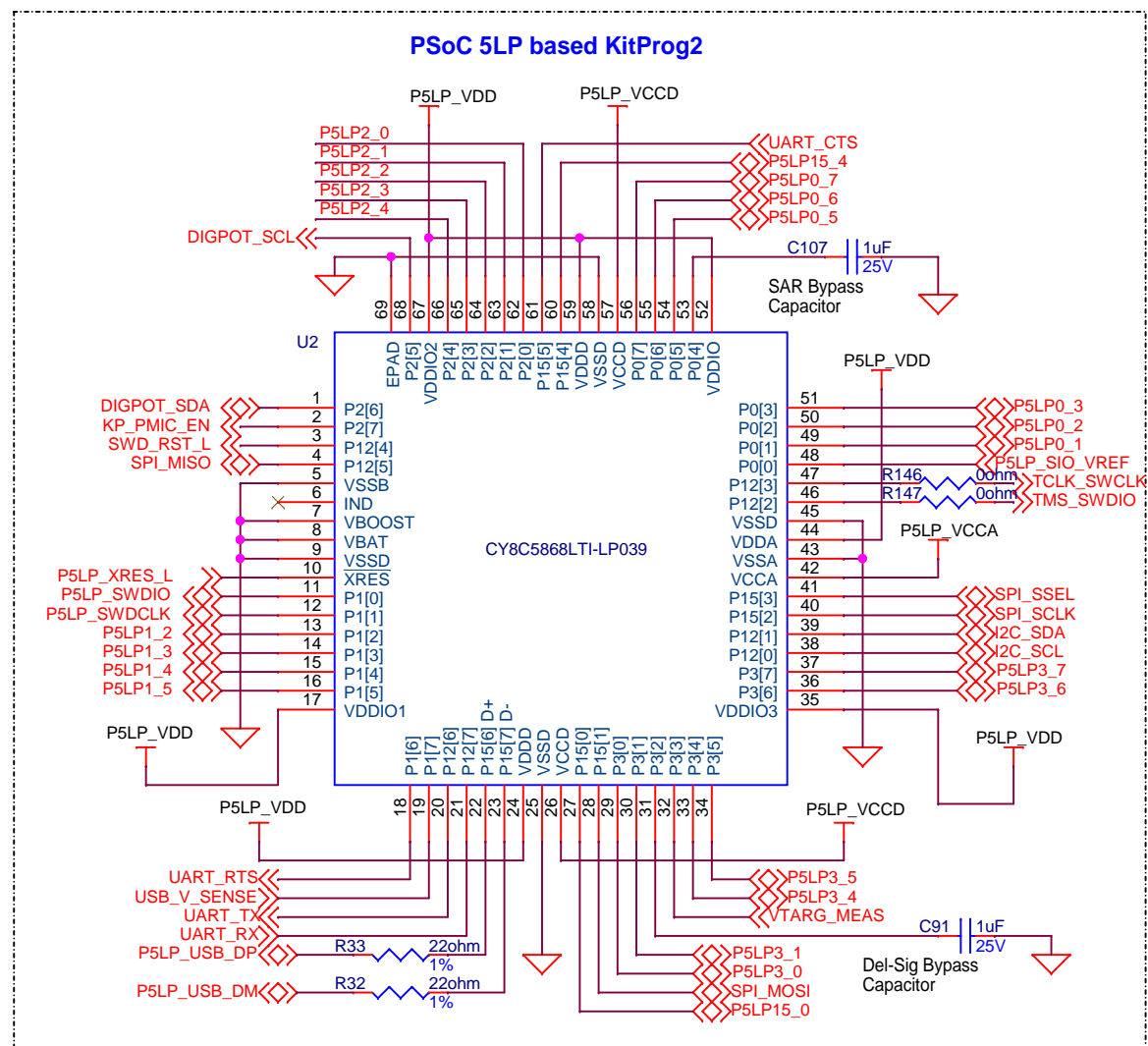

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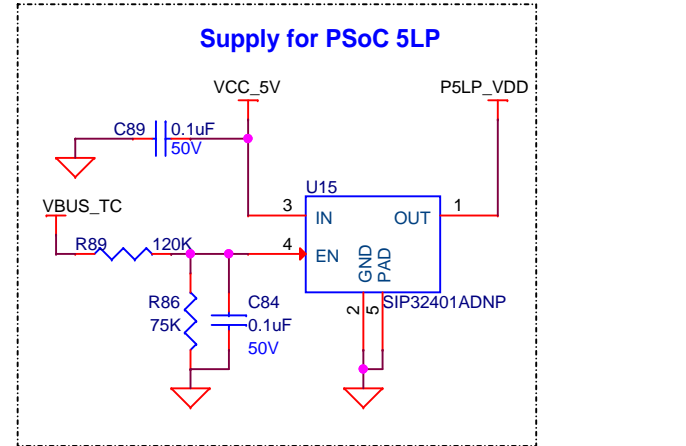
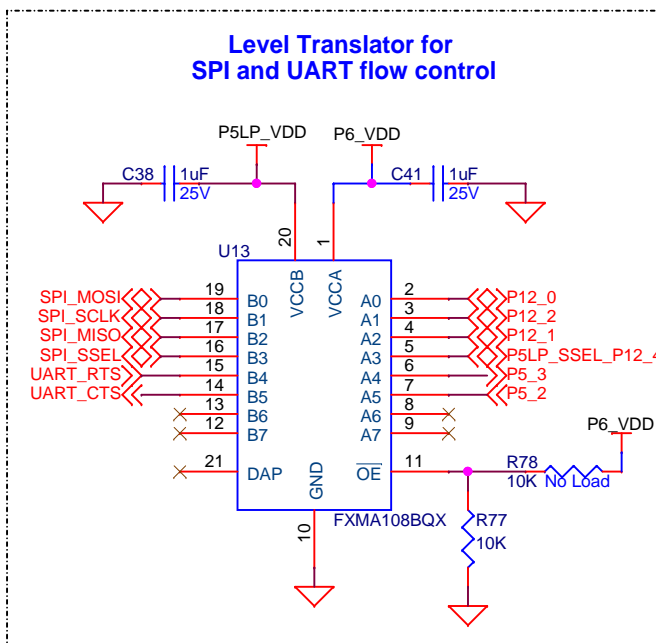
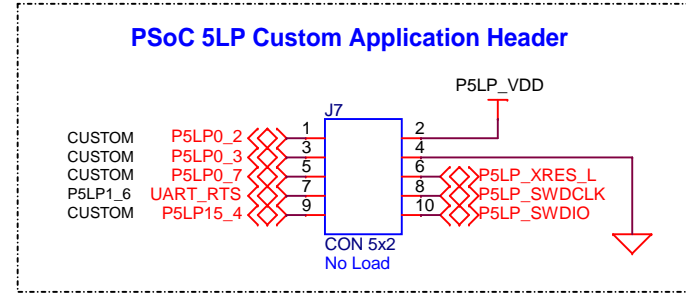
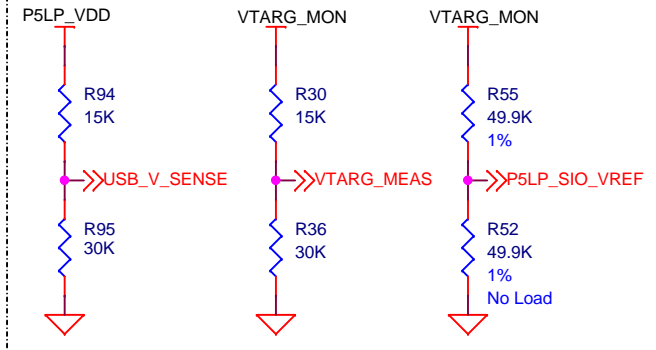
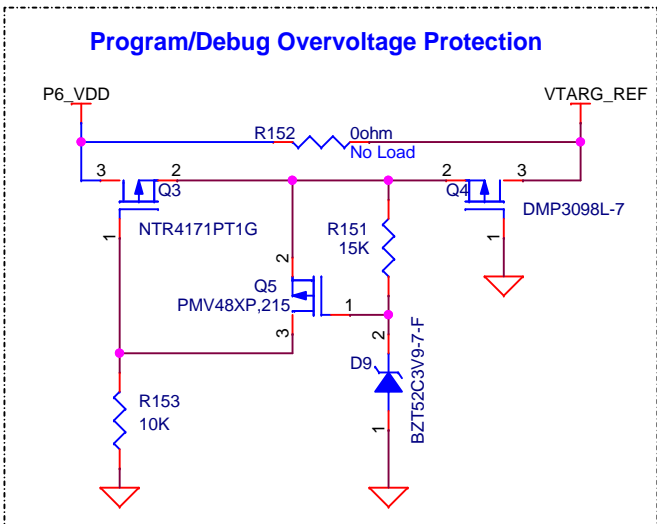
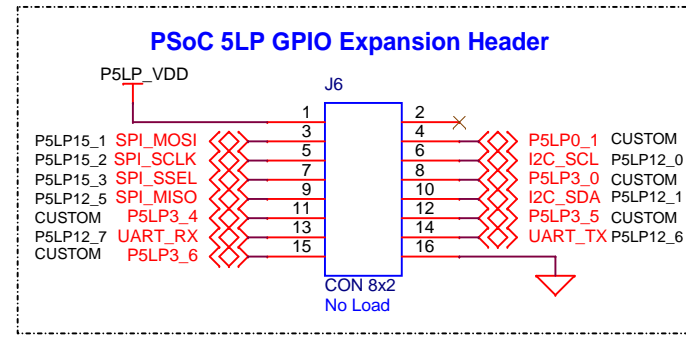
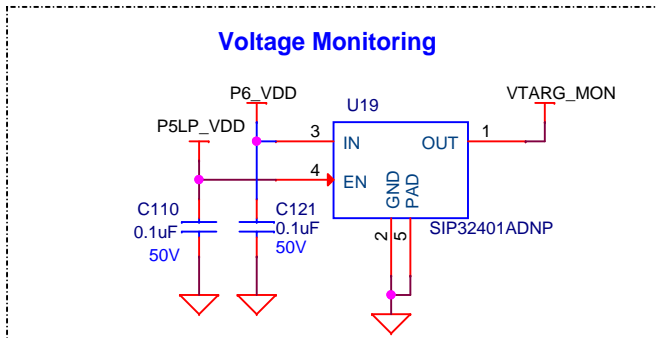
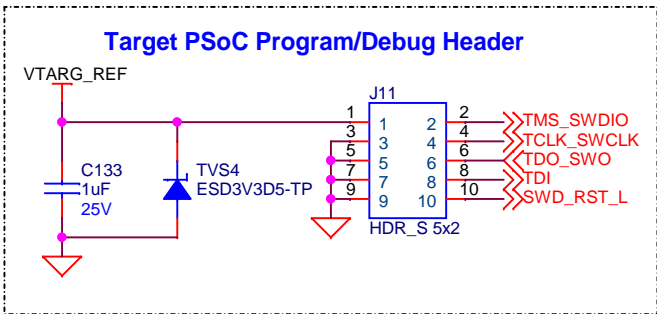
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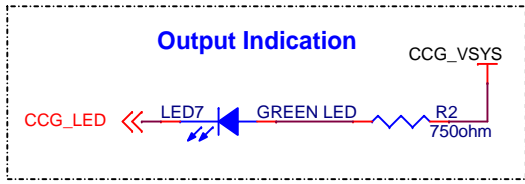
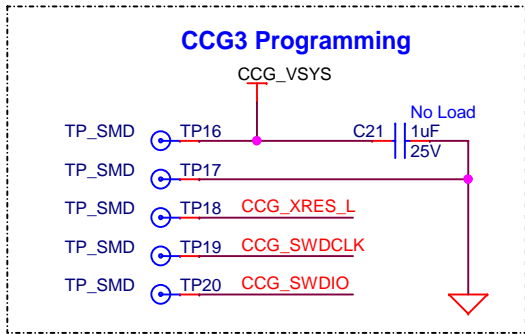
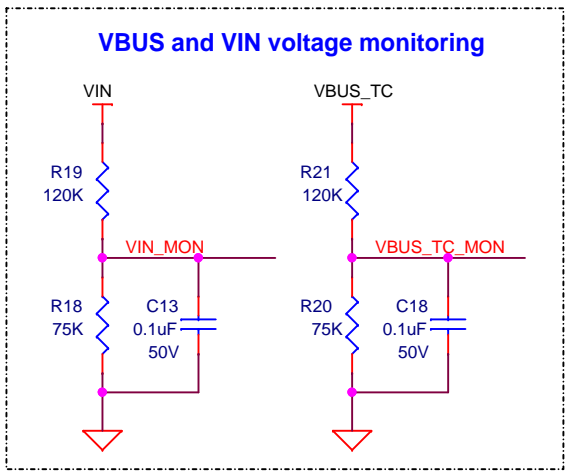
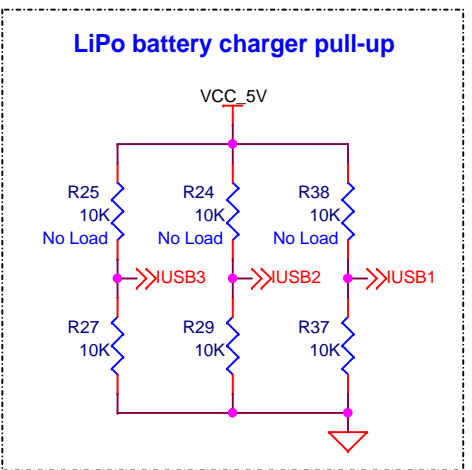
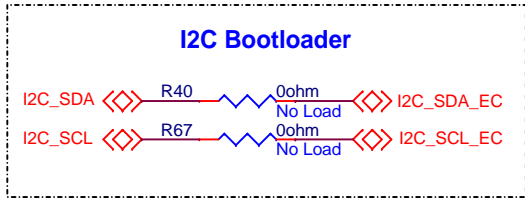
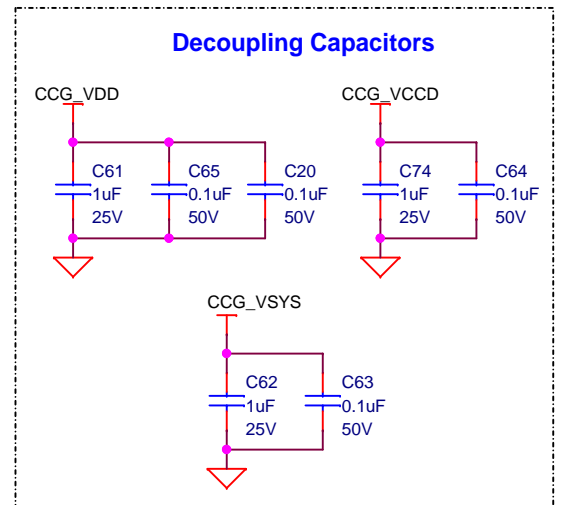
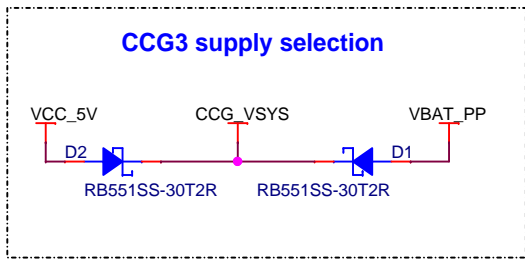
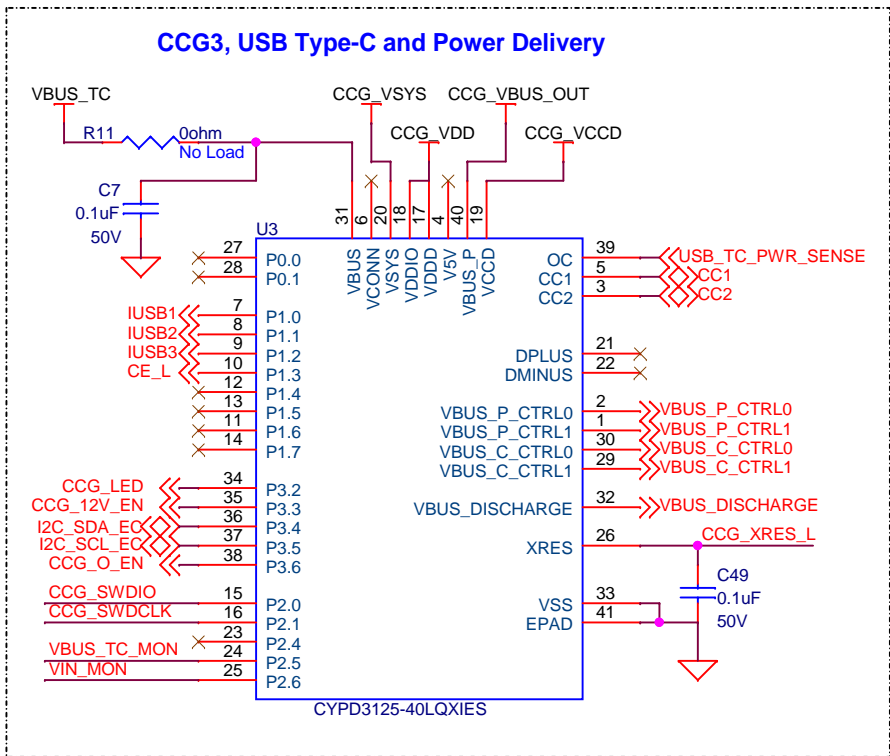
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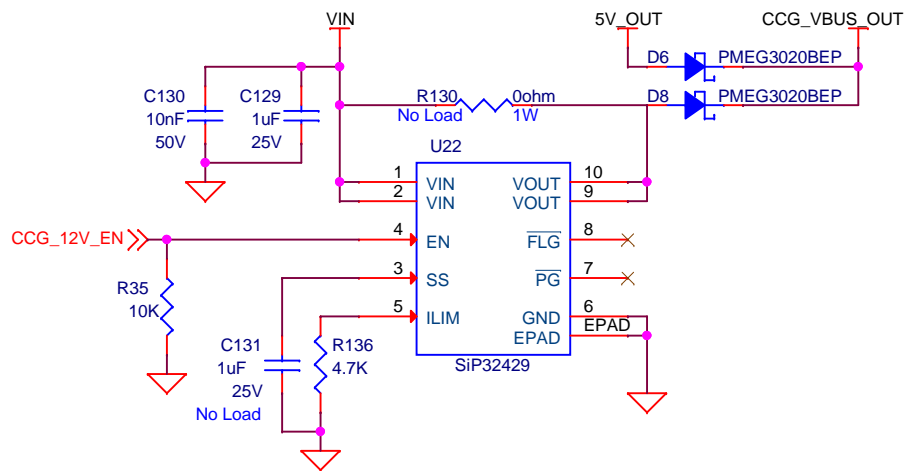


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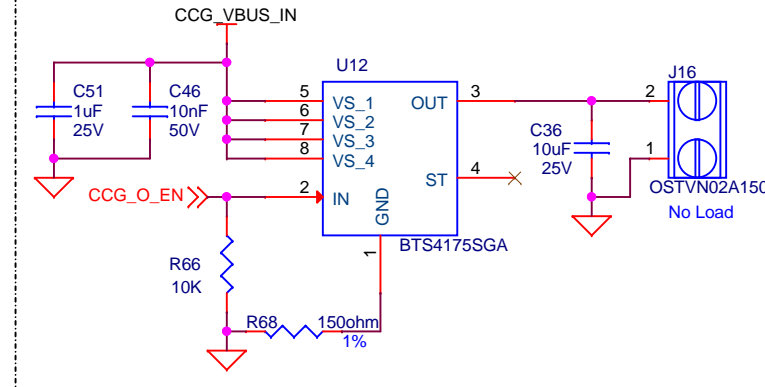
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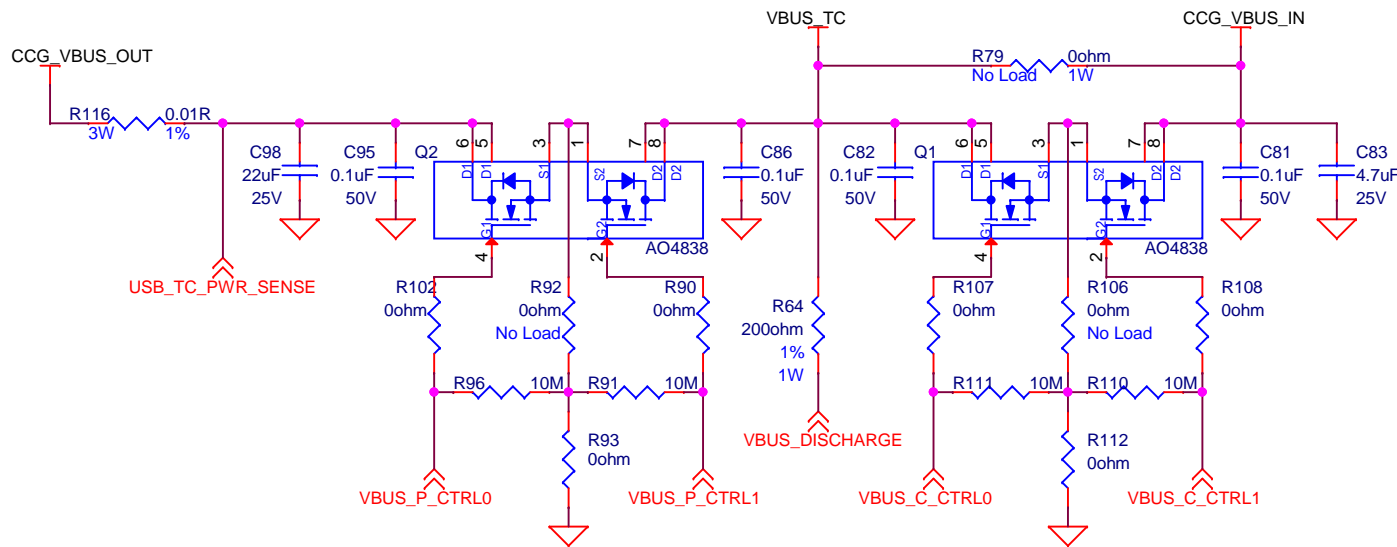
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CCG3 12V @1A Output



VBUS Provider/Consumer Path



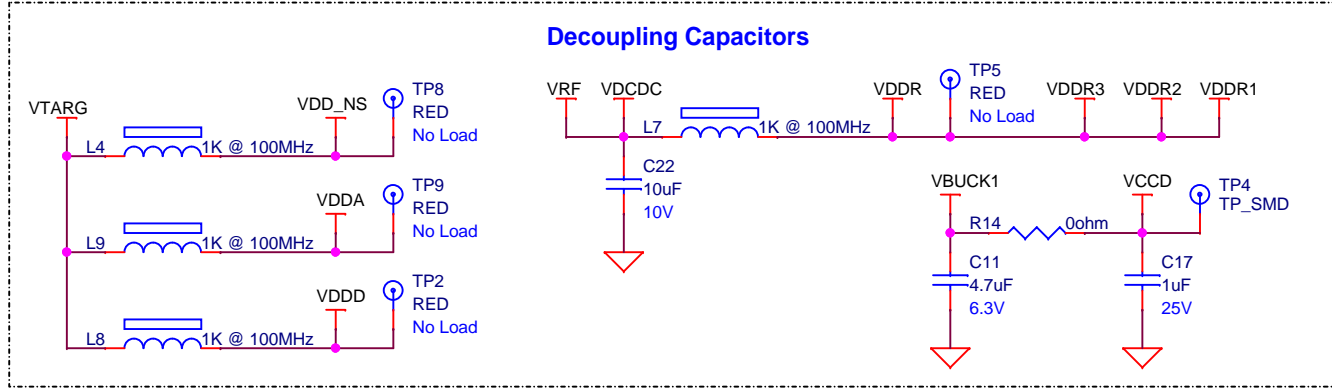
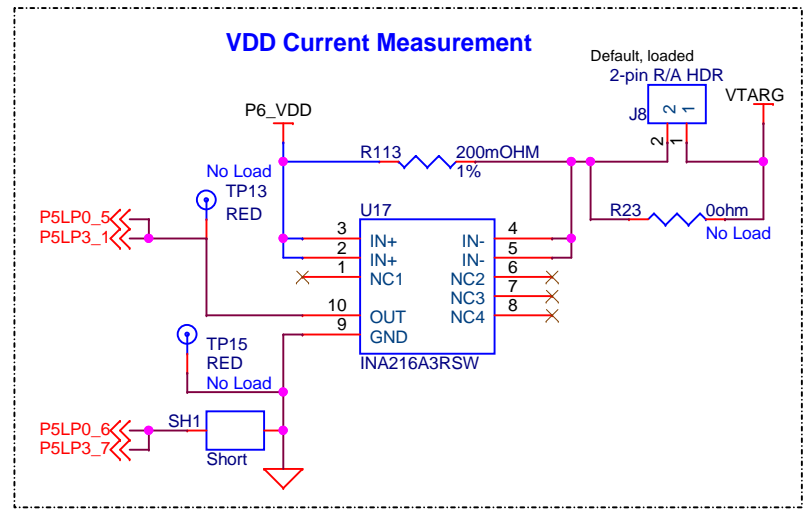
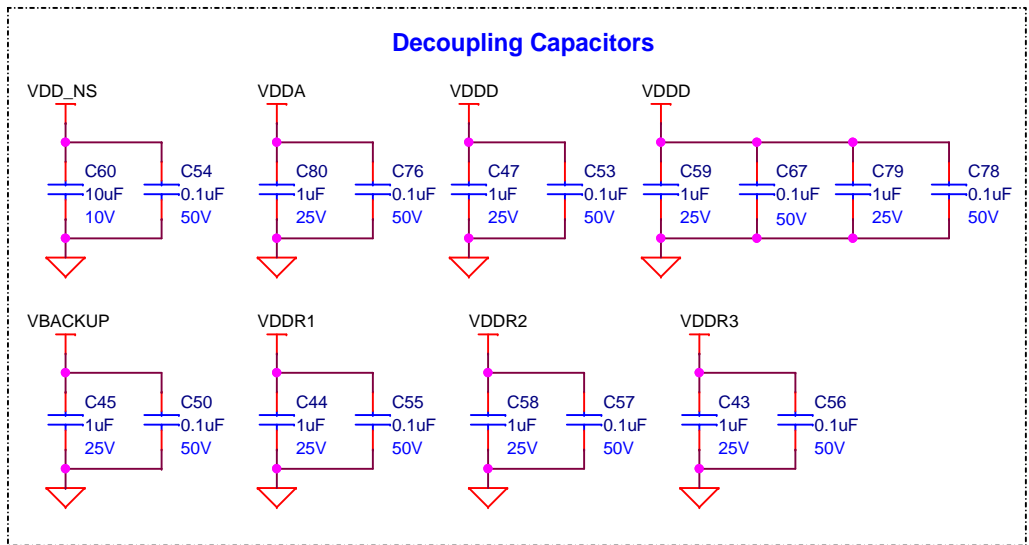
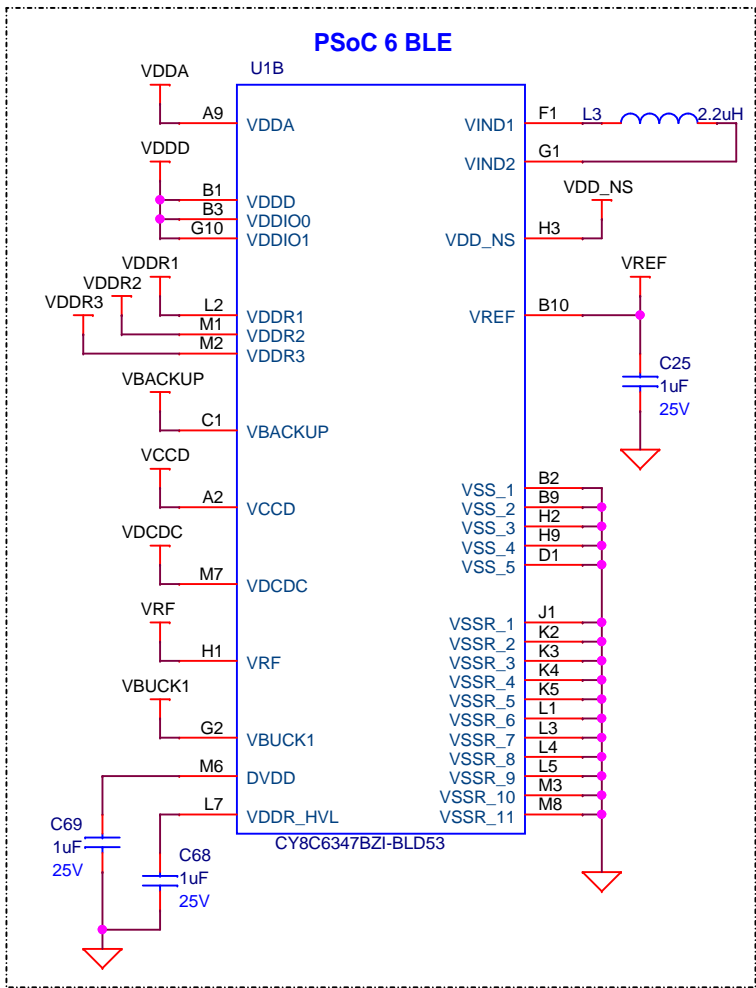
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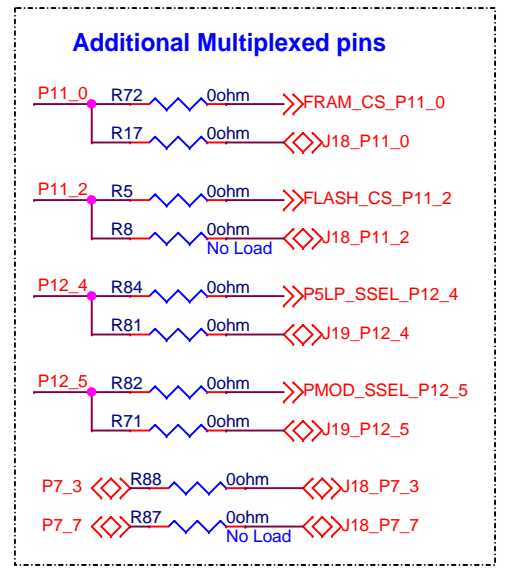
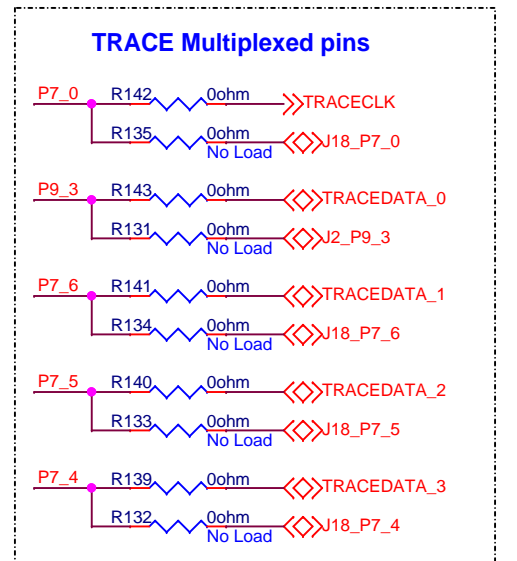
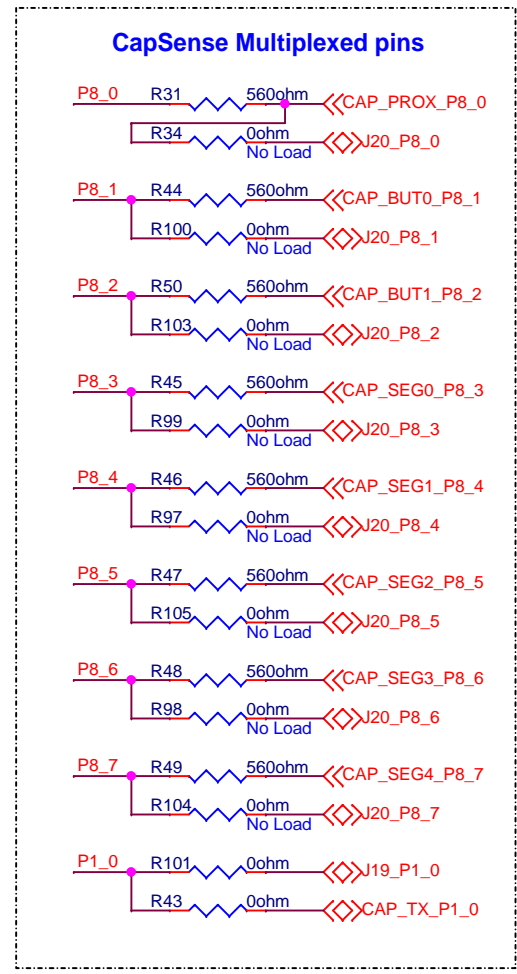
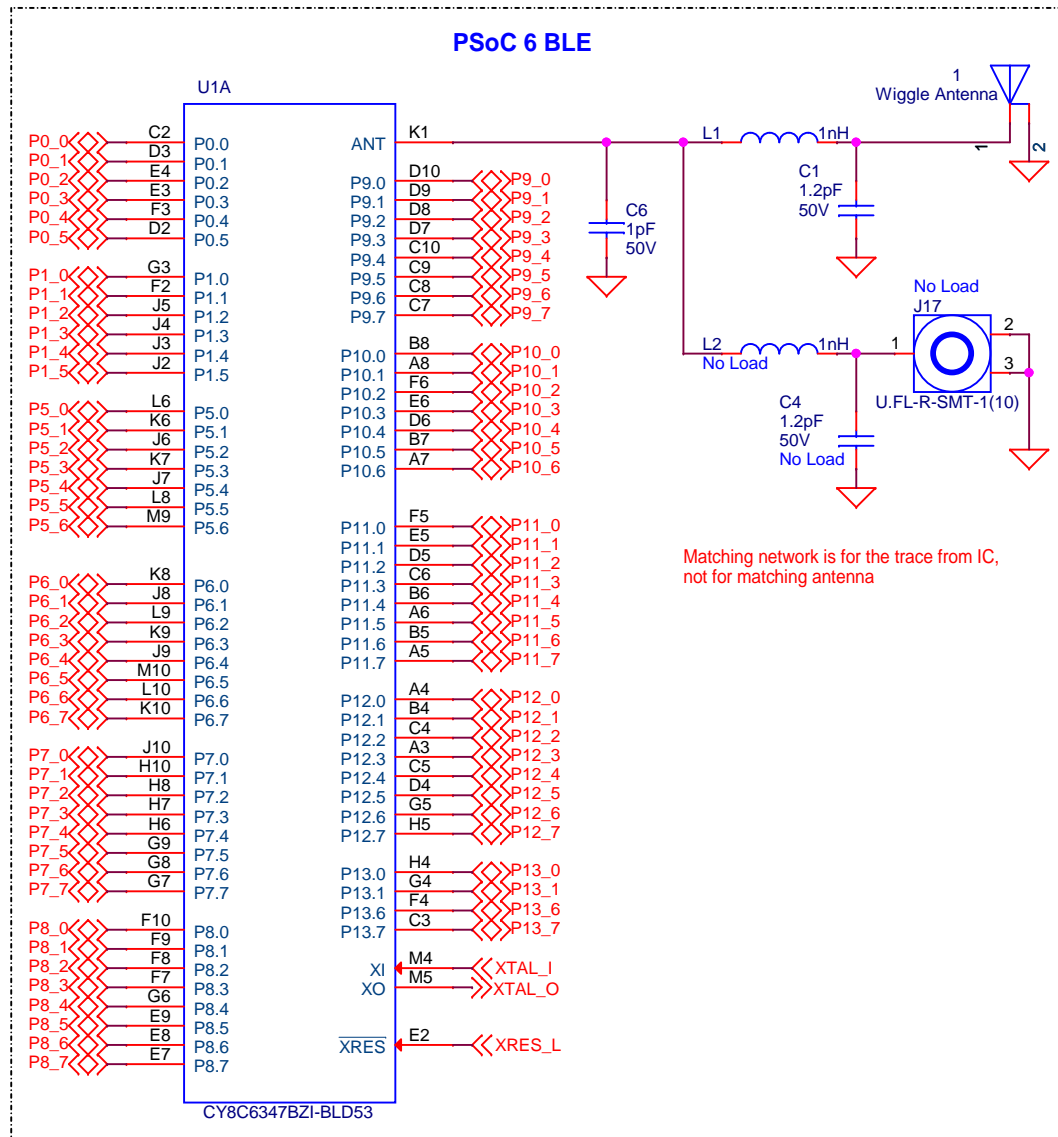
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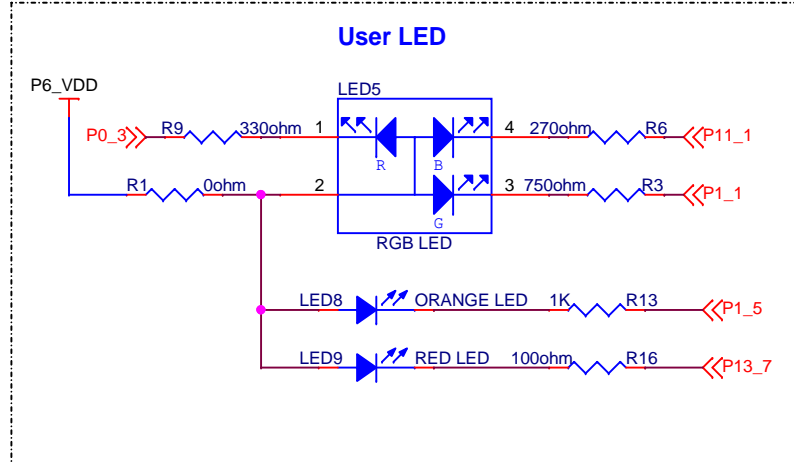
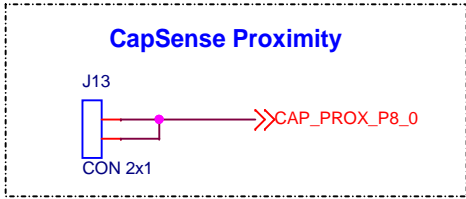
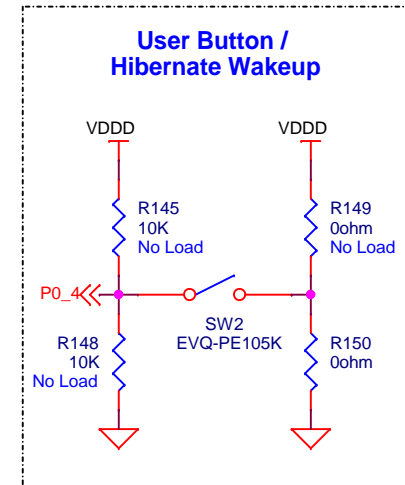
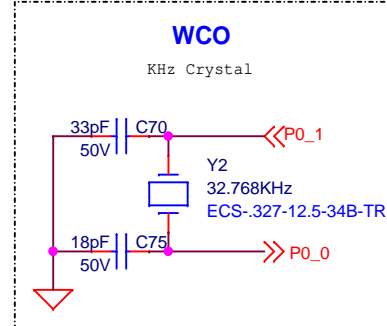
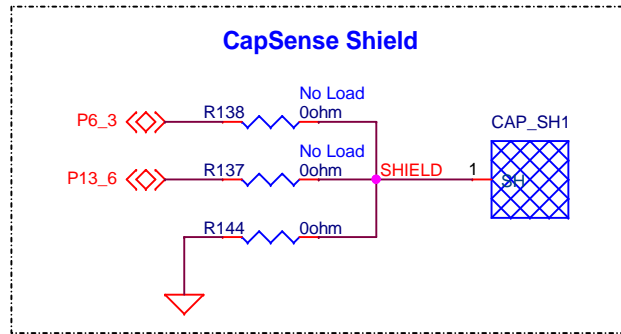
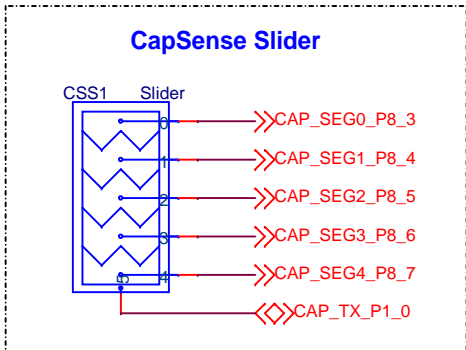
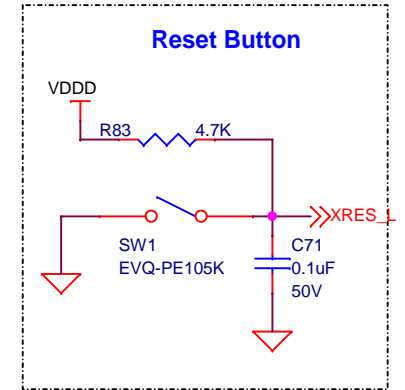
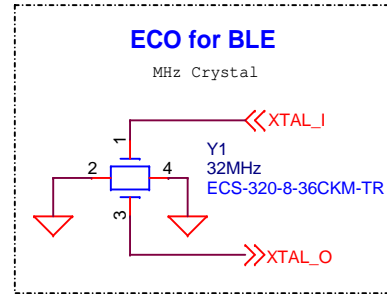
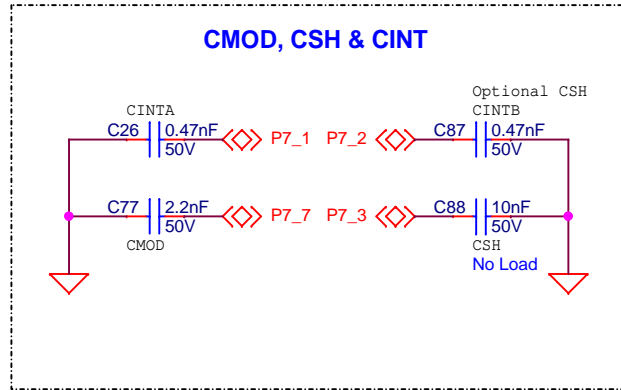
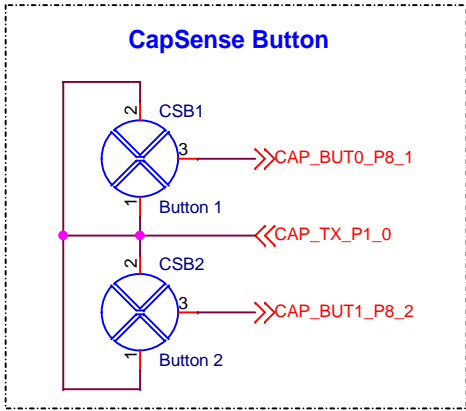
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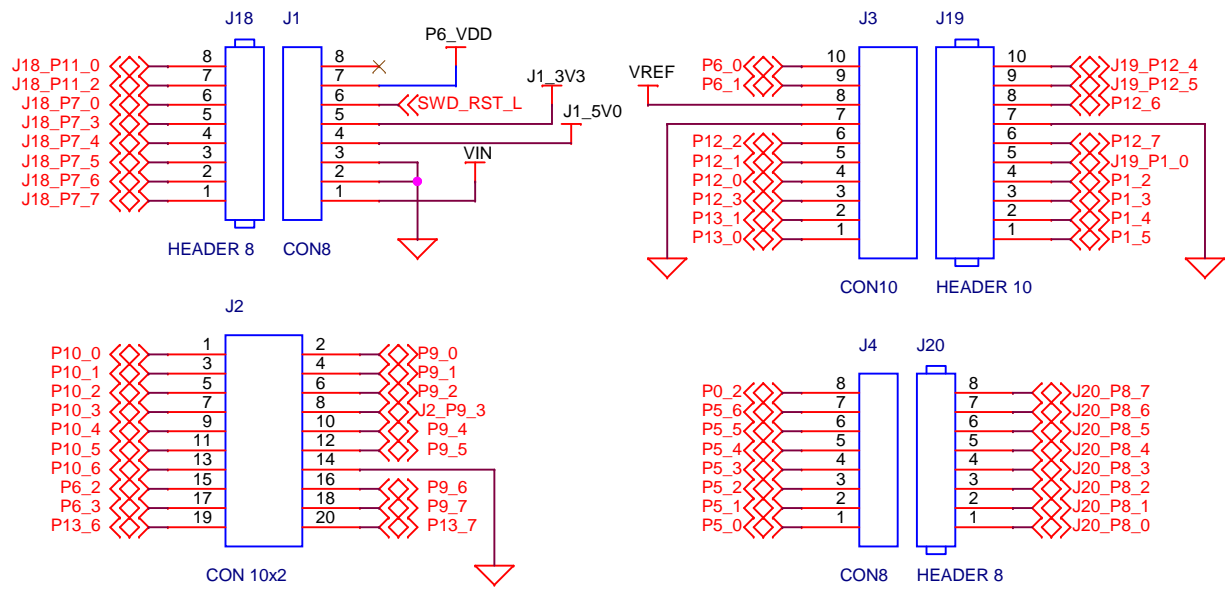


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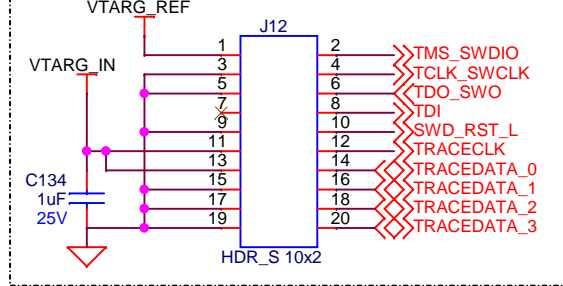
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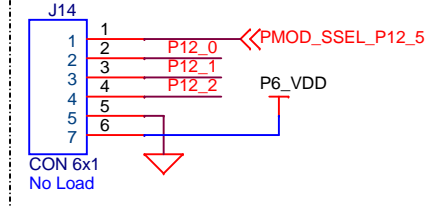
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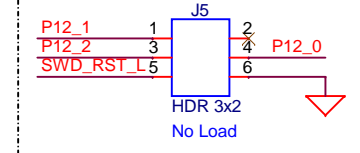
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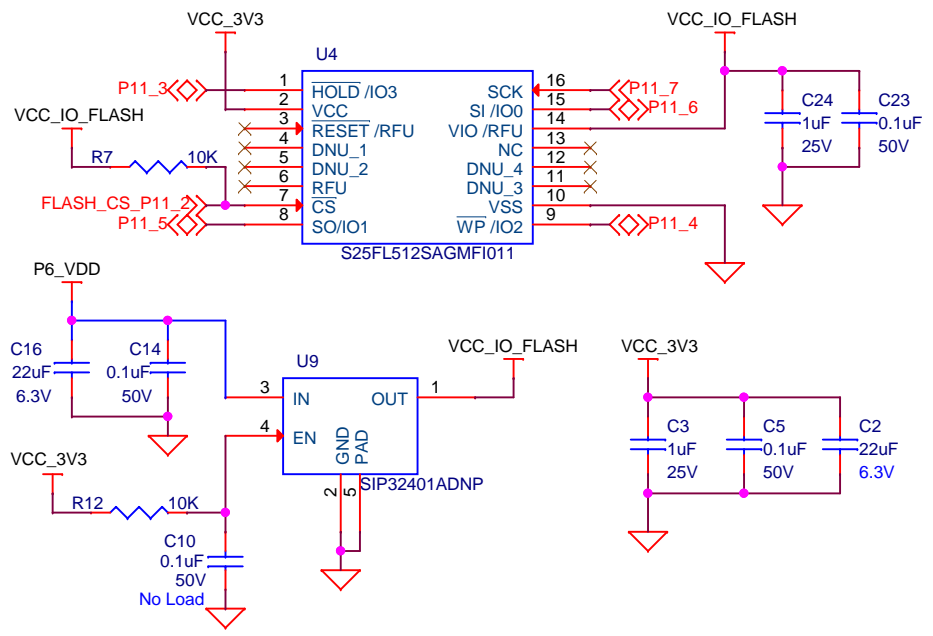
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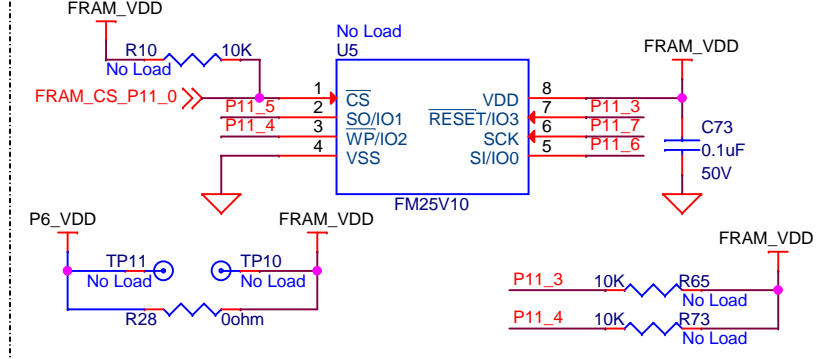
ICSP Header



QSPI Flash (SMIF)



F-RAM



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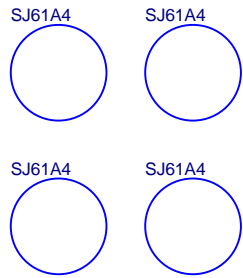
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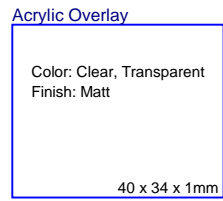
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Accessories

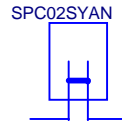
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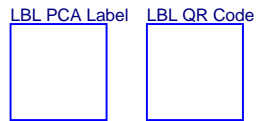
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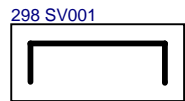
Jumper Shunt



PCBA label



USB connector bracket



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Revision History

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01	Initial internal release	08/29/2016
02	Internal release	10/03/2016
03	Internal release	11/25/2016
04	Initial external release under NDA	01/19/2017
05	3.3V protection diode changed to load SW (U59) Added PMIC control section (U58, U56, U57 and passives) Removed series resistor for SPI and UART HW flow control Voltage Monitoring domain and Protection Circuit o/p changed to P6_VDD Changed trace data line connection (to 9.3, 7.6, 7.5, 7.4) C22 Cap on VRF changed to 10uF Removed SW8 and connected CINT directly, CMOD connection changed to 7.7 Shield # changed to 13.6/6.3 Added additional LED on pin 13.7 and 1.5 Added option to change logic for user SW and added pull-up/down Back annotated from layout	5/2/2017



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