R23 Circuit Description

1 RF circuit

1.1 Main functions of RF circuit:

The baseband modulate the uplink signal, and then transmit it on RF carrier by the antenna; Demodulate the received wireless signal transmitted by the base station by the receiving circuit then get the forward signal; at the same time, provide the steady en-control 26MHz frequency source.

1.2 Structure of RF circuit:

We can divide it to 4 units according to the functions: Antenna unit, frequency synthesized unit, receiving unit, transmitting unit.

1.2.1 Antenna unit

Antenna unit is composed by antenna groupware, antenna switch and FEM RDA6232. This antenna groupware is the transceiver of the wireless signal that is composed by inside antenna, and could fetch up the disadvantages such as the low efficiency and the poor radiance direction by the high performance match. This phone has the antenna switch and diplexer. The antenna switch is used as the auto-test mechanical switch, which is located at the RF channel and parallel connected to the antenna. When producing and testing, it is connected to the test cable. Diplexer is used to isolate the received and transmitted signals, which can reduce the interference.

1.2.2 Frequency-synthesized unit

The AD6548 has a single fast-locking fractional synthesizer used for VCO control in both receive and transmit mode. The entire system including VCO, tank, fractional N dividers, sigma delta compensation, charge pump and loop filters are fully integrated. The only external

component is the frequency reference. The synthesizer is controlled via the serial interface. The VCO is fed into the respective dividers to generate the appropriate LO frequencies for the RX and TX bands.

Fractional N Dividers

The fractional N divider allows the PLL system to have a smaller step size than the comparison frequency which is set by the external reference to 26 MHz. This feature allows all the GSM frequency band raster to be achieved, with fast lock times and good phase noise characteristics.
The divider section consists of a dual modulus 8/9 prescaler, integer M & A dividers, and fractional N system based on sigma-delta modulation to generate the required fractional divide ratio. The Denominator of the fractional divider can be set to 3 different values, (1040, 1170, 1235), depending on the mode of operation. For example a denominator of 1040 with an input fraction F maintains an average value of F/1040 allowing 25 kHz steps when operated at a reference of 26 MHz.

Phase Frequency Detector/Charge Pump

A Phase Frequency Detector (PFD) is used for the PLL phase detector. The charge pump is designed such that good matching of up and down currents is achieved over a wide output operating range. The charge pump output is internally routed to the integrated synthesizer loop filter.

Synthesizer Loop filter

To minimize complexity of the external PCB layout the Main Synthesizer loop filter is also fully integrated into the IC. No external components or adjustments are required.

Voltage Controlled Oscillator

The integrated voltage controlled oscillator (VCO) is a complete self-calibrating subsystem. This employs a fully auto-mated digital self-calibration function to ensure optimum phase noise performance over the entire frequency range. The VCO generates frequencies between 2520MHz and 2985MHz as required to operate in the four GSM bands for RX and TX.

Reference Oscillator

The AD6548 requires only an external low cost crystal as the frequency

reference. The circuitry to oscillate the crystal and tune its frequency is fully integrated. For good noise immunity the oscillator is a balanced implementation requiring the crystal to be connected across 2 pins. There is a programmable capacitor array included for coarse tuning of fixed offsets (e.g. crystal manufacturing tolerance), and an integrated varactor for dynamic control. The oscillator is designed for use with a 26MHz crystal.

1.3. Transmitting unit

The transmit section of the AD6548 radio implements a translation loop modulator. This consists of a quadrature modulator, high speed phase-frequency detector (PFD) with charge pump output, loop filter, TX VCO and a feedback down converting mixer. The VCO output (divided by 2 for low band) is fed to the power amplifier with a portion internally fed back into the down-converting feedback mixer to close the feedback loop.
The Quadrature modulator takes the baseband I & Q signals and translates these into a GMSK signal at the Transmit Inter-mediate Frequency (TX IF). After bandpass filtering and limiting the TX IF signal is used as the reference input to the Phase Frequency Detector (PFD) of the transmit PLL.

Phase Frequency Detector (PFD)

The PFD ensures that the transmitted signal contains the required modulation and is accurately locked to the desired GSM channel. The downconverted feedback signal from the TX VCO and the Quadrature Modulator output are phase compared by the PFD. The PFD charge pump generates a current pulse proportional to the difference in phase which is applied to the loop filter.

Loop filter

To minimize complexity of the external PCB layout the TX loop filter is fully integrated into the IC. At power up the filter is automatically calibrated as part of the baseband filter cal, eliminating process tolerances. The calibration is fully integrated and requires no extra programming.

TX VCO

The Transmit Voltage Controlled Oscillator (TX VCO) and tank components are a fully integrated subsystem. The subsystem includes

PA drivers so the outputs are used to directly drive the external PAs. The low noise oscillator design and internal filtering mean that external TX SAW filters are not required. In Low band operation the TX VCO output is divided by two and filtered. The TX VCO is automatically calibrated to ensure optimum performance over its operating frequency of 1648 to 1910 MHz.

Feedback Down-Converting Mixer

The feedback down converting mixer is used to translate the TX VCO output frequency to the TX IF. An integrated band pass filter exists between the mixer and the PFD to filter the mixers unwanted side band and higher order mixing products.

Transmit Frequency Plan

Unlike many other translation loop modulators the AD6548 uses only a single VCO source to derive the local oscillator signal for both the Feedback Down-Converting Mixer and the Quadrature modulator.
This ratio was chosen to minimize VCO tuning range, TX IF frequency variation and ensure excellent transmit spectral mask performance.
The Feedback-Down Converting Mixer operates low side injection for the high bands and high side injection for the low bands. The final relationship between the transmitted TX frequency and the LO VCO frequency is different between the two bands.
These relationships are taken account of in the synthesizer architecture and programming.

1.4. Receiving unit
The AD6548 receiver section fully integrates all the RF and baseband signal processing. Each major block is described in the following sections.

Low Noise Amplifiers

The AD6548 includes four fully integrated Low Noise Amplifiers (LNAs), to support quad band applications without further external active components. The LNAs have differential inputs which minimize the effect of unwanted interferers. The inputs are easily matched to industry standard Front End Modules (FEMs) or discrete Rx SAW filters. The outputs of the LNAs are directly coupled to the down-converting mixers. The gain of the LNAs are typically 24 dB. Each LNA can be switch to a low gain mode when receiving large input signals as part of the AGC system.

Down-Converting Mixers

Two quadrature mixers are used to mix down the signals from the LNAs, one for the high bands (1800 and 1900 MHz) and one for the low bands (850 and 900 MHz). The outputs of the mixers are connected to the baseband section through an integrated single pole filter with nominal cut-off frequency of 800kHz. This acts as a "roofing filter" for the largest blocking signals (i.e. those ⩾ 3MHz) and prevents the baseband amplifiers from being overloaded.

Baseband Amplifiers / Low Pass Filters

The baseband amplifiers provide the majority of the analog receiver gain. The filtering is provided by an integrated 5th order Chebyshev filter giving the necessary adjacent channel and blocking filtering, it is also acting as an anti-alias filtering for Baseband IC's converters. A final low pass pole is possibly each of the baseband outputs via internal series resistor along with an external shunt capacitor. The external capacitor is not normally required with ADI baseband ICs. The on chip filter has an auto calibration feature ensuring that the filters are tuned for optimum performance.
The baseband amplifiers have programmable gain for system AGC. A total of 57 dB of gain control is provided in 3dB steps programmable over the serial interface. This together with the LNA gain control gives a total of 77dB of gain control range.
The receive baseband outputs are routed to the common Rx/Tx I/Q ports for connection with the baseband converters.

Baseband Output D.C. Offset Correction

In order to minimize D.C. offsets inherent in the receiver and maximize dynamic range a D.C offset correction circuit is integrated. This correction is triggered over the serial bus and then an offset tracking loop is enabled to minimize residual offsets under all conditions. The tracking loop is fully hardware integrated, requiring no software intervention.

Receiver Local Oscillator (LO) Generator

The Rx LO generator is used to avoid DC offset problems associated with LO leakage into the receiver RF path. By operating the VCO at a frequency other than the desired receive frequencies, any leakage of the VCO will fall out of band. The LO generator is used to convert the

offset synthesized VCO output to the on-frequency quadrature LO required by the chipset. The LO generator is implemented as a regenerative frequency divider, performing a 2/3 multiplication of the VCO output for the high band (DCS1800/PCS1900) and a 1/3 multiplication for low band (E-GSM 900/GSM850).

2. Digital base band circuit principle

2.1. General

The digital base band circuit is composed by central control and data processing unit, power management unit, voice processing unit, display unit and outside interface unit.

2.2. The circuit and principle of each unit

2.2.1. Central control and data processing unit

Platform

MT6253 is capable of running the ARM7EJ-S RISC processor at up to 104 MHz, thus providing fast data processing capabilities. In addition to the high clock frequency, a separate CODE cache is also added to further improve the overall system efficiency. For large amounts of data transfer, high performance DMA (Direct Memory Access) with hardware flow control is implemented, which greatly enhances the data movement speed while reducing MCU processing load.

External Memory Interface

To provide the greatest capacity for expansion and maximum bandwidth for data intensive applications such as multimedia features, MT6253 supports up to 4 external state-of-the-art devices through its 8/16-bit host interface. High performance devices such as Mobile SDRAM and Cellular RAM are supported for maximum bandwidth. Traditional devices such as burst/page mode flash, page mode SRAM, and Pseudo SRAM are also supported. For greatest compatibility, the memory interface can also be used to connect to legacy devices such as Color/Parallel LCD, and multi-media companion chips are all

supported through this interface. To minimize power consumption and ensure low noise, this interface is designed for flexible I/O voltage and allows lowering of the supply voltage down to 1.8V. The driving strength is configurable for signal integrity adjustment.

Radio Interface

MT6253 integrates a mixed-signal Baseband front-end in order to provide a well-organized radio interface with flexibility for efficient customization. It contains gain and offset calibration mechanisms, and filters with programmable coefficients for comprehensive compatibility control on RF modules. This approach also allows the usage of a high resolution D/A Converter for controlling VCXO or crystal, thus reducing the need for expensive TCVCXO. MT6253 achieves great MODEM performance by utilizing 14-bit high resolution A/D Converter in the RF downlink path. Furthermore, to reduce the need for extra external current-driving component, the driving strength of some BPI outputs is designed to be configurable.

2.2.2. External Memory

128Mb NOR FLASH +32Mb PSRAM

2.2.3. Power circuit

The input power management portion of its block accepts power from common sources —the main battery or an external charger — and generates all the regulated voltages needed to power the appropriate handset electronics. It monitors and controls the power sources detecting which sources are applied, verifying that they are within acceptable operational limits, and coordinates battery and coin cell recharging while maintaining the handset electronics supply voltages.

On-chip voltage regulators generate ten programmable output voltages using one switched-mode power supply and several low dropout voltage regulators, all derived from a common trimmed voltage reference.

The PM block includes one backlight or LED drivers with brightness (current) control that are intended for keypad and LCD lighting. A vibration motor driver alerts handset users of incoming calls.

2.2.4. DISPLAY

We use a 176*220 dot matrix 262k color TFT LCD module.

2.2.5. Bluetooth

We use RDA5875 as main Bluetooth transceiver IC. Its working mode or state is controlled by MT6253 via UART interface.