Content

Questions to be answered

(4) A brief description of the circuit functions of the device along with a statement describing how the device operates. This statement should contain a description of the ground system and antenna, if any, used with the device.

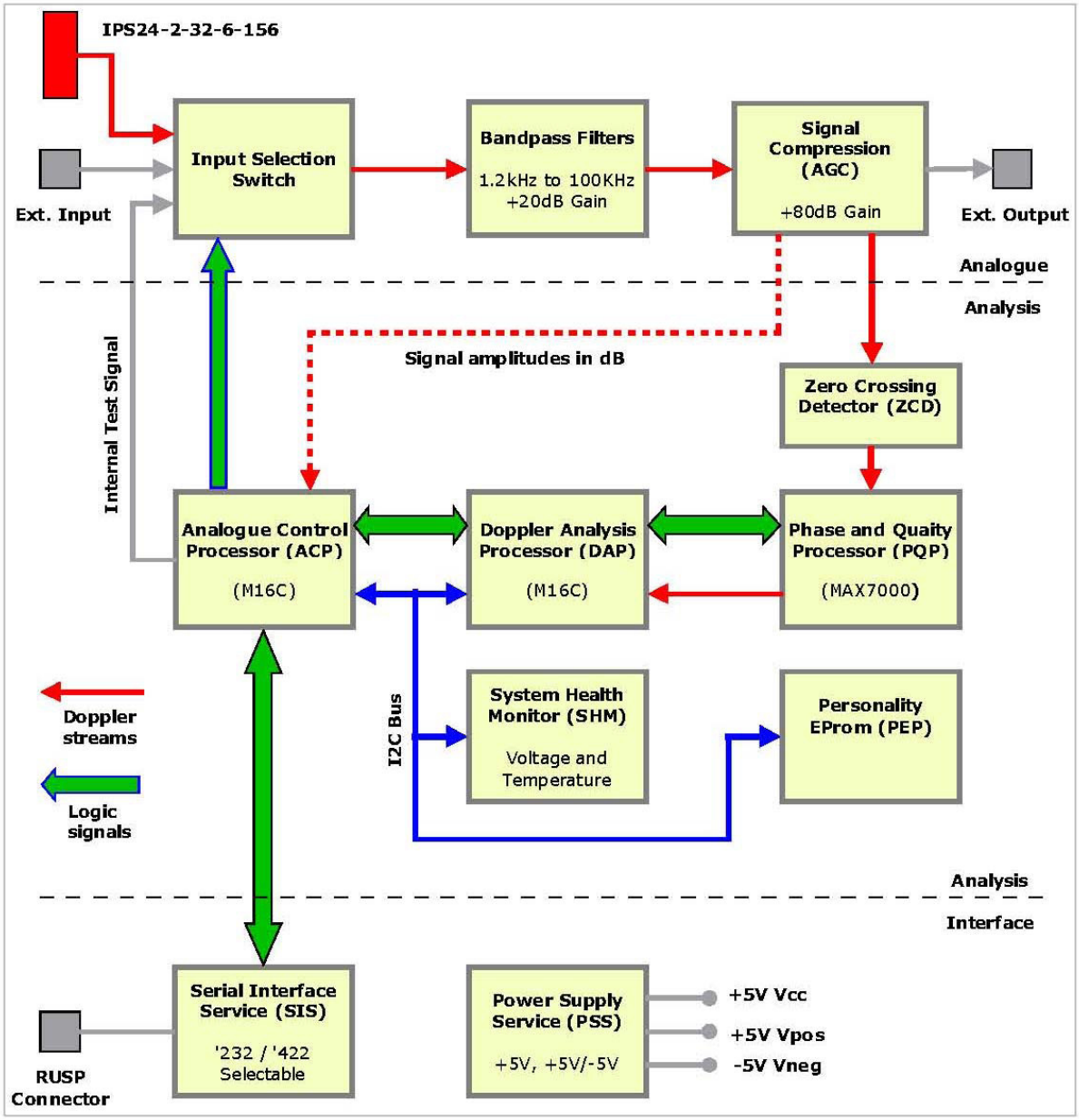
(5) A block diagram showing the frequency of all oscillators in the device. The signal path and frequency shall be indicated at each block. The tuning range(s) and intermediate frequency(ies) shall be indicated at each block. A schematic diagram is also required for intentional radiators.

RRS24F-S1 Hardware

The RRS24F-S1 is assembled on three printed circuit boards using predominately SMD technology. In the remainder of this document these boards are referred to as

- Analogue,
- Analysis and
- Interface.

The function of these boards is illustrated in Figure 1 and described in the remainder of this chapter.



Analogue

This board is mounted directly on Analysis and enclosed in a screening can. It receives the raw Doppler signals from the array and delivers filtered, amplitude compressed Doppler signals to Analysis.

Input Selection Switch

Used to select one of three possible inputs to Analogue.

- Raw Doppler signals from the array antenna
- An externally generated signal connected at the external input connector of the RADAR.
- An internally generated test signal provided by Analysis

Band Pass Filters

The band pass filter is realised as the cascade of a HP VCVS stage and a LP GIC stage. Both stages realise a C 05 20 % 30° response with a minimum design attenuation of 60 dB. These circuit topologies were chosen in order to assemble the filter using a single capacitor value with 5 % tolerance.

The VCVS input stage includes 26.8 dB gain. Combined with the 6 dB insertion loss of the output GIC stage the total gain is 20.8 dB. Using standard 1 % resistor values and 10 nF COG capacitors the -3 dB frequency of the two stages are 1164 Hz and 11.3 kHz.

Signal Compression (AGC)

The AGC stage is based on a variable gain amplifier with a gain-adjustment range of 0 dB to +80 dB. Its output is converted to a quasi D.C. voltage proportional to the true R.M.S. value of the amplified signal. An integrator drives the gain control input of the amplifier to minimise the difference between this R.M.S. related D.C. voltage and a fixed reference voltage of 0.45 V. When the difference at the integrator input becomes zero the signal at the amplifier output (and R.M.S. converter input) has a R.M.S. amplitude of 0.45 V, or 1.27 V pk-pk.

The amplifier gain control voltage is proportional to the amplifier gain required to achieve this level, and so inversely proportional to the input signal level. To implement a RSSI function the control voltage of both channels is regularly sampled by the Analogue Control Processor (ACP). The RUSP command EXOUT can make the compressed signal available at the External Output connector.

Analysis

This board accepts the filtered and compressed signal from Analogue and produces a qualified estimate of the true vehicle speed.

Zero Crossing Detector (ZCD)

It is required to identify the zero crossings of the incoming signal. The Doppler Analysis Processor will later measure the period between these zero crossings to determine the signal frequency and so estimate the vehicle speed.
To identify the zero crossings each channel includes a fast window comparator.

Phase and Quality Processor (PQP)

The PQP is a VHDL project implemented on a 128-macrocell MAX7000-series EPLD running at 4 MHz. It continuously monitors the amplitude and phase of the incoming signals from Analogue. When a valid signal is identified its current phase is posted and an interrupt request passed to DAP.

Doppler Analysis Processor (DAP)

The DAP is a C++ project implemented on a M16C/62 processor running at 16MHz. It handles the whole speed estimation activity from measurement of the period of the incoming signal to the generation of the final qualified speed estimate. Within DAP the period of input signal cycles is sampled with a resolution of 62.5 ns.
The C++ project is arranged as a background task that handles the speed estimation only. All other activities run in real-time, generating interrupt requests through the structure of the M16C. Interrupts are prioritised according to the
Requirements of the measurement cycle, but an interrupt request can itself not be interrupted. DAP is also the I2C bus master.

Analogue Control Processor (ACP)

The ACP monitors the gain control voltage from Analogue and so is aware of temporal variations in signal amplitude. Three signal amplitude thresholds are available. Each consists of an acquire level and a release level. Targets are recognised as they pass the acquire level and paused as they pass the release level. The current threshold is selected using the RUSP command RANGE.
A LED visible from the outside of the RADAR unit is activated by ACP whenever the signal level exceeds the current thresholds with the required phase.
The ACP also implements the RUSP interface. Incoming commands are interpreted by the ACP and either handled locally or passed to DAP over the I2C bus. Vehicle speed information is passed by DAP to ACP for assembly into a RUSP message and transmission to the host.

Personality EPROM (PEP)

The PEP consists of two serial memory devices connected to the I2C bus. The first, USER, receives all incoming RUSP commands. At unit activation the last valid RADAR measurement configuration is automatically reloaded.
The second, SYS, contains the RADAR system parameterisation. It is written by DAP at the first RESET following factory programming. It is subsequently accessible via the RUSP interface using a special command syntax, but only if a specific jumper in Analysis is first set and the power cycled.

System Health Monitor (SHM)

On the I2C bus. Should any supply voltage move outside of its specification then SHM sends an interrupts request to DAP which immediately aborts the current measurement cycle. It is then able to request the current voltage level on all three supply busses from SHM.
A temperature excursion similarly generates an interrupt request of DAP, which again aborts the current measurement cycle. DAP then shuts down Analogue (load reduction) and waits for the temperature to decrease. Should the temperature again fall below the reset threshold than a system reset is triggered, after which the host can restart traffic monitoring.

Interface

Interface represents the transition between the internal RADAR electronics and the external Host. Its printed circuit board includes a physical separation between these two sections. This barrier is maintained by isolating supply voltage converters and optical isolation components.

Power Supply Service (PSS)

PSS provides clean, stabilised power supply lines for the RADAR unit. They are fully isolated from the nominally 12V input supply line. The internal supply busses are as follows.

+5 V at a maximum current of 660 mA for the all digital components.
Revision 1

±5 V at a maximum current of 300 mA for the array antenna and Analogue.

The specified input voltage range is +9 V to +16 V. Absolute maximum voltage is 24 V of either polarity for extended periods without damage. The supply input is fused at 750 mA (self repairing). Nominal supply current in operation at 12 V is 250 mA.

A bimetallic fuse isolates the RADAR unit from the external supply at internal temperatures exceeding +90 °C.

Interface Service (SIS)

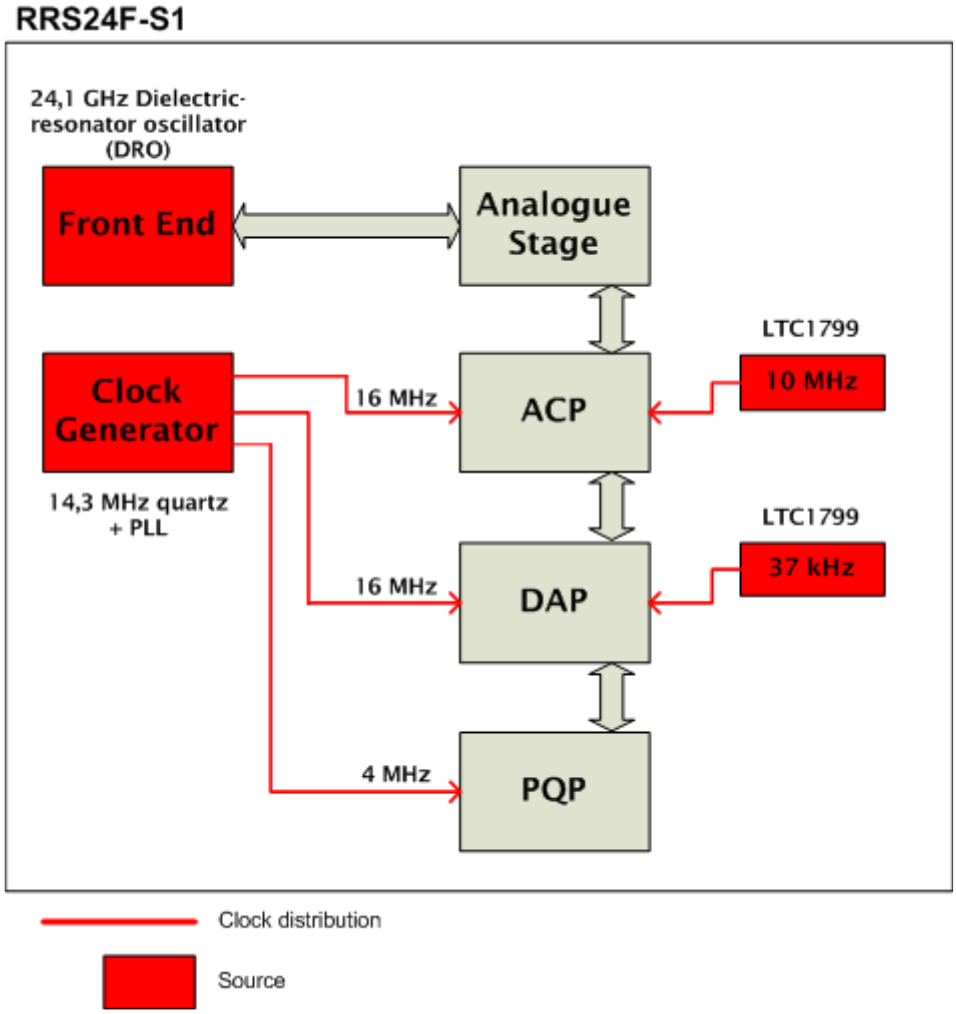
SIS is located on the Host side of Interface. It is powered by a separate non-isolating converter connected to the +12 V supply input. RUSP messages pass between SIS and ACP via optical isolation components.

SIS is configured to use a ‘232 or ‘422 interface dependent on the state of the #232-pin of the external RUSP connector.

#232 grounded: SIS provides a ‘232 interface.
#232 open: SIS provides a ‘422 interface.

In both modes of operation the interface runs at 19200 Baud, even parity, eight-bit data, one stop bit. (19200; E; 8; 1).

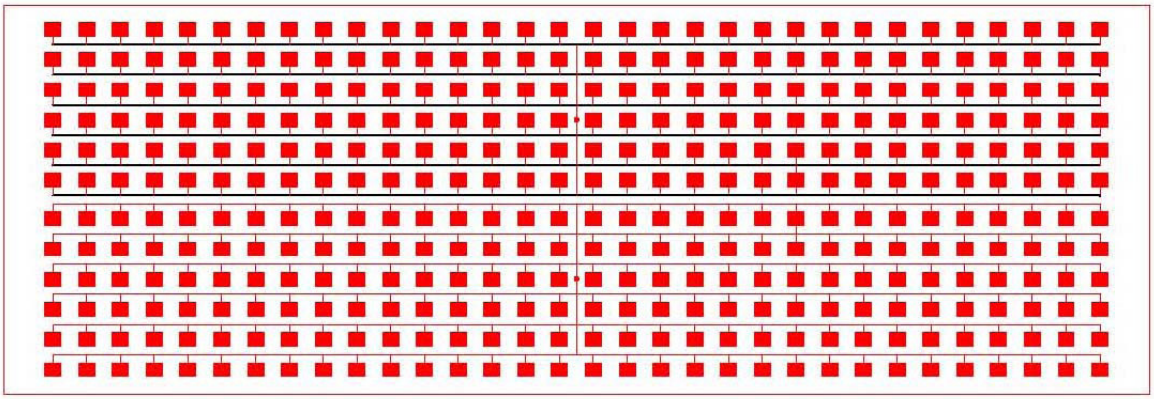
Frequency of all oscillators



Planar antenna

IPS24-2-32-6-156

The IPS24-2-32-6-156 is a planar antenna design incorporating a complete K-band transceiver. The array design is shown in here.



Description

- CW RADAR-transceiver centred at 24.100 GHz for fixed frequency operation
- advanced PHEMT-oscillator with low current consumption
- RF-pre-amplifier for lowest noise operation
- separate transmit and receive path for maximum gain
- stereo (dual channel) operation for direction of motion identification
- base-band amplifier, bandwidth limited for lowest noise performance

Electrical Characteristics

Parameter	Symbol	min	typ.	max.	units	comment
transmit frequency	f	24.075	24.100	24.125	GHz	meeting ETSI #300 440
output power (EIRP)	Pout			20	dBm	meeting ETSI #300 440
temperature drift	Df		250		kHz/°C	
antenna pattern	horizontal		5	6	deg	E-plane
	squinting angle		0		deg	E-Plane
	vertical		19	20	deg	H-plane
side lobe level	horizontal		-20	-20	dB	E-plane
	vertical		-20	-15	dB	H-plane
I/Q imbalance	amplitude			6	dB	
	phase	60	90	120	deg	
IF output	voltage offset		VCC/2		Volt	
IF-amplifier	gain		30		dB	
	bandwidth	400		10000	Hz	

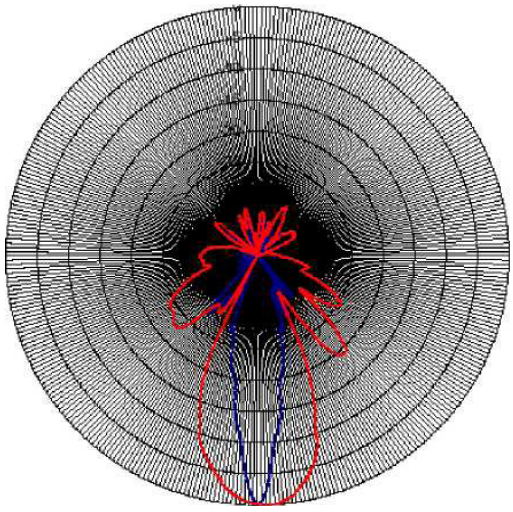
pos. supply voltage	Vpos		4.75	5.0	5.25	Volt	
pos. supply current	Ipos			65	80	mA	IF-amp. included
neg. supply voltage	Vneg		-5.25	-5.0	-4.75	Volt	
neg. supply current	Ineg			10	20	mA	
operating temperature	Top		-20		+60	°C	
outline dimens.		263.0x110.4x12				mm	

Beam Form

IPS24-2-32-6-156
S.N. 156000029

3dB-width
H-plane: 5,0°
E-plane: 20,3°

Side lobes
H-plane: -27,0 dB
E-plane: -19,0 dB



Cartesian Representation