User Manual

LILLY-9 1X V1.2

Version 2.0 English

Table of contents:

Änderungshistorie

Version	Datum	Bearbeiter	Änderung
1.0	31.10.2005	JT	Erste Ausgabe
1.1	13.03.2006	JT	Ergänzungen
1.2	29.03.2006	SK	Ergänzungen
2.0	09.04.2009	JT	Ergänzungen

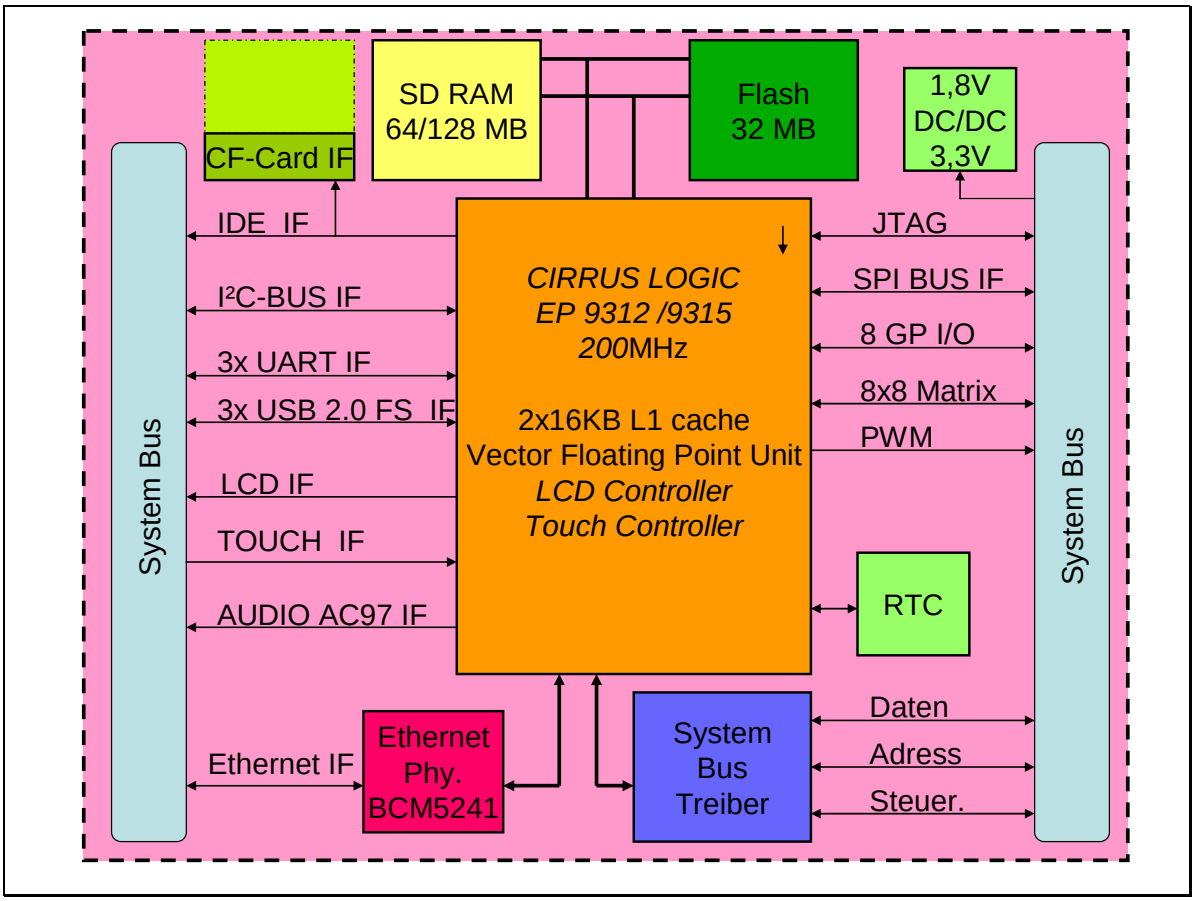
System on Module (SoM) TYP LILLY9 XX V1.2

1. Technical Data

1.1. Generally

The SoM „**LILLY-9 XX**“ is a CPU- Core module which bases on the ARM920T of the family of CIRRUS logic EP93xx.
This Core Modules differ by its CPU-achievement and periphery. By the common system plugs, which are same at all modules of their occupancy and mechanical position, the modules can be exchanged under each other. At this LILLY-9 15 SoM forms an exception the plug J1B is armed with 140 pins. These extended pins contain the PCMCIA signals which exist only on the **LILLY-9 15** Module.

1.2. Schematic LILLY-912



Schematic : LILLY-912 Modul

On the LILLY-912 Modul there are following oszillators:

1. CPU 14,7456 MHz
2. CPU interne RTC 32,768kHz
3. Ethernet 25.000MHz
4. Externer RTC 32,768kHz

These **LILLY-9 XX** Modules are available in the following variants:

1.3. Interfaces and functions

	LILLY-9 15	**LILLY-9 12**		**LILLY-9 07**	**LILLY-9 02**	**LILLY-9 01**
CPU	EP9315	EP9312		EP9307	EP9302	EP9301
Przessor MHz	200	200		200	200	166
Systembus MHz	100	100		100	100	66
Mat. CoProzessor	1	1		1	1	0
Serielle TTL	3	3		3	2	2
SPI- Bus	1	1		1	1	1
I²C- Bus	1	1		1	1	1
IrDA	1	1		1	1	1
USB2.0 low-speed / full-speed Host	3	3		3	2	2
PS/2-Keyboard	1	1		0	0	0
Matrixkeyboard	8X8	8X8		8X8	0	0
GPIOs	8	8		8	8	8
Graphic IF	1	1		1	0	0
LCD - TFT/STN	1/1	1/1		1/1	0/0	0/0
Resistiver Touch IF	4-8Wire	4-8Wire		4-8Wire	0	0
Multiplexer	8	8		8	5	5
ADC	12 bit	12 bit		12 bit	12 bit	12 bit
AC´97	1	1		1	1	1
EIDE	1	1		0	0	0
Compact Flash Slot	1	1		0	0	0
Ethernet 10/100 Mbps	1	1		1	1	1
PCMCIA	1	0		0	0	0
PWM	1	2		2	2	2
GPIO's	Ja	Ja		Ja	Ja	Ja
PWM	1	2		2	2	2
JTAG	1	1		1	1	1
System-Bus	1	1		1	1	1
Supply Voltage	3,3V , 5V	3,3V , 5V		3,3V	3,3V	3,3V

1.4. CPU / Memory

	LILLY-915	**LILLY-912**		**LILLY-907**	**LILLY-902**	**LILLY-901**
CPU	EP9315	EP9312		EP9307	EP9302	EP9301
MHz	200	200		200	200	166
S DRAM	32 / **64**/128	32 / **64**/128		32 / **64**/128	**32** / 64	**32** / 64
Flasch	8/**16**/32	8/**16**/32		8/**16**/32	8/**16**/32	8/**16**/32

1.5. Supply

- 5 V - ca. mA only for Compact Flash/ can connect to 3.3 V
- 3.3 V - ca. 350 mA

1.6. Total weight / measures

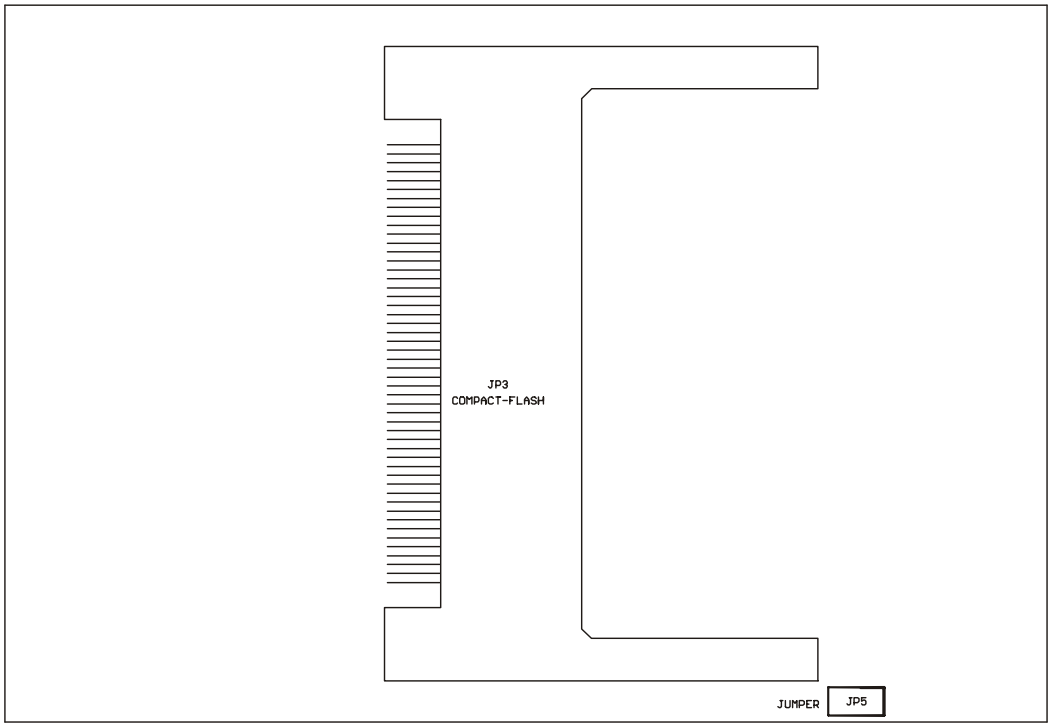
- Total weight: approx. 20 g
- Measures L = 74, B = 51, H = 12 mm

1.7. Temperature range

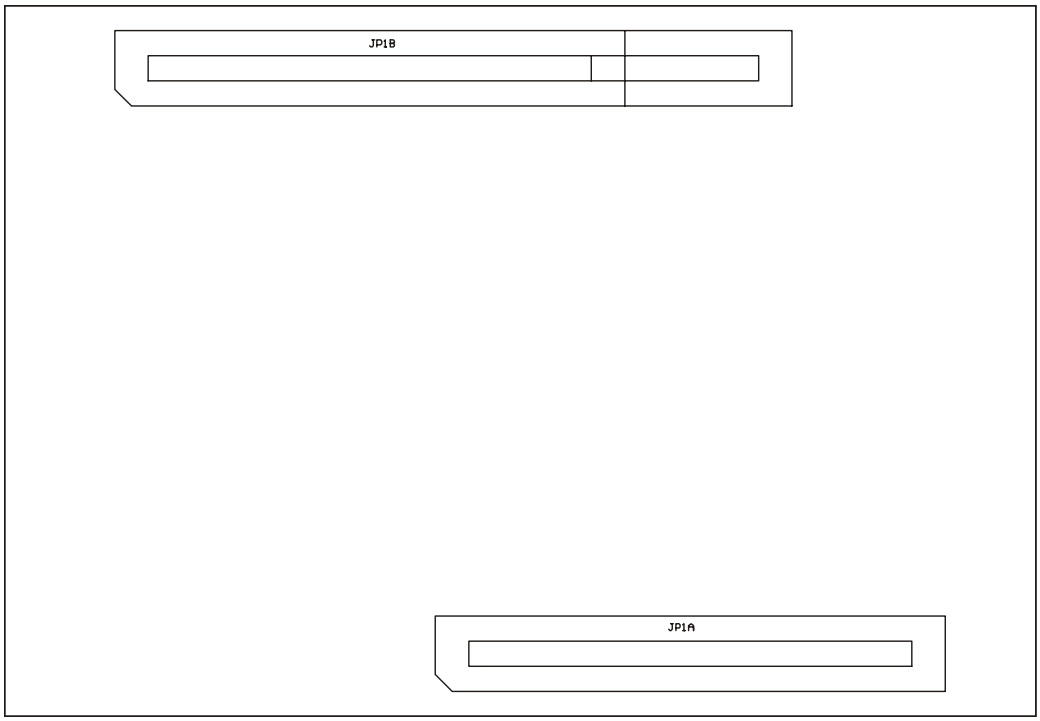
- Standard: 0..70 °C
- Industrial: -40..85°C (184MHz) optional

2. View

2.1. View of component side



2.2. View of solder side



3. Pin allocation

3.1. JP1A and JP1B System bus plug

PIN	JP 1B	Bez.		JP1A	Bez.
1	GND	Masse		VCC_BAT	Batterie Spannung
2	GND	Masse		GND	Masse
3	SCLK	Pixel clock in/out		TFTDCK	TFTShiftClock
4	SFRM	SPI Frame Clock		TFTDE	TFTData Enebel
5	SSPRX	SPI input		HSYNC	HSYNC
6	SSPTX	SPI output		VSYNC	VSYNC
7	BIT_CLK	AC97 bit clock		TFTB0	TFTBlueData0
8	AC97RST	AC97 reset		TFTB1	TFTBlueData1
9	SYNC	AC97 sync		TFTB2	TFTBlueData2
10	SDA_OUT	AC97 output		TFTB3	TFTBlueData3
11	SDA_IN	AC97 input		TFTB4	TFTBlueData4
12	TCLK	JTAG clock in		TFTB5	TFTBlueData5
13	TDI	JTAG data in		TFTG0	TFTGreenData0
14	TDO	JTAG data out		TFTG1	TFTGreenData1
15	TMS	JTAG test mode select		TFTG2	TFTGreenData2
16	TRST	JTAG reset		TFTG3	TFTGreenData3
17	GPIO1	General Purpose IO1		TFTG4	TFTGreenData4
18	GPIO4	General Purpose IO4		TFTG5	TFTGreenData5
19	GPIO5	General Purpose IO5		VCC3	VCC 3,3V
20	GPIO6	General Purpose IO6		VCC3	VCC 3,3V
21	GPIO8	General Purpose IO8		TFTR0	TFTRedData0
22	GPIO9	General Purpose IO9		TFTR1	TFTRedData1
23	GPIO10	General Purpose IO10		TFTR2	TFTRedData2
24	PWM2	Pulse Width Modulation out2		TFTR3	TFTRedData3
25	SLA0	Flash programming voltage control		TFTR4	TFTRedData4
26	/RESIN	Reset in		TFTR5	TFTRedData5
27	SLA1	Flash programming voltage control		PWM1	Pulse Width Modulation out1
28	RESET	Reset out		VCC	VCC 5V
29	KBDATA	KeyboardData		XP	Touch
30	KBCLK	KeyboardClock		SXP	Touch
31	VCC3	VCC 3,3V		XM	Touch
32	VCC3	VCC 3,3V		SXM	Touch
33	ROW0	Key matrix row outputs		YP	Touch
34	COL0	Key matrix column inputs		SYP	Touch
35	ROW1	Key matrix row outputs		YM	Touch
36	COL1	Key matrix column inputs		SYM	Touch
37	ROW2	Key matrix row outputs		GND	Masse
38	COL2	Key matrix column inputs		GND	Masse
39	ROW3	Key matrix row outputs		/RESET	Reset
40	COL3	Key matrix column inputs		UIDE_D8	IDE Data8

PIN	JP 1B	Bez.		JP1A	Bez.
41	ROW4	Key matrix row outputs		UIDE_D7	IDE Data7
42	COL4	Key matrix column inputs		UIDE_D9	IDE Data9
43	ROW5	Key matrix row outputs		UIDE_D6	IDE Data6
44	COL5	Key matrix column inputs		UIDE_D10	IDE Data10
45	ROW6	Key matrix row outputs		UIDE_D5	IDE Data5
46	COL6	Key matrix column inputs		UIDE_D11	IDE Data11
47	ROW7	Key matrix row outputs		UIDE_D4	IDE Data4
48	COL7	Key matrix column inputs		UIDE_D12	IDE Data12
49	GND	Masse		UIDE_D3	IDE Data3
50	GND	Masse		UIDE_D13	IDE Data13
51	B_MD0	Buffered Data Bus IO0		UIDE_D2	IDE Data2
52	B_MD1	Buffered Data Bus IO1		UIDE_D14	IDE Data14
53	B_MD2	Buffered Data Bus IO2		UIDE_D1	IDE Data1
54	B_MD3	Buffered Data Bus IO3		UIDE_D15	IDE Data15
55	B_MD4	Buffered Data Bus IO4		VCC	VCC 5V
56	B_MD5	Buffered Data Bus IO5		VCC	VCC 5V
57	B_MD6	Buffered Data Bus IO6		UIDE_D0	IDE Data0
58	B_MD7	Buffered Data Bus IO7		UIDE_DRQ	IDE DMA Request
59	B_MD8	Buffered Data Bus IO8		/UIDE_IOW	IDE Write
60	B_MD9	Buffered Data Bus IO9		/UIDE_IOR	IDE Read
61	B_MD10	Buffered Data Bus IO10		/UIDE_IORDY	IDE IOReady
62	B_MD11	Buffered Data Bus IO11		/UIDE_DACK	IDE DMA Ack
63	B_MD12	Buffered Data Bus IO12		UIDE_INT	IDE Interrupt
64	B_MD13	Buffered Data Bus IO13		UIDE_A1	IDE Adresse1
65	B_MD14	Buffered Data Bus IO14		UIDE_A0	IDE Adresse0
66	B_MD15	Buffered Data Bus IO15		/UIDE_PDIAG	IDE PDIAG
67	VCC3	VCC 3,3V		/UIDE_CS0	IDE Chip Select0
68	VCC3	VCC 3,3V		UIDE_A2	IDE Adresse2
69	B_MA0	Buffered Adress Bus 0		/UIDE_DASP	IDE DASP
70	B_MA1	Buffered Adress Bus 1		/UIDE_CS1	IDE Chip Select1
71	B_MA2	Buffered Adress Bus 2		EECLK	EEPROM/Two-wire Interface clock
72	B_MA3	Buffered Adress Bus 3		EEDAT	EEPROM/Two-wire Interface data
73	B_MA4	Buffered Adress Bus 4		GND	Masse
74	B_MA5	Buffered Adress Bus 5		GND	Masse
75	B_MA6	Buffered Adress Bus 6		USBD0+	USBData0+
76	B_MA7	Buffered Adress Bus 7		USBD1+	USBData1+
77	B_MA8	Buffered Adress Bus 8		USBD0-	USBData0-
78	B_MA9	Buffered Adress Bus 9		USBD1-	USBData1-
79	B_MA10	Buffered Adress Bus 10		USBD2+	USBData2+
80	B_MA11	Buffered Adress Bus 11		TXD+	Transmit/IrDA +
81	B_MA12	Buffered Adress Bus 12		USBD2-	USBData2-
82	B_MA13	Buffered Adress Bus 13		TXD-	Transmit/IrDA -
83	B_MA14	Buffered Adress Bus 14		LED1	LED1
84	B_MA15	Buffered Adress Bus 15		RXD+	Receive +
85	GND	Masse		LED2	LED2
86	GND	Masse		RXD-	Receive -

PIN	JP 1B	Bez.		JP1A	Bez.
87	B_/WR	Buffered Write		TXD0	Transmit out
88	B_/RD	Buffered Read		RXD0	Receive in
89	B_DQM0	Buffered data mask0		/CTS0	Clear to send
90	B_DQM1	Buffered data mask1		/DSR0	Data set ready/
91	/CS0	Chip Select0		VCC3	VCC 3,3V
92	/CS1	Chip Select1		VCC3	VCC 3,3V
93	/CS2	Chip Select2		/DTR0	Data Terminal Ready
94	/CS3	Chip Select3		/RTS0	Ready to send
95	INT0	Interrupt0		/RI0	ReadIO
96	INT1	Interrupt1		TXD1	Transmit/IrDA output
97	INT2	Interrupt2		RXD1	Receive/IrDA input
98	INT3	Interrupt3		TXD2	Transmit
99	VCC3	VCC 3,3V		RXD2	Receive
100	VCC3	VCC 3,3V		TEN	TransmitEnable
101	NC	not connected	Pin allocation only for LILLY - 9 15		
102	NC	not connected			
103	NC	not connected			
104	NC	not connected			
105	NC	not connected			
106	NC	not connected			
107	NC	not connected			
108	NC	not connected			
109	B_MA16	Buffered Adress Bus 16			
110	B_MA17	Buffered Adress Bus 17			
111	B_MA18	Buffered Adress Bus 18			
112	B_MA19	Buffered Adress Bus 19			
113	B_MA20	Buffered Adress Bus 20			
114	B_MA21	Buffered Adress Bus 21			
115	B_MA22	Buffered Adress Bus 22			
116	B_MA23	Buffered Adress Bus 23			
117	B_MA24	Buffered Adress Bus 24			
118	B_MA25	Buffered Adress Bus 25			
119	NC	not connected			
120	NC	not connected			
121	/MCDIR	Data transceiver direction control			
122	/MCDEN	Address bus transceiver enable			
123	/MCAEN	Data bus transceiver enable			
124	/MCEL	Memory card low byte select			
125	/MCEH	Memory card high byte select			
126	/MCREG	Memory card register			
127	/MCWAIT	Wait Input			
128	/MCRST	Card reset			
129	/MCR	Memory card read			
130	/MCW	Memory card write			
131	/IOR	IO Read			

PIN	JP 1B	Bez.		JP1A	Bez.
132	/IOW	IO Write	Pin belegung nur für LILLY - 9 15		
133	MCBVD2	Voltage detection			
134	MCBVD1	Voltage detection/status change			
135	MCD2	Card detect 2			
136	MCD1	Card detect 1			
137	VS2	Voltage sense 2			
138	VS1	Voltage sense 1			
139	WP	Write protect			
140	READY	Ready			

3.2. JP5 BOOTMODE

open: Boot from flash
closed: Serialboot

4. Dimensioning

4.1. Measure drawing circuit board

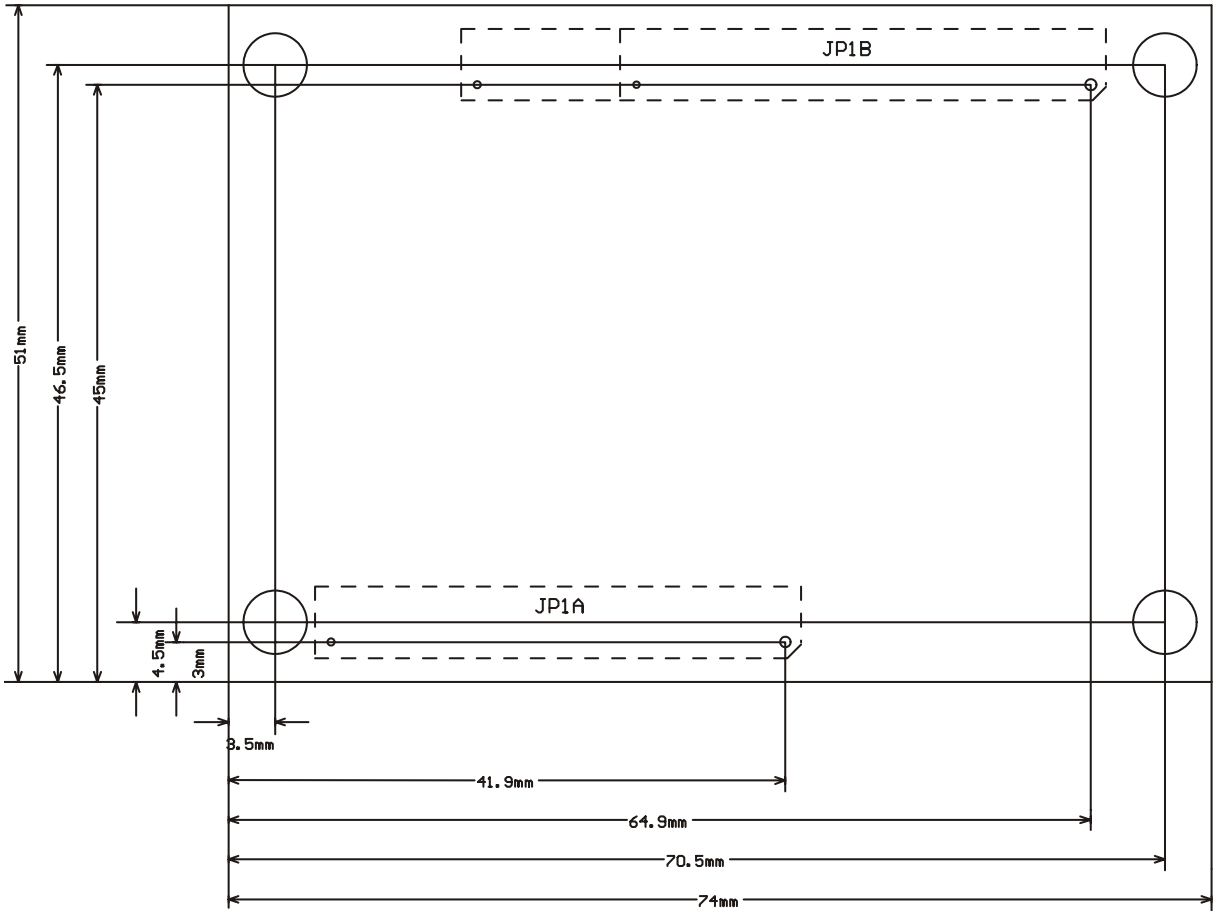


Illustration 1

5. Software

The Software is described in it's own Document
HB_2336_ARM-Linux-WinCE on the CD.