NOTES: (UNLESS OTHERWISE SPECIFIED)

*** Top ***

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
V7.0	Updated 0402 footprints per SUGA specification	Oct 7, 2013	Paul Clegg
V8.0	Disconnected GE_MDC & GE_MDIO, Fixed missing trace	07-NOV-2013	Paul Clegg
V9.0	Changed diameter of TP1-TP10	07-JAN-2014	Paul Clegg
V10.0	Deleted U3 & U7, R13 & R21 to 15 Ohm, R10 R15 R20 R28 to 300 Ohm	12-MAR-2014	Paul Clegg
V10.0 cont.	Added R55 & TS13	12-MAR-2014	Paul Clegg
V11.0	Changed diameter of TS13, Fixed pads of R10 R14 R15 R20 R21 R28	21-MAR-2014	Paul Clegg

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Revision History

Revision	Date	Changes
V1.0.0	Aug 30, 2011	Preliminary release.
V2.0.0	Nov 28, 2011	Changed LAN jack.
V3.1.0	May 2, 2013	Changed RF front end circuit. Added U2, U6.
		Added C20 (5.6pF), L3 (39nH).
		Changed value of R206, C501, R33~R37, R207, C1.
V5.0	10-Sep-2013	Initial Altium Design
V6.0	24-Sep-2013	Updated 0402 footprints, rotated U3 & U6, added testpoints

PCB stack-up for fabrication

Layer	Name	Assignment
1	Top	Components, CPU, DDR
2	GND1	Ground Plane
3	SIG1	Signal Layer
4	PWR	3.3VDC Plane
5	SIG2	Signal Layer
6	SIG3	Signal Layer
7	GND2	Ground Plane
8	Bottom	Components

PCB requirements

Dimension: See PCB Fab drawing
Thickness: 1.6mm
Number of layers: 8
Copper thickness: 1oz top & bottom; 0.5~1oz all internal layers.
Material: FR4
Surface treatment: immersion gold plated.
Minimum wire width: 3.5mil (Layer_2, Layer_5), 5mil other layers
Minimum wire spacing: 5mil
Minimum via hole diameter: 8mil

Unless otherwise specified:

Resistors are SMD(0402), +/-5%, 1/16W
Resistors specified as SMD(0603) are +/-5%, 1/10W
Resistors specified as SMD(0805) are +/-5%, 1/8W
Ceramic capacitors >= 10uF are SMD(0805)
Ceramic capacitors >= 0.22uF, <10uF, are SMD(0603)
Ceramic capacitors <= 0.1uF are SMD(0402)
Ceramic and Electrolytic capacitors are 6.3V or higher
Ferrite beads are SMD(0603).

UNLESS OTHERWISE NOTED ALL DIMENSIONS ARE INCHES [MM]:

TOLERANCES:
DECIMALS
.XX±.01 [.3]
.XXX±.005 [.13]
ANGLES: ±0.5
ROUNDNESS:±.005 [.13]
FLATNESS: ±.005 [.13]
CONCENTRICITY:±.005 [.13]

MATERIAL:

FINISH:

CAD OPERATOR: Paul Clegg	DATE: 21-MAR-2014	
CHECKED: Paul Clegg	DATE: 21-MAR-2014	
APPROVED: Paul Clegg	DATE: 21-MAR-2014	

SUGA ELECTRONICS LTD.

TITLE: Wifi Module SCHEMATIC DIAGRAM
Model SWP23MA-3

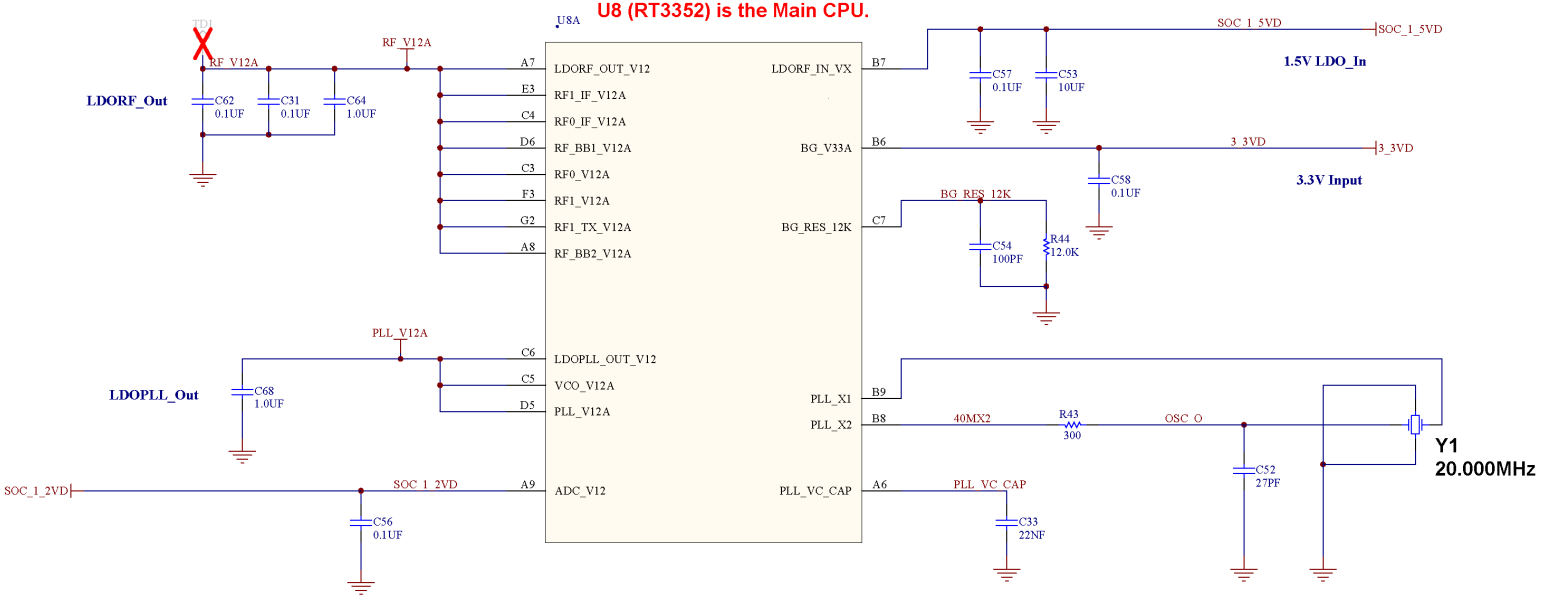
SIZE: B		PART NO.: 28-600006-001	REV.: V11.0
SCALE: NONE	DO NOT SCALE DRAWING	DRAWING NO.: 78-600006-001	SHEET: 1 OF 21

*** CPU_1 ***

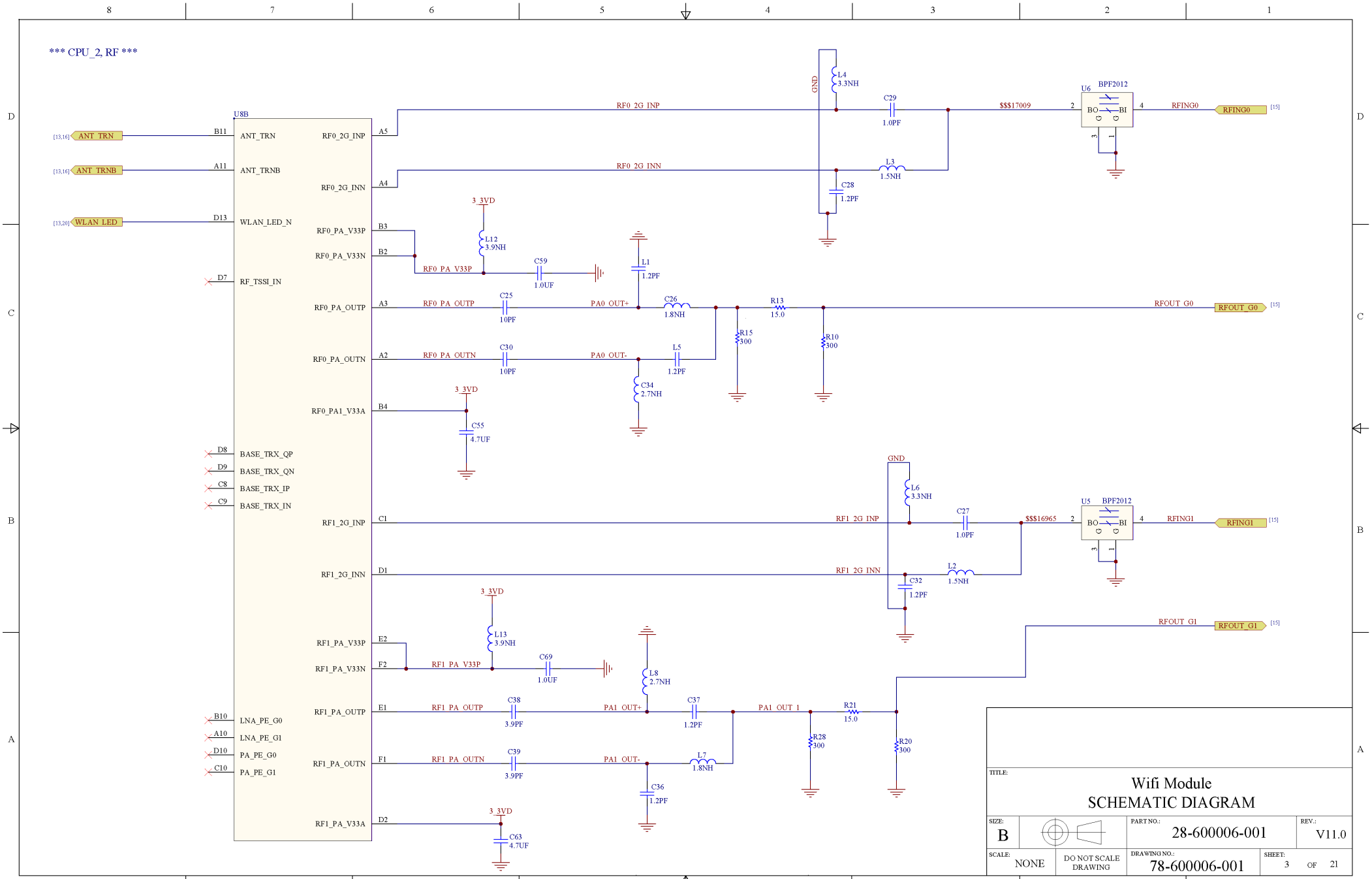
Pin LDORF_OUT_V12 is RF_V12A output.

Pin LDOPLL_OUT_V12 is PLL_V12A output.

U8 (RT3352) is the Main CPU.



TITLE: Wifi Module SCHEMATIC DIAGRAM			
SIZE: B		PART NO.: 28-600006-001	REV.: V11.0
SCALE: NONE	DO NOT SCALE DRAWING	DRAWING NO.: 78-600006-001	SHEET: 2 OF 21



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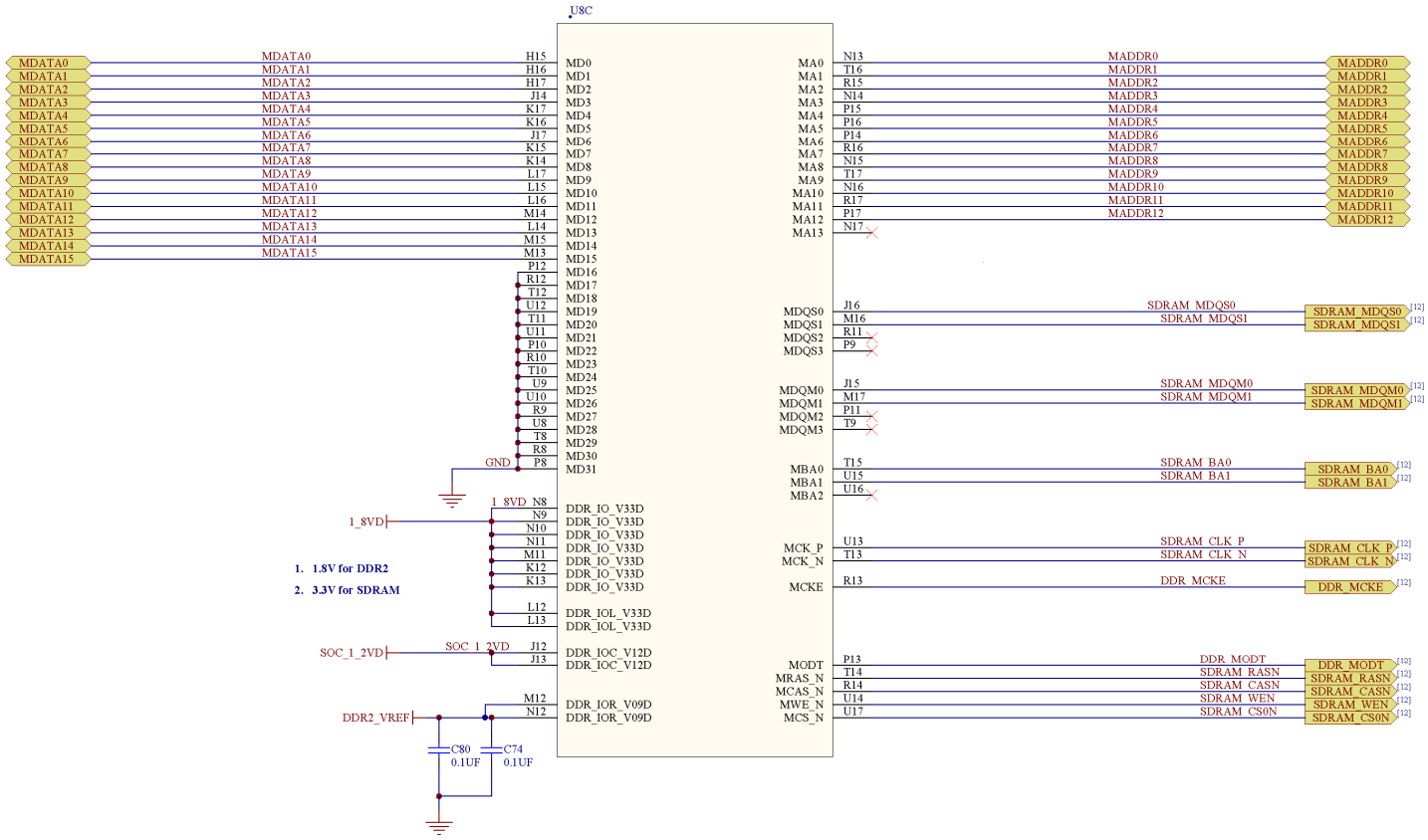
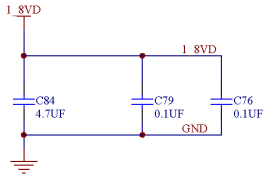
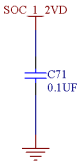
SIZE: B	PART NO.: 28-600006-001
REV.:	V11.0
SCALE: NONE	DO NOT SCALE DRAWING
DRAWING NO.:	78-600006-001
SHEET:	3 OF 21

*** CPU_3, DDR I/F ***



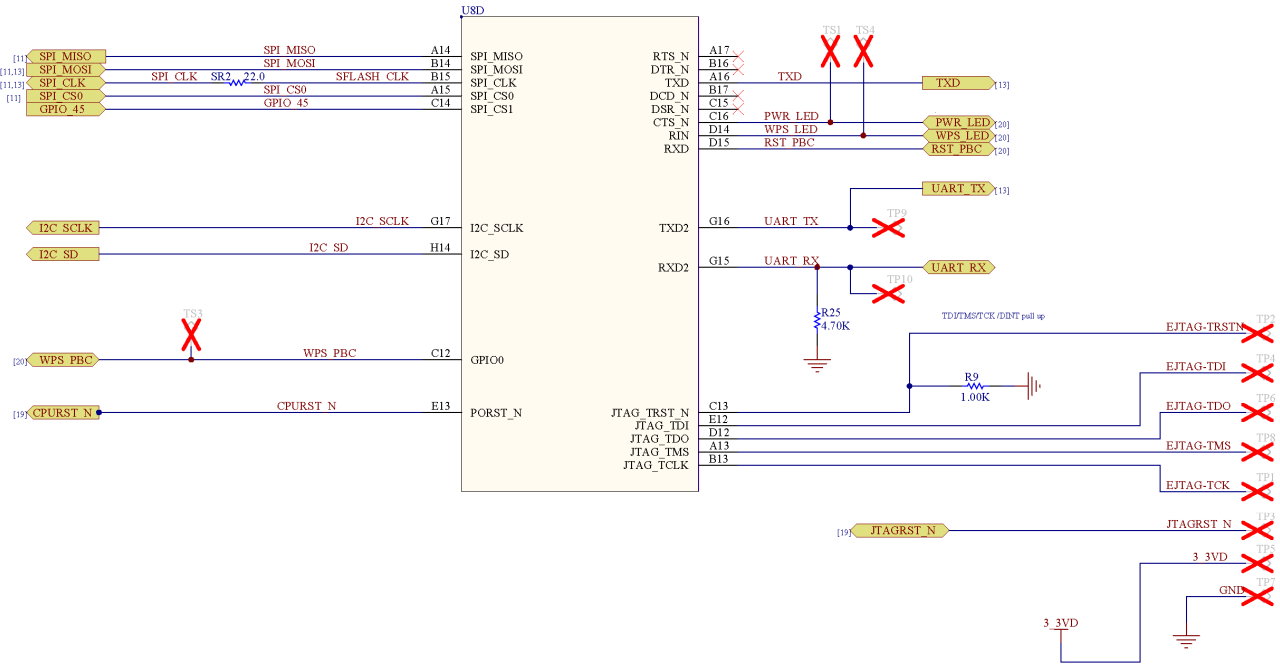




TITLE:
Wifi Module
SCHEMATIC DIAGRAM

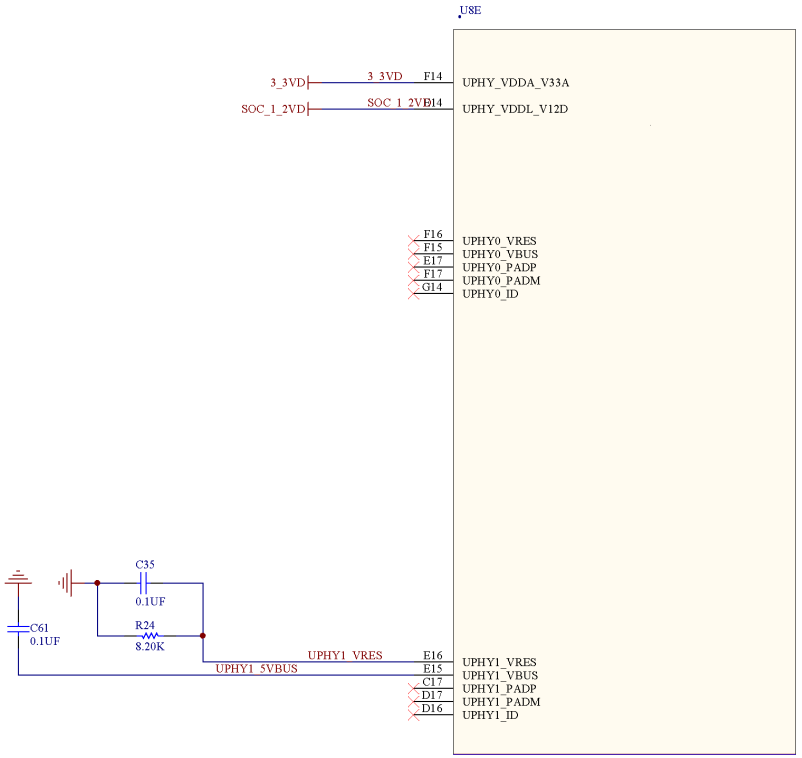
SIZE:		PART NO.:	REV.:
B		28-600006-001	V11.0
SCALE: NONE	DO NOT SCALE DRAWING	DRAWING NO.: 78-600006-001	SHEET: 4 OF 21

*** CPU_4 ***



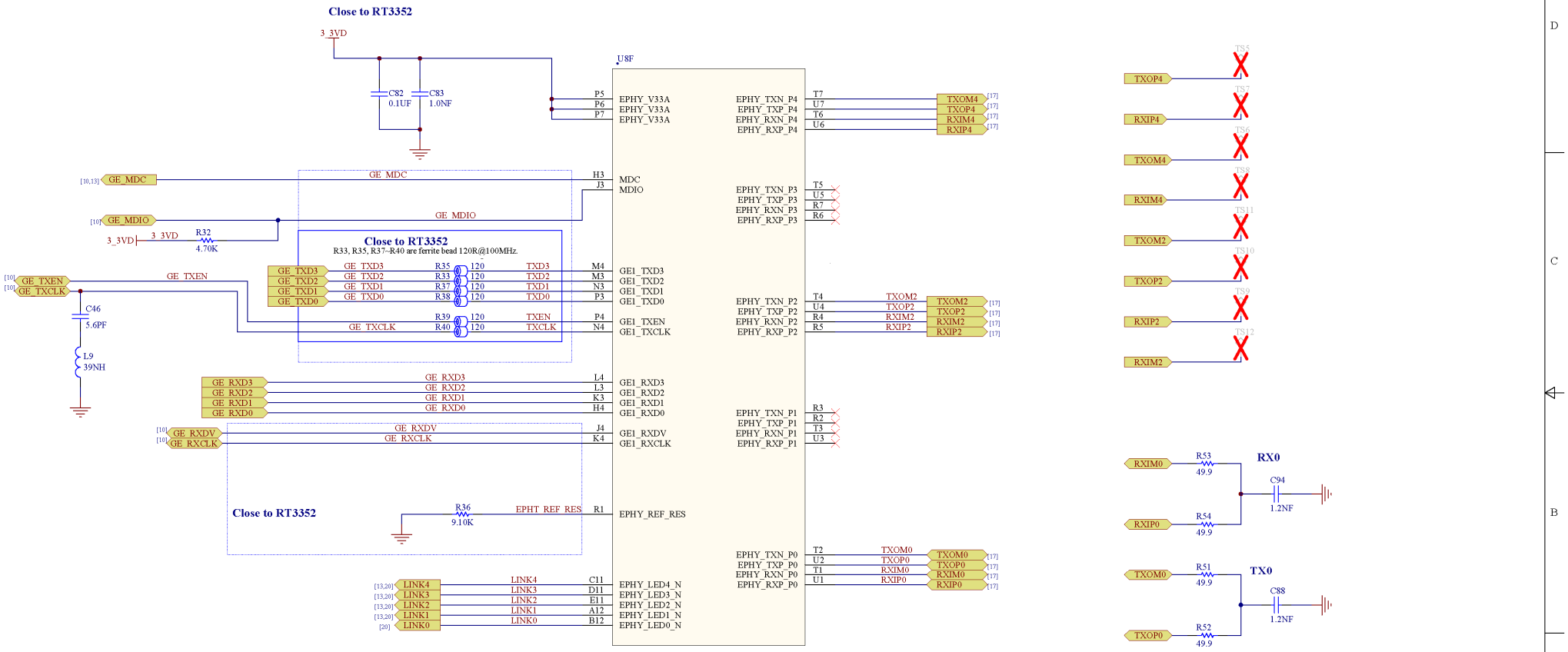
TITLE: Wifi Module SCHEMATIC DIAGRAM			
SIZE: B		PART NO.: 28-600006-001	REV.: V11.0
SCALE: NONE	DO NOT SCALE DRAWING	DRAWING NO.: 78-600006-001	SHEET: 5 OF 21

*** CPU_5, USB I/F ***



TITLE: Wifi Module SCHEMATIC DIAGRAM			
SIZE: B		PART NO.: 28-600006-001	REV.: V11.0
SCALE: NONE	DO NOT SCALE DRAWING	DRAWING NO.: 78-600006-001	SHEET: 6 OF 21

*** CPU_6, LAN I/F ***



PHY address 5d0 -> Internal PHY for port 0

PHY address 5d1 -> Internal PHY for port 1

PHY address 5d2 -> Internal PHY for port 2

PHY address 5d3 -> Internal PHY for port 3

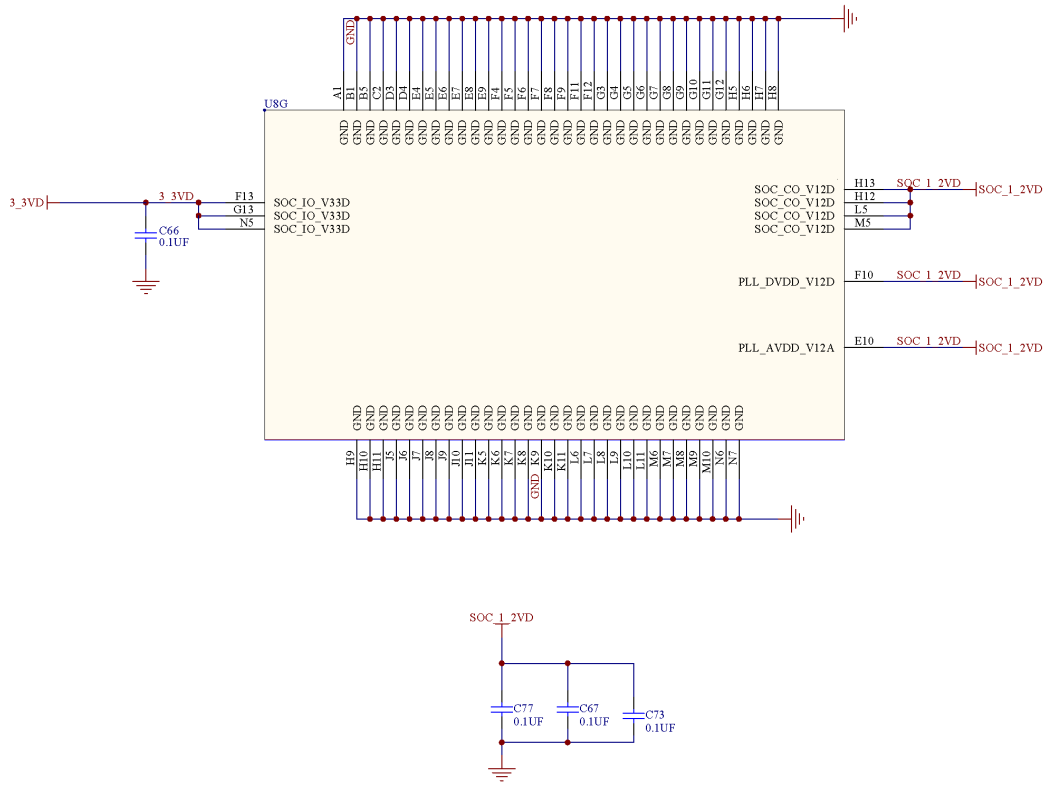
PHY address 5d4 -> Internal PHY for port 4

PHY address 5d5 -> default for the external Port 5

PHY address 5d5 ~ 5d31 are free for the external

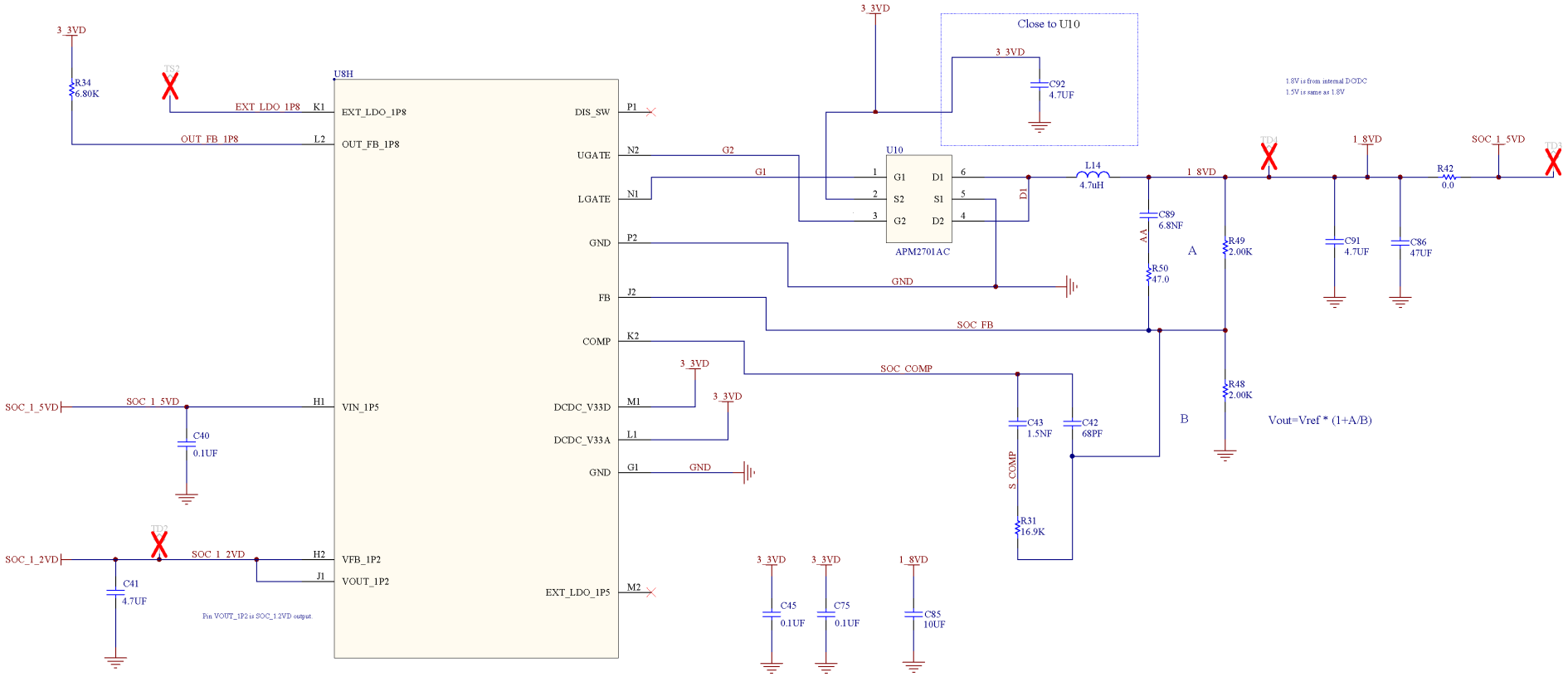
TITLE: Wifi Module SCHEMATIC DIAGRAM			
SIZE: B		PART NO.: 28-600006-001	REV.: V11.0
SCALE: NONE	DO NOT SCALE DRAWING	DRAWING NO.: 78-600006-001	SHEET: 7 OF 21

*** CPU_7 ***



TITLE: Wifi Module SCHEMATIC DIAGRAM			
SIZE: B		PART NO.: 28-600006-001	REV.: V11.0
SCALE: NONE	DO NOT SCALE DRAWING	DRAWING NO.: 78-600006-001	SHEET: 8 OF 21

*** CPU_8, DC/DC ***



TITLE: Wifi Module SCHEMATIC DIAGRAM			
SIZE: B		PART NO.: 28-600006-001	REV.: V11.0
SCALE: NONE	DO NOT SCALE DRAWING	DRAWING NO.: 78-600006-001	SHEET: 9 OF 21

*** CPU_9, none ***

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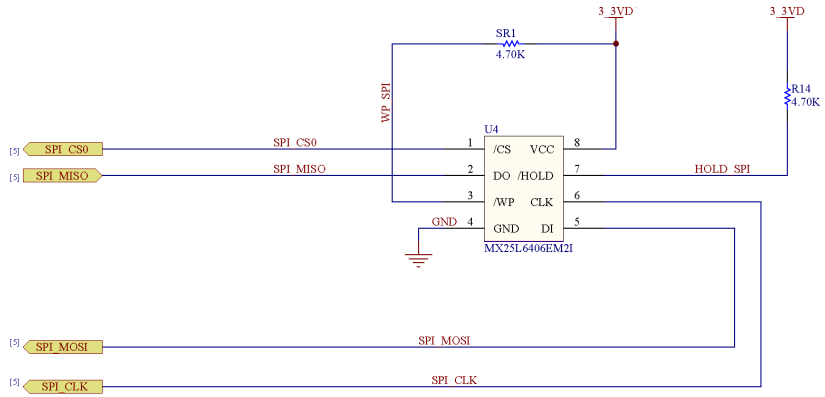
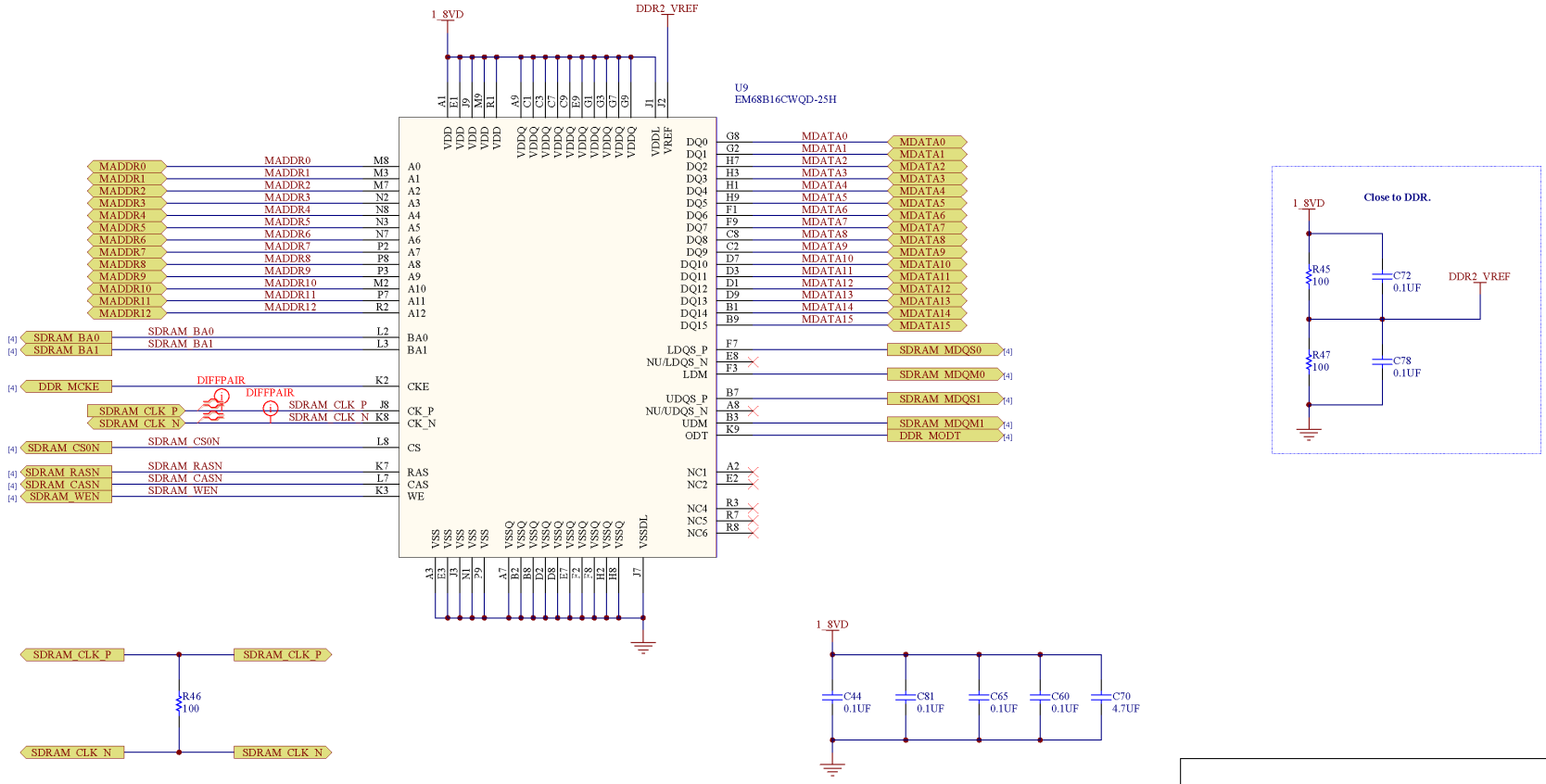
TITLE: Wifi Module SCHEMATIC DIAGRAM			
SIZE: B		PART NO.: 28-600006-001	REV.: V11.0
SCALE: NONE	DO NOT SCALE DRAWING	DRAWING NO.: 78-600006-001	SHEET: 10 OF 21

*** MEMORY_1, SPI Flash ***



TITLE: Wifi Module SCHEMATIC DIAGRAM			
SIZE: B		PART NO.: 28-600006-001	REV.: V11.0
SCALE: NONE	DO NOT SCALE DRAWING	DRAWING NO.: 78-600006-001	SHEET: 11 OF 21

*** MEMORY_2, DDR ***

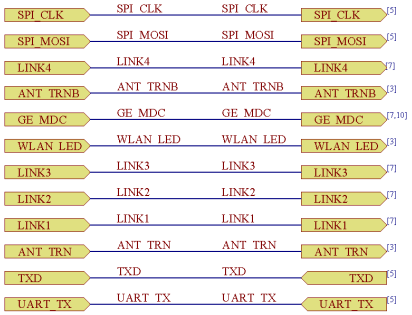


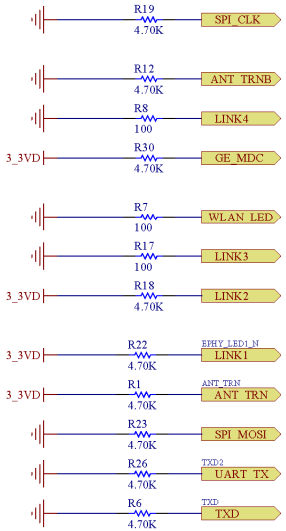
TITLE:
Wifi Module
SCHEMATIC DIAGRAM

SIZE:	PART NO.:	REV.:
B	28-600006-001	V11.0

SCALE:		DRAWING NO.:	SHEET:
NONE	DO NOT SCALE DRAWING	78-600006-001	12 OF 21

*** MEMORY_3, Boot Option ***





RT3352 Boot Up Strapping

Pin Name	Description	Value=0	Value=1
SPI_CLK	XTAL_FREQ _HI	20MHz	40MHz
ANT_TRNB	Big Endian	Little Endian	Big Endian
EPHY_LED4_N	DRAM_FROM _EE	from boot strapping	from EEPROM
MDC	DRAM_TYPE	SDRAM	DDR2
WLAN_LED_N	DRAM_TOTAL _WIDTH	16	32
{EPHY_LED3_N, EPHT_LED2_N}	DRAM_SIZE	INIC/AP(SDR)/AP(DDR2) 00: 2MB/8MB/32MB 01: 8MB/16MB/64MB 10: 16MB/32MB/128MB 11: 32MB/64MB/256MB	
EPHY_LED1_N	DRAM_WIDTH	SDRAM(DDR2) 0: 16(8) 1: 32(16)	
ANT_TRN	CPU_CLK _SEL	384MHz	400MHz
{SPI_MOSI, TXD2, TXD}	CHIP_ MODE[2:0]	000 : AP 001 : iNIC-USB 010 : iNIC-RGMII 011: iNIC-MII 100 : iNIC-RVMII 101 : Reserved 110 : SCAN 111 : TEST/DEBUG	

TITLE:
Wifi Module
SCHEMATIC DIAGRAM

SIZE:	PART NO.:	REV.:
B	28-600006-001	V11.0

SCALE:		DRAWING NO.:	SHEET:
NONE	DO NOT SCALE DRAWING	78-600006-001	13 OF 21

*** WLAN_1, none ***

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TITLE: Wifi Module SCHEMATIC DIAGRAM			
SIZE: B		PART NO.: 28-600006-001	REV.: V11.0
SCALE: NONE	DO NOT SCALE DRAWING	DRAWING NO.: 78-600006-001	SHEET: 14 OF 21

*** WLAN_2, none ***

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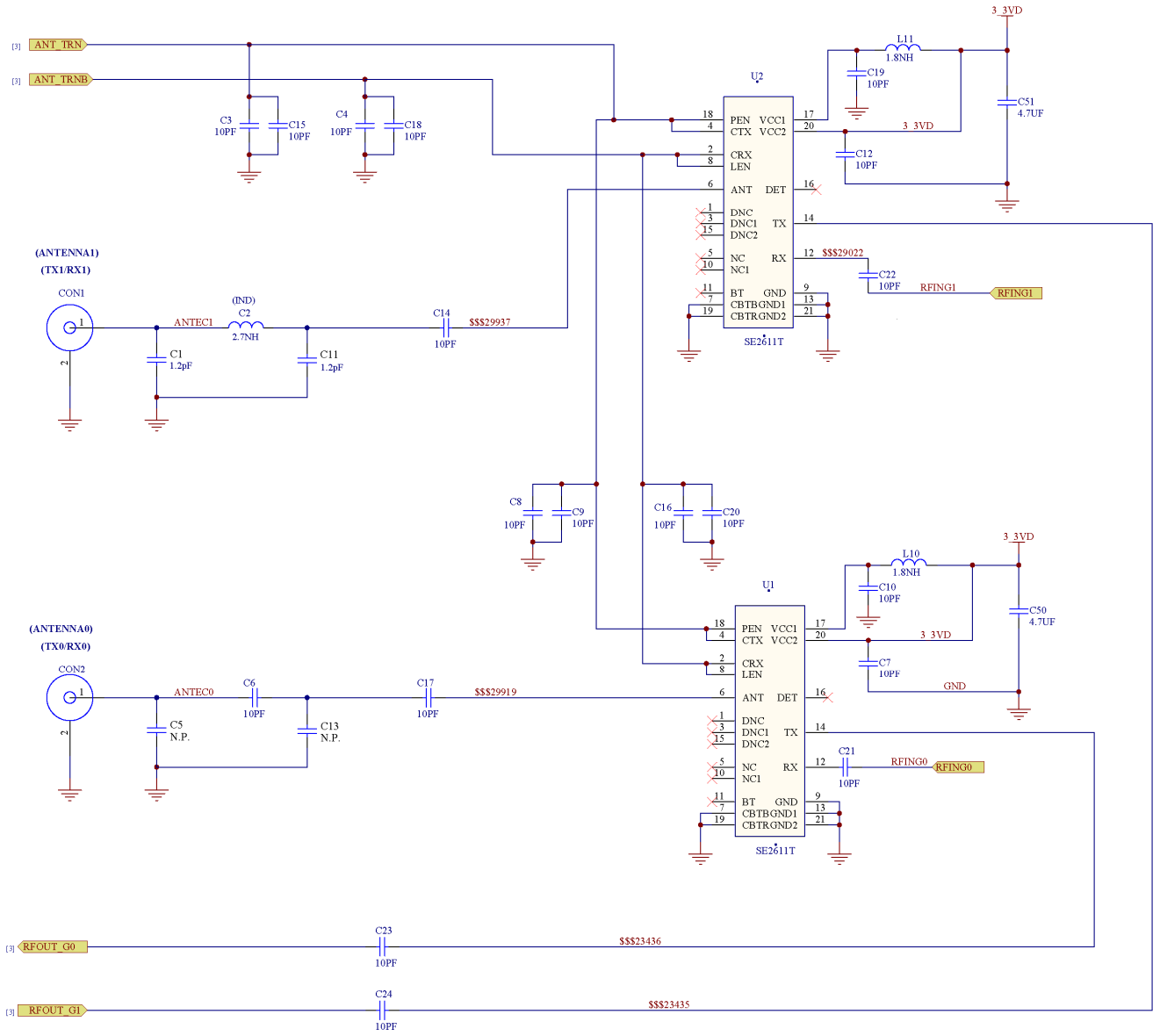
TITLE: Wifi Module SCHEMATIC DIAGRAM			
SIZE: B		PART NO.: 28-600006-001	REV.: V11.0
SCALE: NONE	DO NOT SCALE DRAWING	DRAWING NO.: 78-600006-001	SHEET: 15 OF 21

*** WLAN_3 ***



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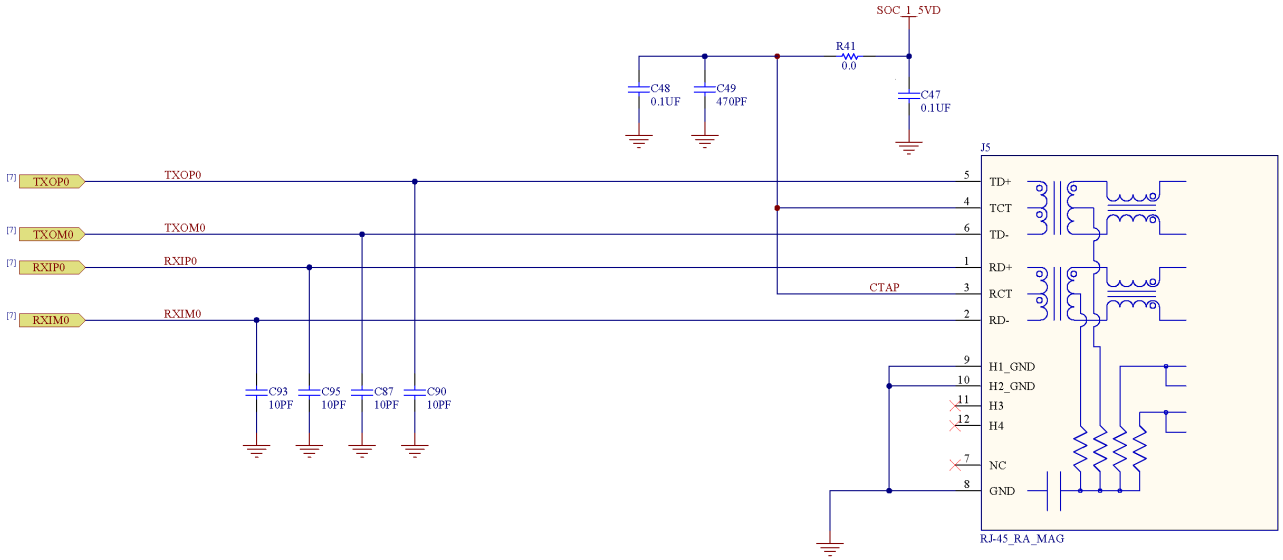
SIZE: B		PART NO.: 28-600006-001	REV.: V11.0
SCALE: NONE	DO NOT SCALE DRAWING	DRAWING NO.: 78-600006-001	SHEET: 16 OF 21

*** ETHERNET_1 ***



TITLE: Wifi Module SCHEMATIC DIAGRAM			
SIZE: B		PART NO.: 28-600006-001	REV.: V11.0
SCALE: NONE	DO NOT SCALE DRAWING	DRAWING NO.: 78-600006-001	SHEET: 17 OF 21

*** ETHERNET_2, none ***

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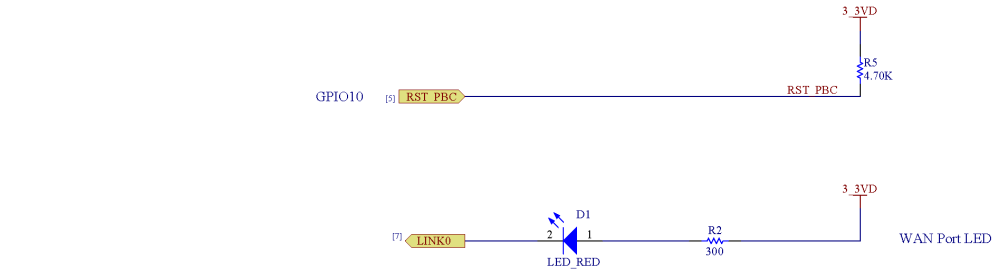
TITLE: Wifi Module SCHEMATIC DIAGRAM			
SIZE: B		PART NO.: 28-600006-001	REV.: V11.0
SCALE: NONE	DO NOT SCALE DRAWING	DRAWING NO.: 78-600006-001	SHEET: 18 OF 21



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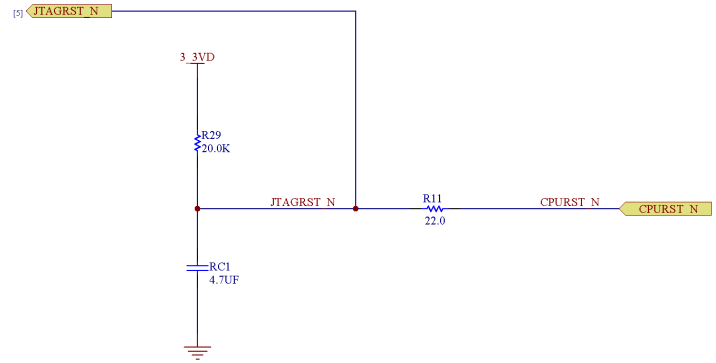
SIZE: B		PART NO.: 28-600006-001	REV.: V11.0
SCALE: NONE	DO NOT SCALE DRAWING	DRAWING NO.: 78-600006-001	SHEET: 19 OF 21

Reset Circuit



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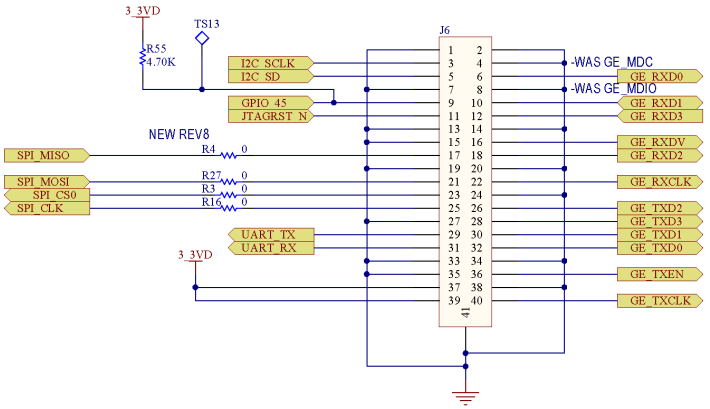
SIZE: B		PART NO.: 28-600006-001	REV.: V11.0
SCALE: NONE	DO NOT SCALE DRAWING	DRAWING NO.: 78-600006-001	SHEET: 20 OF 21

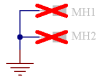
*** CONNECTOR ***

*** MAIN BOARD TO BOARD CONNECTOR ***



*** SHIELD LOCATOR PINS ***

*** Mounting Holes for Grounded Standoffs ***



TITLE: Wifi Module SCHEMATIC DIAGRAM			
SIZE: B		PART NO.: 28-600006-001	REV.: V11.0
SCALE: NONE	DO NOT SCALE DRAWING	DRAWING NO.: 78-600006-001	SHEET: 21 OF 21