Suga Electronics Limited

SWP23MA-3 Circuit Description

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SWP23MA-3 is a 2T2R AP/Router module which includes a main CPU (U8, RT3352) with a 802.11b/g/n media access controller (MAC) and baseband, a 2.4GHz radio and FEM, a 400 MHz MIPS 24K CPU core, two RF power amplifier (PA), a SPI flash, a 32M*16 DDR2, two 2.4GHz antennas with gain 2dBi, a 20MHz crystal, a 10/100 Ethernet port, a 40-pin fine pitch connector.

This module requires less and includes everything needed to build an AP router. The embedded high performance CPU can process advanced applications effortlessly, such as router, security, and VoIP.

The main CPU is a 2T2R 2.4GHz 802.11b/g/n all-in-one AP router-on-a-chip, with an integrated RF front-end module, intelligent NIC (iNIC) design available, providing existing wireless LAN platforms with an easy upgrade path to 802.11n.

The SPI flash is programmed with boot-loader, firmware and calibration data.

The DDR2 provides the data cache to the embedded high performance main CPU to process advanced management.

The 40-pin fine pitch connector provides power supply, data exchange, I/O control and debug. The 20MHz crystal provides working clock for the CPU. The 10/100 RJ45 Ethernet port can act as LAN or WAN port to meet the user need.

2x 2dBi 2.4GHz TX/RX antenna is used to transmit and receive 2.4GHz RF signals. About the transmitting paths (TX0/TX1), the 2.4GHz RF transmitted signal is generated from the internal of the main CPU. Then, it is transmitted to the RF power amplifier (PA).

Finally, it is transmitted to the 2.4GHz TX/RX antenna and is broadcasted out. About the receiving paths (RX0/RX1), the 2.4GHz RF signal is received by the 2.4GHz TX/RX antenna. Then, it is transmitted to the PA. Then, it is transmitted to the main CPU. Finally, it is demodulated and converted into data bits to meet the IEEE 802.11 b/g/n standards.