Suga Electronics Limited

SWP23MA-0/ SWP23MA-1 Circuit Description

Version 1.0

SWP23MA-0/ SWP23MA-1 is a 2T2R AP/Router module which includes an main chip RT3352 with an 802.11n media access controller (MAC) and baseband, a 2.4GHz radio and FEM, a 400 MHz MIPS 24K CPU core, a SPI flash, a 32M*16 DDR2, two 2.4GHz antennas with gain 2dBi, a 20MHz crystal, a 10/100 Ethernet port, two 2x 8pin-2.0mm pitch connectors.

This module requires less and includes everything needed to build an AP router from a single chip. The embedded, high performance CPU can process advanced applications effortlessly, such as routing, security, and VoIP. The reserved USB pin can connect a external USB port which can access external storage for digital home applications. The module also includes a wide selection of interfaces to enable many possible applications.

RT3352 is a 2T2R/2.4G 802.11n all-in-one AP router-on-a-chip, with an integrated RF front-end module, intelligent NIC (iNIC) design available, providing existing wireless LAN platforms with an easy upgrade path to 802.11n.

SPI flash is programmed the boot loader firmware and calibration data.

The DDR2 provide the data cache to embedded high performance CPU RT3352 to process advanced management.

Two 2x 8pin-2.0mm pitch connectors is provided the power and some certain IO communicated, the 20MHz crystal provide the base core clock for the RT3352, and the 10/100 Ethernet port can act as the LAN or WAN port to meet the user needed.

2x 2dBi 2.4GHz TX/RX antenna is used to transmit and receive 2.4GHz RF signals. As the transmitted paths (TX0/TX1), the 2.4GHz RF transmitted signal is generated from internal of RT3352 and transmitted via the 2.4GHz TX/RX antenna then broadcast out. And in the received paths (RX0/RX1), the 2.4GHz RF signal is received by the 2.4GHz TX/RX antenna and goes into the RT3352 processor, then is demodulated and converted into data bits to meet the IEEE 802.11 b/g/n standards.

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