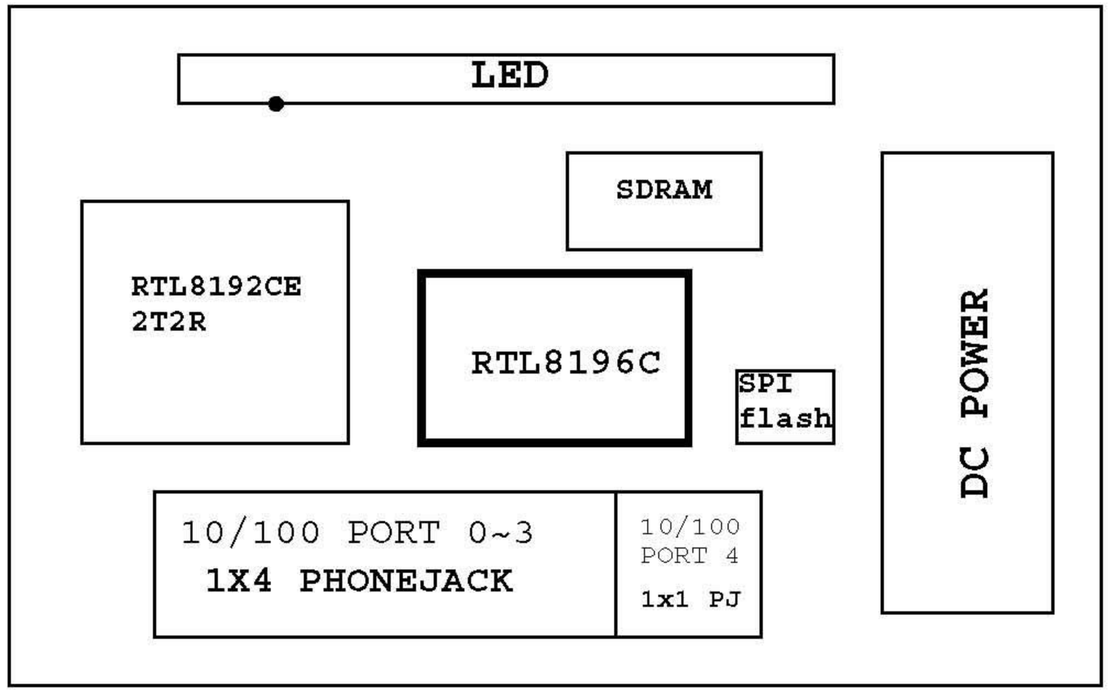

RTL8196C GPIO definition			
RTL8196C pin	GPIO Name	I/O	Function
pin 100	GPIOA2	O	PD#
pin 98	GPIOA6	O	SYSTEMLED
pin 96	GOIPA3	I	WPS
Pin 97	GOIPA4	O	WPSLED
pin 99	GPIOA5	I	Reset/Default
pin 108	GPIOB7	I	WAKE#

Title		
Size A	Document Number PLACEMENT	Rev V211
Date: Thursday, April 22, 2010	Sheet 1 of 7	

REVISION HISTORY

Revision	Release Date	Summary
REV:2.0	2010/04/15	Change New Chip RTL8196C HDK Design

Title: <Title>		
Size: A	Document Number: <Doc>	Rev: <RevCode>
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RTL8196C

10/100M PHY Interface

RDIN4 / RDIP4
TDON4 / TDOP4
RDIN3 / RDIP3
TDON3 / TDOP3
RDIN2 / RDIP2
TDON2 / TDOP2
RDIN1 / RDIP1
TDON1 / TDOP1
RDIN0 / RDIP0
TDON0 / TDOP0

VDD33 Capacitors For SDRAM

C101 0.1uF, C190 0.1uF, C191 0.1uF, C192 0.1uF, C193 0.1uF, C194 0.1uF, C195 0.1uF, C196 0.1uF

VDD10 Capacitors For SDRAM

C197 0.1uF, C198 0.1uF, C199 0.1uF, C201 0.1uF, C202 0.1uF

AVDD10PCIE: C204 10uF(0603), C205 1uF

LED/Push Button Interface

DEFAULT, WPS, WPSLED, SYSLED

JTGTRST R101 0 WPS
JTGTDI R155 0 DEFAULT
JTGTMS R156 0 WPSLED

R169 10K, R170 10K, R172 10K, R173 10K, R174 NC, R175 NC

JTGTDO, JTGTDI, JTGTMS, JTGCLK, RESETB

J11 HEADER 6X2 (pitch=2.54mm) — JTAG

16M 16bit SDARM x1

U11 ISSITS42S16800B-6TL

D0–D15, A0–A12, BA0, BA1, DQM0, DQM1, WEB, CASB, RASB, SD_CSUB, CKE

SDRAM_CLK: R187 NC/10K

SD_CLOCK R201 49.9 SDRAM_CLK

C208 NC, C210 NC, C209 NC

Layout Guide:

Put termination near the RTL8196C Chip side

MWEB R158 0 WEB
MCASB R160 0 CASB
MRASB R162 0 RASB
MSD_CSUB R163 0 SD_CSUB
MD0–MD15 R164–R179 0 D0–D15

Configure Interface

MA1–MA14

U17 RTL8196C

VDD10, LED_PORT2, LED_PORT3, VDD33, LED_PORT4, GPIOB7, GPIOC0, VDD10_USB, GND, USB_DN, USB_DP, AVDD33_USB_PCIE, HSON, HSOP, AVDD10_PCIE, REFCLKN, REFCLKP, AGND_PCIE, HSIN, HSIP, AVDD33_25M, 40M_SEL, 40M_CLK, 25M_XO, 25M_XI, AVDD33_BG

C206 0.1uF, C207 0.1uF, C211 0.1uF, AVDD10USB, AVDD33USB

R213 10K 40M_SEL, R215 NC/10K, AVDDBG

R214 12K(1%) R12K, PERSTB

R211 4.7K UORXD, R216 2.5K(1%) UOTXD

C224, C229 close to U2

HSIN, HSIP, HSIN_E, HSIP_E

PCI-E Interface: PERSTB, CLK+_HOST, CLK-_HOST, HSON, HSOP, HSIN, HSIP

CK_40M, WAKE#, CLKREQ#, PD#

R218 0 WAKEn, R219 NC/0 CLKREQn, R220 NC/0 JTGCLK

LED Interface

LED_PORT0–LED_PORT4

C241–C253 0.1uF, C242 0.1uF

L1110(0603) VDD10_A, C233 10uF(0805)

L112 0(1206) VDD33_A, C240 NC/10uF(0805)

C225–C228 0.1uF, C234–C236 0.1uF

C200 0.1uF, C220 10uF(0805), C221 0.1uF, C222 10uF(0805)

C237–C239 0.1uF

R201 49.9 ohms for lowing EMI

R205 NC/10K

U18 NC/MX25L1635DM 16-PIN SOP300Mil(SO16-wide)

NC/SIO3, VCC, SO/SIO1, CS, SCLK, SI/SIO0, WP/SIO2, VSS

SF_CSB, A19_SPIO1, A20_SPIO0, A18_SPIO2, SF_SCK

C212 0.1uF

R206 NC/10K, R207 NC/10K

SF_SCK1 R209 22 SF_SCK

C214 10K pull down for saving power

8 pins SPI Flash

U19 MX25L1635DM2I-12G/200mil(SO8-wide)

C219 0.1uF, R210 10K, R212 10K, R217 NC/10K

A17_SPIO3

UART

J15 PINTX4 — UOTXD, UORXD

NC/25MHz Crystal: 25M_XO, 25M_XI, C213 NC/27pF, Y11, C214 10K

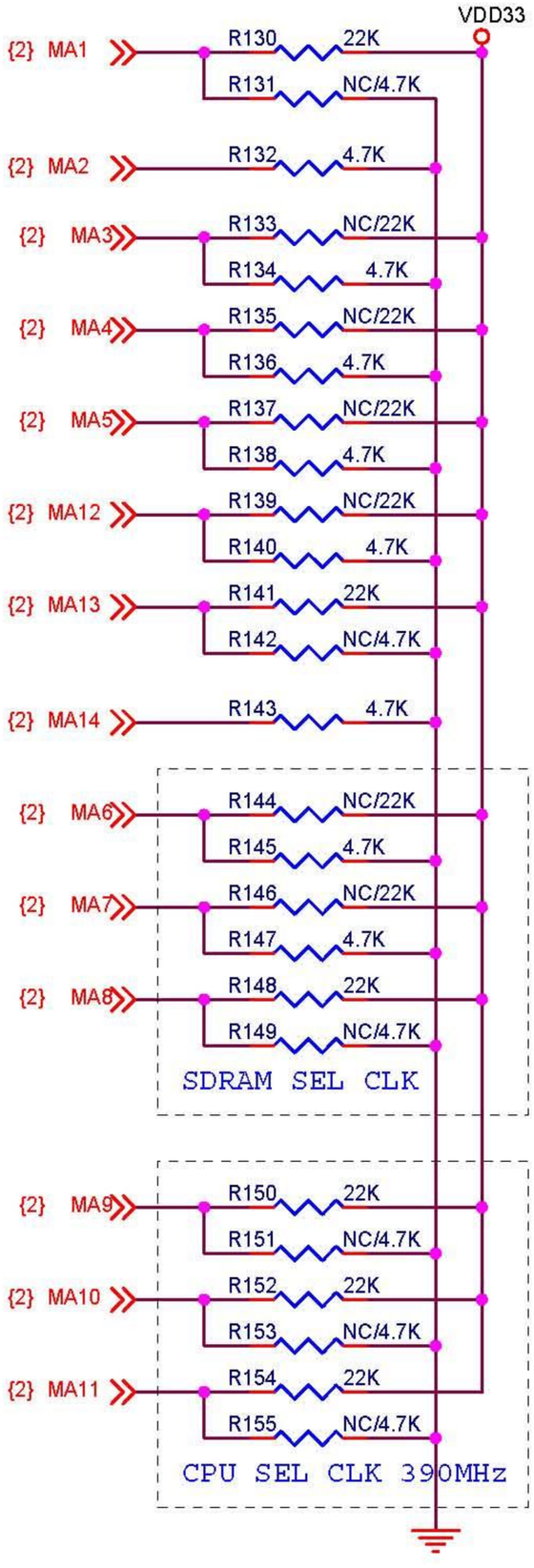
Y11, 25MHz crystal load capacitance uses 16pF

SPI Flash	Single I/O Dual I/O	Quad I/O
8 pins SPI	R210=10K R212=10K	R210=NC R212=NC
16 pins SPI	R205=10K R206=10K	R205=NC R206=NC

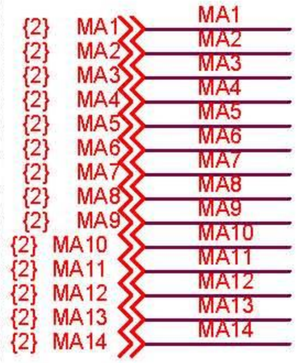
Title: 802.11n 10/100M Wireless Router

Size: Custom | Document Number: CPU/SDRAM/FLASH | Rev: V211

Date: Thursday, April 01, 2010 | Sheet 2 of 7



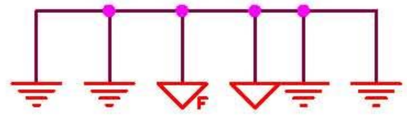
Configure Interface



Signal	Function	Descrpition
MA1	BOOTSEL	0: NOR Flash(default) 1: SPI Flash
MA3	Clklx_from_clkm	0: default 1: Clk_lx come from clk_m
MA4	Enable external reset	0: disable (default) 1: enable
MA5	SYNC_LX_OC	0: default 1: set SYNC_OC=SYNC_LX =SYNC_LX_OC for testing
MA[6:8]	(DRAM SEL CLK) clk_m2x_freq_Sel[0:2]	H/W strap can set 3 bits[0:2]
MA[9:11]	(CPU SEL CLK) clk_cpu_freq_Sel[1:3]	H/W strap can set 3 bits[1:3]
MA12	ck_cpu_div_sel	0: default 1: pll_cpu divide by 2
MA13	en_router_mode	0: 1 port AP mode 1: 5 port router mode (default)

SDRAMClkSel[2:0]
000: 65.625 MHz
001: 78.125 MHz
010: 125 MHz
011: 150 MHz
100: 156.25 MHz(default)
101: 168.75 MHz
110: 193.75 MHz
111: 237.5 MHz

CPUClkSel[2:0]
000: 250 MHz
001: 270 MHz
010: 290 MHz
011: 310 MHz
100: 330 MHz
101: 350 MHz
110: 370 MHz
111: 390 MHz



Title: 802.11n 10/100M Wireless Router

Size: A | Document Number: Configure Interface | Rev: V211

Date: Wednesday, March 31, 2010 | Sheet 3 of 7

{2} DEFAULT
{2} WPS
{2} WPSLED
{2} SYSLED
DEFAULT
WPS
WPSLED
SYSLED

LED/Push Button Interface

VDD33
C158 10uF(0805)
C159 10uF(0805)
C160 0.1uF
C161 0.1uF
C167 0.1uF
C162 0.1uF
C163 NC
C164 NC
C165 NC

D11 LED-G
R108 1K
VDD33
POWER ON LED

D12 LED-G
WPSLED
C134 100pF
R109 330
VDD33
WPS LED

R110 10K
J12
R112 100
DEFAULT
RESET BUTTON
RESET/RELOAD DEFAULT

VDD10 optional for Switch Regulator

Lowering EMI

SD11 SK14
R114 NC/1R0(0603)
C139 NC/100pF(0603)
C140 10nF
U15 RT8258
BST PHASE
VIN FB
GND EN
EN_VDD10
L102 3.3uH/3A
VDD10OUT
R113 200K(1%)
C141 NC
C142 0.1uF
C143 10uF(X5R0805)
C144 470uF/6.3V
L103 0(1206)
VDD10
C145 10uF(0805)
C146 0.1uF
C148 10uF(X5R0805)
C149 0.1uF
R116 820K(1%)
Vout=0.8(1+R113/R116)=1V
VDD33
C155 0.1uF
R118 20K
R119 100K
C156 0.47uF
VDD33
C151 10uF(0805)
C152 10uF(0805)
C153 10uF(0805)

DC INPUT
J14
VDC PGND
PowerJack (DIP)
Power adapter usage

L106 WIDE BAND CHOKE (DIP)
L108 WIDE BAND CHOKE (DIP)
C171 0.1uF
C172 100pF
C177 220uF/25V
C169 10uF(X5R1206)
C181 0.1uF
VIN
PGND

U16 FP6101
Vin LX
SCP LX
IN- GND
FB GND
C184 0.47uF
R221 1K
C183 22nF
Lowering EMI
L105 33uH/3A
SD12 SD34
R127 1K
C173 0.1uF
R123 56K1%
R126 10K1%
C179 0.1uF
C180 10uF(0805)
C176 470uF/10V
L107 0(1206)
VDD33
C174 10uF(0805)
C175 0.1uF

SCAN Mode
VDD33
LAN
R115 120 D16 LED-G Link/Act Port-0 LED_PORT0 {2}
C147 100pF
R117 120 D18 LED-G Link/Act Port-1 LED_PORT1 {2}
C154 100pF
R120 120 D20 LED-G Link/Act Port-2 LED_PORT2 {2}
C157 100pF
R121 120 D22 LED-G Link/Act Port-3 LED_PORT3 {2}
C166 100pF
WAN
R122 120 D24 LED-G Link/Act Port-4 LED_PORT4 {2}
C168 100pF

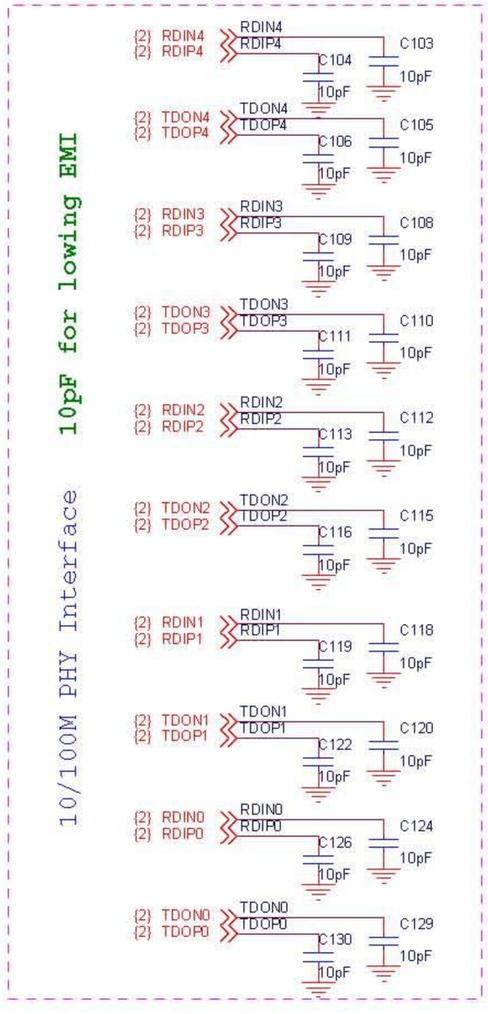
FD1 PCB 光學點
FD2 PCB 光學點
FD3 PCB 光學點
H1 NPTH
H2 NPTH

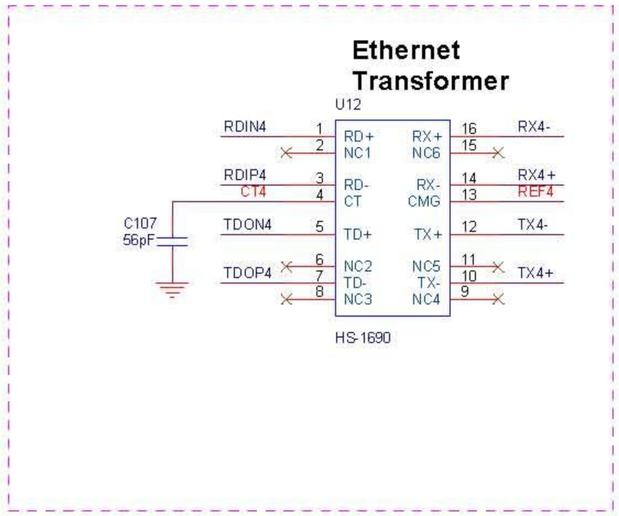
IC HOLE
H3 NPTH
H4 NPTH
H5 NPTH
H6 NPTH
H7 NPTH
H8 NPTH
H9 NPTH

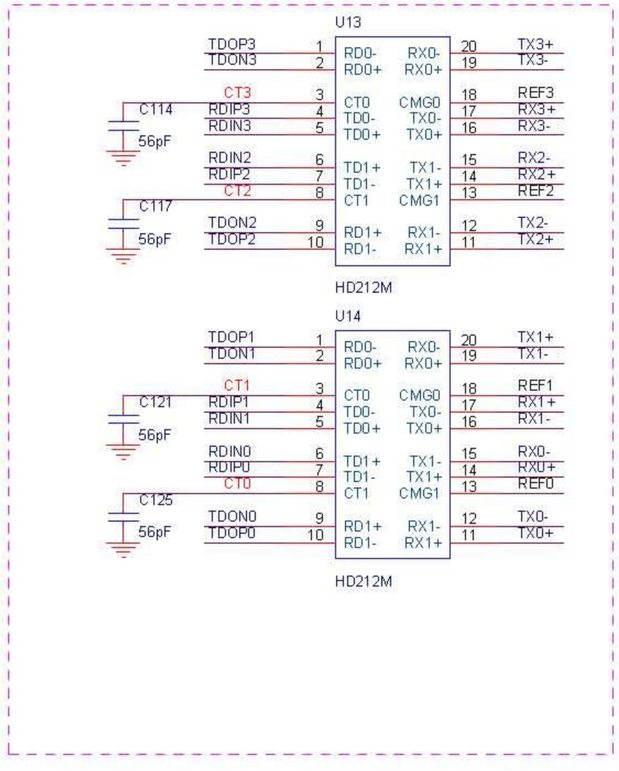
H11 MB62/CB62 SHIELD
GND GND GND GND
H10 SMA-MASK

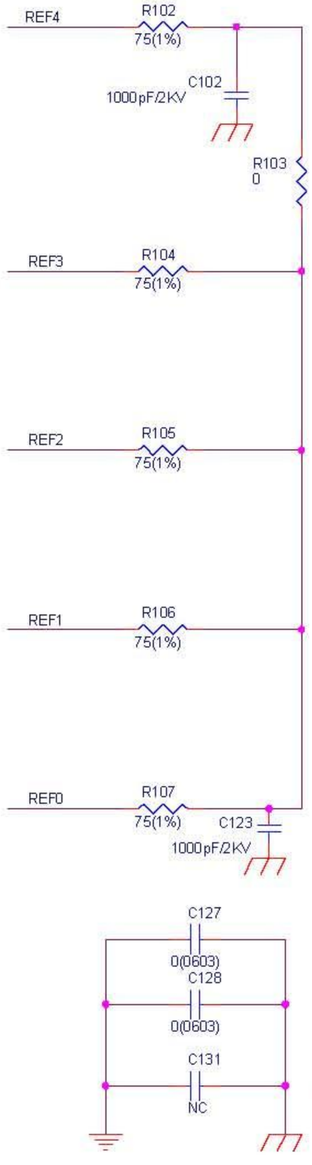
J13
R128 100
R129 10K
VDD33
WPS
C185 NC
WPS CONFIGURE

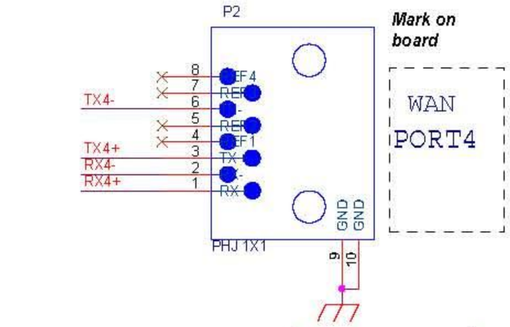
Title	802.11n 10/100M Wireless Router		
Size: Custom	Document Number: POWER/LEDs		Rev: V211
Date: Thursday, April 01, 2010	Sheet 4 of 7		

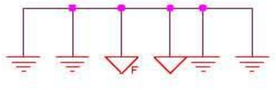












Title	802.11n 10/100M Wireless Router		
Size B	Document Number MDI 10/100M		Rev V210
Date: Thursday, April 01, 2010	Sheet 5 of 7		

RF 50 ohms trace

ANT3
SMA 90度

ANT1
IPEX connector

RF PATH A

ANT2
IPEX connector

RF PATH B

These components inside of pink color line region are removed for 1T1R option

PAVCC0

VD15R1

VDD15D

DVDD3.3B

DVDD3.3PCIE

DVDD3.3R

DVDD3.3A

U1

RTL8192CE

WLAN LED

LED_WLAN

VDD33

VDD15D

DVDD3.3-1

PAVCC1

Power and Ground

1.5V Trace

1.2V Trace

PCI-E Interface

CLK-_SLAVE R38 0 CLK-_HOST

CLK+_SLAVE R41 0 CLK+_HOST

C25,C21 close to RTL8192CE

CLK+_HOST {2}
CLK-_HOST {2}
HSON {2}
HSOP {2}
HSIN {2}
HSIP {2}
PERSTB {2}
CLK+_HOST {2}
CLK-_HOST {2}

HSON_E C25 0.1uF HSON

HSOP_E C21 0.1uF HSOP

Output

Output

Input

Xtal

XO_1 X2 XI_1

40MHz DIP Crystal

Choose X2 Crystal
40MHz DIP , C44=27pF,
C43=33pF

40MHz CLK to RTL8196C

R56 0 CK_40M {2}

R45 NC/0 CK_40M {2}

Title	802.11n 10/100M Wireless Router
Size: Custom	Document Number: RTL8192CE
Rev: V120A	
Date: Thursday, April 22, 2010	Sheet 6 of 7