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RESUME / *SUMMARY*

This document is the application notes of the HiLo 3G module.

Mots clés / *Keywords* : : HiLo3G, Application Notes

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1. OVERVIEW

1.1.Document Objectives

The aim of this document is to describe some examples of hardware solutions for developing some products around the SagemCom HiLo3G Module. Most parts of these solutions are not mandatory. Use them as suggestions of what should be done to have a working product and what should be avoided thanks to our experience.
This document suggests how to integrate the HiLo3G module into machine devices such as automotive, AMM (Automatic Metering Management), tracking system: connection with external devices, layout advises, external components (decoupling capacitors…), etc.

1.2.Reference Documents

[1] URD1 OTL 5696.1 004 72362 Ed 04 - HiLo 3G technical specifications
[2] URD1 OTL 5696.1 006 72370 Ed 01- AT Command Set for SAGEM HiLo3G Modules

1.3.Document Modifications

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1.4.Conventions

SIGNAL NAME: All signal names available on the pins of the HiLo3G module are written in *`italic`*.
☞Specific attention must be granted to the information given here.

2. Block Diagram

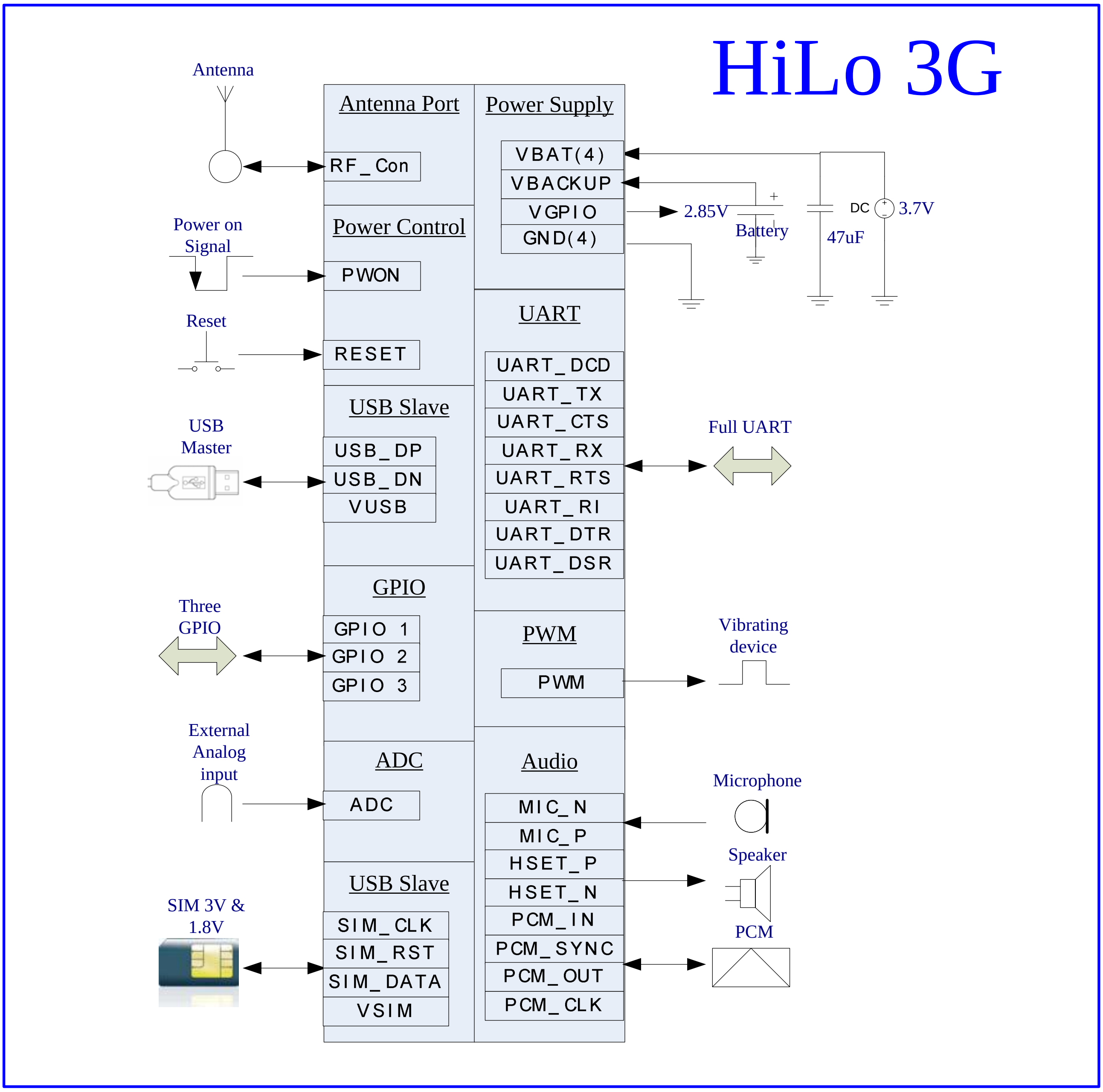


Figure 1: HiLo3G module Block diagram

3. Functional Integration

Advancements in Silicon technologies head toward functionality improvement with less power consumption. The HiLo3G module with its industrial 40 pins connector meets all these requirements, using the latest high end technology in a very compact design of only 27 x 27 x 4.8 mm and weighs less than 7 grams.

☞ All digital I/Os among the 40 pins are in the 2.9V domain suitable for most systems except SIM I/O's, which can also be in the 1.8V domain depending on SIM-card use and PWON in the 1.8V domain.

☞ Analogical I/O are in the following power domains:

- VSIM → SIM I/Os in the 1.8V or 2.9V domain
- VBACKUP → 3V domain
- VGPIO→ 2.9V domain
- VBAT→ from the 3.2V to the 4.4V domain. 3.7V is normal.
- VUSB→ 5V domain
- ADC→ 2.1V domain
- MIC_N/P→ 1.8V domain
- HSET_N/P→ VBAT domain
- Antenna→ RF power Amplifier is on VBAT domain
- Operation temperature→ from the -40℃ to the +85℃

☞ Do not power on the module I/O with a voltage over the specified limits. This could damage the module.

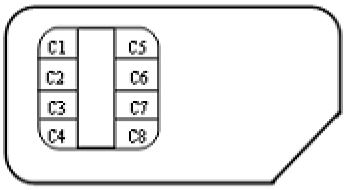
☞ Acoustic engineering competencies are mandatory to obtain accurate audio performance from customer products.

☞ Radio engineering competencies are mandatory to obtain accurate radio performance from customer products.

Figure 2: HiLo3G module connector side

Figure 3: HiLo3G module back side

3.1.How to connect a SIM card



PIN No.	Name
C1	VCC
C2	RST
C3	CLK
C4	NA
C5	GND
C6	VPP
C7	I/O
C8	N/A

Figure 4: SIM Card signals

The HiLo3G module provides SIM signals to the 40 pins. A SIM card holder with 6 pins must be adopted to use the SIM function.

☞Decoupling capacitors must be added on `VSIM`, `SIM_DATA`, `SIM_RST`, and `SIM_CLK` signals as close as possible to the SIM card connector to avoid EMC issues and pass SIM card approval tests.

☞Use ESD protection components to protect SIM card and module I/Os against Electro Static Discharges.
The following schematic shows how to protect SIM access of a 6 pins connector. This must be performed every time a SIM card holder is accessed by the end user customer.

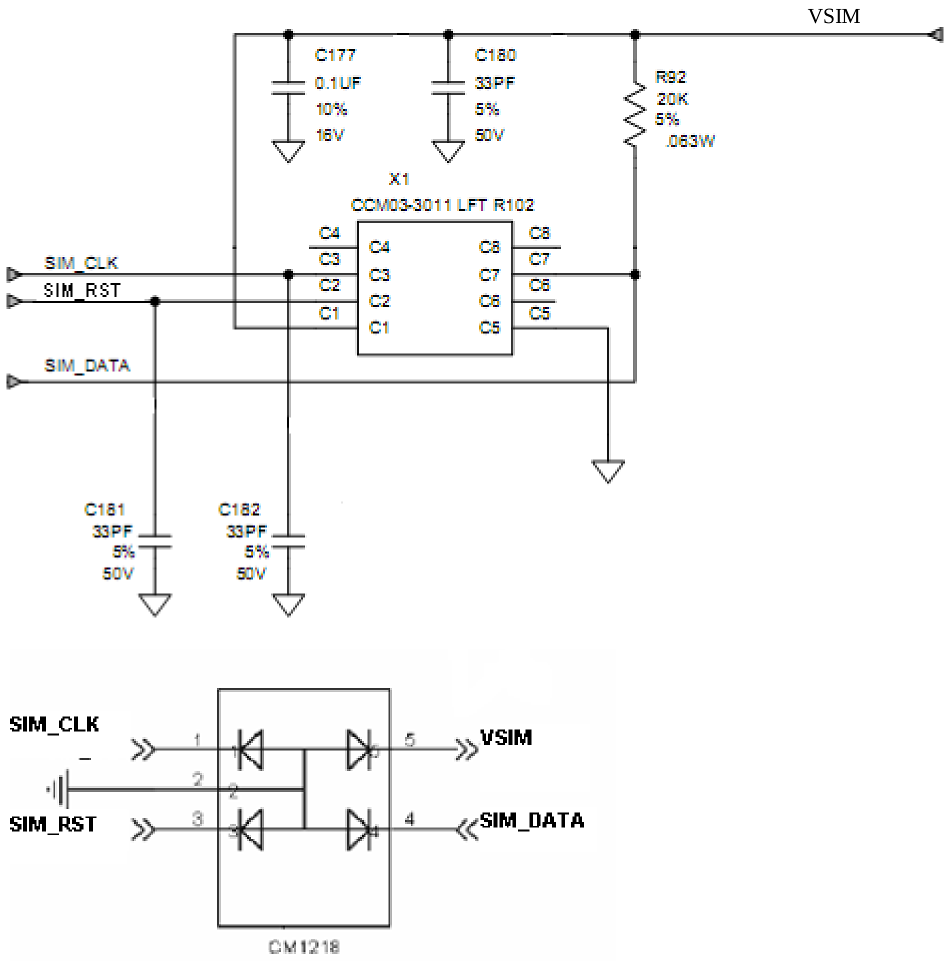


Figure 5: EMC and ESD protection components close to SIM

☞In cases of long SIM bus lines over 100mm, using serial resistors to avoid electrical overshoots on SIM bus signals is recommended. Use 56 Ω for the clock line and 10Ω for the reset and data lines.

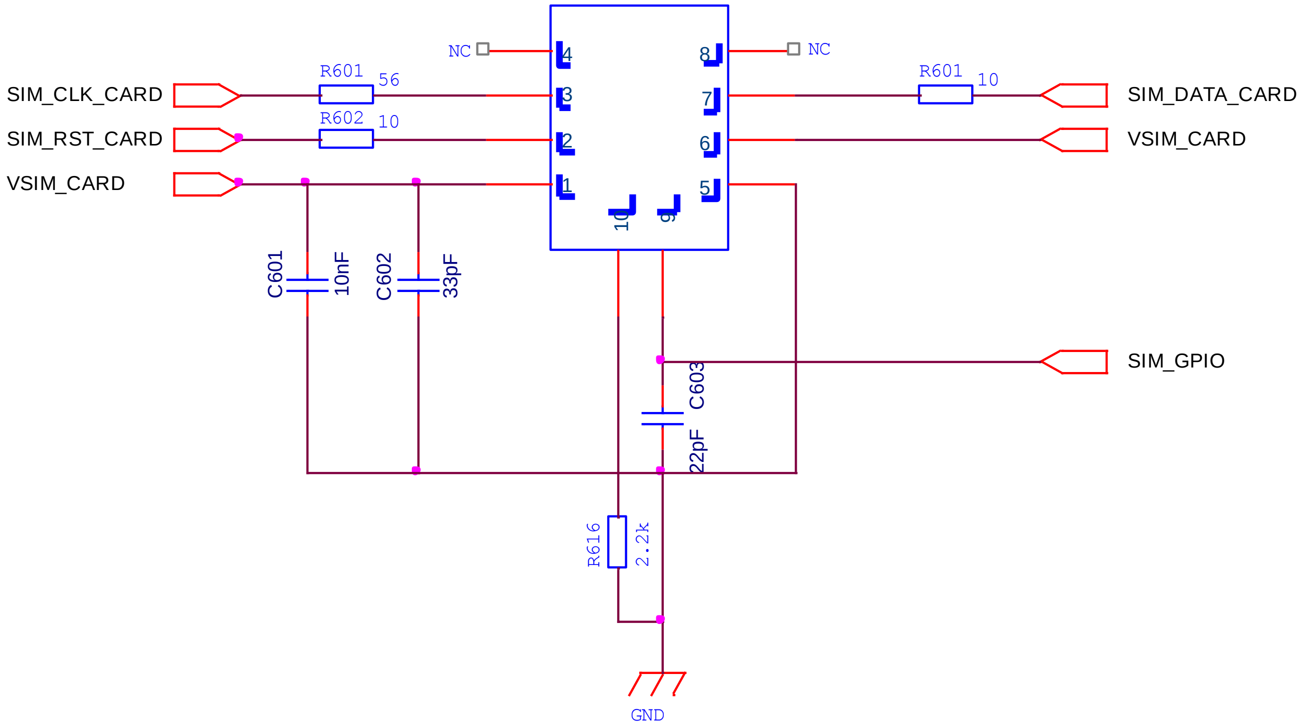


Figure 6: Serial resistors for protection of long SIM bus lines

The schematic here above includes the hardware SIM card presence detector. It can be connected to any GPIO and managed with an AT command.

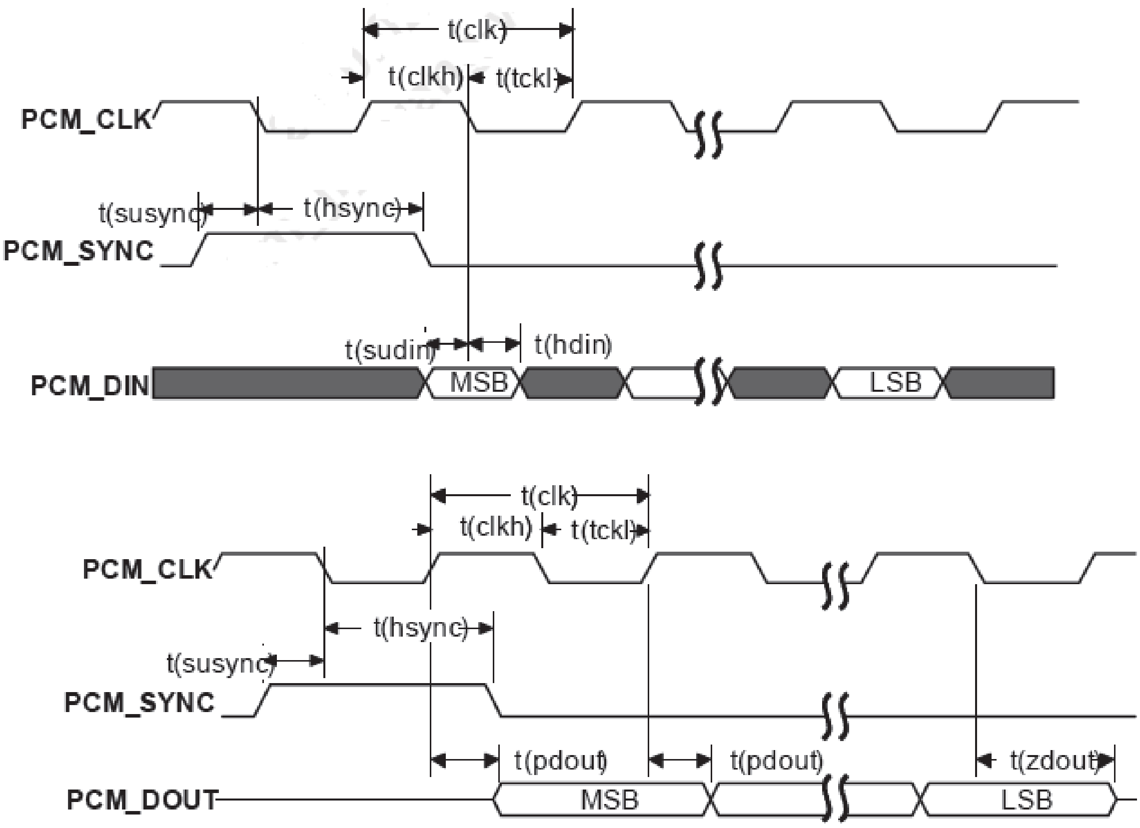
☞The SIM card must not be removed from its holder while it is still powered. First switch the module off properly with the AT command, then remove the SIM card from its holder.

3.2. Connect Audio

The HiLo3G module features two input audio paths and two output audio paths. The two input paths, one is differential analog microphone and the other is PCM digital input. The two output paths, one is a differential analog 32Ω speaker and the other is PCM digital output.
In this following chapter design examples will be given including protections against EMC and ESD and some notes about the routing rules to follow to avoid TDMA noise sometimes present in this sensitive area of design.

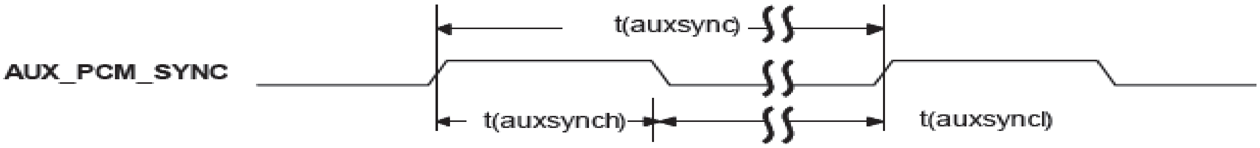
3.2.1 PCM Digital Audio

HiLo3G can be used for connections to an external codec through the integrated PCM interface. The interface supports an 8 kHz short sync mode at 2048 kHz and an 8 kHz long sync mode at 128 kHz. In the short-sync (primary PCM) mode, the HiLo3G can be a master or a slave. In the long-sync (auxiliary PCM) mode, the HiLo3G is always a master; there is no slave support.

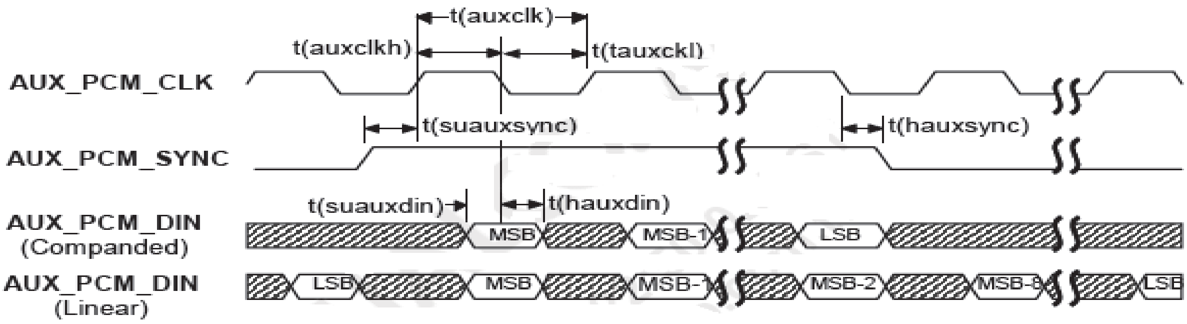


Parameter	Description	Min	Typ	Max	Unit
T(sync)	PCM_SYNC cycle time	–	125	–	µs
T(synch)	PCM_SYNC high time	400	500	–	ns
T(syncl)	PCM_SYNC low time	–	124.5	–	µs
T(clk)	PCM_CLK cycle time	–	488	–	ns
T(clkh)	PCM_CLK high time	–	244	–	ns
T(clkl)	PCM_CLK low time	–	244	–	ns
T(susync)	PCM_SYNC setup time high before falling edge of PCM_CLK	60	–	–	ns
T(hsync	PCM_SYNC hold time after falling edge of PCM_CLK	60	–	–	ns
T(sudin)	PCM_DIN setup time before falling edge of PCM_CLK	50	–	–	ns
T(hdin)	PCM_DIN hold time after falling edge of PCM_CLK	10	–	–	ns
T(pdout)	Delay from PCM_CLK rising to PCM_DOUT valid	–	–	350	ns
T(zdout)	Delay from PCM_CLK falling to PCM_DOUT HIGH-Z	–	160	–	ns

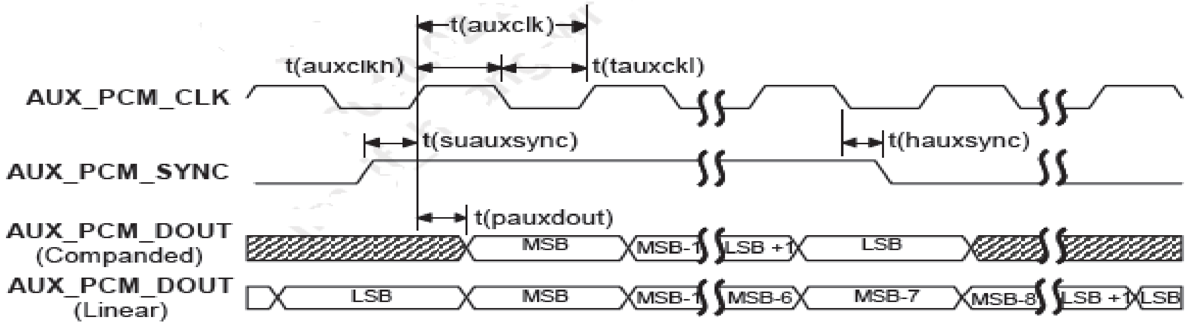
Figure 7: Primary PCM mode timing parameter



AUX_PCM_SYNC



EXT_CODEC to



to EXT CODEC

Parameter	Description	Min	Typ	Max	Unit
T(auxsync)	AUX_PCM_SYNC cycle time	–	125	–	µs
T(auxsynch)	AUX_PCM_SYNC high time	62.4	62.5	–	µs
T(auxsyncl)	AUX_PCM_SYNC low time	62.4	62.5	–	µs
T(auxclk)	AUX_PCM_CLK cycle time	–	7.8	–	µs
T(auxclkh)	AUX_PCM_CLK high time	3.8	3.9	–	µs
Parameter	Description	Min	Typ	Max	Unit
T(auxclkl)	AUX_PCM_CLK low time	3.8	3.9	–	µs
T(suauxsync)	AUX_PCM_SYNC setup time high before falling edge of PCM_CLK	1.95	–	–	µs
T(hauxsync)	AUX_PCM SYNC hold time after falling edge of PCM_CLK	1.95	–	–	µs
T(suauxdin)	AUX_PCM_DIN setup time before falling edge of AUX_PCM_CLK	70	–	–	ns
T(hauxdin)	AUX_PCM_DIN hold time after falling edge of AUX_PCM_CLK	20	–	–	ns
T(pauxdout)	Delay from AUX_PCM_CLK rising to AUX_PCM_DOUT valid	–	–	50	ns

Figure 8: Auxiliary PCM mode timing parameter

3.2.2 Analog Audio

Analog audio is connected via MIC_N and MIC_P as input and HSET_N and HSET_P as output to the HiLo3G. Please note that external circuitries are mainly needed for the microphone and speaker.

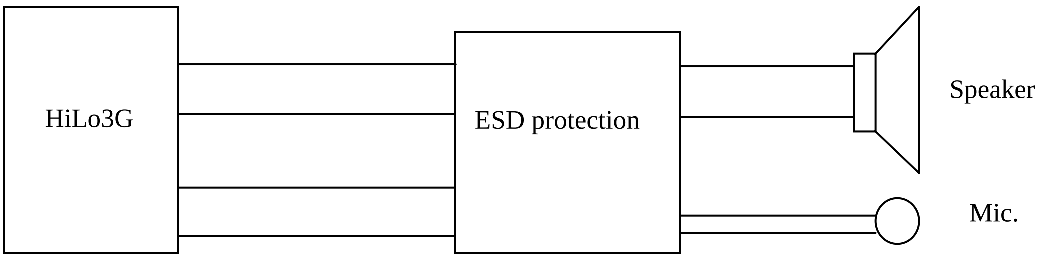


Figure 9: Analog audio connections

3.2.2.1 Microphone Note

☞Careful attention must be given to the microphone device design because it must not be sensitive to RF disturbances.

☞If you must have deport microphone out of the board using long wires, extra care must be given to avoid EMC and ESD effects. It is also the case when your design is ESD sensitive. In those cases, add the following protections to improve your design.

☞To ensure proper operation of such sensitive signals, they must be isolated from others by analog grounding on customer board layouts.

☞To use an external bias voltage for the microphone, simply use a capacitor of 10µF to prevent this bias voltage from being re-injected inside the module.

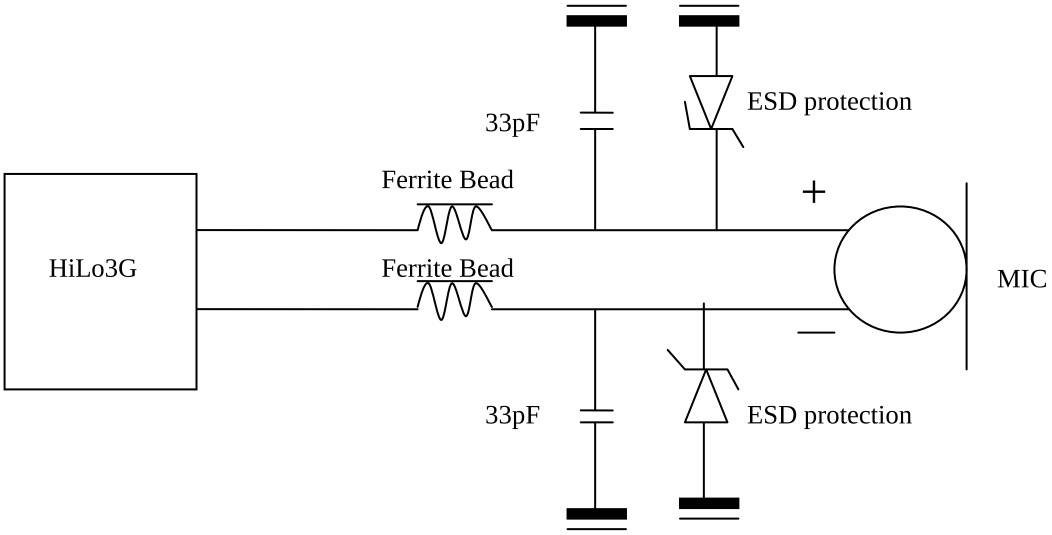


Figure 10: Filter and ESD protection for microphone

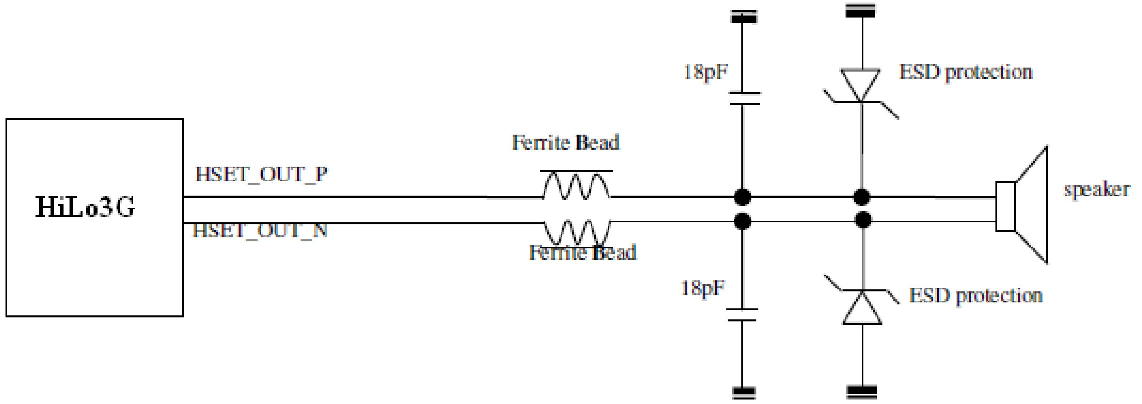
3.2.2.2 Note for Speaker

☞The differential analog output of the HiLo3G is able to drive a 32 Ohms telephone receiver directly. In case there is a need to drive something different, e.g. an 8 Ohms speaker, an external amplifier isrequired.

☞*HSET_P*, *HSET__N* tracks must be larger than other tracks: 0.3 mm.

☞Differential signals have to be routed in parallel.

☞To use an external audio amplifier connected to a loud-speaker, use serial capacitors of 10nF on the HiLo3G audio outputs to connect the audio amplifier.



Reference Bead: Murata BLM18HD102SN1D

Figure 11: Filter and ESD protection for 32 ohms speaker

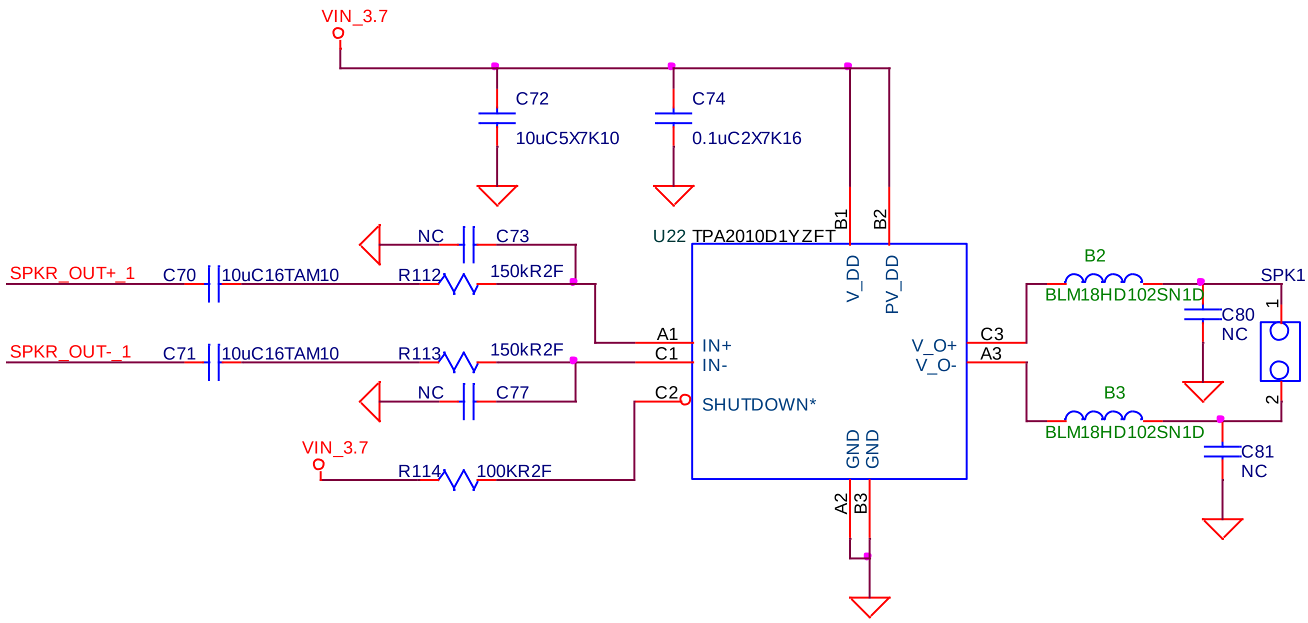


Figure 12: Example of D class TPA2010D1 1Watt audio amplifier connections

3.2.2.3 Recommended Microphone Characteristics

☞Microphone: 8 and 16 kHz sampling rate, 16 bit.

☞In addition to the headset with microphone, the only external components required to implement this feature is one 2.2 k resistor and two 0.1µF caps.

Parameter	Comments	Min	Typ	Max	Units
MIC bias voltage		–	1.8	–	V
MIC bias current	Programmable	0.020	–	1.50	mA
MIC bias voltage accuracy	Minimum load	-3	–	+3	%
MIC bias voltage load regulation		30	–	–	Ω
Load capacitor	At HSED_BIAS pin; ensures stability	0.1	–	1.0	uF

Supply current Active state Idle state		–	 50 10	 100 100	 uA nA

Parameter	Test conditions	Min	Typ	Max	Units	Notes
Full-scale input voltage	Voltage across either MIC1P and MIC1N, MIC2P and MIC2N, or LINEIN_LP and LINEIN_LN, 0 dB gain	0.89	1	1.12	Vrms	
	Voltage across either MIC1P and MIC1N, MIC2P and MIC2N, or LINEIN_LP and LINEIN_LN, 24 dB gain	56.2	61.3	70.8	Vrms	
Gain error (absolute)	0 and 24 dB gain settings for all inputs. Measured at 13 dB below the maximum input level for the given gain setting.	-1	0.2	1	dB	
Output referred noise	0 dB gain, input grounded A-weighted	–	-86.92	- 88.91	dBFS	
	24 dB gain, input grounded A-weighted	–	-83.92	- 83.92	dBFS	
Input impedance	Differential mode	16	20	24	kΩ	
	Single-ended mode	8	10	12	kΩ	
Parameter	Test conditions	Min	Typ	Max	Units	Notes
THD+N ratio	0 dB analog gain Input frequency = 1.02 kHz Output = -1 dBFS	40	90.84	–	dB	Measurement BW = 22 to Fs/2; (no A-weighting)
	24 dB analog gain Input frequency = 1.02 kHz Output = -1 dBFS	40	82.43	–	dB	
Input capacitance	At each pin, for all inputs	–	–	5	pF	
Input offset voltage		-5	–	5	mV	
Signal-to-noise ratio	0 dB gain, input grounded A-weighted	TBD	TBD	–	dB	
	24 dB gain, input grounded A-weighted	TBD	TBD	–	dB	
Sensitivity			- 39 dB ~-42 dB SPL(0 dB = 1 V/Pa @ 1kHz)			

Figure 13: Microphone performance requirements

3.2.2.4 Recommended Speaker Characteristics

Item to be inspected	Acceptance criterion
Input power: rated / max	0.1W (Rate)
Audio chain impedance	32 ohm +/- 10% at 1V 1KHz
Frequency Range	300 Hz ~ 4.0 KHz
Sensitivity (S.P.L)	>105 dB at 1KHz with IEC318 coupler
Distortion	5% max at 1K Hz, nominal input power

Figure 14: Speaker performance requirements

3.3 PWM

One PWM pin is available on the HiLo3G. It's a general purpose PWM which can be used for driving a vibrating device, keypad backlight or LED. The PWM pin can be controlled through AT commands, allowing several periods and duty cycles. More details are given in the AT commands specifications document.

User application can set PWM output:

☞Frequency between: 0.125Hz and 8KHz

☞Duty range from: 0 to 100%

3.3.1 PWM for Buzzer connection

HiLo3G module can manage PWM output to drive a buzzer. The buzzer can be used as an abnormal state alarm.

☞Resistors must be added to protect the buzzer. The value of these resistors depends on the buzzer and the transistor. Normally, they can be set at 1KΩ.

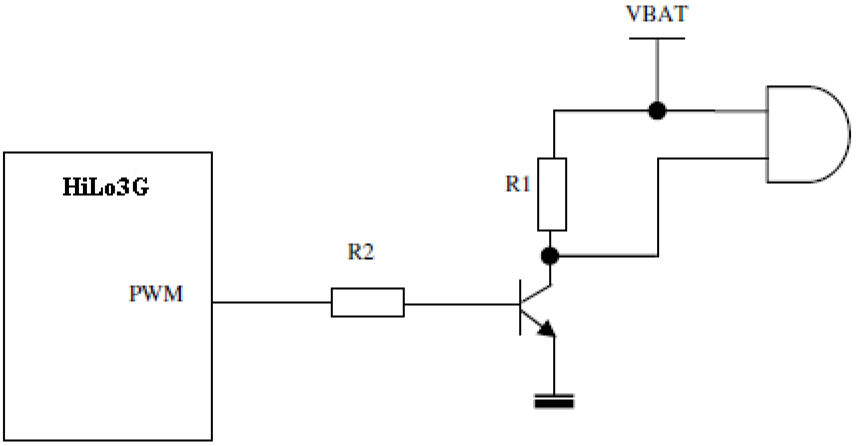


Figure 15: Buzzer connection

3.3.2 Network LED

The HiLo module can manage a network LED. The LED can be connected either to one of the available GPIO or to the PWM.
The transistors can be found a in a single package referenced as UMDXX or PUMDXX Family.
Value of resistor R depends on characteristic of chosen LED; it is used to limit the current through the diode.
Use the AT command to set the GPIO or PWM used to control the LED.

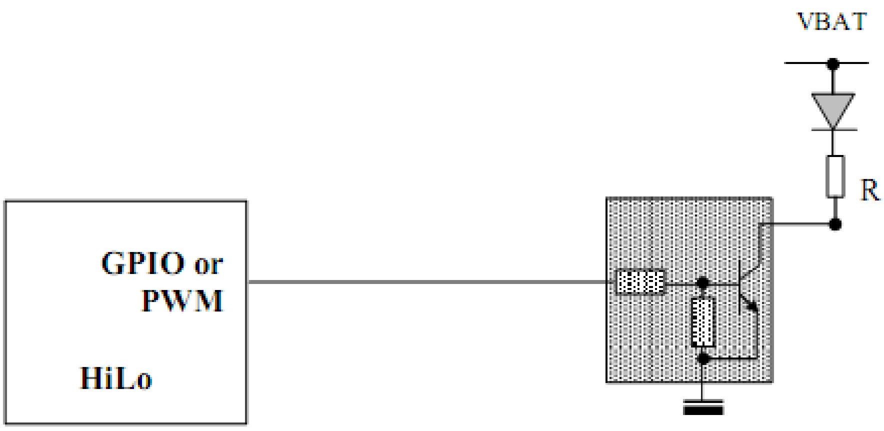


Figure 16: Network LED connection

3.4 Power Requirements

The host system must supply 3.2V ~ 4.4V to VBAT.

☞Within normal 2G and 3G operational modes, the maximum average current is about 1.1A depending on RF output power. In 2G mode peak current can be as high as 2A under matched antenna condition. Peak currents could occur up to 1.75A in the case of a mismatched antenna. In the 3G mode and under antenna mismatch condition, peak current may increase up to 700mA.

☞VBAT traces are required to be as short and as wide as possible. Connectors that introduce additional resistance must be avoided whenever possible. In case it is necessary to change the PCB layer carrying the VBAT lines have several routing options in parallel available to connect VBAT traces on different layers relative to each other.

☞VBAT ceramic decoupling capacitors of at least 100µF/10V are required to ensure good RF performance. Placing them close to the connection pad of the module and connecting them with low resistance tracks to VBAT and GND is strongly recommended.

☞Host power must be capable of sourcing enough current to accommodate the maximum power in cases of 2G transmission bursts. This can be done, for example, by adding a large capacitor with a low ESR value.

☞PCB tracks must be well dimensioned to support 2.2A maximum current. Voltage ripple caused by serial resistance of power supply path could result in voltage drop cases.

☞The HiLo3G does not manage battery charging.

3.5 UART

The HiLo3G has one UART port that can be used in the low-speed, full-speed, and high-speed modes. The UART communicates with serial data ports that conform to the RS-232 interface protocol. With a properly written and user-defined download program, the UART can be used as the serial data port for testing and debugging.

☞Management of external access to the V24 interface, in order to allow easy software upgrades is recommended.

☞Baud rate up to 4Mbps

☞Unused signals remain disconnected.

Signal name	Signal use (DTE point of view)
UART_DSR	Signal UART interface is ON
UART_DCD	Signal data connections in progress
UART_TX	Transmit data
UART_CTS	Signal HiLo3G is ready to receive AT commands, has woken up

UART_RX	Receive data
UART_RTS	Wakes up the module when Ksleep=1 is used
UART_RI	Signal incoming calls (voice and data), SMS, etc.
UART_DTR	Prevents the HiLo3G from entering into the sleep mode Switches between the data mode and the command modes Wakes up the module.

3.5.1 Complete V24—Connection HiLo3G -host

A V24 interface is provided on the 40 pins of the HiLo3G module with the following signals: *RTS/CTS*, *RXD/TXD*, *DSR*, *DTR*, *DCD*, *RI*.

☞The use of this complete V24 connection is required whenever your application exchanges data.

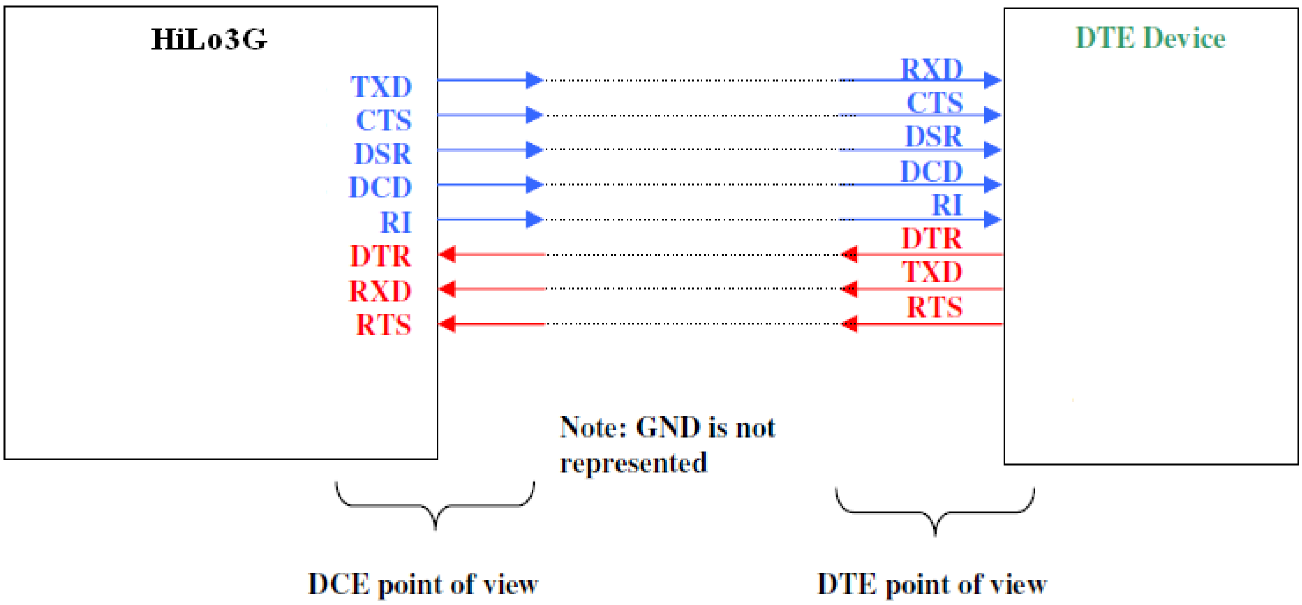


Figure 17: Complete V24 connection between the HiLo3G and the host

This configuration allows the use flow control RTS & CTS to avoid any overflow error during data transfer. Also, CTS is used to signal when the HiLo3G is ready to receive an AT command after a power up sequence or a wake up from the sleep mode.

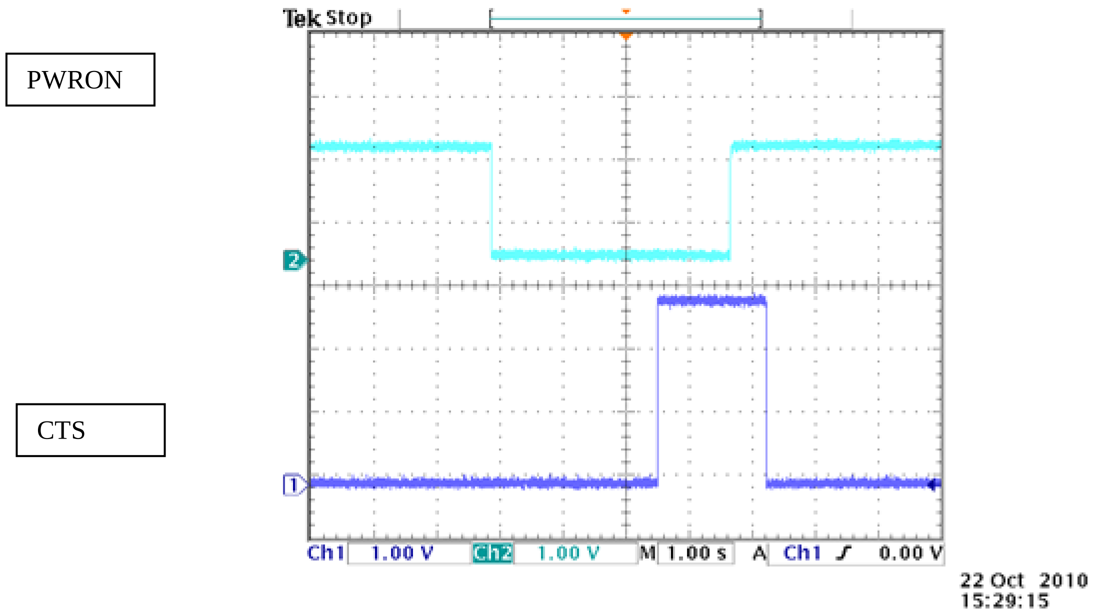


Figure 18: CTS versus PWRON signal during the power on sequence

In addition, this signal configuration enabled all signals :
• *RI* signal used when programmed to indicate an incoming voice or data call or SMS incoming message, etc.
• *DCD signal* used to signal the GPRS connections
• *DSR signal* used to signal that the module UART interface is ON
• *DTR signal* used to prevent the HiLo3G from entering into the sleep mode, switching between Data and AT commands, hanging up a call or waking up the module etc.

☞Pull-up resistors of 100KΩ to VGPIO must be connected to *DCD*, *DSR* and *RI* signals.

☞Avoid supplying the UART before the HiLo3G is ON, this may result in power up sequence error.

3.5.2 Complete V24 Interface with PC

To use theV24 interface, some adaptation of components is necessary to convert the signals from the HiLo3G to +/- 5V signals compatible with a PC.

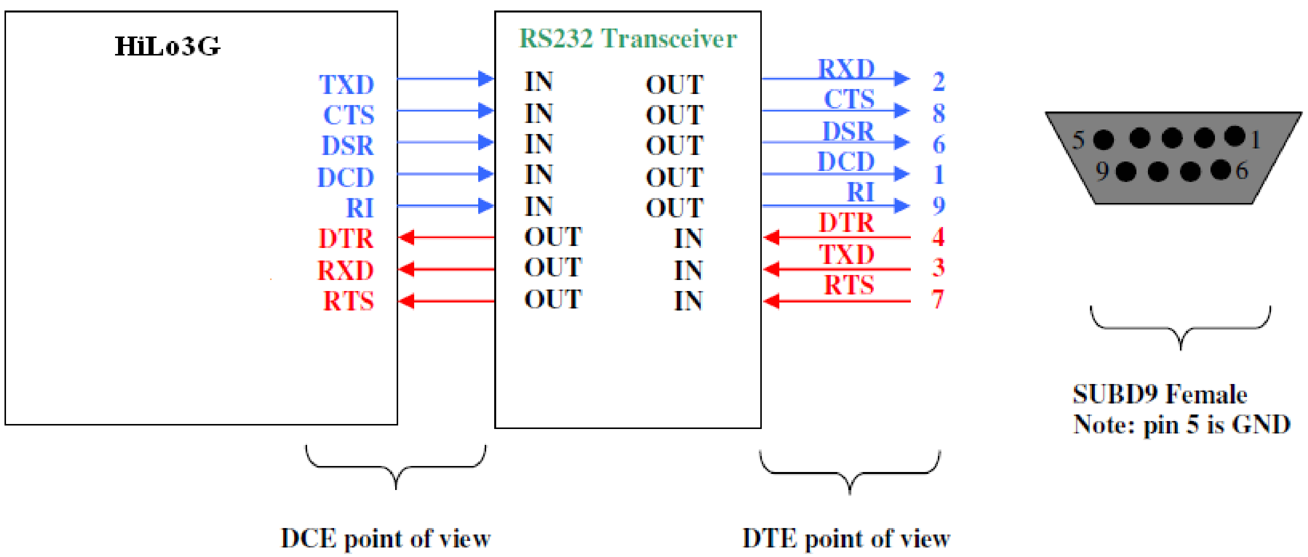


Figure 19: Connection to a data cable

☞Pull-up resistors of 100KΩ to VGPIO must be connected to *DCD*, *DSR* and *RI* signals.

☞Avoid supplying the UART before the HiLo3G is ON, this could result in bad power up sequence. To have a proper behavior use the signal VGPIO to enable the RS232 Transceiver.

3.5.3 Partial V24 (RX-TX-RTS-CTS)—Connection HiLo3G -host

When using only *RX/TX/RTS/CTS* instead of the complete V24 link, the following schematic could be used.

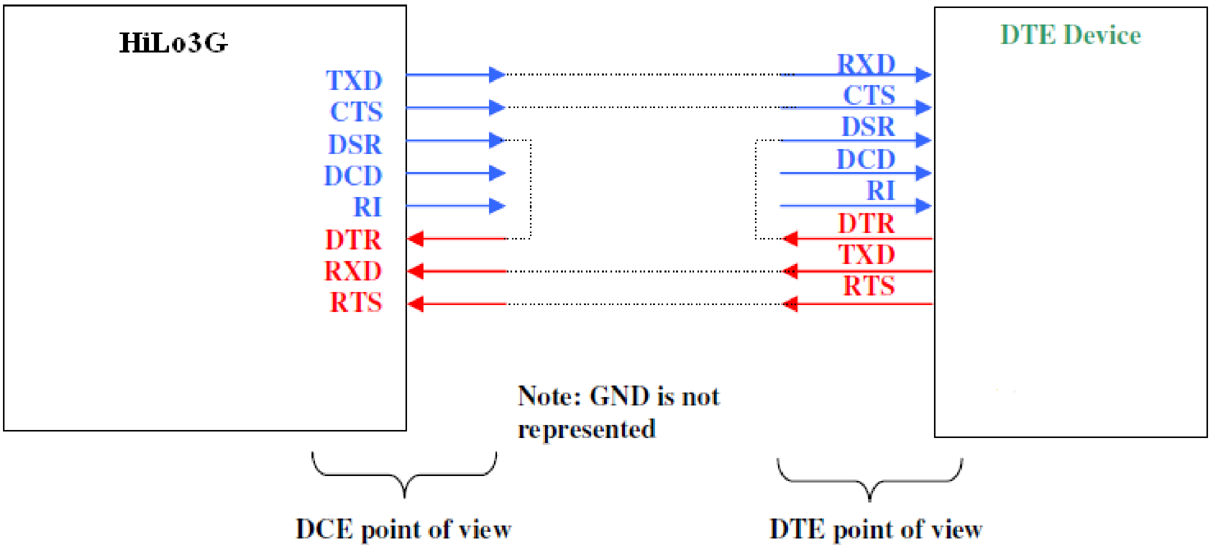


Figure 20: Partial V24 connection (4 wires) between HiLo3G and host

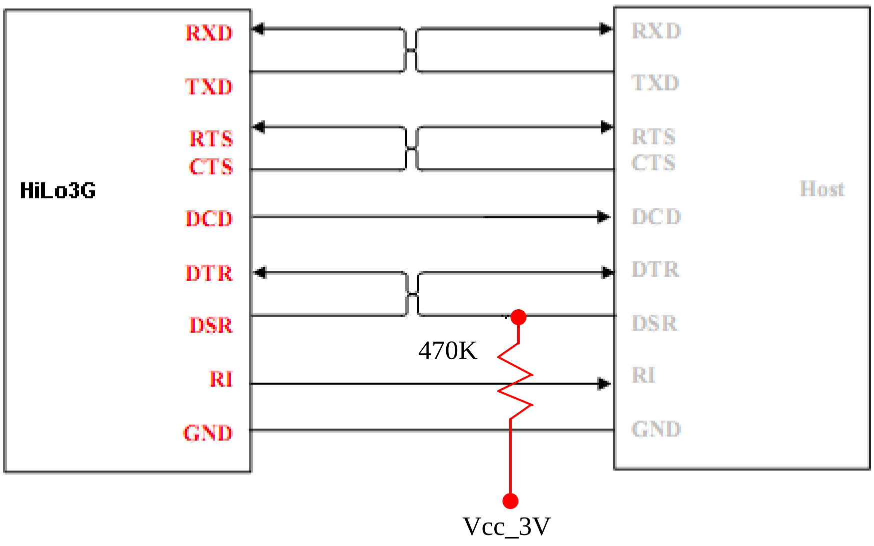
☞As *DSR* is active (low electrical level) once HiLo3G is switched on, *DTR* is also active (low electrical level), therefore AT command AT+Ksleep can switch between the two sleeps mode available for HiLo3G.

☞*DTR* input signal is internally pull upped to VGPIO with a 100KΩ, this result in 28µA of extra consumption.

☞*DCD* and *RI* can stay not connected and floating when not used. Otherwise use 100KΩ pull up to VGPIO.

This configuration allows using the flow control RTS & CTS to avoid any overflow error during the data transfer, CTS is moreover used to signal when HiLo3G is ready to receive an AT command after a power up sequence or a wake up from sleep mode.

☞However this configuration does not allow the signaling signals like:
• *RI* signal used when programmed to indicate an incoming voice or data call or SMS incoming etc…
• *DCD* signal used to signal the DATA connections
• *DSR* signal used to signal the module UART interface is ON (need to pull high *DSR* with 470K ohm to external 3V, shown as below)



• *DTR* signal used to prevent HiLo3G from entering into sleep mode or to switch between Data and AT commands or to hang up a call or to wake up the module etc…

3.5.4 Partial V24 (RX-TX)—Connection HiLo3G -host

When using only *RX/TX* instead of the complete V24 link, the following schematic could be used.

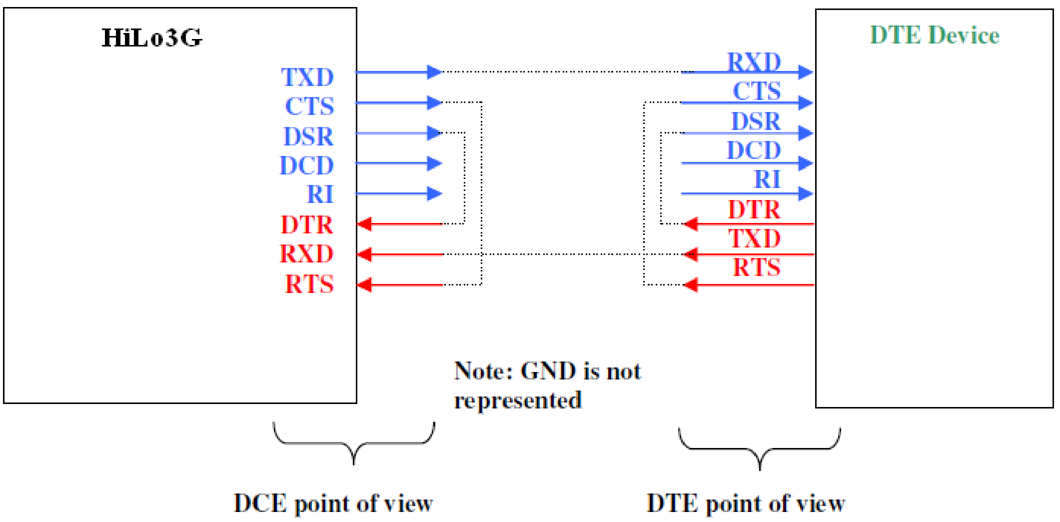


Figure 21: Partial V24 connection (2 wires) between HiLo3G and host

☞ As *DSR* is active (low electrical level) once HiLo3G is switched on, *DTR* is also active (low electrical level), therefore

AT command AT+Ksleep can switch between the two sleep modes available for HiLo3G.

☞*DTR* input signal is internally pulled up to VGPIO with a 100KΩ, this result in 28µA of extra consumption

☞As *CTS* is active (low electrical level) once HiLo3G is switched on, *RTS* is also active (low electrical level), therefore AT command AT+Ksleep can switch between the two sleep modes that are available for HiLo3G. The HiLo3G's firmware allows the rise of CTS during the sleep state even when looped to RTS signal.

☞*DCD* and *RI* can stay disconnected and floating when not used. Otherwise use 100KΩ pull up to VGPIO.

☞Moreover this configuration does not allow the signaling signals as below:
• *RI* signal used when programmed to indicate an incoming voice or data call or SMS incoming etc…
• *DCD* signal used to signal the GPRS connections
• *DSR* signal used to signal the module UART interface is ON
• *DTR* signal used to prevent the HiLo3G module from entering into sleep mode

3.6 GPIO

There are three GPIOs available on HiLo3G. Customer application can directly use them through the appropriate AT command as:
- Output: pin is set to High or Low state
- Input: pin is read on request and answer is given to the customer application

As input, different cases are possible to cover the maximum possibility of customer application:
• Synchronous answer to the AT command
• Asynchronous answer to the AT command. The customer application prior to the request has configured the GPIO to react on falling/rising edges. The customer application is notified asynchronously by AT command answer when the configured trigger occurs.

Configuration type	Configuration description
Input	1. No pull-up 2. Pull-up 3. Pull-down 4. Keeper
Output	1. No pull-up 2. Pull-up 3. Pull-down 4. Keeper 5. Programmable drive current (2–16 mA in 2 mA steps) 6. Tri-state

Figure 22: Programmable GPIO configurations

Thanks to some other special AT commands, GPIOs can for example be used:
1. Make an I/O toggling while the module is attached to the network
2. Make an I/O toggling when a programmed temperature is reached
3. As input to detect the presence of an antenna (with some external additional electronic)
4. As input to detect the SIM card presence …etc

3.7 ADC

There is one ADC input pin which can be used to read the value of the voltage applied. Following characteristics must be fullfilled to allow proper performances:
• The input signal voltage must be within 0V and up to 2.1V
• The input impedance of the pin is 2KΩ
• The input capacitance is typically 53pF.

The AT command AT+KADC will return the voltage value with the following characteristics:
• 12 bits resolution
• Maximum sampling frequency is 2.4MHz.

3.8 Backup Battery

3.8.1 Backup Battery Function Feature

3.8.1.1 With Backup Battery

A backup battery can be connected to the module in order to supply internal RTC (Real Time Clock) when the main power supply is removed. Thus, when the main power supply is removed, the RTC is still supplied with power and the module keeps the time register running.

- If *VBAT* < 3V, internal RTC is supplied by *VBACKUP*.
- If *VBAT* ≧3V, internal RTC is supplied by *VBAT*.

3.8.1.2 Without Backup Battery

Without backup battery

☞If VBAT ≥ 1.5V, internal RTC is supplied by VBAT.

☞If VBAT < 1.5V, internal RTC is not supplied.

☞To calculate the backup battery capacity; consider that current consumption for RTC on the backup battery is up to 2µA depending on the temperature.

Pin Name	Min	Max
VBACKUP		2uA

3.8.2 Charge by Internal HiLo3G Charging Function

The charging function is available on HiLo3G without any additional external power supply (the charging power supply is provided by the HiLo3G).

☞Charge of the back-up battery occurs only when main power supply *VBAT* is provided.

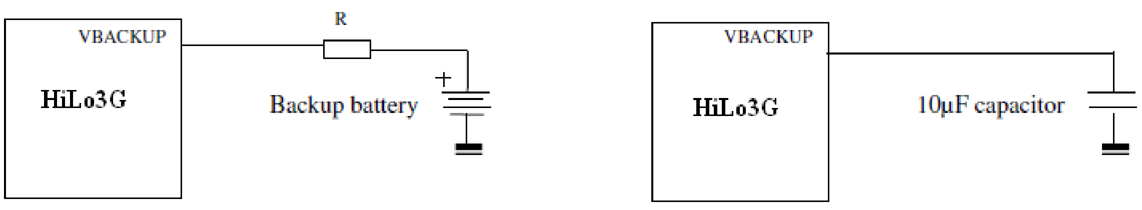


Figure 23: Backup battery or 10µF capacitor internally charged

The resistor R depends on the charging current value provided by the battery manufacturer.

3.8.3 Backup Battery Technology

3.8.3.1 Capacitor Battery

These kinds of backup battery do not have the drawbacks of the Lithium Ion rechargeable battery.
As there are only capacitors:

- The maximum discharge current is generally bigger,
- There is no need to regulate the charging current.

Moreover, this kind of battery is available in the same kind of package than the Lithium Ion cell and fully compatible on a mechanical perspective. The only disadvantage is that the capacity of this kind of battery is significantly smaller than Manganese Silicon Lithium Ion battery. But for this kind of use (supply internal RTC when the main battery is removed), the capacity is generally enough.

3.9 USB

There is one set USB_DP and USB_DN bi-directional differential USB data lines are compliant to the USB2.0 specification.
HiLo3G is USB-Slave while customer application is USB-Master.
• Integrated high-speed USB PHY
• USB 2.0 specification-compliant as a peripheral
•The USB 2.0 specification requires hosts such as PCs to support all three USB speeds, namely low-speed (1.5 Mbps), full-speed (12 Mbps) and high-speed (480 Mbps). The USB 2.0 specification allows peripherals to support any one or more of these speeds.
• USB selective suspend and remote wake-up

☞The USB_DP and USB_DN signals are routed as a ~90 Ω differential pair. These signals must be routed side by side and on the same layer and their trace length should match as close as possible.

☞2 pF capacitor is required to be installed between USB_DP and USB_DN and put close to the HiLo3G.

☞These signals have relatively fast edges, so they should be routed away from sensitive circuits and signals such as the 19.2 MHz TCXO, sleep XTAL, and RF. Therefore, do not route these signals on surface layers, it is preferred to be routed in the inner layer routing sandwiched between power and ground.

4. Power Management

The host system shall supply 3.2V~4.4V to VBAT for powering the baseband, logics circuit and RF circuit.

4.1 Power Modes

Depending on the state of the HiLo3G, different power consumption modes can be identified.

☞Active mode (Active communication)
All systems on HiLo3G are active. In this mode, the module is registered to the network and a voice/data call is actively transmitting data.

☞Sleep mode (Active idle)
All systems on HiLo3G are active including the USB bus. In this mode, the module is registered to the network but it is idle/paging only. No voice/data call connection is established.

☞Fly mode
The processor is still active but the radio section is powered down. This mode can be controlled by sending an AT command to the module.

4.2 Module Power up

There are two ways to start HiLo3G, one is using PWON and the other is using USB.

4.2.1 PWON Power up

To start the module, first power up *VBAT*, which must be in the range 3.2V ~ 4.4V, and able to provide 1.75A during the TX bursts.

☞*PWON* is a low level active signal internally pulled up to a dedicated power domain to 2.9V.
As *PWON* is internally pulled up, a simple open collector or open drain transistor can be used for ignition.

☞To start the module, a low level pulse must be applied on *PWON* during 500ms.

After a few seconds, the *CTS* goes to the active state when the module is ready to receive AT commands.
☞ *VGPIO* is a supply output from the module that can be used to check if the module is alive.
• When *VGPIO* = 0V the module is OFF
• When *VGPIO* = 2.9V the module is ON

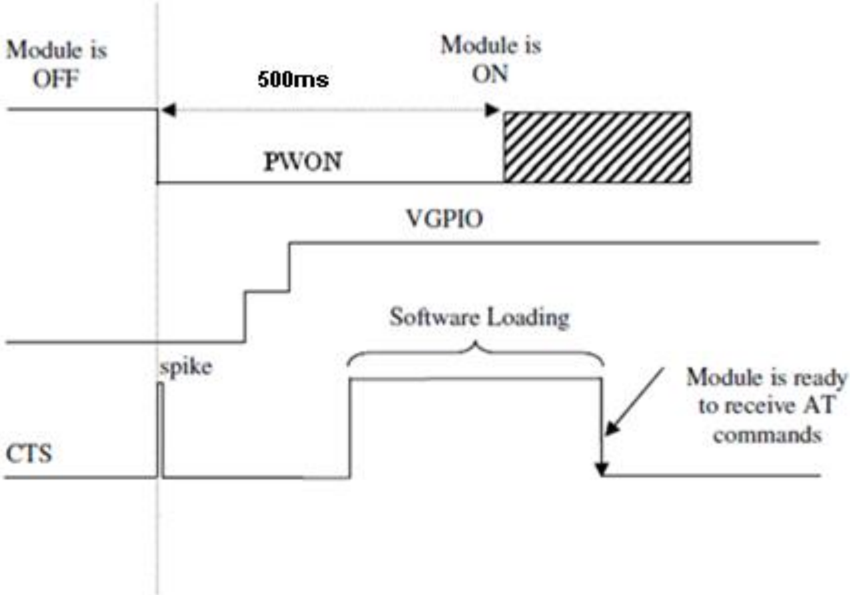


Figure 24: Power on sequence

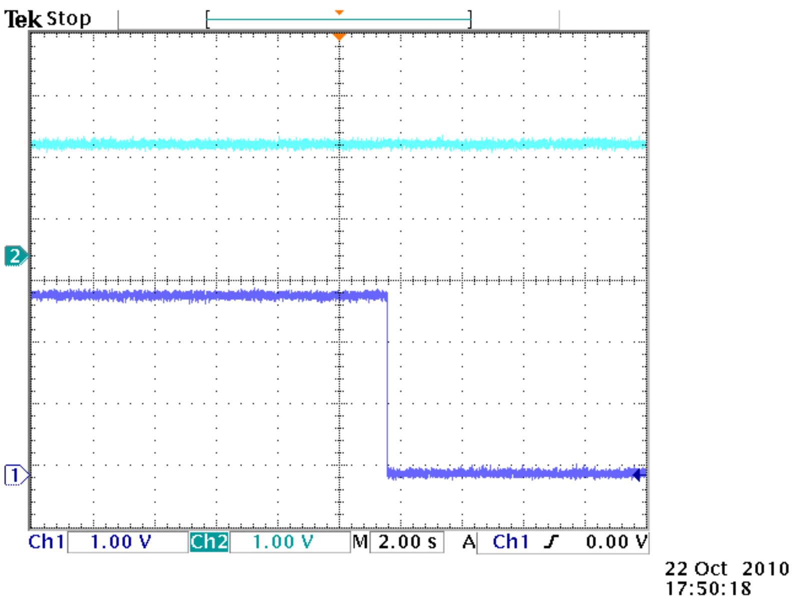


Figure 25: Power off sequence

☞ Send AT COMMAND “AT+CPOF “ to power off module.

4.2.1.1 IO DC Presence before Power on

When the VBAT is available but the module not yet started, the following I/O's raised their output.

☞VBACKUP raise to 3V
☞PWON raise to 1.8V

4.3 Power on and Sleep Diagrams

Those 2 diagrams show the behaviors of the module and the DTE during the power on and then in the sleep modes.
Note: The module cannot enter sleep mode if USB bus is connected.

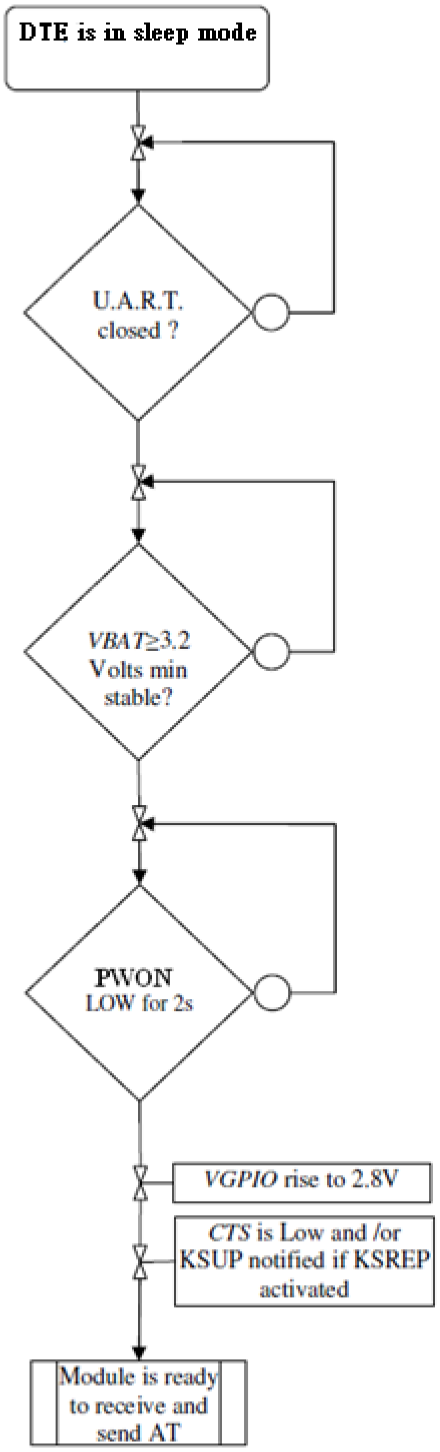


Figure 26: Diagram for the power on

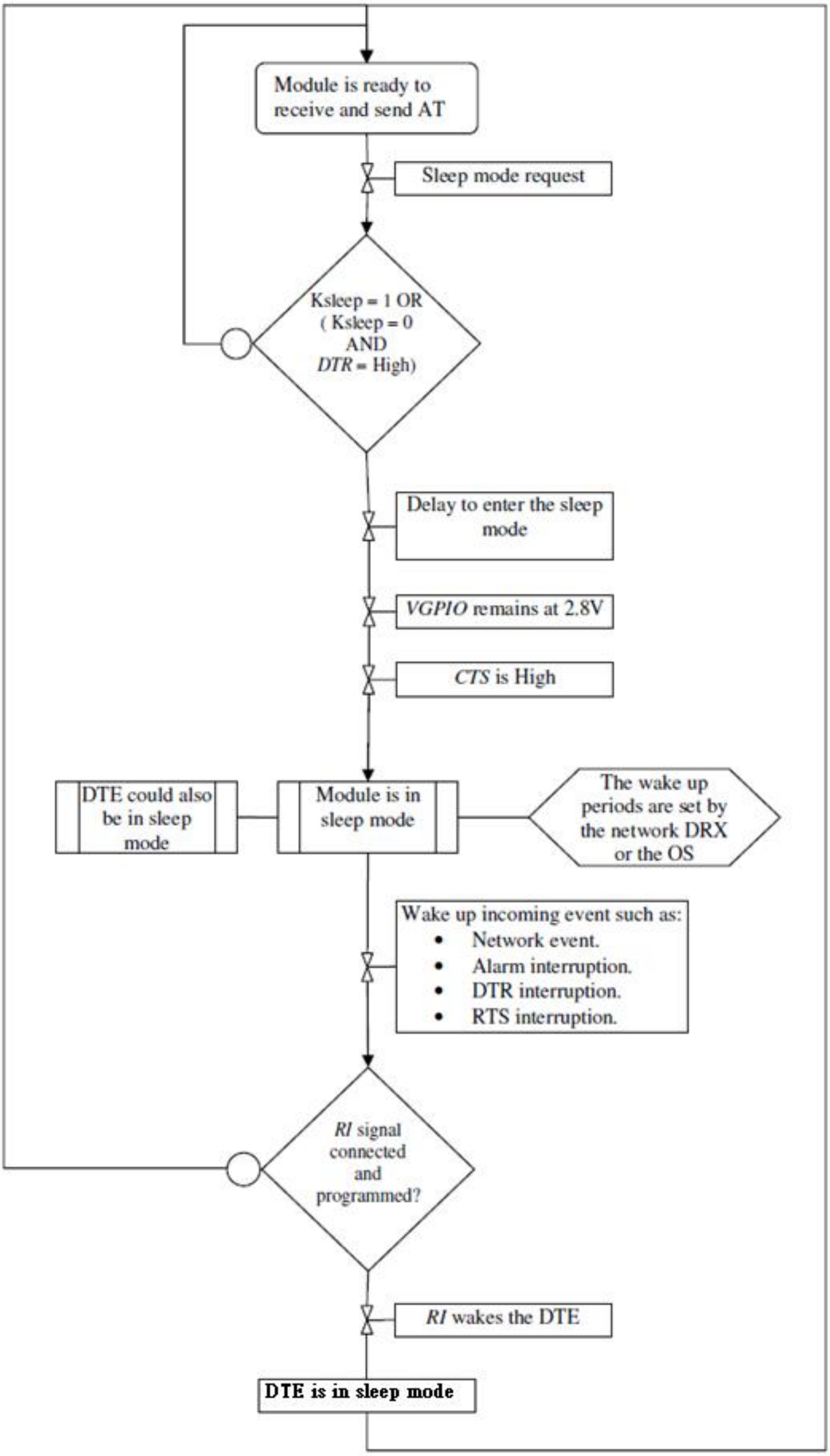


Figure 27: Diagram for the sleep mode

4.4 Module Power off

4.4.1 UART Interface

To stop the module, use the AT command AT+CPOF. If the *PWON* is not pulled down the module will switch to OFF mode after the AT command, otherwise the module restarts immediately (an OFF sequence is performed followed by a power ON sequence).

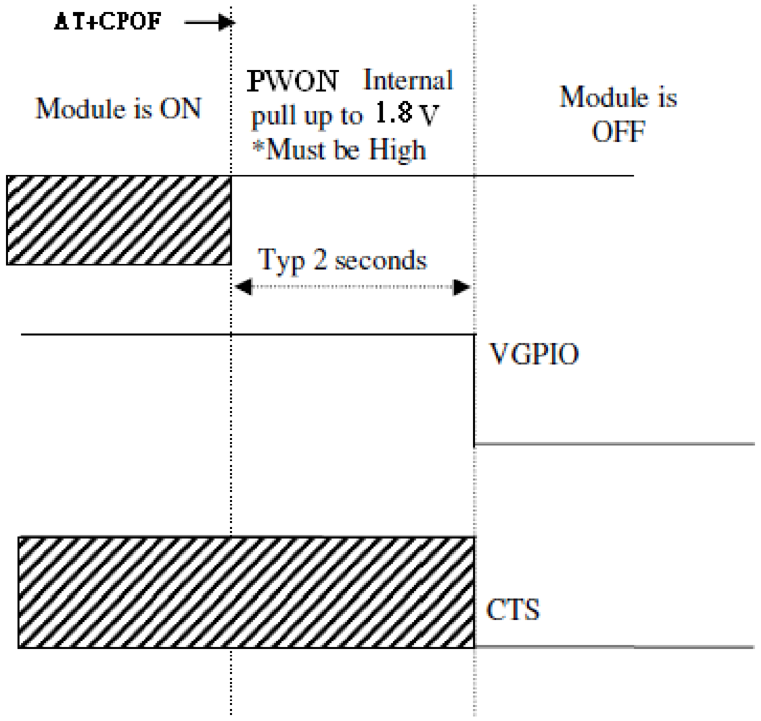


Figure 28: Power off sequence for PWON, VGPIO and CTS

4.4.2 USB Interface

As the module can also start when an USB cable is plugged, the sequence to stop the module needs the USB interface to be OFF or VBUS disconnected just after the command is sent and acknowledged by the module. Thus, to stop the module when the USB interface is being used, use the AT command AT+CPOF, then disconnect VBUS (unplug the USB cable or use a commanded switch to switch off VBUS) signal when the module acknowledges (responds OK) the command, otherwise the module restarts immediately (an OFF sequence is performed followed by a power ON sequence).

4.5 Sleep Mode

The AT command “AT+KSLEEP” allows configuring the sleep mode.

When AT+KSLEEP=1 has been configured:
• The HiLo module decides by itself when it enters in sleep mode (no more task running).
• “0x00” character on serial link wakes up the HiLo3G module.

When AT+KSLEEP=0 has been configured:
• The HiLo3G module is active when *DTR* signal is active (low electrical level).
• When *DTR* is deactivated (high electrical level), the HiLo3G module enters in sleep mode after a while.
• On *DTR* activation (low electrical level), the HiLo3G module wakes up.

When AT+KSLEEP=2 has been configured:
• The Hilo3G module will never enter sleep mode.
In sleep mode the module reduces its power consumption and remains waiting for the wake up signals either from the network, from the operating system or from the host controller.
Note: The module cannot enter sleep mode if USB bus is connected.

5. ESD & EMC Recommendation

Using human body model from JEDEC JESD 22-A114 standard, HiLo3G can hold 2KV on each of the 40 pins and contact areas such as antenna pads and connector.

5.1 Handling HiLo3G

HiLo3G are packaged in boxes.
HiLo3G contains electronic circuits sensitive to human hand's electrostatic electricity.
Handling without ESD protection could result in permanent damages or even destruction of the module.

5.2 ESD Recommendations

If customer's design must be capable of standing the voltage for more than 2KV on electrostatic discharge, the following recommendation must be followed.

ESD current can penetrate into the device via the typical following components:
• SIM connector
• Microphone
• Speaker
• Battery / data connector
• All pieces with conductive paint.

☞ In order to avoid ESD issues, efforts shall be done to decrease the level of ESD current on electronic components located inside of the device (customer's board, input of the HiLo3G, etc…)

5.2.1 Avoid ESD

☞ Ensure good ground connections of the HiLo3G to the customer's board.

☞ Flex (if any) shall be shielded and FPC connectors shall be correctly grounded at each extremity.

☞ Put capacitor 100nF on battery, or better put varistor or ESD diode in parallel on battery and charger wires (if any) and on all power wires connected to the module.

☞ Uncouple microphone and speaker by putting capacitor or varistor in parallel of each wire of these devices.
Here are the pin number to be protected over 2KV and references of varistors.

Pin1/2/39/40: VBAT
Pin5/6/7: USB
Pin10: VGPIO
Pin15/16/24/25: USIM
Pin19/20: Microphone
Pin21/22: SPK

Part	Vendor	Part number
Varistor	LITTLEFUSE	V0402MHS12NR
Varistor (for USB line)	COOPER	0402ESDA-MLP1

5.3 EMC recommendations

In case of EMC issue due to a headset audio device, the solution may consist in inserting a filter on the wires of the microphone and of the speaker.

6. Radio Integration

HiLo3G incorporates the technology for RF transceiver that converts received signals directly from RF-to-baseband and transmits signals directly from baseband-to-RF (known as direct conversion or zero intermediate frequency (ZIF) processing). This technique eliminates the need for large IF surface acoustic wave (SAW) filters and supporting IF and LO circuits.

6.1 Antenna Connection

HiLo3G provides two methods to connect an antenna, one is spring contact and the other is UFL RF connector.

☞Definition of the reference antenna connector:
• Strictly 50 Ohms matched impedance PCB tracks
• Straight PCB tracks

☞Antenna gain:
• Radiation pattern: depending on antenna position and size of the device
• Gain averaged in space in all frequencies: > -3dBi
• Maximum VSWR: < 1.5:1 with 50 Ohms reference impedance

In order to get the best sensitivity and output power, it is recommended to implement a matching circuit between the module and the antenna:

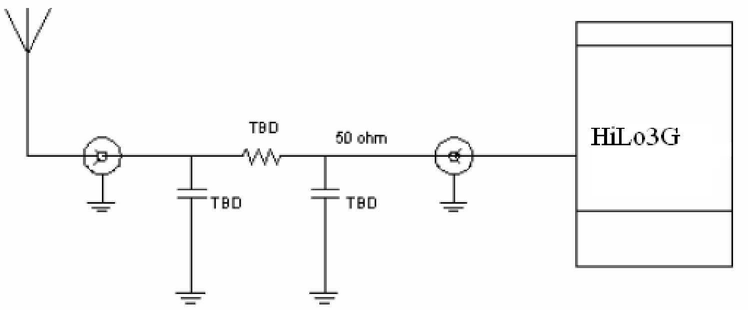


Figure 29: Antenna connection reference

6.1.1 Antenna Connector

A 50-Ohm RF connector on the HiLo3G PCB is available for antenna (RF cable) connection.

Reference
HIROSE U.FL-R-SMT-1 (10)

6.1.2 Spring Contact

☞50 Ω line matching

☞Recommends to solder the spring contact on the whole surface instead of only 2 points

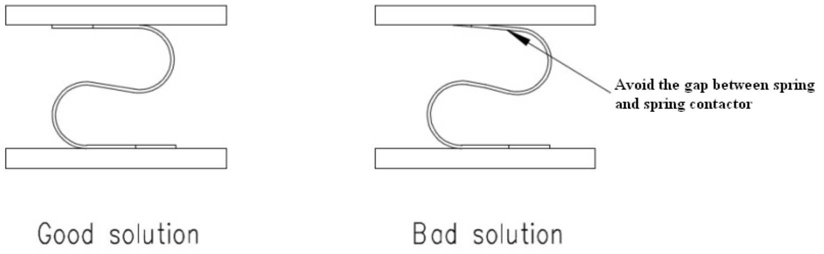


Figure 30: Spring contact

6.1.3 Antenna Notice

☞Antenna for HiLo3G should be resonated in the operating bands (GSM 850, 900, 1800, 1900 + UMTS band 1, 2, 5,8) depending on HiLo3G reference.

☞Pay attention to the RF-impedance of the HiLo3G (50Ω)

☞Use low loss antenna cable (max. 0.5dB).

☞To avoid interference choose an antenna type radiating off the device.

☞Circular polarized antennas are preferred.

☞Verify the operation of the antenna by measurement of the total radiated power.

☞Avoid placing a transmit antenna close to sensitive areas (danger from interference).

☞Apply EMC-design rules and follow shielding concepts.

☞ Separate of EMC-sensitive and high-emission areas.

6.2 Ground Link Area

Good ground GND contact between the module and customer's board is required to have the best radio performances (spurious, sensitivity…)

☞ All HiLo3G GND pins must be connected to the GND of the customer's board.

☞ Solder the three pads of the shielding on the ground pads of customer board, then the HiLo3G will have a good ground contact with the customer board.

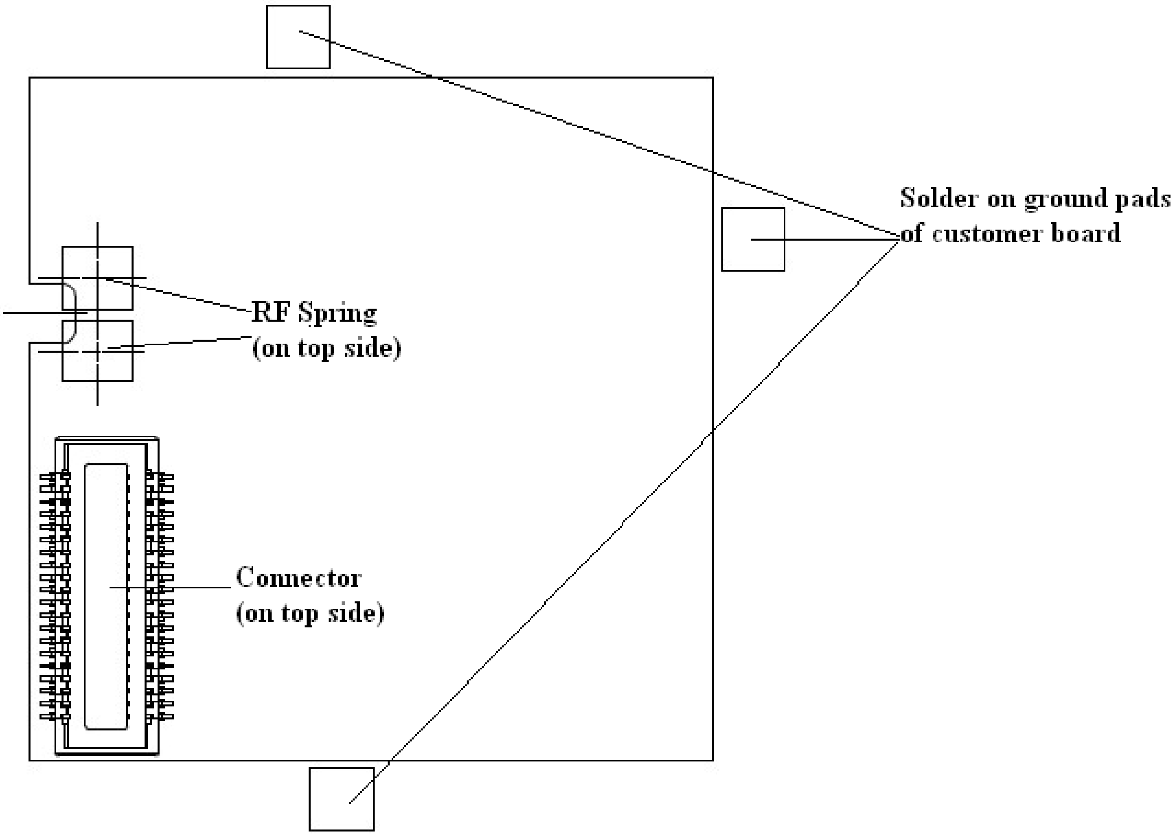


Figure 31: Ground HiLo3G to customer board

6.3 Layout

☞Isolate RF line and antenna from other bus or signals

☞No signals on 50 ohms area and if that is not possible, add ground shielding using different layers.

☞Do not add any ground layer under the antenna contact area.

☞ Do not add signal unvarnished layout trace on the first layer of the customer board, or unvarnished via holes under the module shield area or it will result on short circuit on those signals. This is mandatory.

☞Free CAD software can be used to compute the stack-up parameters that leads to a compliant 50Ω RF track.

6.4 Mechanical Surrounding

☞Do not apply mechanical pressure over the HiLo3G shield, doing so could damage the mechanical structure of the shield and lead to internal short-circuits or other undesirable issues.

☞Avoid letting any metallic part be around the antenna area

☞Keep FPCs and battery contact (if any) away from antenna area.

☞ FPC's (if any) have to be shielded

6.5 Other Recommendation—test for production/design

SagemCom guarantees the RF performances in conductive mode but strongly recommends making RF measurements in an anechoic chamber in radiated mode (tests conditions for FTA): the radiated performances strongly depend on radio integration (layout, antenna, matching circuit, ground area…..)

7. Audio Integration

Audio mandatory tests for FTA are done in handset mode only so a particular care must be taken to the design of audio (mechanical integration, gasket, electronic) in this mode.
The audio norms which describe the audio tests are 3GPP TS 26.131 & 3GPP TS 26.132.

7.1 Mechanical integration and acoustics

Particular care to Handset Mode:
To get a better audio output design (speaker part) :

☞The speaker must be completely sealed on the front side.

☞The front aperture must be compliant with speaker supplier's specifications

☞The back volume must be completely sealed.

☞The sealed back volume must be compliant with speaker supplier's specifications

☞Take care of the design of the speaker gasket (elastomer).

☞ Foresee a stable and large enough area for the gasket of the artificial ear.

To get a better audio input design (microphone part) :

☞Take care of the design of the microphone (elastomer).

☞All receivers must be completely sealed on the front side.

☞ Microphone sensitivity depends on the shape of the device eg. about –40 ±3 dBV/Pa.

☞Promote the use of pre-amplified microphone. If needed, use a pre-amplification stage.

As audio input and output are strongly linked:

☞Place the microphone and the speaker as far as possible from one another.

7.2 Electronics and layout

Avoid Distortion & Burst noise

☞ Audio signals must be symmetric (same components on each path).

☞Differential signals must be routed parallel.

☞Audio layer must be surrounded by 2 ground layers.

☞The link from one component to the ground must be as short as possible.

☞If possible separate the PCB of the microphone and the one of the speaker.

☞Reduce as many as possible the number of electronics components (loss of quality, more dispersion).

☞Audio tracks must be larger than 0.5 mm.

8. Recommendations on layout of customer's board

8.1 General recommendations on layout

There are many different types of signals in the module which are disturbing each other. Particularly, Audio signals are very sensitive to external signals as *VBAT*... Therefore it is very important to respect some rules to avoid disruptions or abnormal behavior.

☞ Magnetic field generated by *VBAT* tracks may disturb the speaker, causing audio burst noise. In this case, modify layout of the *VBAT* tracks to reduce the phenomena.

8.1.1. Ground

☞ A ground plane as complete as possible

☞ Ground of components has to be connected to the ground layer through many vias not regularly distributed.

☞Top and bottom layer shall have as much as possible of ground planes. Flood the empty remain surface of the layout of those two layers with a ground plane connected to main ground with as much vias as possible.

8.1.1.1 Ground layout guidelines

☞Proper grounding is crucial to end-product performance. At least one layer must be a dedicated ground plane. This ground plane is the common point referenced by all end-product circuits.

☞In addition to the dedicated ground plane layer, any unused space on all PCB layers should be filled with ground to provide the most robust grounding from layer to layer.

☞Bypass capacitors should be connected directly to their surface layer ground fill. Multiple vias should connect each capacitor directly to the main ground plane, with one via in the capacitor's pad plus several vias within the surface layer ground fill area.

8.1.1.2 Digital ground

Digital ground should via directly to the main ground plane. In addition, each layer between layers 1 and main ground should include ground fills directly below the center grid area's digital pins, with each stack of vias connecting to each ground fill area. The large mass of copper tied together using this technique provides the best possible electrical ground and thermal conductivity.

8.1.1.3 Analog/RF ground

The analog/RF ground pins are connected together with one another, but isolated from the digital ground (until main ground). Like the digital pins, the analog/RF pins should via directly to the main ground plane. In addition, each layer between layers 1 and main ground should include ground fills directly below the outer layer's analog/RF pins, with each stack of vias connecting to each ground fill area. The large mass of copper tied together using this technique provides the best possible electrical ground and thermal conductivity.

8.1.2 Power supplies

☞Layer for power supply signals (*VBAT*, *VGPIO*) is recommended.
☞Any loop of power signals layout must be avoided on the design.
☞Suitable power supply (*VBAT*, *VGPIO*) track width and thickness.

8.1.3 Clocks

☞Clock signals must be shielded between two grounds layer and bordered with ground vias.

8.1.4 Data bus and other signals

☞ Data bus and commands have to be routed on the same layer, none of the lines of the bus shall be parallel to other lines
☞ Lines crossing shall be perpendicular
☞Suitable other signals track width, thickness.
☞Data bus must be protected by upper and lower ground plans

8.1.5 Radio

☞ Provide a 50 Ohm micro strip line for antenna connection

8.1.6 Audio

☞Differential signals have to be routed together, parallel (for example *HSET_P*/*HSET_N*).
☞Audio signals have to be isolated, by pair, from all the other signals (ground all around each pair).
☞Cancel any loops between *VBAT* and *GND* next to the speaker to avoid the TDMA burst noise in the speaker during a communication.

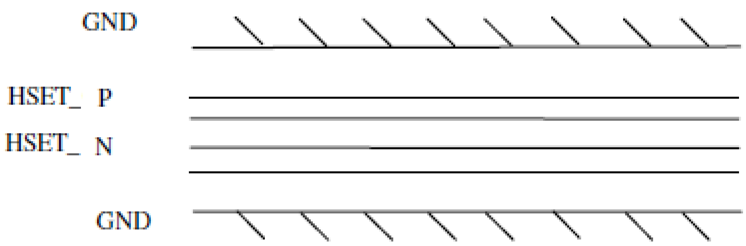


Figure 32: Layout of audio differential signals on a layer n

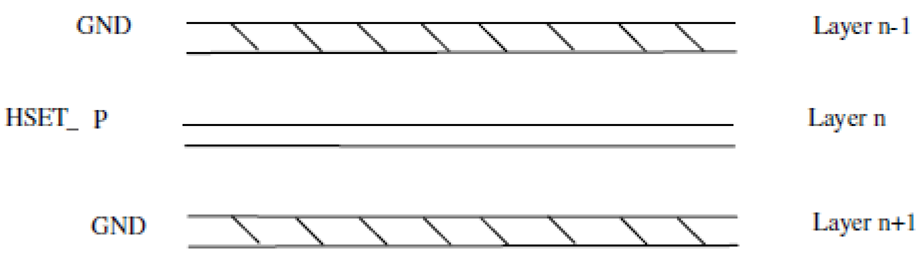


Figure 33: Adjacent layers of audio differential signals

8.1.7 Shielding

A few shielding comments are provided for designer consideration:

☞At least the following devices and circuits should be shielded:

- High-speed memory
- RF front-end components
- Crystal circuits
- DC/DC circuits
- RF circuitry

☞Recommended shield partitioning:

- RF matching components, do not locate matching inductors too close to shield walls (this may cause electromagnetic coupling and inductor de-Q).
- Memory devices must be shielded.
- The crystal circuits (other than the reference for RF frequency synthesizers) must be very close to their corresponding pins.
- Metalized plastic is not as effective as metal cans.
- Shielded inductors might be needed in the DC/DC circuits, or they might need to be placed in their own shield area.

8.2 Example of layout for customer's board

The following figure shows an example of layer allocation for a 6- layers circuit (for reference only):
Depending on the customer's design the layout could also be done using 4 layers.

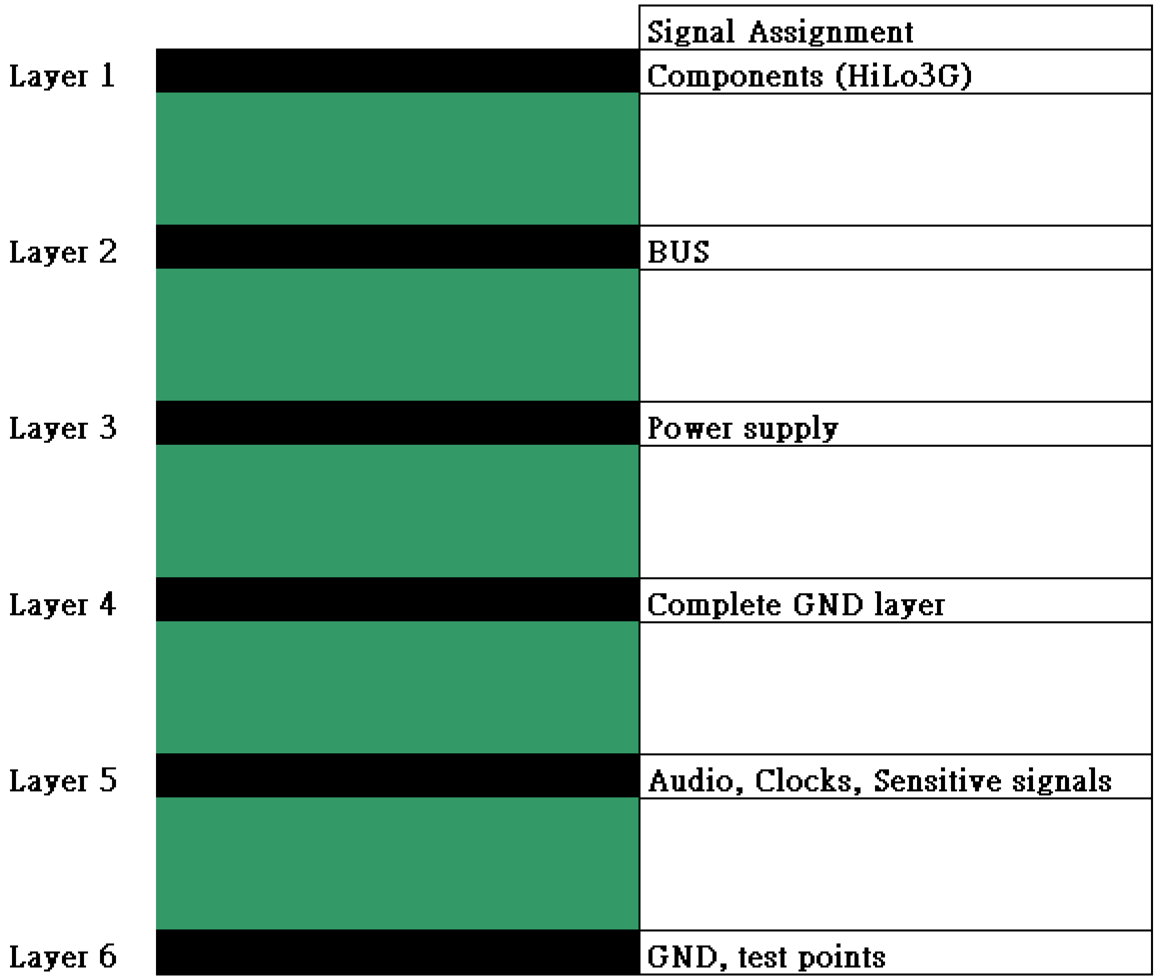


Figure 34: Reference 6 layers PCB stack

9. Label

The HiLo3G is labeled with its own FCC ID (VW3HILO3G) on its shield side. When the module is installed in customer's product, the FCC ID label on the module will not be visible. To avoid this case, an exterior label must be stuck on the surface of customer's product signally to indicate the FCC ID of the enclosed module. This label can use wording such as the following: "Contains Transmitter module FCC ID: VW3HILO3G" or "Contains FCC ID: VW3HILO3G".

10. CE/FCC/IC warning statement

10.1 FCC Regulations:

- This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

- This device has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiated radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.
-Increase the separation between the equipment and receiver.
-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-Consult the dealer or an experienced radio/TV technician for help.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

10.2 RF Exposure Information

This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based time-averaging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of §2.1091.

The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons, must not be collocated or operating in conjunction with any other antenna or transmitter, except in accordance with FCC multi-transmitter product procedures.

The end user has no manual instructions to remove or install the device and a separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

Maximum antenna gain allowed for use with this device is 0 dBi.
When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: "Contains FCC ID: VW3HILO3G".

10.3 IC Regulations:

Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

IMPORTANT NOTE:
IC Radiation Exposure Statement:
This equipment complies with IC RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.
This device and its antenna(s) must not be co-located or operating in conjunction with any other antenna or transmitter.

This Class B digital apparatus complies with Canadian ICES-003.
Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p) is not more than necessary for successful communication.

10.4 R&TTE Regulations:

In all cases assessment of the final product must be mass against the Essential requirements of the R&TTE Directive Articles 3.1(a) and (b), safety and EMC respectively, as well as any relevant Article 3.3 requirements.

The maximum antenna gain for frequeny 900 is 0 dBi; for frequeny 1800 is 0 dBi and the antenna separation distance is 20cm.

10.5 Declaration of Conformity

We, Sagemcom SAS,
Address: 250 Route de l'Empereur, 92848 Rueil Malmaison Cedex France
Declare under our own responsibility that the product:
Model: HiLo3G
Intended use: Quad-Band GSM/GPRS/EDGE and Tri-Band WCDMA/HSDPA MODULE

Complies with the essential requirements of Article 3 of the R&TTE 1999/5/EC Directive, if used for its intended use and that the following standards have been applied:

Health (Article 3.1(a) of the R&TTE Directive)

Applied Standard(s):

- EN62311: 2008

Safety (Article 3.1(a) of the R&TTE Directive)

Applied Standard(s):

- EN 60950-1:2006+A11:2009

Electromagnetic compatibility (Article 3.1 (b) of the R&TTE Directive)

Applied Standard(s):

- EN 301 489-1 V1.8.1/-7 V1.3.1/-24 V1.4.1

Radio frequency spectrum usage (Article 3.2 of the R&TTE Directive)

Applied Standard(s):

- EN 301 511 V9.0.2
- EN 301 908-1/ -2 V4.2.1

All the reports of the applied standards have the Positive Opinion of Notified Body:
CETECOM, Untertuerkheimer Str. 6 – 10 66117 Saarbruecken
Identification mark: **0682** (Notified Body) **CE** CE 0682
The technical documentation relevant to the above equipment will be held at:
Sagemcom SAS
250 Route de l'Empereur, 92848 Rueil Malmaison Cedex France