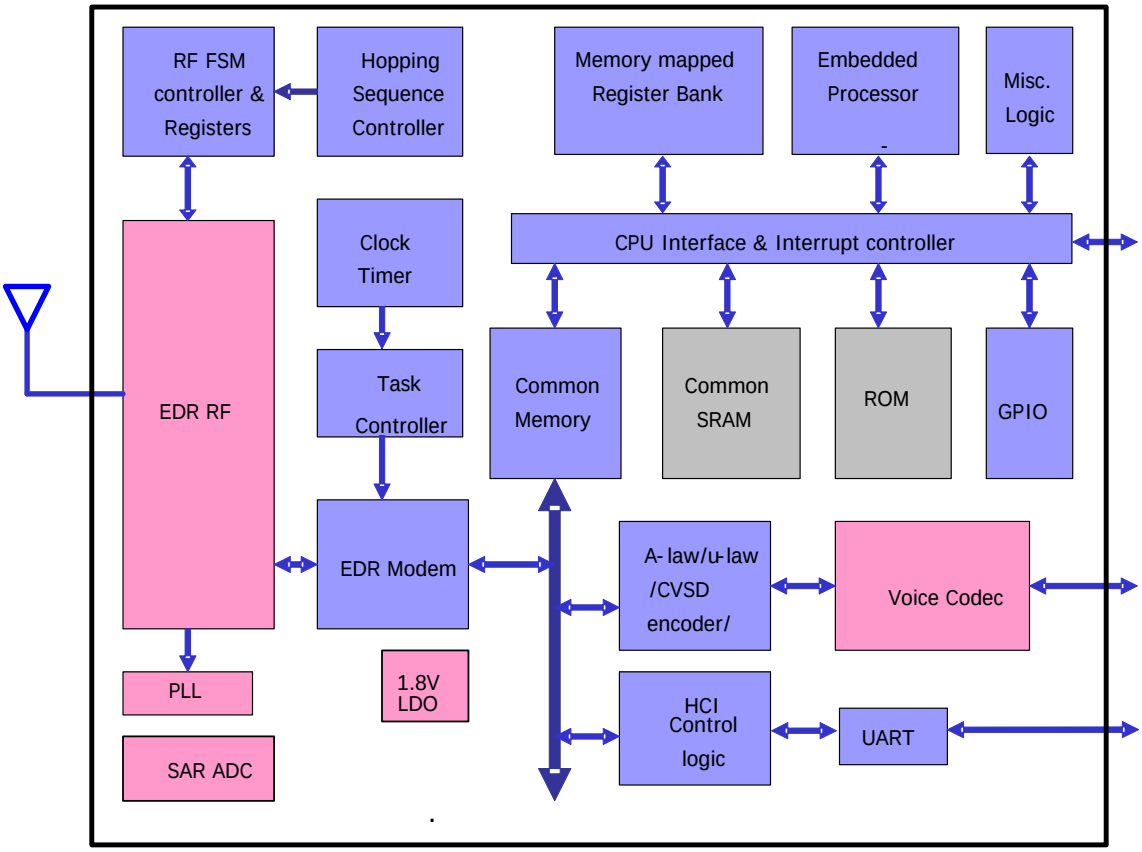
5 Functional Description

5.1 Overall Architecture

The ISSC IS1610N integrates an enhanced EDR Bluetooth RF & BB core, HCI controller, Audio controller and an ENHANCED 8051 processor with an internal mask ROM for program memory and SRAM for data memory. An innovative interconnection structure called the Common-Memory Architecture (CMA) is designed to provide a fast and flexible data movement scheme between the embedded processor, Bluetooth core, and peripheral hardware within this SRAM data memory space.

For audio and power management, IS1610N provide embedded audio code and some power management to reduce the external components.

Figure 1 – Block diagram for IS1610N



5.2 Radio Frequency (RF)

5.2.1 Transmitter

The internal PA has a maximum output power of +4dBm with level control 8dB from amplitude control. This is applied into Class2/3 radios without external RF PA. If you want a larger output power for Class1 application, the external PA can be used.

The transmitter features IQ direct conversion to minimize the frequency drift. And it can excess 30dB power range with temperature compensation machine.

5.2.2 Receiver

The LNA can be operated into two type modes. One type is TR-combined mode for single port application. The other type is TR-separated mode for dual port application that used an external PA/LNA application.

The image rejection filter is to reject image frequency for low-IF architecture. This filter for low-IF architecture is implied to reduce external BPF component for super heterodyne architecture.

The ADC is utilized to sample input analogue wave to convert into digital for de-modulator analysis. Before the ADC, a channel filter has been integrated into receiver channel that can reduce the external component count and increase the anti-interference capacity.

For avoiding temperature variation issues, a temperature sensor with temperature calibration is utilized into bias current and gain control of LNA, Mixers, and RF AMP.

5.2.3 Synthesizer

The internal loop filter is used to reduce external RC components. This can reduce cost and variations for components. This internal LC tank for VCO is utilized to reduce variation for components. The cost is down at the same time.

A fully integrated synthesizer has been created. There requires no external VCO, varactor diode, resonator and loop filter.

5.3 SAR ADC Voltage Converter

The 10-bit Successive-Approximation analog to digital converter (SAR ADC) features 1 dedicated channel for battery power detection and 1 channel for external peripheral temperature sensing. This ADC has 10 bits resolution that provides a high accurate monitoring for battery voltage. The operating current is very low and almost consumes no power when disabled.

5.4 MODEM

There are three different modulations for Bluetooth v2.0 w/ EDR. In figure 2, we summarized these modulations and data rate.

Figure 2 – Modulation type for Bluetooth v2.0 w/ EDR

Data Rate	Modulation	Bits/Symbol
BDR: 1 Mbps	GFSK	1
EDR: 2 Mbps	π/4 DQPSK	2
EDR: 3 Mbps	8DPSK	3

5.4.1 Basic Data Rate MODEM (BDR)

On the Bluetooth v1.2 specification and below, 1 Mbps was the standard data rate based on Gaussian Frequency Shift Keying (GFSK) modulation scheme. This basic rate modem meets BDR requirements of Bluetooth v2.0+EDR specification.

Figure 3 – Data format for BDR

Access Code	Header	Payload

5.4.2 Enhanced Data Rate MODEM (EDR)

On the Bluetooth v2.0+EDR specification, Enhanced Data Rate (EDR) has been introduced to provide 2 and 3 Mbps data rates as well as 1 Mbps. This enhanced data rate modem meets EDR requirements of Bluetooth v2.0+EDR specification. For the viewpoint of baseband, both BDR and EDR utilize the same 1MHz symbol rate and 1.6 KHz slot rate. For BDR, 1 symbol represents 1 bit. However each symbol in the payload part of EDR packets represents 2 or 3 bits. This is achieved by using two different modulations, π/4 DQPSK and 8DPSK.

Figure 4 –Data format for EDR

Access Code	Header	Guard	Sync	Payload	Trailer

For this modulation, each symbol carries 2 bits of information. For its constellation diagram, although there are 8 possible phase states, the encoding scheme guarantees the trajectory of the modulation between symbols is restricted to 4 states. For a given starting point, every phase change between symbols is restricted to +45°, +135°, -45°, and -135°.

Figure 5 –Phase shift & bit pattern for 2 MHz data rate

Phase Shift	Bit Pattern
+45° (+π/4)	00
+135° (+3π/4)	01
-135°(-3π/4)	11
-45°(-π/4)	10

For this modulation, each symbol carries 3 bits of information. For its constellation diagram, it is similar toπ/4 DQPSK but the trajectory of the modulation between symbols has 8 possible phase states. For a given starting point, every phase change between symbols is restricted to 0°, +45°, +90°, +135°, +180°, -135°, -90°, and -45°.

Figure 6 –Phase shift & bit pattern for 3 MHz data rate

Phase Shift	Bit Pattern
0° (+0)	000
+45° (+π/4)	001
+90° (+π/2)	011
+135° (+3π/4)	010
+180° (+π)	110
-135° (-3π/4)	111

-90° (-π/2)	101
-45° (-π/4)	100

5.5 Baseband

The following modules implemented in hardware constitute the Bluetooth Baseband Core. The frequency hopping sequence generator produces the correct hop frequency control sequence based on the Bluetooth clock, Bluetooth device address, and the current operating mode.

The access code generates the access code based on the Lower Address Part (LAP) of the Bluetooth device address. The access code is comprised of the preamble, sync word and trailer bits. The detection of the access code uses correlation to detect a valid access code.

Bluetooth uses two types of FEC: 1/3 repetition code and (15, 10) shorten Hamming code respectively. The former basically repeats each transmitted bit three times while the latter has 15 bits of codeword which contains 5 parity bits. The code has capability of correction of all single-bit errors in each codeword.

The purpose of HEC is to protect the header bits. Dedicated header error code generator calculates the HEC bits in the header of a transmitted packet. While on the receiver side, HEC detects corrupted headers.

A 16-bit CRC is adopted to protect payload data transmitted using certain types of Bluetooth packets.

Information confidentiality can be protected by encryption of the packet payload. Dedicated encryption/decryption hardware is designed into the baseband core.

5.6 MCU

The embedded processor embedded with this version is a single-cycle 8051 CPU. The embedded processor will be referred to as simply the processor, 8051, or MCU throughout the remainder of this document. There are a few minor differences between a standard 8051 and this CPU. These include:

1. Alteration of memory timings to match internal and external memory configurations.
2. Modification of idle mode to disable internal CPU clocking. Only externally-clocked interrupt sources can allow the CPU to recover from idle mode.

A single-port synchronous interface is provided to memory. From this single port, the bandwidth is divided among the 7 interfaces spread amongst 5 physical busses described below:

- Embedded processor bus
- Baseband TX bus
- Baseband RX bus
- HCI TX bus
- HCI RX bus
- Audio bus
- DMA bus

In addition, attached to the embedded processor bus are a register bank, a dedicated single-port memory (data segment 1), and flash memory (program segment). The processor coordinates all link control procedures and data movement using a set of pointer registers. For example, when an HCI packet (from the host via USB or UART) is received into the HCI buffer, the processor is interrupted. The processor can then read a status register to determine the HCI packet type and determine whether to set up the Baseband pointer registers for this memory region for RF-retransmission, or to otherwise directly perform packet processing with the CPU.

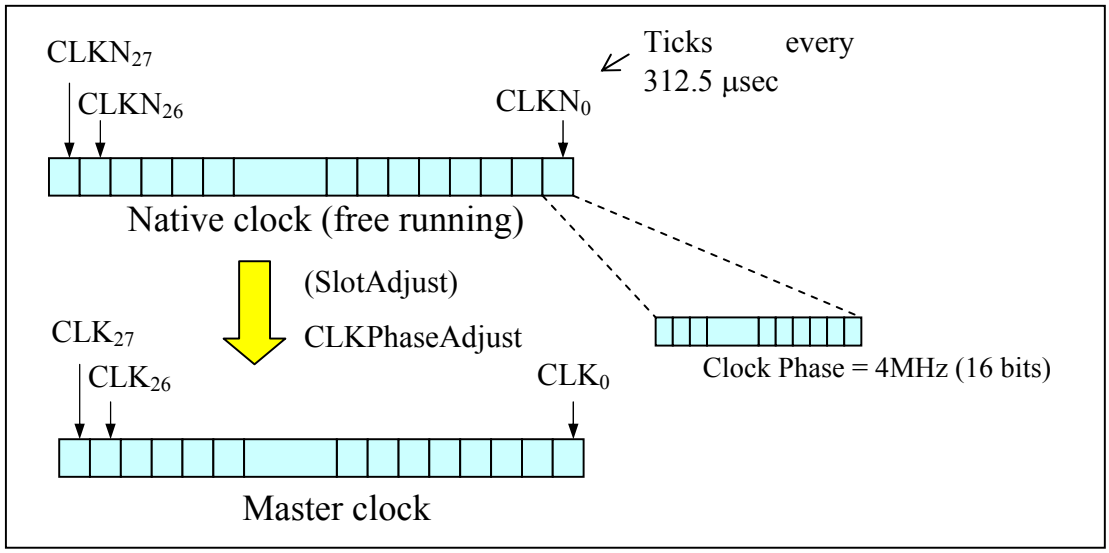
5.7 Bluetooth Clock and Timers

A Bluetooth standard 28-bit counter running at 3.2 kHz implements the native clock defined by Bluetooth specification 1.2. This clock provides the transmission and receiving timing of a half time slot (312.5 μs). Another finer counter implemented in 16 bits is also provided as the phase of a half time slot. This phase information is very helpful when a Bluetooth slave wants to adapt to its master's clock. It is running at 4MHz. The counter is pre-scalable for the purpose of power saving operations. The diagram below describes a standard Bluetooth native clock and master clock. The clock signal is also used as a slot boundary signal to trigger a baseband packet transmission or receipt.

There are four timers provided by the system, two timers for TX/RX and general purpose and the others for general purpose.

The powerful pre-scheduling functions for the transceiver are realized by two sets of programmable timers, namely Task0SlotTimer/Task0PhaseTimer and Task1SlotTimer/ Task1PhaseTimer. Each set of timers is associated with the task of transmission or receiving. When the timer is configured by firmware, it will automatically execute the TX or RX task at a specific time. Sub-tasks and timing for a TX task remain to be defined.

Figure 7 –Bluetooth clock



5.8 Peripherals

Hardwired control logic is presented in front of the UART devices for HCI protocol handling and packet buffering. This control logic is part of the HCI controller defined in Bluetooth specification 1.2. This logic is partially responsible for the HCI protocol handling to/from the host and it also maps the registers of the UART devices indirectly to the 8051 such that the system can receive or send a HCI packet to/from the respective host interface. Major functions of this logic include:

- HCI packet formatter and de-formatter (identifying the packet type)
- Frame boundary determination, segmentation and reassembly of HCI packets.
- HCI packet transmission, receiving, and buffering (using common memory HCI buffer).
- Independent receive / transmit channels
- Universal device interface

An embedded UART (Universal Asynchronous Receiver Transmitter) is included in this design. In order to reduce gate count, only the functions required for the HCI logic are included. These include the following:

- Full-Duplex operation
- Programmable BAUD rate (using 16-bit input clock divider to obtain Baud Rate x16 or x24 or x13 clock base)
- 7 or 8 Data bits
- 1 or 2 Stop bits
- Even / Odd / Mark / Space / None Parity configurations
- Break Generation / Detection
- Maskable individual interrupts to CPU and combined Error interrupt to HCI
- Selectable Direct CPU interface or interface to HCI module

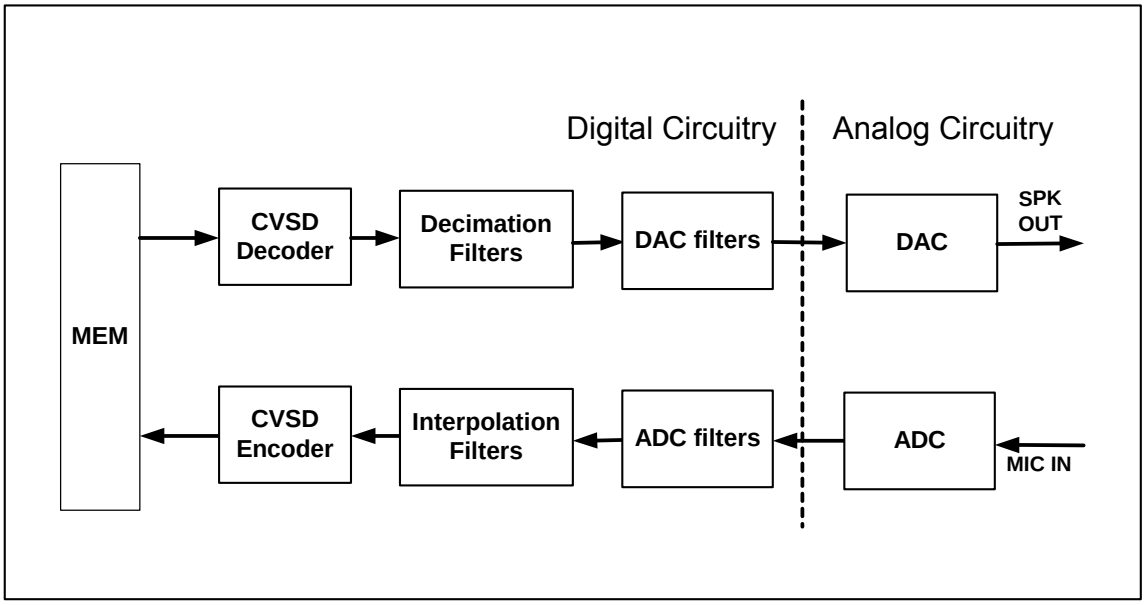
5.9 Voice Codec

The mono audio codec is described by the following figure. There are several stages for input and output that all can be programmed for varying gain response characteristics.

At the microphone input side, you may use single-end input or differential input. One critical point in maintaining a high quality signal is to provide a stable bias voltage source for the condenser microphone's FET. DC blocking capacitors may be used at both positive and negative sides of input. Internally, this analog signal is converted to 15-bit 8 kHz linear PCM data.

The voice data taken from common memory is converted to an analogue value by a DAC. A multistage amplifier drives the audio signal and provides a differential signal between Line_out+ and Line_out-. The output amplifier is capable of driving a speaker directly if its impedance is greater than 16Ω.

Figure 8 –The stages for audio processing



5.10 Miscellaneous (Watchdog Timer, and Clock Divider)

System related functions such as watchdog timer, Endian control, and interrupt vectors are also provided. The purpose of the watchdog timer is to provide a reset to CPU in case when the CPU fails to service the watchdog timer in a pre-defined (programmable) period. In this situation, the CPU will be reset, and a flag will be set to indicate that the reset was due to a watchdog "timeout". In addition, it also provides resets to the other modules in Bluetooth baseband.

