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**Bluetooth Single Chip v2.1 + EDR**  
Datasheet: IS1611N      Version: 1.0

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**ISSC**

**Integrated System Solution Corporation**

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## 1 General Description

ISSC IS1611N is a compact, high integration, ultra-low cost, low power consumption CMOS RF & baseband single chip system IC for Bluetooth 2.1 with EDR (Enhanced Data Rate) 2.4GHz applications. It is fully compliant with the Bluetooth specification and completely backward-compatible with BT1.1, 1.2 or 2.0 systems. IS1611N incorporates a Bluetooth 1M/2M/3Mbps baseband and RF, single-cycle 8051 CPU, TX/RX MODEM, Memory controller, Task/Hopping controller, USB/UART interfaces, CVSD/A-law/ $\mu$ -law decoder and the ISSC Bluetooth software stack. It also integrates voice CODEC, voltage sensors, battery detector, LDOs to reduce external components requirement for various Bluetooth's applications.

The IS1611N used for embedded Bluetooth applications also runs its upper software layers from the on-chip memory. Together with an internal voice codec a complete Bluetooth headset application can be realized. The new BT 2.1 system support eSCO and simple pairing that can reduce the current consumption and user friendly.



## 2 Features

### System Specification

- Compliant with Bluetooth Specification v.2.1 with EDR in 2.4 GHz ISM band

### Baseband Hardware

- Main input clock of 16MHz clock input
- Build-in 1.8V voltage regulator
- Voltage Detection circuit useful for battery monitoring in portable applications
- Firmware execution from either internal ROM or external flash
- New features for Bluetooth 2.1
  - Encryption Pause and Resume
  - Erroneous Data Reporting
  - Extended Inquiry Response
  - Link Supervision Timeout Changed Event
  - Non-Flushable Packet Boundary Flag
  - Secure Simple Pairing
  - Sniff Subtracting
- Support both Pico-net and Scatter-net applications
- Hard-wired logic for modulation, demodulation, access code correlation, whitening, forward error correction (FEC), header error check (HEC), shorten hamming code, CRC generation/checking, frame check sequence (FCS), encryption bit stream generation, and transmit pulse shaping
- Full Bluetooth RF Interface & Lower Link Controller functions
- Adaptive Frequency Hopping (AFH) avoids occupied RF channels
- Support 64 kb/s PCM format (A-Law or  $\mu$ -Law), or CVSD (Continuous Variable Slope Delta Modulation) for SCO channel operation.
- Fast Connection supported
- Supports 802.11 Wireless Co-existence



### **RF Hardware**

- Fully Bluetooth 2.1 + 1/2/3 Mbps single chip EDR system in 2.4 GHz ISM band.
- Combined TX/RX RF terminal simplifies external matching and reduces external antenna switches.
- +4dBm output power with level control 8dB from amplitude control.
- For Class2/3, transmitter support without the requirement for external power amplifier or TR switch at the same time.
- Channel filter has been integrated into receiver channel.
- To avoid temperature variation, temperature sensor with temperature calibration is utilized into bias current and gain control.
- Fully integrated synthesizer has been created. There requires no external VCO, varactor diode, resonator and loop filter.
- Crystal oscillation with build-in digital trimming for temperature/process variations.
- Power management including idle, shutdown, and low power modes.

### **Peripherals**

- Support HCI-UART I/O interface
- Built-in single channel voice CODEC.
- Built-in a 1.8V LDO
- Built-in one dedicated 10-bit SAR-ADC for battery voltage detector.

### **Flexible HCI interface**

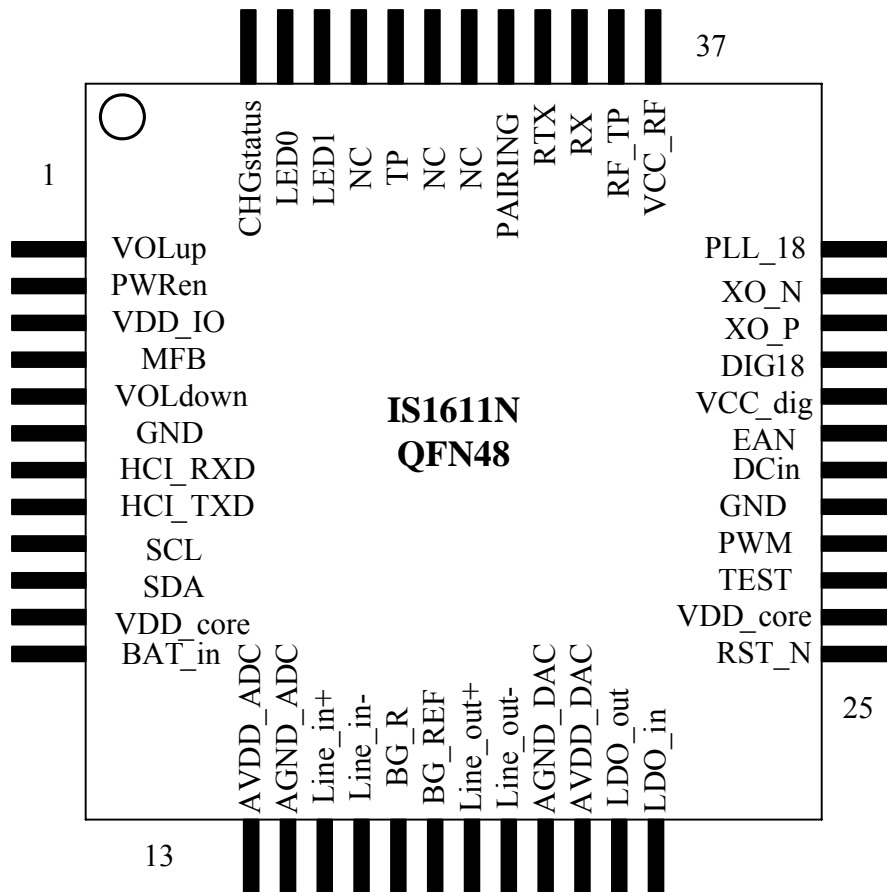
- An embedded UART (Universal Asynchronous Receiver Transmitter) is included in this chip.
- High data transfer rate realized due to automatic transfer to data memory buffers with minimal intervention from MCU required

### **Package**

- QFN 48 standard package



### 3 Pin Assignment





## 4 Pin Descriptions

Pin No.	I/O	Pin Name	Pin Descriptions
1	I	VOLup	Volume up key as the default setting It's active when receiving a LOW level signal.
2	O	PWRen	Power enable signal to latch power outside the chip
3	—	VDD_IO	Digital I/O Power. Connect to 2.7V ~ 3.3V supply.
4	I	MFB	Multi-Function Button as the default setting. It's active when receiving a HIGH level signal.
5	I	VOLdown	Volume Down key as the default setting. It's active when receiving a LOW level signal.
6	—	GND	Digital Ground. Connect to common digital ground.
7	I	HCI_RXD	HCI UART Serial Port Receive Data.
8	O	HCI_TXD	HCI UART Serial Port Transmit Data.
9	O	SCL	EEPROM interface Clock signal
10	I/O	SDA	EEPROM interface for Data signal
11	—	VDD_core	Digital core logic power. Connect to 1.8V (+/- 10%) supply.
12	AI	BAT_in	ADC input, Battery voltage detection input
13	—	AVDD_ADC	Audio ADC Power. Connect to clean 1.8V (+/- 10%) supply.
14	—	AGND_ADC	Analog ground for ADC
15	I	LINE_IN+	Differential audio input (+). 1.6Vp-p maximum differential line input with LINE_IN-. 160mV Vp-p maximum differential microphone input with LINE_IN- (microphone input mode selected via internal register). DC offset relative to ground typically 0.85V. Input impedance: 20K-ohm in typical.
16	I	LINE_IN-	Differential audio input (-). 1.6Vp-p maximum differential line input with LINE_IN+ (line-in mode selected via internal register). 160mV Vp-p maximum differential microphone input with LINE_IN+ (microphone input mode selected via internal register). DC offset relative to ground typically 0.85V. Input impedance: 20K-ohm in typical.
17	—	BG_R	Band gap resistor. Suggested use of resistor with value of 2.4K connected to audio region common ground.
18	—	BG_REF	Band gap reference output. Suggested use of a decoupling capacitor to audio region common ground with value of 50pF (subject to change).



Pin No.	I/O	Pin Name	Pin Descriptions
19	O	LINE_OUT+	Differential audio output (+). 1.6Vp-p maximum differential output used in conjunction with LINE_OUT-. DC offset relative to ground typically 0.85V. Output impedance of 20~30 ohms, with 1K ohm minimum load.
20	O	LINE_OUT-	Differential audio output (-). 1.6Vp-p maximum differential output used in conjunction with LINE_OUT+. DC offset relative to ground typically 0.85V. Output impedance of 20~30 ohms, with 1K ohm minimum load.
21	—	AGND_DAC	Analog ground for DAC
22	—	AVDD_DAC	Audio DAC Power. Connect to clean 1.8V (+/- 10%) supply.
23	AO	LDO_out	1.8V LDO output
24	AI	LDO_in	1.8V LDO input
25	I	RST_N	Reset input signal
26	—	VDD_core	Digital core logic power. Connect to 1.8V (+/- 10%) supply.
27	I	TEST	Test Use Only
28	O	PWM	Buzzer control signal
29	—	GND	Digital Ground. Connect to common digital ground.
30	I	DCin	Connect to DC jack and detected for DC jack plug-in
31	I	EAN	Embedded/External Flash Download enable
32	RP	VCC_DIG	RF digital power input
33	P	DIG_18	Digital 1V8 external capacitor
34	—	XO_P	16MHz Crystal input positive
35	—	XO_N	16MHz Crystal input negative
36	P	PLL18	PLL 1V8 external capacitor
37	RP	VCC_RF	RF IO power input
38	RP	RF_TP	RF test point
39	—	RF_TP	RF test point
40	RP	RTX	TX/RX port
41	I	PAIRING	Fast pairing button as the default setting. It's active when receiving a LOW level signal.
42	I/O	NC	GPIO
43	I/O	NC	GPIO
44	I/O	TP	Test point for mass production
45	I/O	NC	GPIO
46	O	LED1	GPIO and red LED driving as the default setting.
47	O	LED0	GPIO and blue LED driving as the default setting.
48	I	CHGstatus	The indicator for charger status
49	P	GND	Exposed Pad as RF ground.





**Notes:**  
(1)



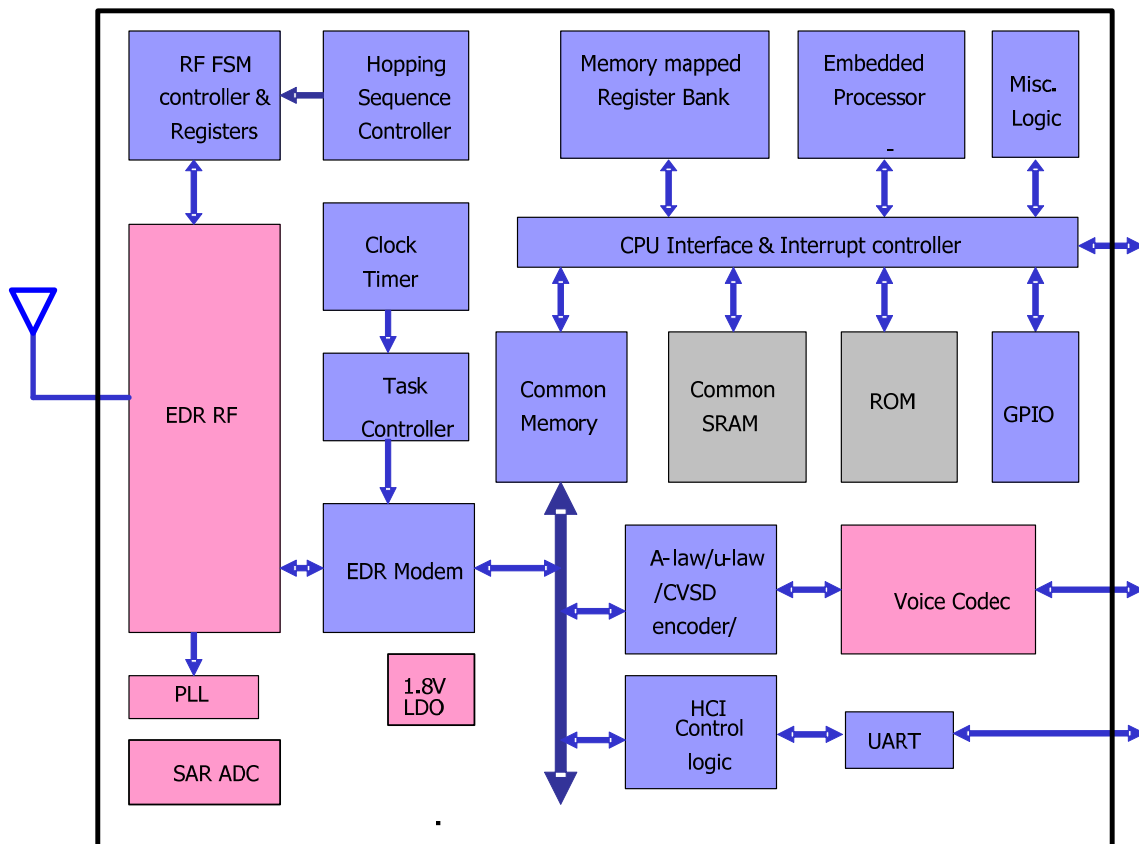
## 5 Functional Description

### 5.1 Overall Architecture

The ISSC IS1610N integrates an enhanced EDR Bluetooth RF & BB core, HCI controller, Audio controller and an ENHANCED 8051 processor with an internal mask ROM for program memory and SRAM for data memory. An innovative interconnection structure called the Common-Memory Architecture (CMA) is designed to provide a fast and flexible data movement scheme between the embedded processor, Bluetooth core, and peripheral hardware within this SRAM data memory space.

For audio and power management, IS1610N provide embedded audio code and some power management to reduce the external components.

Figure 1 – Block diagram for IS1610N





## 5.2 Radio Frequency (RF)

### 5.2.1 Transmitter

The internal PA has a maximum output power of +4dBm with level control 8dB from amplitude control. This is applied into Class2/3 radios without external RF PA. If you want a larger output power for Class1 application, the external PA can be used.

The transmitter features IQ direct conversion to minimize the frequency drift. And it can excess 30dB power range with temperature compensation machine.

### 5.2.2 Receiver

The LNA can be operated into two type modes. One type is TR-combined mode for single port application. The other type is TR-separated mode for dual port application that used an external PA/LNA application.

The image rejection filter is to reject image frequency for low-IF architecture. This filter for low-IF architecture is implied to reduce external BPF component for super heterodyne architecture.

The ADC is utilized to sample input analogue wave to convert into digital for demodulator analysis. Before the ADC, a channel filter has been integrated into receiver channel that can reduce the external component count and increase the anti-interference capacity.

For avoiding temperature variation issues, a temperature sensor with temperature calibration is utilized into bias current and gain control of LNA, Mixers, and RF AMP.

### 5.2.3 Synthesizer

The internal loop filter is used to reduce external RC components. This can reduce cost and variations for components. This internal LC tank for VCO is utilized to reduce variation for components. The cost is down at the same time.

A fully integrated synthesizer has been created. There requires no external VCO, varactor diode, resonator and loop filter.



### 5.3 SAR ADC Voltage Converter

The 10-bit Successive-Approximation analog to digital converter (SAR ADC) features 1 dedicated channel for battery power detection and 1 channel for external peripheral temperature sensing. This ADC has 10 bits resolution that provides a high accurate monitoring for battery voltage. The operating current is very low and almost consumes no power when disabled.



## 5.4 MODEM

There are three different modulations for Bluetooth v2.1 + EDR. In figure 2, we summarized these modulations and data rate.

**Figure 2 – Modulation type for Bluetooth v2.1 + EDR**

Data Rate	Modulation	Bits/Symbol
BDR: 1 Mbps	GFSK	1
EDR: 2 Mbps	$\pi/4$ DQPSK	2
EDR: 3 Mbps	8DPSK	3

### 5.4.1 Basic Data Rate MODEM (BDR)

On the Bluetooth v1.2 specification and below, 1 Mbps was the standard data rate based on Gaussian Frequency Shift Keying (GFSK) modulation scheme. This basic rate modem meets BDR requirements of Bluetooth v2.1+EDR specification.

**Figure 3 – Data format for BDR**

Access Code	Header	Payload
-------------	--------	---------

### 5.4.2 Enhanced Data Rate MODEM (EDR)

On the Bluetooth v2.1+EDR specification, Enhanced Data Rate (EDR) has been introduced to provide 2 and 3 Mbps data rates as well as 1 Mbps. This enhanced data rate modem meets EDR requirements of Bluetooth v2.1+EDR specification. For the viewpoint of baseband, both BDR and EDR utilize the same 1MHz symbol rate and 1.6 KHz slot rate. For BDR, 1 symbol represents 1 bit. However each symbol in the payload part of EDR packets represents 2 or 3 bits. This is achieved by using two different modulations,  $\pi/4$  DQPSK and 8DPSK.

**Figure 4 –Data format for EDR**



Access Code	Header	Guard	Sync	Payload	Trailer
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For this modulation, each symbol carries 2 bits of information. For its constellation diagram, although there are 8 possible phase states, the encoding scheme guarantees the trajectory of the modulation between symbols is restricted to 4 states. For a given starting point, every phase change between symbols is restricted to  $+45^\circ$ ,  $+135^\circ$ ,  $-45^\circ$ , and  $-135^\circ$ .

**Figure 5 –Phase shift & bit pattern for 2 MHz data rate**

Phase Shift	Bit Pattern
$+45^\circ (+\pi/4)$	00
$+135^\circ (+3\pi/4)$	01
$-135^\circ (-3\pi/4)$	11
$-45^\circ (-\pi/4)$	10

For this modulation, each symbol carries 3 bits of information. For its constellation diagram, it is similar to  $\pi/4$  DQPSK but the trajectory of the modulation between symbols has 8 possible phase states. For a given starting point, every phase change between symbols is restricted to  $0^\circ$ ,  $+45^\circ$ ,  $+90^\circ$ ,  $+135^\circ$ ,  $+180^\circ$ ,  $-135^\circ$ ,  $-90^\circ$ , and  $-45^\circ$ .

**Figure 6 –Phase shift & bit pattern for 3 MHz data rate**

Phase Shift	Bit Pattern
$0^\circ (+0)$	000
$+45^\circ (+\pi/4)$	001
$+90^\circ (+\pi/2)$	011
$+135^\circ (+3\pi/4)$	010
$+180^\circ (+\pi)$	110
$-135^\circ (-3\pi/4)$	111
$-90^\circ (-\pi/2)$	101



-45° ( $-\pi/4$ )	100
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## 5.5 Baseband

The following modules implemented in hardware constitute the Bluetooth Baseband Core. The frequency hopping sequence generator produces the correct hop frequency control sequence based on the Bluetooth clock, Bluetooth device address, and the current operating mode.

The access code generates the access code based on the Lower Address Part (LAP) of the Bluetooth device address. The access code is comprised of the preamble, sync word and trailer bits. The detection of the access code uses correlation to detect a valid access code.

Bluetooth uses two types of FEC: 1/3 repetition code and (15, 10) shorten Hamming code respectively. The former basically repeats each transmitted bit three times while the latter has 15 bits of codeword which contains 5 parity bits. The code has capability of correction of all single-bit errors in each codeword.

The purpose of HEC is to protect the header bits. Dedicated header error code generator calculates the HEC bits in the header of a transmitted packet. While on the receiver side, HEC detects corrupted headers.

A 16-bit CRC is adopted to protect payload data transmitted using certain types of Bluetooth packets.

Information confidentiality can be protected by encryption of the packet payload. Dedicated encryption/decryption hardware is designed into the baseband core.





## 5.6 MCU

The embedded processor embedded with this version is a single-cycle 8051 CPU. The embedded processor will be referred to as simply the processor, 8051, or MCU throughout the remainder of this document. There are a few minor differences between a standard 8051 and this CPU. These include:

1. Alteration of memory timings to match internal and external memory configurations.
2. Modification of idle mode to disable internal CPU clocking. Only externally-clocked interrupt sources can allow the CPU to recover from idle mode.

A single-port synchronous interface is provided to memory. From this single port, the bandwidth is divided among the 7 interfaces spread amongst 5 physical busses described below:

- Embedded processor bus
- Baseband TX bus
- Baseband RX bus
- HCI TX bus
- HCI RX bus
- Audio bus
- DMA bus

In addition, attached to the embedded processor bus are a register bank, a dedicated single-port memory (data segment 1), and flash memory (program segment). The processor coordinates all link control procedures and data movement using a set of pointer registers. For example, when an HCI packet (from the host via USB or UART) is received into the HCI buffer, the processor is interrupted. The processor can then read a status register to determine the HCI packet type and determine whether to set up the Baseband pointer registers for this memory region for RF-retransmission, or to otherwise directly perform packet processing with the CPU.



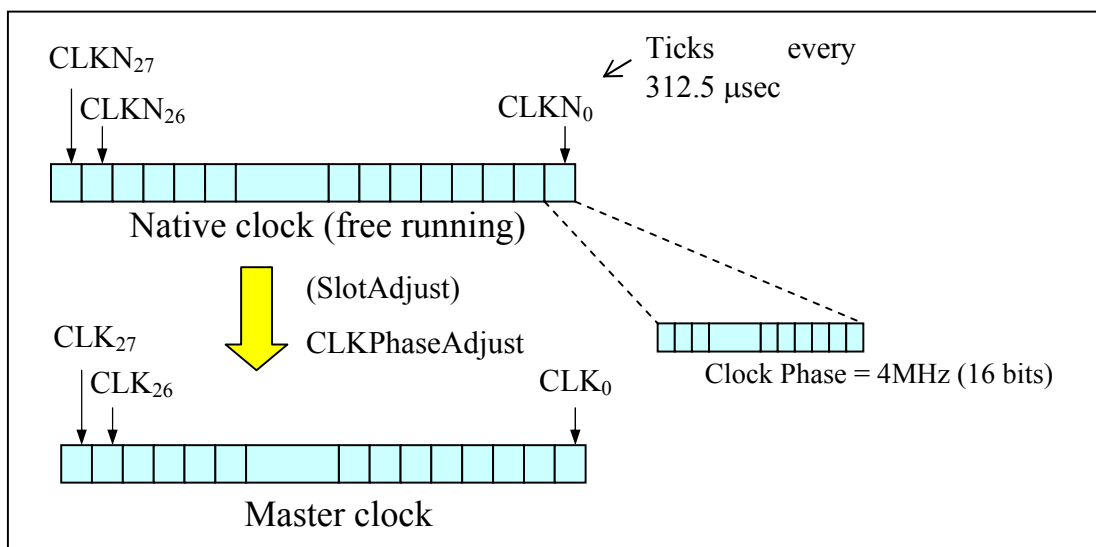
## 5.7 Bluetooth Clock and Timers

A Bluetooth standard 28-bit counter running at 3.2 kHz implements the native clock defined by Bluetooth specification 1.2. This clock provides the transmission and receiving timing of a half time slot (312.5  $\mu$ s). Another finer counter implemented in 16 bits is also provided as the phase of a half time slot. This phase information is very helpful when a Bluetooth slave wants to adapt to its master's clock. It is running at 4MHz. The counter is pre-scalable for the purpose of power saving operations. The diagram below describes a standard Bluetooth native clock and master clock. The clock signal is also used as a slot boundary signal to trigger a baseband packet transmission or receipt.

There are four timers provided by the system, two timers for TX/RX and general purpose and the others for general purpose.

The powerful pre-scheduling functions for the transceiver are realized by two sets of programmable timers, namely Task0SlotTimer/Task0PhaseTimer and Task1SlotTimer/Task1PhaseTimer. Each set of timers is associated with the task of transmission or receiving. When the timer is configured by firmware, it will automatically execute the TX or RX task at a specific time. Sub-tasks and timing for a TX task remain to be defined.

**Figure 7 –Bluetooth clock**





## 5.8 Peripherals

Hardwired control logic is presented in front of the UART devices for HCI protocol handling and packet buffering. This control logic is part of the HCI controller defined in Bluetooth specification 1.2. This logic is partially responsible for the HCI protocol handling to/from the host and it also maps the registers of the UART devices indirectly to the 8051 such that the system can receive or send a HCI packet to/from the respective host interface. Major functions of this logic include:

- HCI packet formatter and de-formatter (identifying the packet type)
- Frame boundary determination, segmentation and reassembly of HCI packets.
- HCI packet transmission, receiving, and buffering (using common memory HCI buffer).
- Independent receive / transmit channels
- Universal device interface

An embedded UART (Universal Asynchronous Receiver Transmitter) is included in this design. In order to reduce gate count, only the functions required for the HCI logic are included. These include the following:

- Full-Duplex operation
- Programmable BAUD rate (using 16-bit input clock divider to obtain Baud Rate x16 or x24 or x13 clock base)
- 7 or 8 Data bits
- 1 or 2 Stop bits
- Even / Odd / Mark / Space / None Parity configurations
- Break Generation / Detection
- Maskable individual interrupts to CPU and combined Error interrupt to HCI
- Selectable Direct CPU interface or interface to HCI module



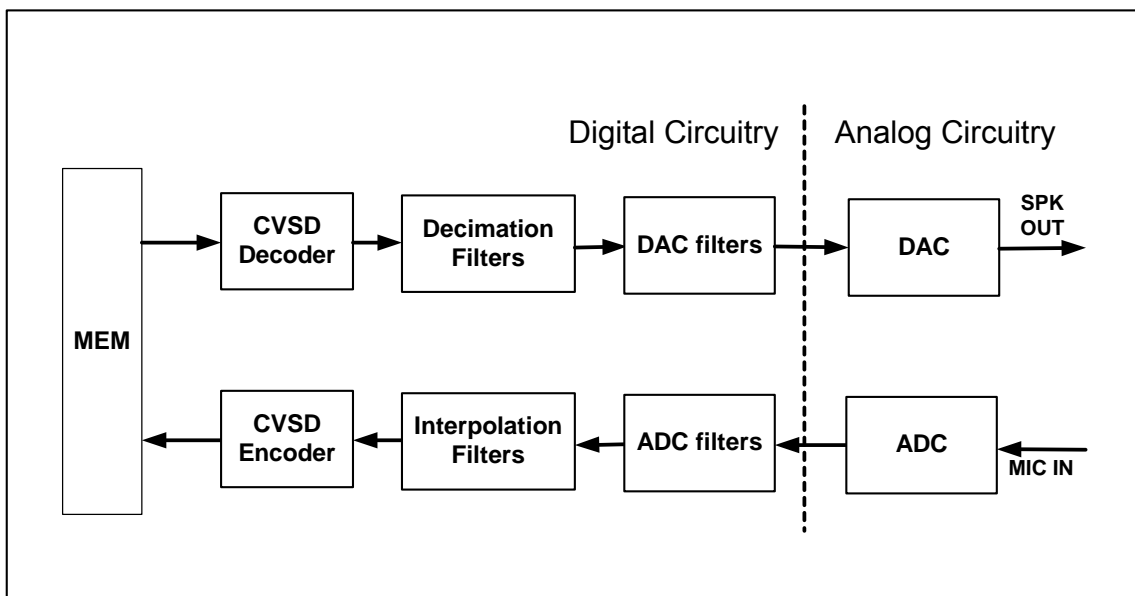
## 5.9 Voice Codec

The mono audio codec is described by the following figure. There are several stages for input and output that all can be programmed for varying gain response characteristics.

At the microphone input side, you may use single-end input or differential input. One critical point in maintaining a high quality signal is to provide a stable bias voltage source for the condenser microphone's FET. DC blocking capacitors may be used at both positive and negative sides of input. Internally, this analog signal is converted to 15-bit 8 kHz linear PCM data.

The voice data taken from common memory is converted to an analogue value by a DAC. A multistage amplifier drives the audio signal and provides a differential signal between Line\_out+ and Line\_out-. The output amplifier is capable of driving a speaker directly if its impedance is greater than 16Ω.

**Figure 8 –The stages for audio processing**





### **5.10 Miscellaneous (Watchdog Timer, and Clock Divider)**

System related functions such as watchdog timer, Endian control, and interrupt vectors are also provided. The purpose of the watchdog timer is to provide a reset to CPU in case when the CPU fails to service the watchdog timer in a pre-defined (programmable) period. In this situation, the CPU will be reset, and a flag will be set to indicate that the reset was due to a watchdog “timeout”. In addition, it also provides resets to the other modules in Bluetooth baseband.



## 6 Electrical Characteristics

### Recommended operate condition

Symbol	Parameter	Min	Typical	Max	Unit
V <sub>DD18</sub>	Digital core supply voltage SAR ADC supply voltage CODEC supply voltage	1.62	1.8	1.92	V
V <sub>DDIO</sub>	I/O supply voltage RF supply voltage	2.43	2.7	3.63	V
T <sub>OPERATION</sub>	Operating temperature range	-40	+25	+85	°C
T <sub>stg</sub>	Storage temperature	-40		+125	°C
V <sub>LDO</sub>	LDO supply voltage	2.1		3.6	V
V <sub>BAT IN</sub>	Input voltage for SAR ADC	0.9		3.6	V

### Audio section

Audio Codec,16Bit Resolution	Min	Typ	Max	Unit
<b>Microphone Amplifier</b>				
Input scale		1.6		Vp-p
Gain resolution				
Stage 1(two levels)	0		14	dB
Stage 2 : 0~26dB, 16 steps		1.73		dB/Step
Mic mode input impedance		20		KΩ
Common Mode Voltage		0.85		V
Bandwidth	3.2		3.84	KHz
<b>Analogue to Digital Converter</b>				
Input Sample Rate		2		MSample/s
Output Sample Rate		8		KSamples/s
<b>Digital to Analogue Converter</b>				
Gain Resolution : -20dB~0dB, 8 Steps		-2.85		dB/Step
Min gain		-20		dB
Max gain		0		dB
<b>Loudspeaker Driver</b>				
Output Voltage Full Scale Swing (differential)		1.6		V Pk-Pk
Output Impedance	16		30	Ω
Common Mode Voltage		0.85		V
Bandwidth	2.62		3.63	KHz



**Digital I/O pins (I/O pins at  $V_{DDIO}$ )**

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
$V_{IH}$	High-level input voltage		2		3.6	V
$V_{IL}$	Low-level input voltage		-0.3		0.8	V
$V_{OH}$	High-level output voltage	$I_{OH} = 4\text{mA}$	2.4		-	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 4\text{mA}$	-	-	0.4	V



**Transmitter section for BDR**

<b>VCC_RF = 2.7V    Temperature = 25°C</b>	<b>Typ</b>	<b>Unit</b>
Maximum RF transmit power	5.5	dBm
RF power variation over temperature range with compensation enable	1.2	dB
RF power variation over temperature range with compensation disable	2.7	dB
RF power control range	35	dB
RF power range control range resolution	0.5	dB
20db bandwidth for modulated carrier	780	kHz
Adjacent channel transmit power F = F <sub>0</sub> ± 2Mhz	-41	dBm
Adjacent channel transmit power F = F <sub>0</sub> ± 3Mhz	-45	dBm
Adjacent channel transmit power F = F <sub>0</sub> ≥ 3Mhz	-50	dBm
Δf <sub>1avg</sub> Maximum Modulation	164	kHz
Δf <sub>2avg</sub> Minimum Modulation	152	kHz
Δf <sub>1avg</sub> / Δf <sub>2avg</sub>	0.98	
Initial carrier frequency tolerance	5	kHz
Drift Rate	7	kHz/50us
Drift (single slot packet)	8	kHz
Drift (five slot packet)	10	kHz
2 <sup>nd</sup> Harmonic Content	-50	dBm
3 <sup>rd</sup> Harmonic Content	-45	dBm





**Receiver section for BDR**

VCC_RF = 2.7V    Temperature = 25°C		Typ	Unit
	<b>Frequency (GHz)</b>		
Sensitivity at 0.1% BER for all packet types	2.402	-87.0	dBm
	2.441	-88.0	dBm
	2.480	-87.5	dBm
Maximum received signal at 0.1% BER		≥-10	dBm
	<b>Frequency (GHz)</b>	<b>Typ</b>	<b>Unit</b>
Continuous power required to block Bluetooth reception (for input power of -67dBm with 0.1% BER) measured at the unbalanced port of the balun	30-2000	≥0	dBm
	2000-2400	-15	dBm
	2500-3000	-15	dBm
C/I co-channel		7	dB
Adjacent channel selectivity C/I F = F <sub>0</sub> + 1 MHz		4	dB
Adjacent channel selectivity C/I F = F <sub>0</sub> - 1 MHz		-3	dB
Adjacent channel selectivity C/I F = F <sub>0</sub> + 2 MHz		-45	dB
Adjacent channel selectivity C/I F = F <sub>0</sub> - 2 MHz		-23	dB
Adjacent channel selectivity C/I F = F <sub>0</sub> + 3 MHz		-48	dB
Adjacent channel selectivity C/I F = F <sub>0</sub> - 5 MHz		-48	dB
Adjacent channel selectivity C/I F = F <sub>image</sub>		-22	dB
Maximum level of inter-modulation interference		-30	dBm
Spurious output level		≤-130	dBm/Hz



**Transmitter section for EDR**

VCC_RF = 2.7V    Temperature = 25°C		Typ	Unit
Maximum RF transmit power		3.0	dBm
Relative transmit power		-1.3	dB
$\pi/4$ DQPSK max carrier frequency stability $w_0$		1.9	kHz
$\pi/4$ DQPSK max carrier frequency stability $w_i$		2.1	kHz
$\pi/4$ DQPSK max carrier frequency stability $ w_0 + w_i $		3.4	kHz
8DPSK max carrier frequency stability $w_0$		1.5	kHz
8DPSK max carrier frequency stability $w_i$		2.9	kHz
8DPSK max carrier frequency stability $ w_0 + w_i $		4.0	kHz
$\pi/4$ DQPSK Modulation Accuracy	RMS DEVM	7	%
	99% DEVM	12	%
	Peak DEVM	17	%
8 DPSK Modulation Accuracy	RMS DEVM	7	%
	99% DEVM	12	%
	Peak DEVM	17	%
In-band spurious emissions	$F > F_0 + 3\text{MHz}$	-45	dBm
	$F < F_0 - 3\text{MHz}$	-45	dBm
	$F = F_0 - 3\text{MHz}$	-41	dBm
	$F = F_0 - 2\text{MHz}$	-28	dBm
	$F = F_0 - 1\text{MHz}$	-30	dB
	$F = F_0 + 1\text{MHz}$	-30	dB
	$F = F_0 + 2\text{MHz}$	-26	dBm
	$F = F_0 + 3\text{MHz}$	-28	dBm
EDR Differential Phase Encoding		No Error	%

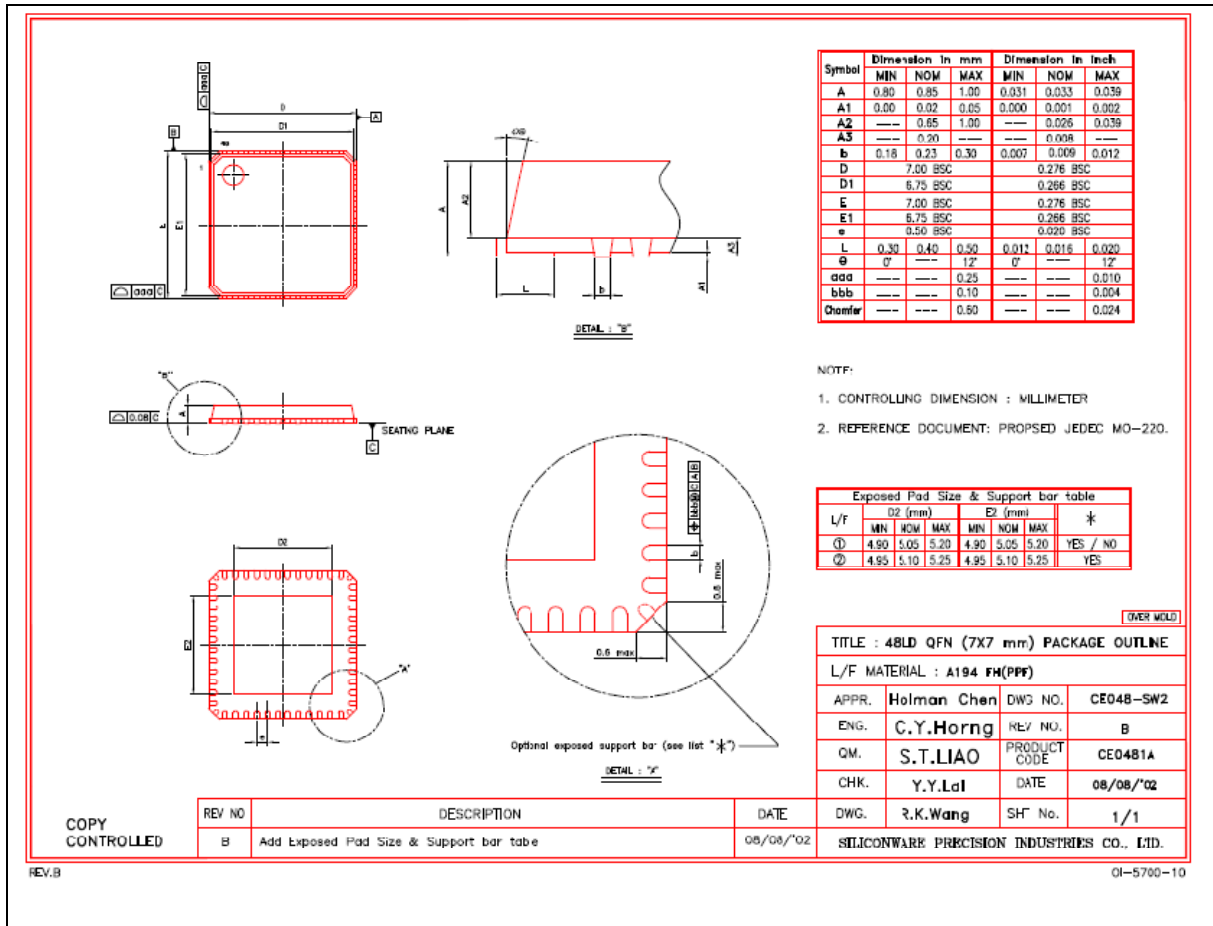


**Receiver section for EDR**

VCC_RF = 2.7V    Temperature = 25°C		Typ	Unit
	Modulation		
Sensitivity at 0.1% BER	$\pi/4$ DQPSK	-85.5	dBm
	8DPSK	-81.5	dBm
Maximum received signal at 0.1% BER	$\pi/4$ DQPSK	$\geq -10$	dBm
	8DPSK	$\geq -10$	dBm
C/I co-channel at 0.1% BER	$\pi/4$ DQPSK	8	dB
	8DPSK	18	dB
Adjacent channel selectivity C/I F = F <sub>0</sub> + 1 MHz	$\pi/4$ DQPSK	-10	dB
	8DPSK	-5	dB
Adjacent channel selectivity C/I F = F <sub>0</sub> - 1 MHz	$\pi/4$ DQPSK	-10	dB
	8DPSK	-6	dB
Adjacent channel selectivity C/I F = F <sub>0</sub> + 2 MHz	$\pi/4$ DQPSK	-40	dB
	8DPSK	-41	dB
Adjacent channel selectivity C/I F = F <sub>0</sub> - 2 MHz	$\pi/4$ DQPSK	-23	dB
	8DPSK	-22	dB
Adjacent channel selectivity C/I F = F <sub>0</sub> + 3 MHz	$\pi/4$ DQPSK	-45	dB
	8DPSK	-45	dB
Adjacent channel selectivity C/I F = F <sub>0</sub> - 5 MHz	$\pi/4$ DQPSK	-45	dB
	8DPSK	-45	dB
Adjacent channel selectivity C/I F = F <sub>image</sub>	$\pi/4$ DQPSK	-20	dB
	8DPSK	-12	dB



## 7 Package Information





## Appendix A. Reflow Profile

1.) Follow: IPC/JEDEC J-STD-020 C

2.) Condition:

Average ramp-up rate (217°C to peak): 1~2°C/sec max.

Preheat : 150~200°C、60~180 seconds

Temperature maintained above 217°C : 60~150 seconds

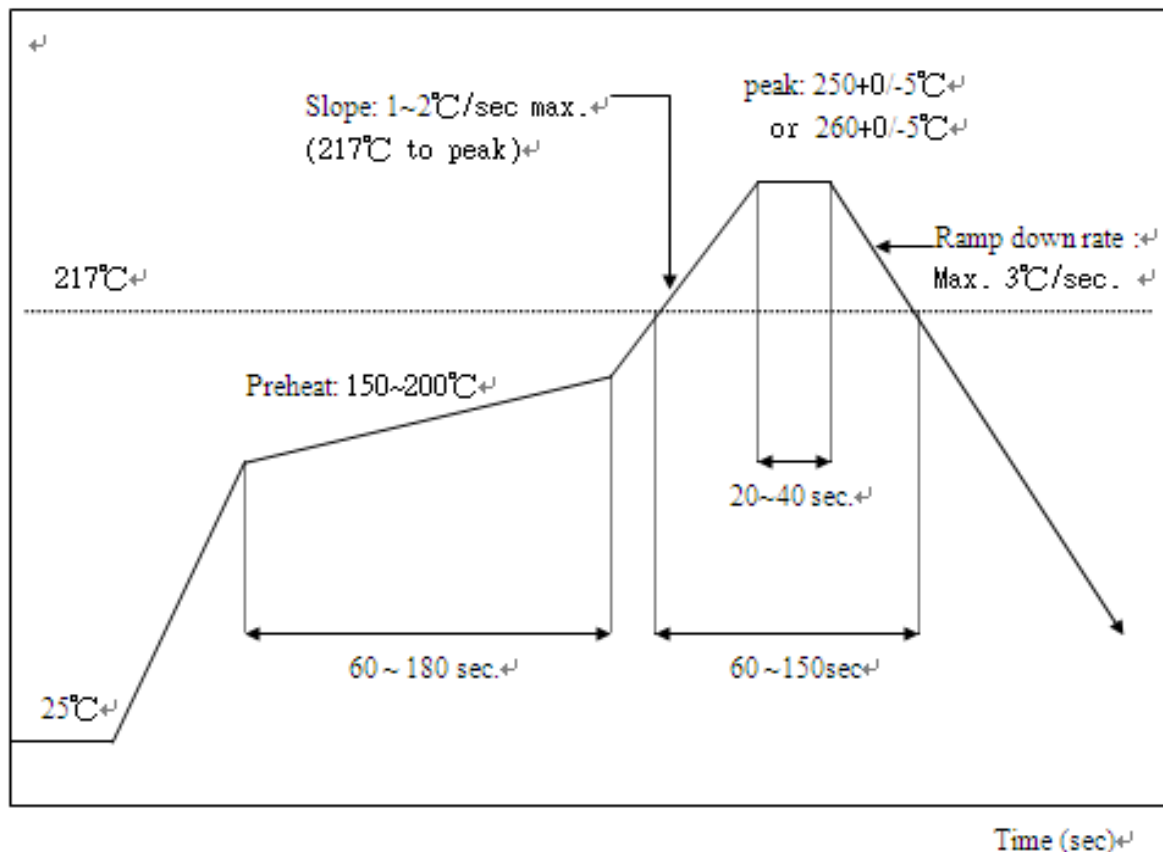
Time within 5°C of actual peak temperature: 20 ~ 40 sec.

Peak temperature : 250+0/-5°C or 260+0/-5°C

Ramp-down rate : 3°C/sec. max.

Time 25°C to peak temperature : 8 minutes max.

Cycle interval : 5 minus





## Appendix B. BQB certification

<https://www.bluetooth.org/tpg/Certificate.cfm?QID=138200>



### Bluetooth SIG Qualification Design (QDL) Certificate

QDL Certificate: This certificate represents the Specifications declared by the Member as having passed the Bluetooth Qualification/Certification Process as specified within the Bluetooth Specifications and as required within the PRD 2.0.

Design Name: **Bluetooth 2.1+EDR Baseband controller**



This Product Design has passed the Bluetooth Qualification Process!

Specification Version: 2.1/2.1+EDR

QDID: B013820

Declared Specifications: Baseband Conformance, Radio, Link Manager, Summary ICS,  
Product Type

Member Company:  
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1, Science-Based Industrial  
Park  
Hsinchu, Taiwan 300  
BQE:  
Jan-Willem Vonk

Requirements:  
1. Testing  
2. Documentation  
3. Assessment  
4. Declaration  
5. Listing  
6. Marking  
7. Compliance to Auditing and  
Enforcement

Project Dates:  
Assessment Date:  
March/21/2008  
Listing Date:  
March/21/2008



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