STAR
RECEIVER EXCITER, RADAR CONTROL AND ACQUISITION SYSTEM MODULE

DESIGN DOCUMENT

INTERMAP

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DOCUMENT HISTORY

Version	Date	Comment/Description of Change	Author(s)
1.00	May 12, 2003	First Draft Release	TRM, WRT
1.01	May 30, 2003	Blockdiagrams updated for review	ML
1.10	June 12, 2003	RF Blockdiagrams changed	ML
1.11	???	???	???
1.12	June 12, 2003	Added software design, signal source, AGC	TM
1.13	February 12, 2004	Noise and spurious signal	ML
2.00	June 01, 2006	Updating of design doc with respect to new STAR4 module developments (05535)	PG, ML

TABLE OF CONTENTS

1 INTRODUCTION

1.1 Purpose

This document describes the design of the GTM receiver exciter, radar control and acquisition module as part of the GTM core technology. The GTM core technology provides the basic subsystems required for an interferometric radar system.

1.2 Scope

This document first provides a functional description and the design requirements. It then describes the detailed design in terms of hardware, software, and mechanics. Finally the theory of operation, test procedures, and calibration is included.

The document assumes that the reader has a basic understanding of interferometric radar systems, airborne remote sensing platforms, Intermap products and processes and computer systems technology.

1.3 Definitions, Acronyms, and Abbreviations

GTM.....Global Terrain Mapper
LRU.....Line Replaceable Units
TCP/IP.....Network Communication protocol
MCC.....Master Control Computer
ANT .....Antenna Module
RCVEX-RCAS .....Receiver Exciter – Radar Control and Acquisition System Module
PWRDIST .....Power Distribution Module
NAV .....Navigation Module
WGASS-XTRANS .....Wave Guide Assembly – X-Band Transmitter

1.4 References

1. DOC1000_v 1.01d – GTM SRS
2. DOC1002_v1.1 – GTM System ICD
3. DOC1008_v1.00 – GTM Hardware ICD

2 FUNCTIONAL DESCRIPTION

The GTM RCVEX-RCAS Module controls the waveform generation, RF timing parameters and raw phase data recording in the GTM System.

Please refer to the following diagram:

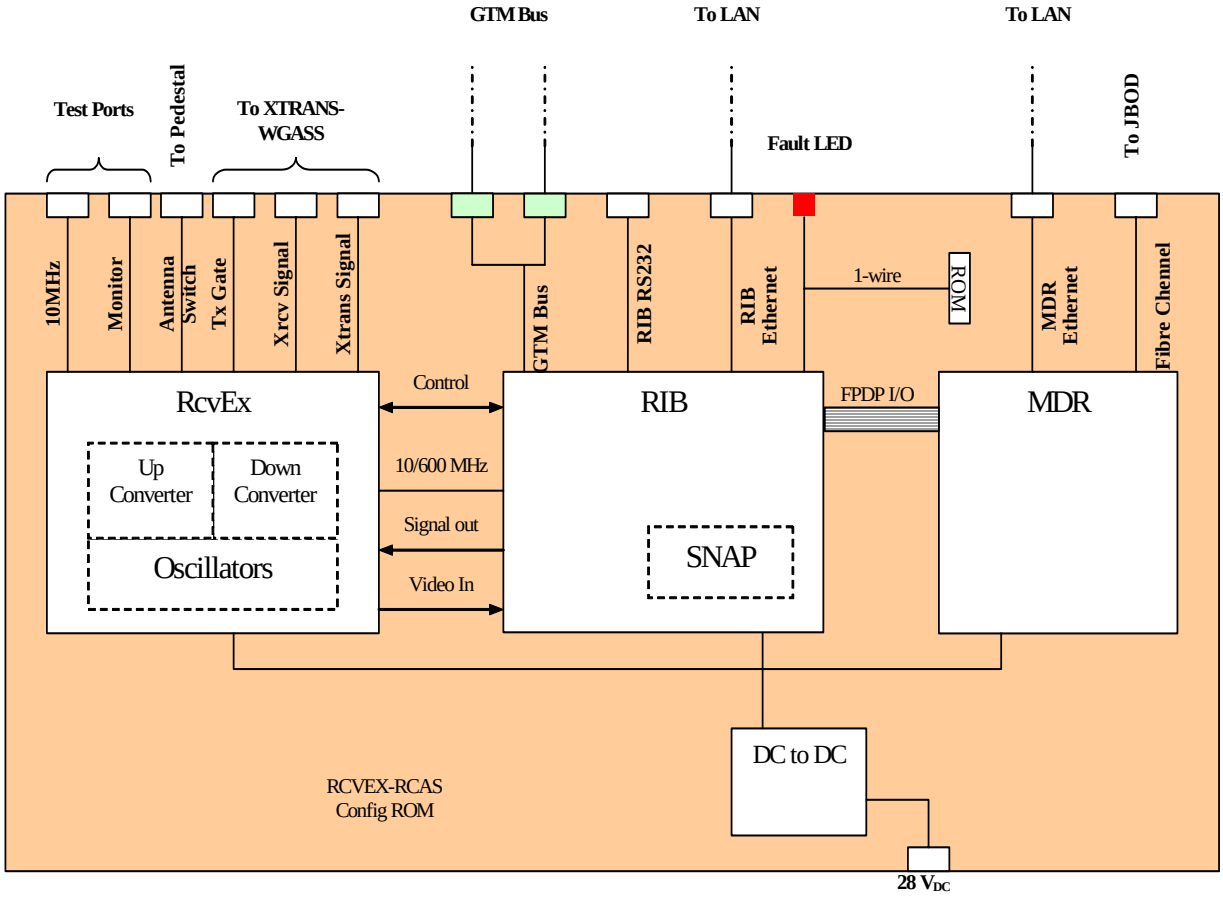
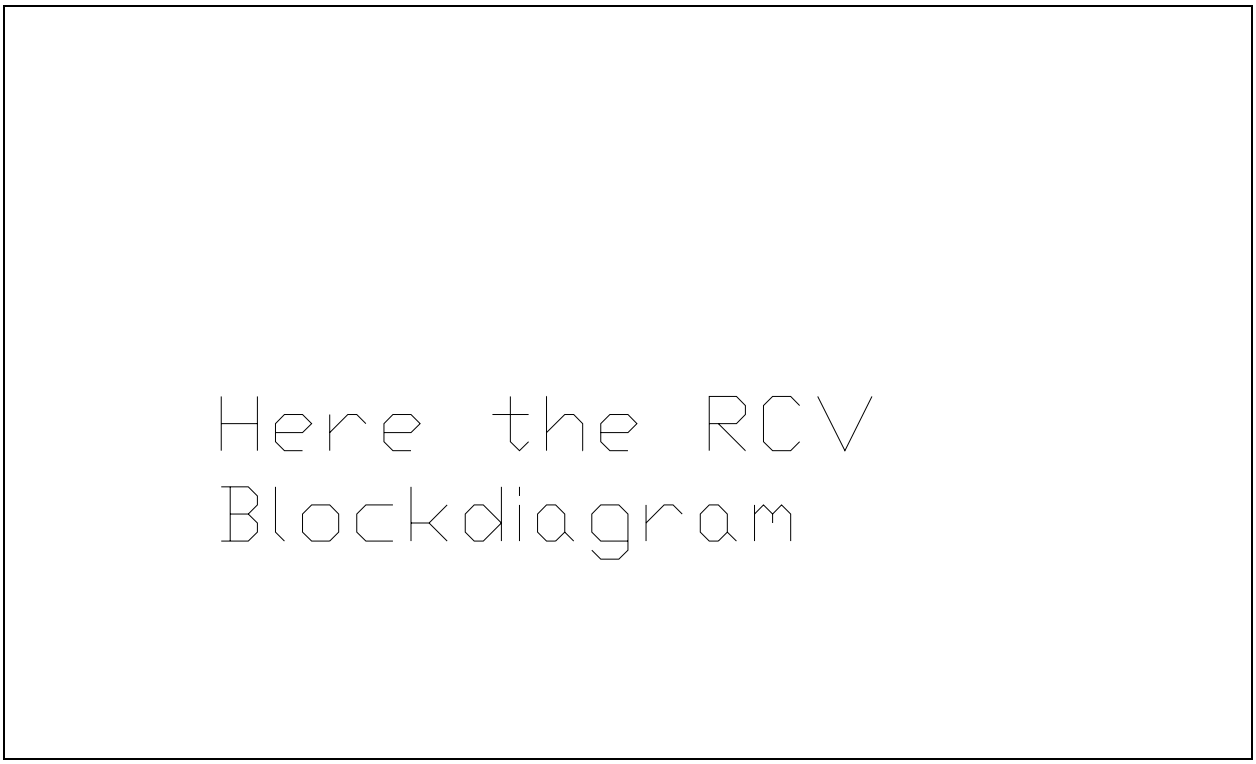


Figure 1 - RCVEX-RCAS module block diagram

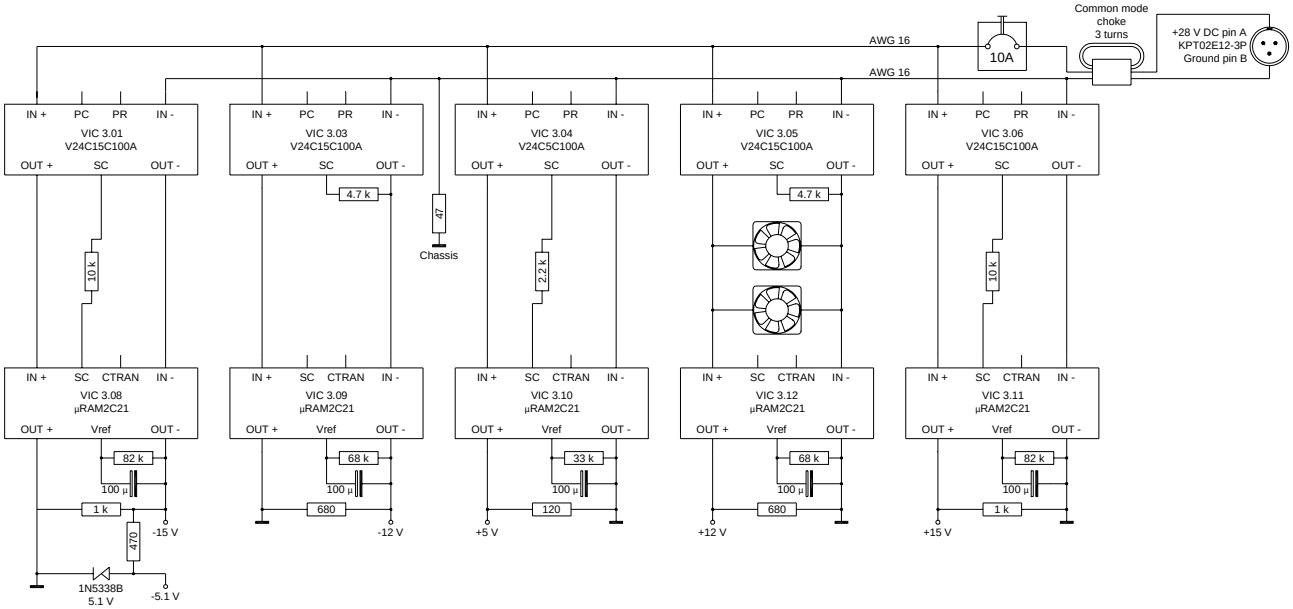
The Module contains a RIB board, a Midas Data Recorder and the receiver-exciter RF components. The RCVEX-RCAS module receives commands over the Ethernet and translates them to the appropriate RF timing and signal generation in the Receiver Exciter. Additionally, the RCVEX-RCAS module controls the start and stop of data transfer through the fibre channel interface the MDR. All data recorded through the MDR is time stamped to GPS time.

The module creates a module status packet and broadcasts it to the GTM system. All Data sent from the module will be time stamped to GPS time.

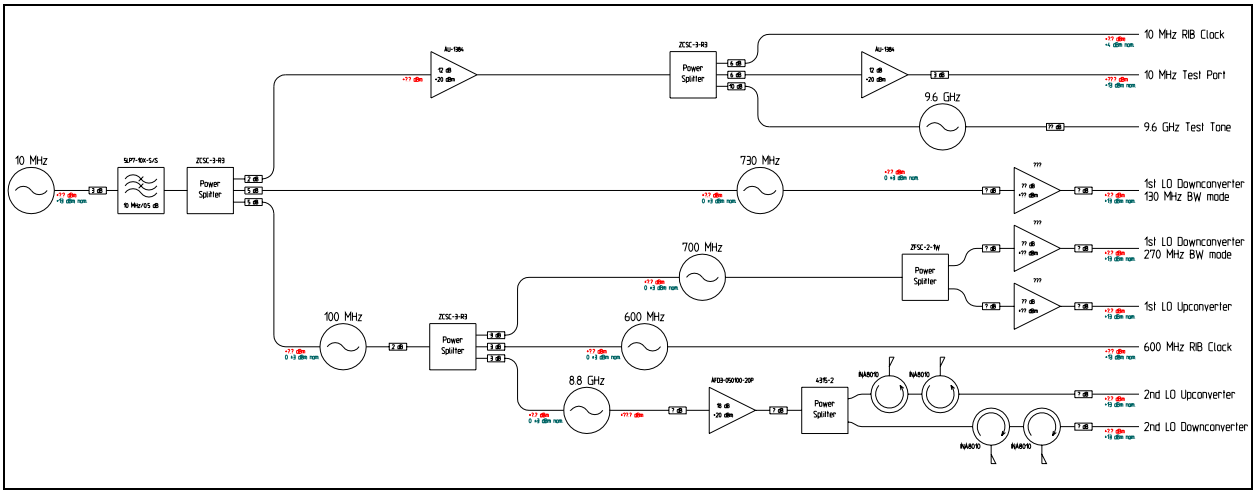
2.1 Functional Blockdiagram



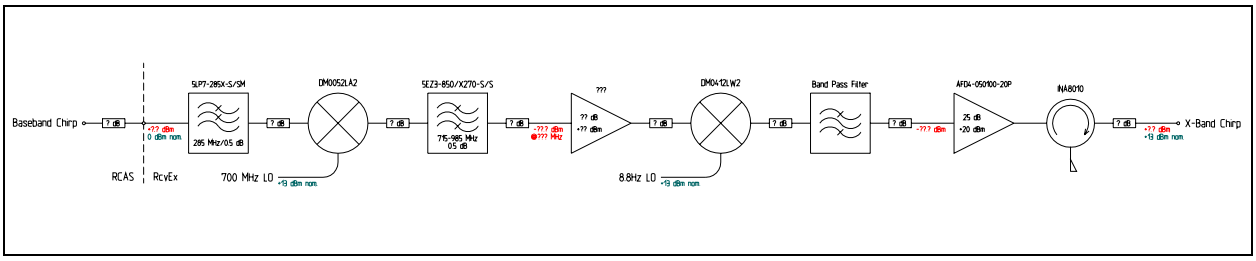
2.2 Power Diagram



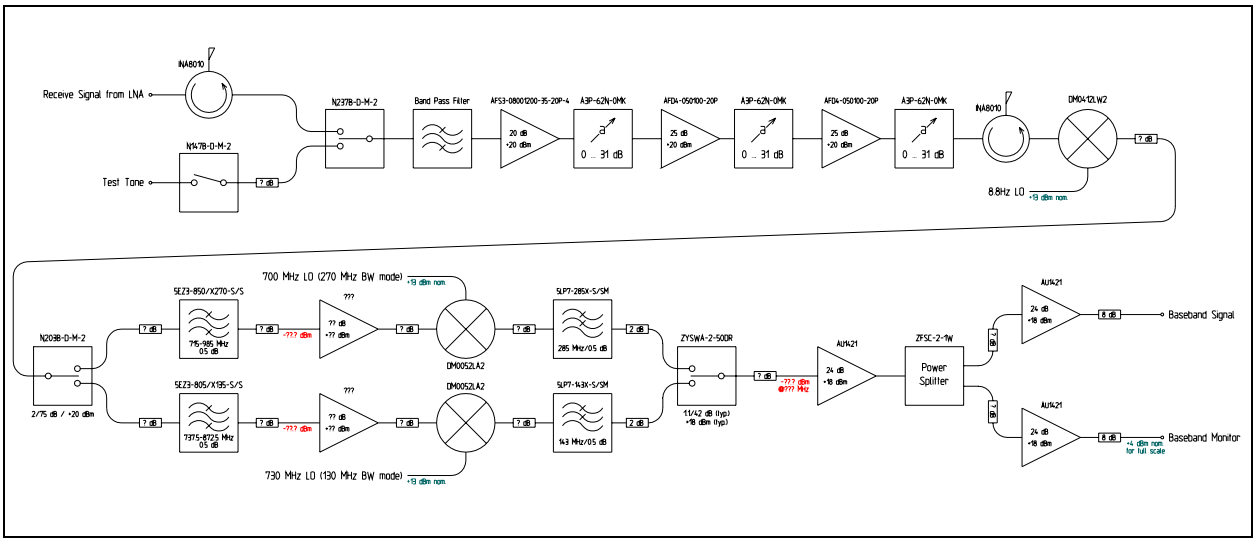
2.3 RF Blockdiagrams



Oscillator section

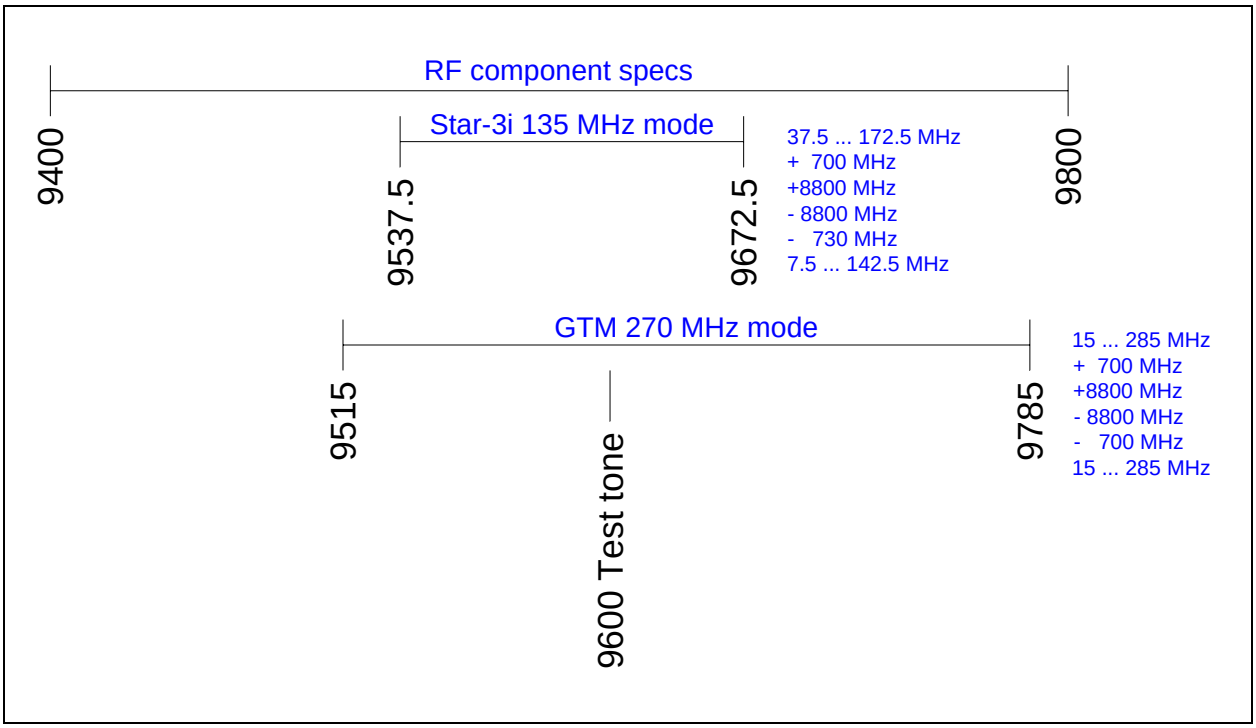


Upconverter section

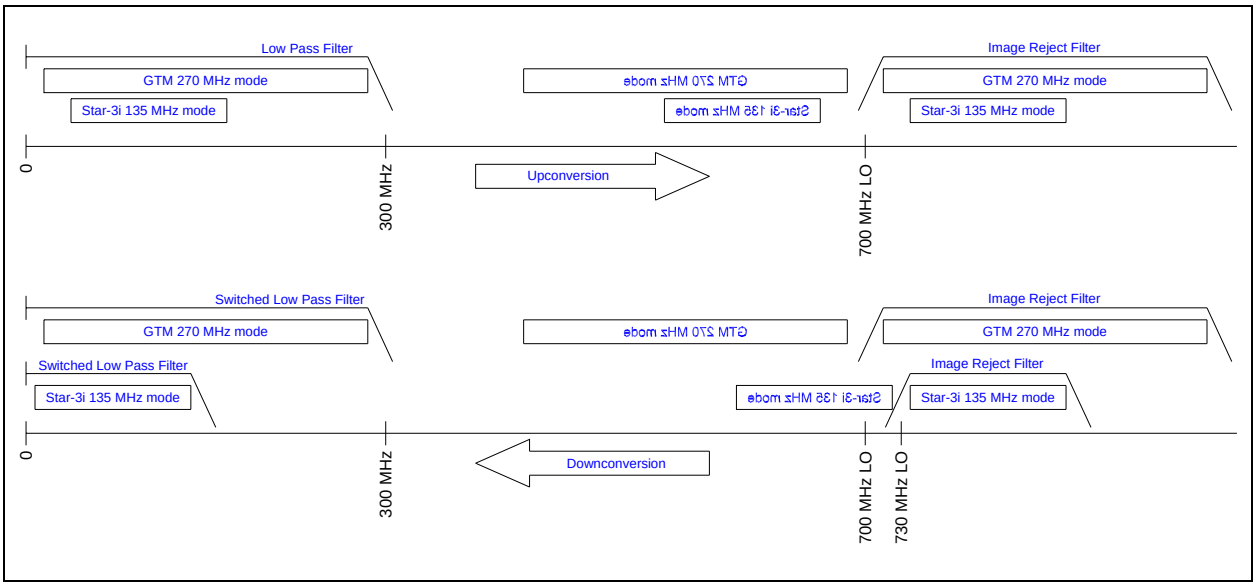


Downconverter section

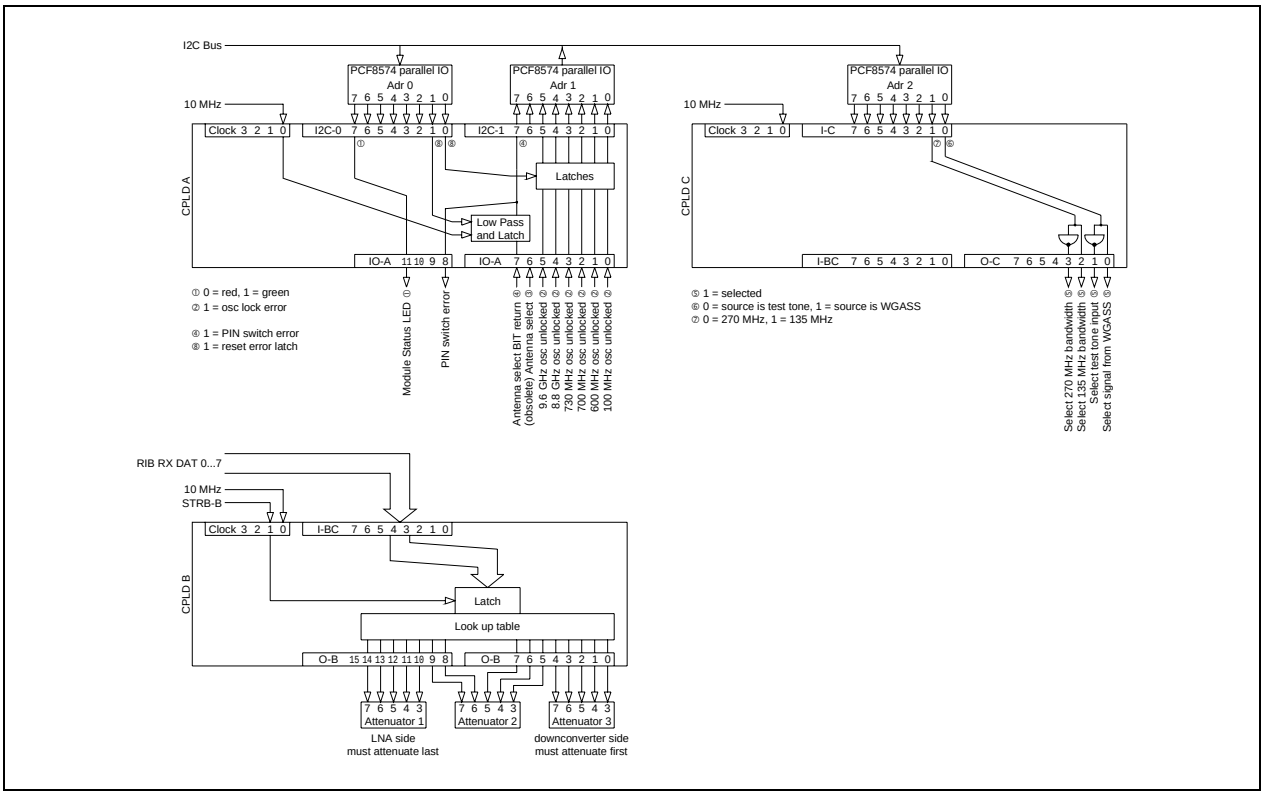
2.4 Frequency plan



2.5 Filter plan



2.6 CPLDs



See also: 8.1 Antenna PIN-switch Error Detection

3 DESIGN REQUIREMENTS

3.1 Receiver Interface

3.1.1 RIB

The RIB controls the generation of the baseband chirp and provides system-timing parameters (PRI, Tx Gate, Data Gate). The PRI is made available on the GTM Bus. The RIB is also responsible for the time stamping and digitization of the received baseband signal. The digitized signal is sent to the MDR for recording to the JBOD through the FPDP interface.

The RIB contains the embedded SNAP Microcontroller

3.1.2 MDR

The MDR is the interface between the digitization function of the RIB and the JBOD, which is the permanent storage of the digitized signal before data processing on the ground. The MDR will support a 2Gbit Fibre channel (FPDP-II, 160Mbytes/s). However, it will maintain backwards compatibility with existing Star-3i 1Gbit Fibre channel JBODs. Recording of data through the MDR is dependant on the configuration by the MCC through the available dedicated MDR LAN connection.

3.1.2.1 MDR Ethernet Interface

The MDR Ethernet connection port must be available on the front panel.

3.1.2.2 MDR Serial Interface

The MDR Serial connection port must be available on the front panel.

3.1.2.3 JBOD Interface

A Fibre Channel connection port must be available on the front panel.

3.2 Receiver Exciter (RCVEX)

The receiver exciter is the main implementation of the RF Design. It up converts the base-band signal to the x-band transmit frequency (9.605GHz CF). The signal is amplified and broadcast by the TRANS-WGASS. The module also down converts the amplified receive signal where the signal power may be attenuated before being digitized and recorded by the RCAS.

3.2.1 Calibrated RCVEX drive output power

The drive power of the RCVEX to the XTRANS module will be calibrated to a level standardized for all RCVEX modules, so they can be interchanged and are not matched to a specific XTRANS module.

3.2.2 Test Tone

A separate oscillator must be provided, generating a coherent X-band test tone that can be received in order to test the phase locked coherence of all other RCVEX oscillators and verify the overall receiver gain.

3.3 Automatic Gain Control (AGC)

The return signal attenuation will be adjusted by an AGC in the RCAS microcontroller and hardware. The AGC will automatically adjust the RCVEX return signal attenuation to achieve optimal recording level.

Additionally, the AGC may be disable, and the attenuation adjusted manually.

3.4 10MHz STALO reference clock

The RCVEX-RCAS will provide a 10MHz STALO clock internally in the module. The clock will be available on the GTM Bus for synchronization.

3.5 Test Ports Interface

The RCVEX-RCAS must provide sufficient signal test ports to allow completion of ATP and verification of module performance.

3.6 WGASS-TRANS Interface

The following connections ports must be available between the RECEX-RCAS and the WGASS-XTRANS:

3.6.1 Xtrans Signal

An RF out signal must be available on the front panel.

3.6.2 Transmit Gate

A Transmit Gate signal must be available on the front panel.

3.6.3 Xrec Signal

A Video in (receive signal) signal must be available on the front panel.

4 INTERFACE

What connectors are available on this module?

5 HARDWARE DESIGN

5.1 PCBs

5.2 FPGA core

- register maps?

5.3 PIN Switch Interface Box

Schematics:

Sensor assignment:

temperature sensor 1:	PIN switches (location undefined)
temperature sensor 2:	PIN switches (location undefined)
temperature sensor 3:	not installed
temperature sensor 4:	not installed
humidity sensor 1:	not installed
humidity sensor 2:	not installed

-

6 SOFTWARE DESIGN

6.1 Command Interface

6.1.1 Rib Configuration commands:

Any commands that modify the current rib configuration (setPRF, setTxGate, setRadarMode, etc..) must wait until a *ribCfgEvent* Interrupt is generated from the FPGA. If no interrupt is generated after a specific wait period, the command Response will return with an error code of 'Module Error'.

The module must also not allow the current rib configuration to change when the signal source is not set to 'Transition mode'. Those commands will return with an error code of 'not ready'.

6.1.2 Signal Source Command

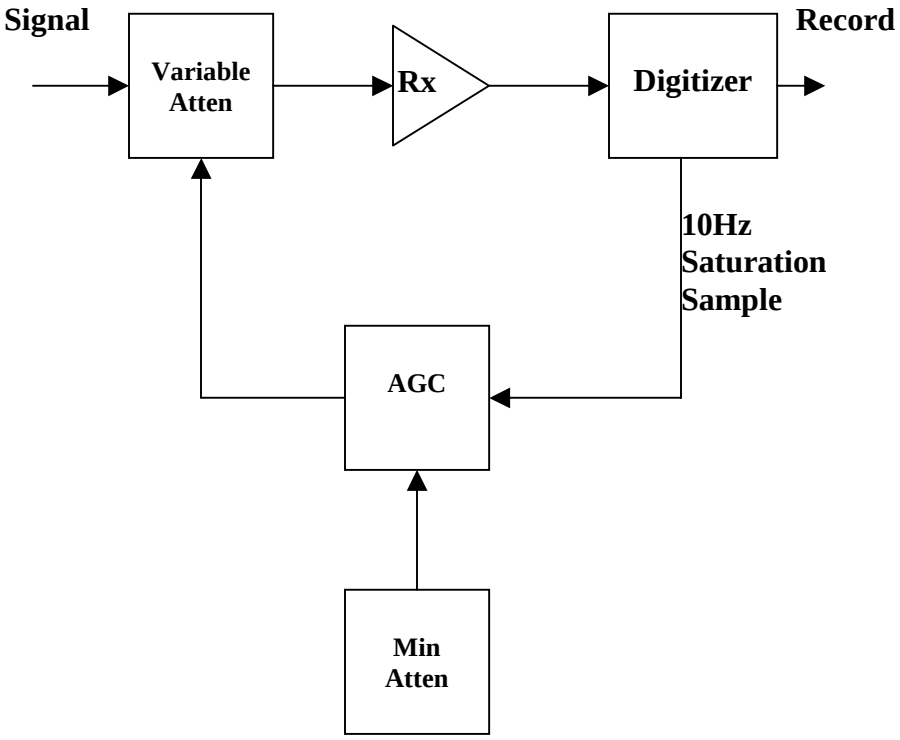
When the module is commanded to set its signal source, it will modify the Radar Mode register to contain the signal source information as outlined in the System ICD. The command will not return until a R*adarModeEvent* interrupt is received. If no interrupt is generated, the command Response will return with an error code of 'Module Error'.

When a *setSignalSource* command is executed on the RCAS, the following sequence of events occur:

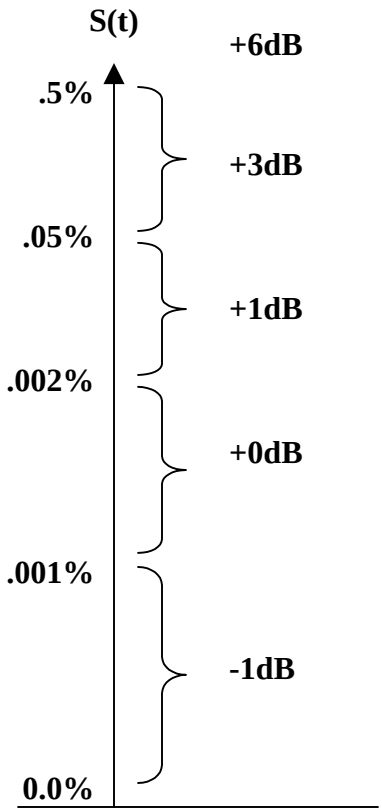
1) The Firmware checks the current Signal Source on the RIB FPGA. If the current mode is greater than 0x00 (i.e. not in Transition) and the new mode is not 0x00 (Transition), the command response it returned with a 'not ready error'. (i.e. The firmware will not allow direct transition from Noise Test -> Syntar without going through a transition state).
2) The new signal source / radar mode register is set to the RIB *RadarMode* register (0x360002) as per the System ICD.
3) The new configuration is enabled by writing a bit in the RIB config register (0x360001)
4) The firmware waits for the *RadarModeEvent* to occur (via interrupt). If no event occurs in 300ms, the command Response is returned with the 'module error' flag set.
5) The RCAS status packet is updated to contain the current Radar Mode / Signal Source
6) The RCAS generates an internal 'variable interrupt', which triggers the status server to send a new status packet.
7) The firmware Command Response returns with 'no error' flag set.

6.1.3 AGC

The automatic gain control is based entirely on saturation. Refer to the following Control Syste Diagram



The attenuation is adjusted by the AGC based on saturation as follows:



Attenuation Adjustment = A_{adj}

$A_{adj} = -1u(0) + u(s - 0.01) + u(s - 0.02) + 2u(s - 0.05) + 3u(s - 0.5)$

In general:

$A_{adj} = C_0u(s - S_0) + C_1u(s - S_1) + \ldots + C_Nu(s - S_N)$

The coefficients descried above will be set in the Configuration ROM.

7 MECHANICAL DESIGN

Physical design (chassis)

Electrical characteristics

8 THEORY OF OPERATION

8.1 Antenna PIN-switch Error Detection

The antenna PIN-switch error detection compares the control signal outgoing to the antenna PIN-switch with the self test return signal (which is combined in the PIN-switch interface box from the return signals of the three individual PIN-switches). The combined PIN-switch return signal indicates errors such as non-differential signal levels or failures of the PIN-switches. The intent of this circuit is to detect PIN-switch errors, make this error condition accessible to the MCC software and shut down transmission of RF power in order to prevent further damage of the PIN-switches or the transmitter, by inhibiting the transmit gate signal in the WGASS module.

Under normal conditions the PIN-switch return signal is low (TTL). In case of an error this signal goes high (permanent error, e.g. a signal is not differential or disconnected) or toggles with a 50% duty cycle according to the PRF (e.g. when a PIN-switch is stuck in one position). Very short positive spikes might occur due to propagation delays between drive signal and return signals and due to EMI, as the signal is routed from the pedestal to the RCVEX module.

Basically the CPLD code resembles a low pass filter. The PIN-switch return signal is sampled every 10 µs (10 MHz clock divided by 100). In case of an error signal, an error counter is incremented by 5, while in case of no error the counter is decremented by 1, unless it is already zero.
If the error counter has reached a value of 1000 or more, the PIN-switch error output signal (IO-A-D08 on pin 30c of the IO-card DIN-header, respectively pin H on the WGASS-RCWEX link J3.05 and J4.05) goes high and is latched. A logic 1 on the I^2C parallel interface adress 0, pin I2C-01 resets the error latch.

So for a permanent PIN-switch error return signal, the CPLD requires 1000 / 5 * 10 µs = 2 ms to switch into the error state, for a error return signal switching with 50% duty cycle, the CPLD requires typically 1000 / (5 – 1) * 10 µs = 2.5 ms. The CPLD will not switch into an error state, if the error return signal is on in average less than 20% and never longer than 2 ms.

What happens in the system when a command is sent??

How is it connected?

How does it control?

9 NOISE AND SPURIOUS SIGNALS

9.1 Summary

Transmit losses:	XTRANS output to antenna, radome losses
Receive losses:	Antenna to WGASS wave guide port, radome losses
Noise figure:	1.64 dB (total for WGASS and RCVEX module)
Effective noise bandwidth:	197 MHz (135 MHz mode, without digital baseband filtering)
	167 MHz (135 MHz mode, with digital baseband filtering)
	345 MHz (270 MHz mode, without digital baseband filtering)
	285 MHz (270 MHz mode, with digital baseband filtering)
Phase noise:	-50 dBc single side band for a 1 ms delay
Spurious signals:	-40 dBc max., -50 dBc goal
Harmonics:	-40 dBc max., -50 dBc goal (inband)
AM modulation:	-40 dBc max., -50 dBc goal
Dynamic range :	tbd from STAR4-RF-calc.

9.2 Noise figure

The noise figure of the system modules can be separated into the following contributions:

9.2.1 Losses between the wave guide input of the WGASS module and the LNA input

0.69 dB for STAR4 which matches well with specified data for the main contributing conponents: cross guide couplers, transmit/receive circulator, LNA protection ferrite switches, wave guide to coax transition and coax cable to LNA.

9.2.2 LNA noise figure

0.93 dB for the STAR-4 LNA.

9.2.3 Additional noise acquired in following RF stages

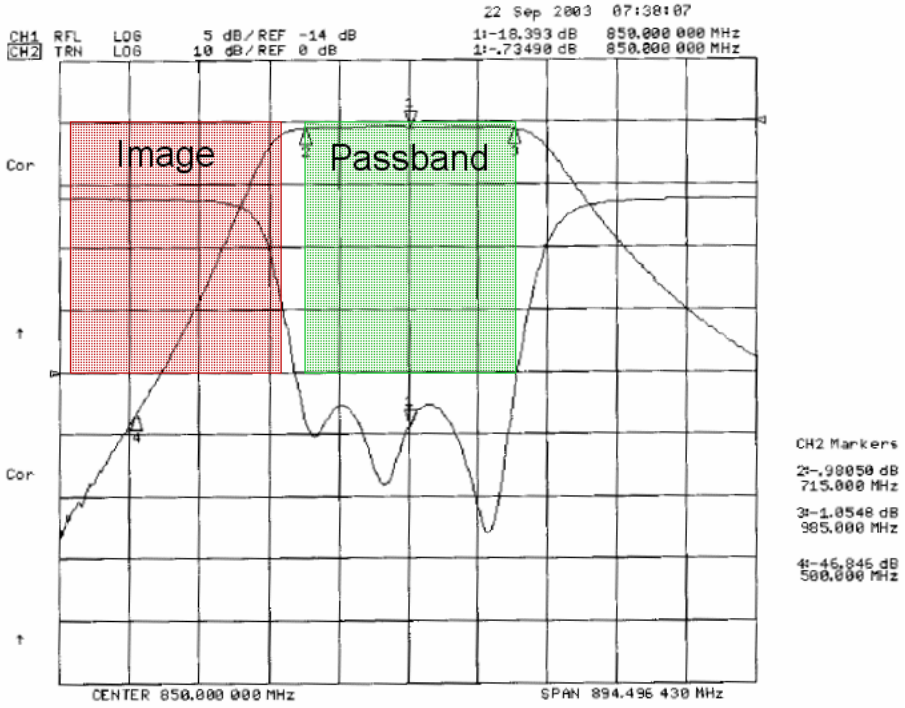
Once the signal is amplified by the first LNA, the level must be kept in the consecutive stages at least 16 dB above thermal noise in order to keep additional acquired noise negligibly small.

For the STAR-4 the losses beween the LNA (inside the WGASS module) and the first catch up amplifier (insider the RCVEX) typically add another 0.12 dB.

9.3 Effective noise bandwidth

Another potential source for additional noise is aliasing during down conversion and final baseband sampling. In the 8.8 GHz down conversion stage passband and image are separated by more than 1400 MHz respectively ±8% of the LO. This easily allows supression of the image sideband by more than 30 dB, so that no excess noise is downconverted.
At the 700/730 MHz downconversion the frequency scheme is significantly more narrow, so that some excess noise from the image band will be acquired. In both cases the gap around the LO allowing the filter to roll off is only 11% of the pass band width. The filter specification in this

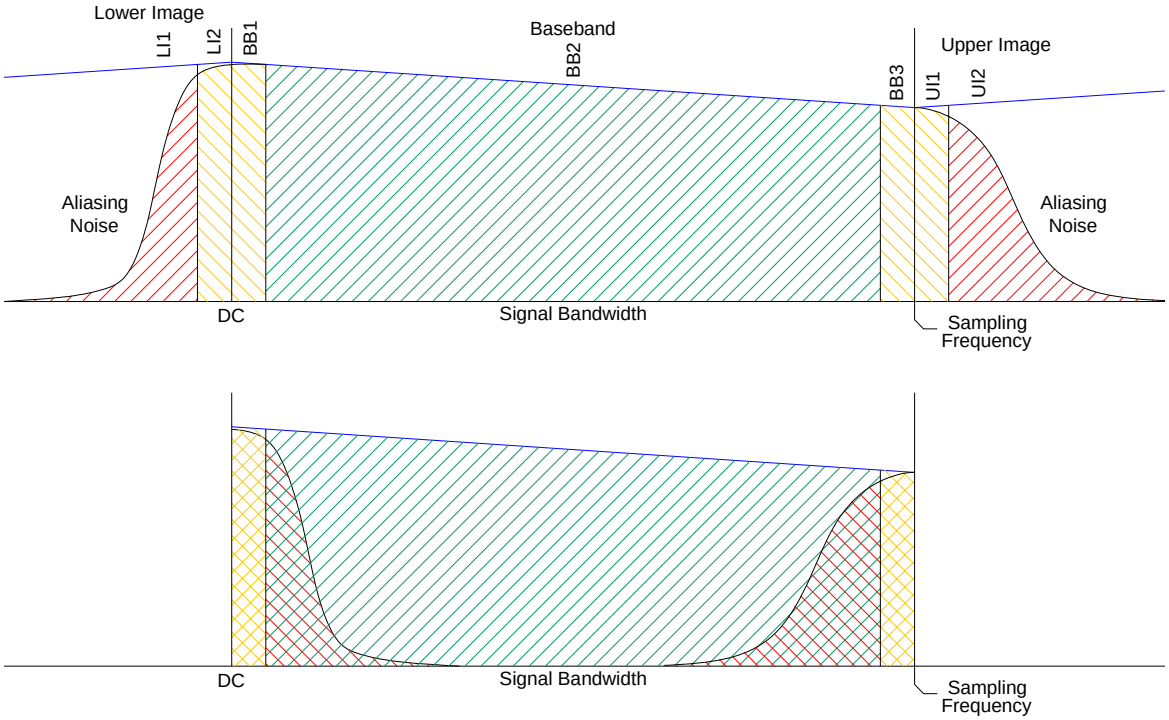
case is a trade off between flat passband response and steep increase of rejection in the image band. Beyond approximately 16 dB filter rejection, the contribution of the image band is negligible. From the manufacturer´s charts (Lorch, Filtek) the 3 dB pass band width is typically 1.22 x the 0.5 dB width for filters with 4 to 10 sections. Additionally the manufacturers require a 0 to 10% safety margin in band width , in order to meet passband specs.
The following graph shows the measured filter characteristics for the 270 MHz mode image rejection filter.



Characteristics of the image reject filter for the 270 MHz mode

A useful key number describing this noise aliasing, is the effective noise bandwidth. Effective bandwidth in this context refers to the integral of bandwidth times attenuation (linear power ratio, relative to the passband level). The effective noise bandwidth con be separated into the portions LI1 through UI2 as shown in the diagram.

The lower image LI1 and LI2 are determined by the IF filters of the 700/730 MHz down conversion, while the upper image UI1 and UI2 are mainly determined by the baseband lowpass filters. With digital filtering of the raw data, noise from the sections around DC, L2 and BB1, and around the sampling frequency, BB3 and UI1, can be removed. In any case noise from the sections LI1 and UI2 are mirrored into the signal bandwidth and add to the effective noise bandwidth.



Mirrored noise from aliasing, increases the effective noise bandwidth

(measurements: 2004-03-02)	135 MHz mode	270 MHz mode
LI1	25 MHz	11 MHz
LI2	7.5 MHz	15 MHz
BB1	7.5 MHz	15 MHz
BB2	135 MHz	270 MHz
BB3	7.5 MHz	15 MHz
UI1	7.5 MHz	15 MHz
UI2	7 MHz	4 MHz
Effective noise bandwidth with digital baseband filtering	167 MHz	285 MHz
Effective noise bandwidth without digital baseband filtering	197 MHz	345 MHz

A technically challanging approach to reduce this additional noise bandwidth, could be the use of image reject mixers. Typically this type of mixer provides 18 dB min. image rejection, but only within a relative IF bandwidth limited to 1:2. MITEQ also offers as a special multioctave version with a IF bandwidth of 10 – 300 MHz.

9.4 Total system noise figure

For simplicity and in order to define a single number for the entire SAR system, all losses, noise figures and noise bandwidths can be summarized in the total system noise figure.

Mode	135 MHz	270 MHz
Transmit losses (XTRANS to WGASS)	0.13 dB	
Transmit losses (inside WGASS)	0.49 dB	
Transmit losses (WGASS to antenna)	1.73 dB	
Transmit losses (Radome)	0.3 dB (est. ??)	
Receive losses (Radome)	0.3 dB (est ??)	
Receive losses (antenna to WGASS)	1.73 dB	
Receive losses (inside WGASS)	0.69 dB	
Noise figure LNA	0.93 dB	
Additionall noise aquired in following RF stages	0.12 dB	
effective noise bandwidth vs. signal bandwidth, converted to dB	0.92 dB	0.23 dB
Total system noise figure	7.34 dB	6.65 dB

9.5 Phase noise

Phase noise are random or periodic phase fluctuations with an offset typically greater 1 Hz off carrier which decorrelate the precise phase relationship between pulses. Changes in phase slower than 1 Hz are considered phase drift and are not captured in this phase noise analysis, as this frequency range contributes a negligible phase change from pulse to pulse.

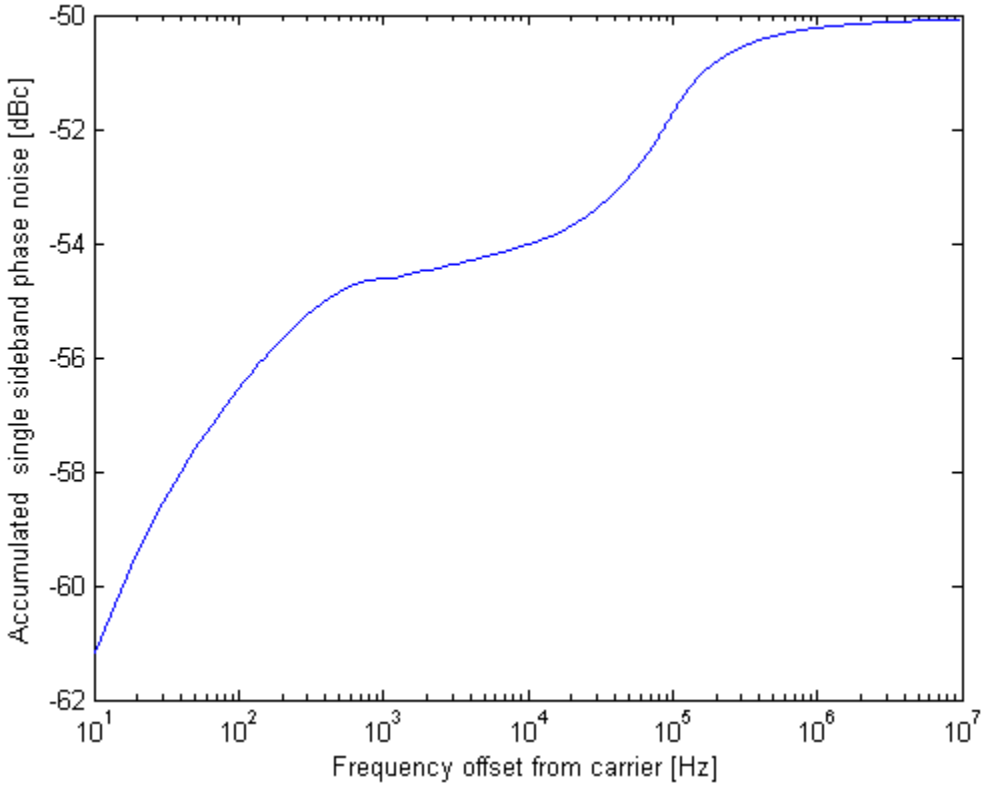
The system phase noise is dominated by the 2nd LO PLL at 8.8 GHz. STAR4 uses a LPLM oscillator built and recommended by MITEQ that has virtually the same specifications as the PLM model from STAR3i.

The guaranteed phase noise data for a MITEQ 8 GHz LPLM oscillator are:

Offset from carrier	Single sideband phase noise
100 Hz	-80 dBc / Hz
1 kHz	-100 dBc / Hz
10 kHz	-107 dBc / Hz
100 kHz	-107 dBc / Hz
1 MHz	-127 dBc / Hz
10 MHz	-145 dBc / Hz

In order to calculate the rms phase difference for a specific delay, these data have to be multiplied by a weighting function and integrated. The weighting function oscillates in linear scale between 0 and 2 and defines the contribution of a side band frequency for a specific delay.

The following figure shows the rising accumulated single side band phase noise power vs. integrated bandwidth for a 1 ms delay for the STAR4 8.8 GHz LO based on the specified data. For a 0.5 ms delay the numbers are approximately 1 dB lower.



The major phase noise is accumulated around 100 kHz carrier offset, while the total noise power stabilizes beyond 1 MHz carrier offset. Based on a total single sideband phase noise power of –50 dBc for a 1 ms delay the rms phase difference calculates to 0.36 deg. respectively to a 150 mm rms error in 10 km slant range with a 1 m baseline for a single unaveraged resolution cell.

9.6 Spurious signals

Spurious signals are unwanted constant tones generated in the system. They typically come from LO leakage which is attenuated only to a certain extent. The power of spurious signals that show up in the received baseband is maintained and equally distributed in range after compression. For this reason the power of spurious base band signals is equivalent to thermal noise and should be kept below this system noise floor. As a guide line the power of spurious signals should stay 13 dB below the noise power of the received baseband signal in oder to contribute less than 0.2 dB to the combined power.

Typical spurious signals in the upconverter at the X transmit signal output are:

8.800 GHz = 2^{nd} LO. With a specified LO/RF isolation of 30 dB and a filter rejection of typically >60 dB, the nominal spurious power is at –62 dBm compared to nominally 0 dBm signal power. Additionally this frequency is filtered in the receiver chain with >60 dB attenuation and it is typically out of the specified frequency range of the planar antennas.

9.500 GHz = 1^{st} LO + 2^{nd} LO. As the sidebands in the first upconverter have only a 15 MHz separation to the LO at 700 MHz, the LO must be notched with a narrow 1% 3dB-BW bandstop filter. With LO/RF isolation of >35 dB and a notch depth >60 dB the expected spurious output power is below -70 dBm respectively 70 dB below signal power. Additionally in the downconverter section this attenuated another >20 dB by the IF filter in 135 MHz mode respectively converted to DC in the 270 MHz mode.

Typical spurious signals in the downconverter chain are:

9.600 GHz Leakage of the test tone oscillator, when switched off. With two switches in series, this level is designed to stay below –165 dBm, respectively 76 dB below the total noise power, when switched off.

8.800 GHz = 2^{nd} LO. Not expected to propagate effectively through the following IF downconverter chain and filters, designed for frequencies below 1000 MHz.

730 MHz = 1^{st} LO. Attenuated by the mixer LO/IF isolation and the baseband low pass filter to a level of nominally –73 dBm (= 0.03 inc) at the baseband output.

700 MHz = 1^{st} LO. Attenuated by the mixer LO/IF isolation and the baseband low pass filter to a level of nominally –63 dBm (= 0.08 inc) at the baseband output.

9.7 Harmonics

Harmonics are signal coherent sidebands that also contribute quasi noise power as they are not correctly compressed by the range compression. Of practical relevance are only x 3 harmonics that are generated by all active devices like amplifiers and mixers. For our type of application only baseband harmonics are of relevance, as all harmonics of upconverted signals are out of band and chirp signals do not generate intermodulation products.

Baseband signals that generate inband harmonics are:

Upconverter:	135 MHz mode:	37.5 MHz to 57.5 MHz
	270 MHz mode:	15 MHz to 95 MHz
Downconverter :	135 MHz mode:	7.5 to 47.5 MHz
	270 MHz mode:	15 MHz to 95 MHz

Design rule is to keep inband harmonics below –40 dBc. At this level noise power from harmonics will not dominate and is at the same level as noise from quantisation and saturation. Also S/N ratios of 40 dB for the received signal are typically not reached.

In order to keep harmonics below –40 dBc, a good design rule is to stay 10 dB below the specified 1 dB compression point. With a third order intercept point IP3 of typically 10 dB higher, the power level of x 3 harmonics is at –40 dBc.

For inband harmonics the 1st LO mixer in the upconverter comes close to this limit, while in the downconverter baseband mixers and amplifiers stay even >20 dB below the specified 1 dB compression point at nominal signal level, generating negligible harmonic signals at levels of –60 dBc.

9.8 AM noise

Amplitude modulation of the received signal generates equivalent sidebands after compression, i.e. sideband power of this multiplicative noise is compressed too, however generating “ghost images”. For modulation frequencies within the baseband frequency range, the sidebands show up in range, for lower modulation frequencies of Hz to kHz, they show up in azimuth.

Although this unwanted signal is fully coherent, the same limits as for incoherent noise are applied and the design specification is to keep AM sideband power below –40 dBc.

It must be mentioned, that slope and ripple within the baseband basically also is AM. However this AM contributes only little sideband power very close to the correlation main peak. In practice with a baseband ripple of 1 dB and a slope of 5 dB the correlation sidebands adjacent to the mainlobe are below –19 dBc.
The forward characteristics and impedance matching of nearly all components in the downconverter contribute to basebend ripple and slope. Design goal is to keep the resulting overall ripple below 1 dB and the slope better than 5 dB.

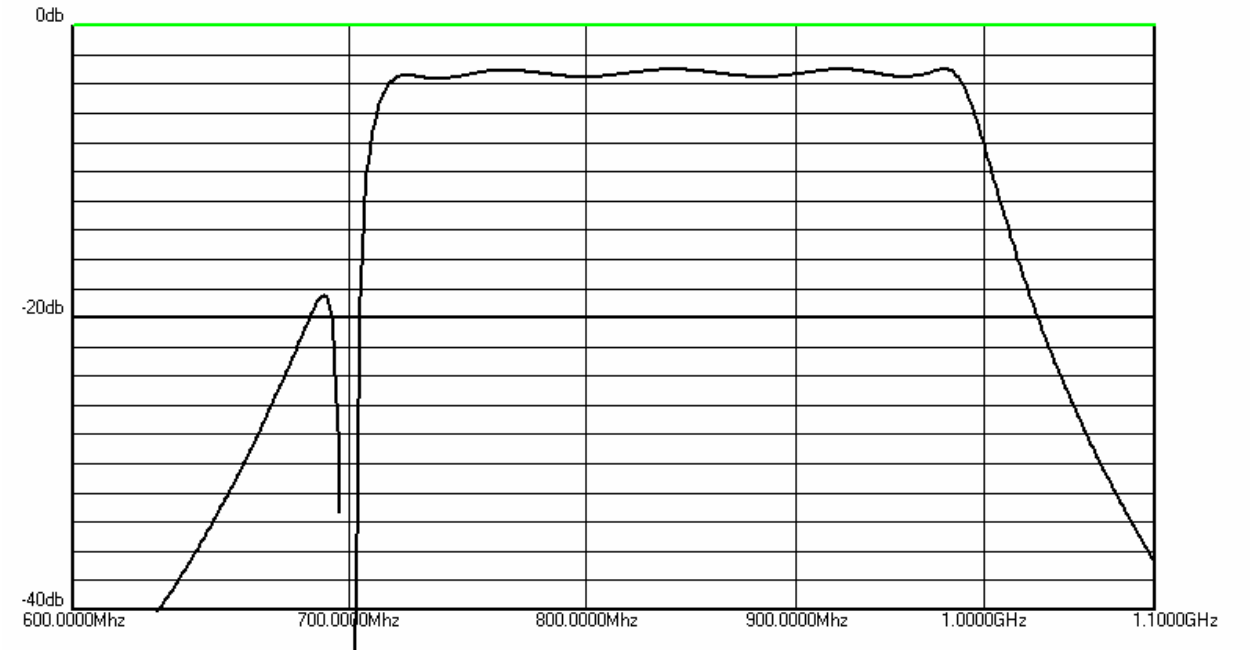
Typical data from replicas:	135 MHz mode slope / ripple	270 MHz mode slope / ripple
STAR-4:	1.4 dB / ±0.8 dB	1.6 dB / ±1.6 dB

9.9 Dynamic range

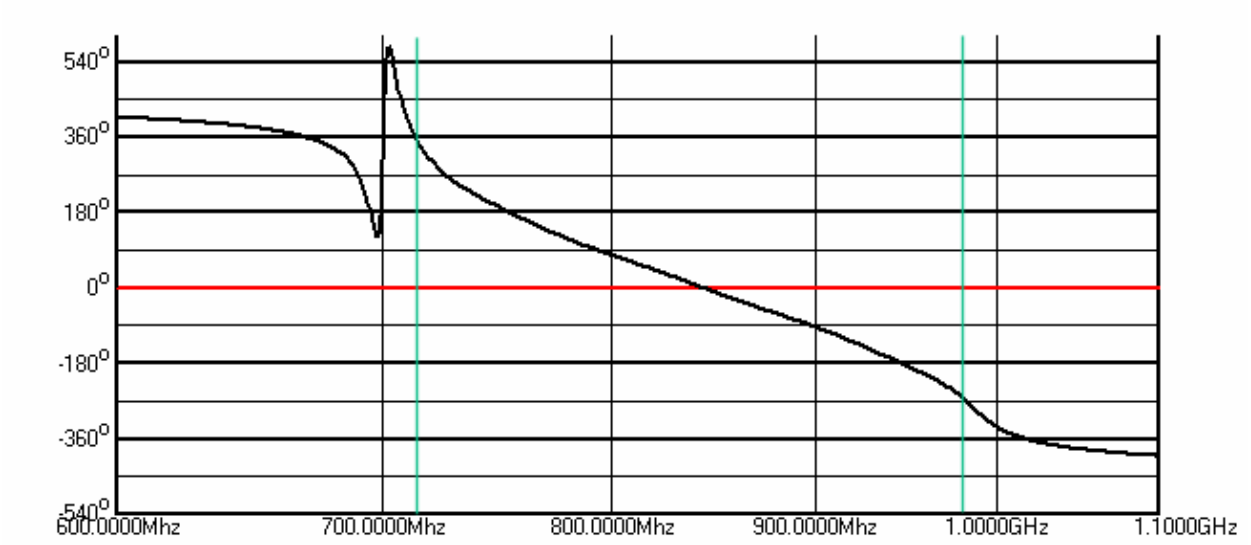
… see STAR4-RF-Calculator

10 PHASE INTRODUCED BY FILTERS

The following diagram shows the proposed filter combination for the upconverter chain. It is composed of a 1% notch filter at 700 MHz, a 3 dB pad and a 0.5 db ripple Tchebycheff band pass filter. The notch filter is designed to add 60 dB LO supression to the LO/RF isoltaion of the mixer. With this filter combination the 700 MHz LO leakage is nominally 70 dB below the transmitted signal power.



Upconverter filter characteristics with 700 MHz notch filter



Total phase of the upconverter filter combination (green: passband)

As the linear phase term can be ignored (it relates to constant propagation delay of approximately 1.5 m) the higher order terms of the phase vs. chirp frequency typically do not

exceed in total ±90 deg. Simulations show, that such phase terms, if captured in the reference chirp for range compression, do not degrade the range compression.

Tool for filter calculation: AADE Filter Design V3.0 (freeware, installation file fdinstall.exe can be found in the RCVEX ressources folder).

11 MAINTANANCE

11.1 Test Procedures

How to test?

11.2 Calibration

How to calibrate??

APPENDIX 1: DRAWINGS

APPENDIX 2: SCHEMATICS