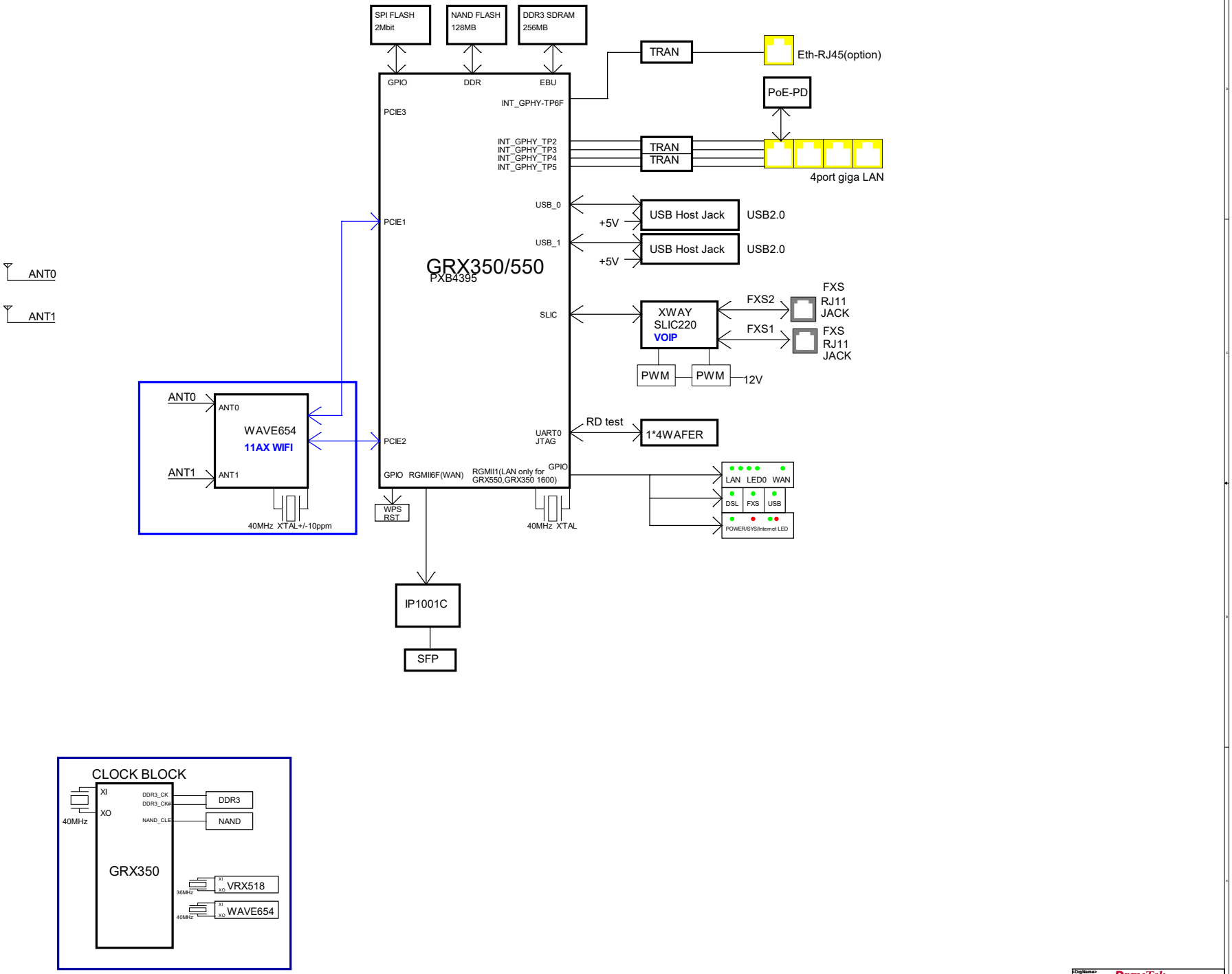
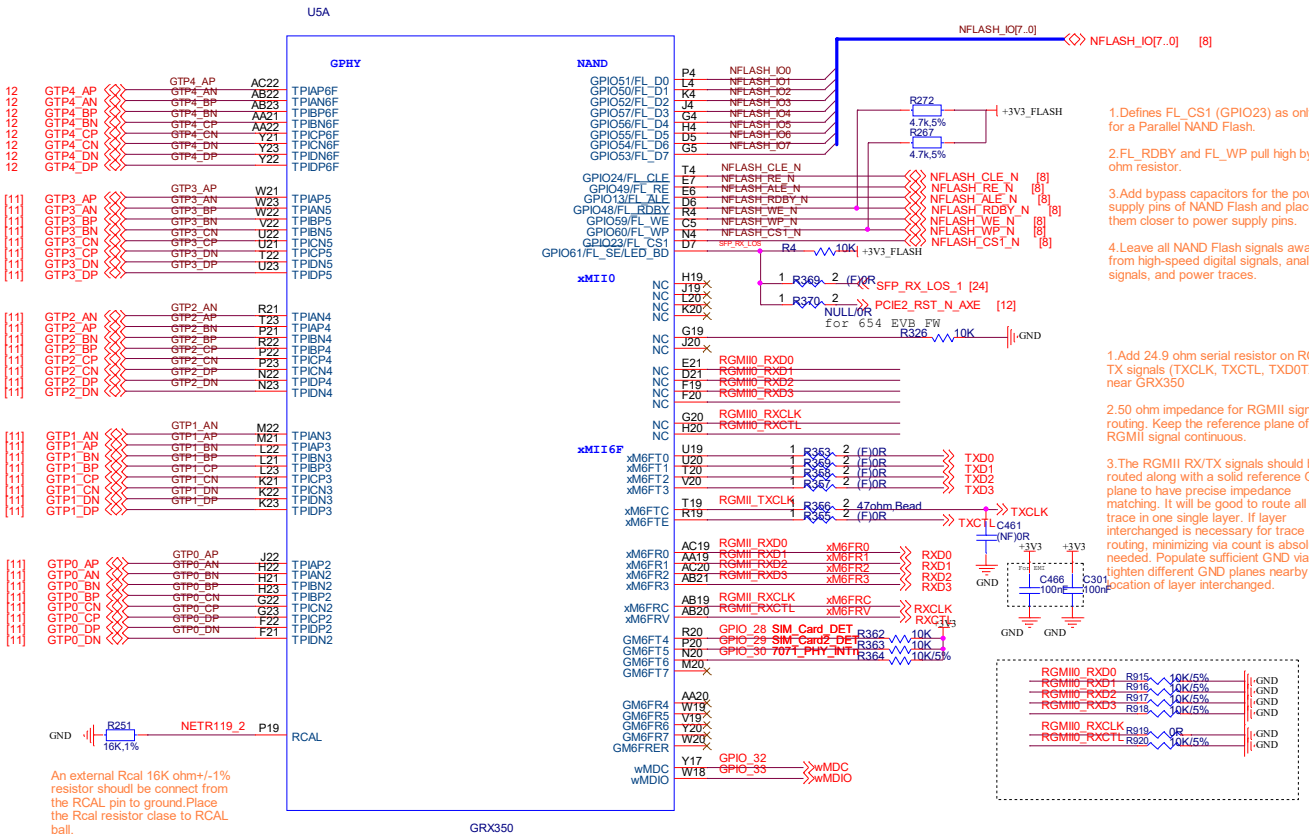

SPI FLASH
2Mbit
NAND FLASH
128MB
DDR3 SDRAM
256MB
GPIO
DDR
EBU
TRAN
Eth-RJ45(option)
PoE-PD
INT_GPHY-TP6F
PCIE3
INT_GPHY_TP2
INT_GPHY_TP3
INT_GPHY_TP4
INT_GPHY_TP5
TRAN
TRAN
4port giga LAN
USB_0
USB Host Jack
USB2.0
+5V
PCIE1
USB_1
USB Host Jack
USB2.0
+5V
GRX350/550
PXB4395
ANT0
ANT1
SLIC
XWAY
SLIC220
VOIP
FXS2
FXS
RJ11
JACK
FXS1
FXS
RJ11
JACK
PWM
PWM
12V
ANT0
ANT0
WAVE654
11AX WIFI
ANT1
ANT1
40MHz X'TAL+/-10ppm
PCIE2
UART0
JTAG
RD test
1*4WAFER
GPIO
RGMII6F(WAN)
RGMII1(LAN only for
GRX550,GRX350 1600)
GPIO
LAN
LED0
WAN
DSL
FXS
USB
POWER/SYS/Internet LED
WPS
RST
40MHz X'TAL
IP1001C
SFP
CLOCK BLOCK
XI
XO
40MHz
DDR3_CK
DDR3_CK#
NAND_CLE
DDR3
NAND
GRX350
36MHz
VRX518
40MHz
WAVE654



1.100 ohm characteristic impedance control for TPI differential signal routing. Keep the reference plane of signal continuous.

2.The TPI signals should be routed along with a solid reference GND plane to have precise impedance matching. It will be good to route all the trace in one single layer. If layer interchanged is necessary for trace routing, minimizing via count is absolutely needed. Populate sufficient GND vias to tighten different GND planes nearby the location of layer interchanged.

An external Rcal 16K ohm+/-1% resistor shoudl be connect from the RCAL pin to ground.Place the Rcal resistor clase to RCAL ball.

1.Defines FL_CS1 (GPIO23) as only CS for a Parallel NAND Flash.

2.FL_RDBY and FL_WP pull high by 10K ohm resistor.

3.Add bypass capacitors for the power supply pins of NAND Flash and place them closer to power supply pins.

4.Leave all NAND Flash signals away from high-speed digital signals, analog signals, and power traces.

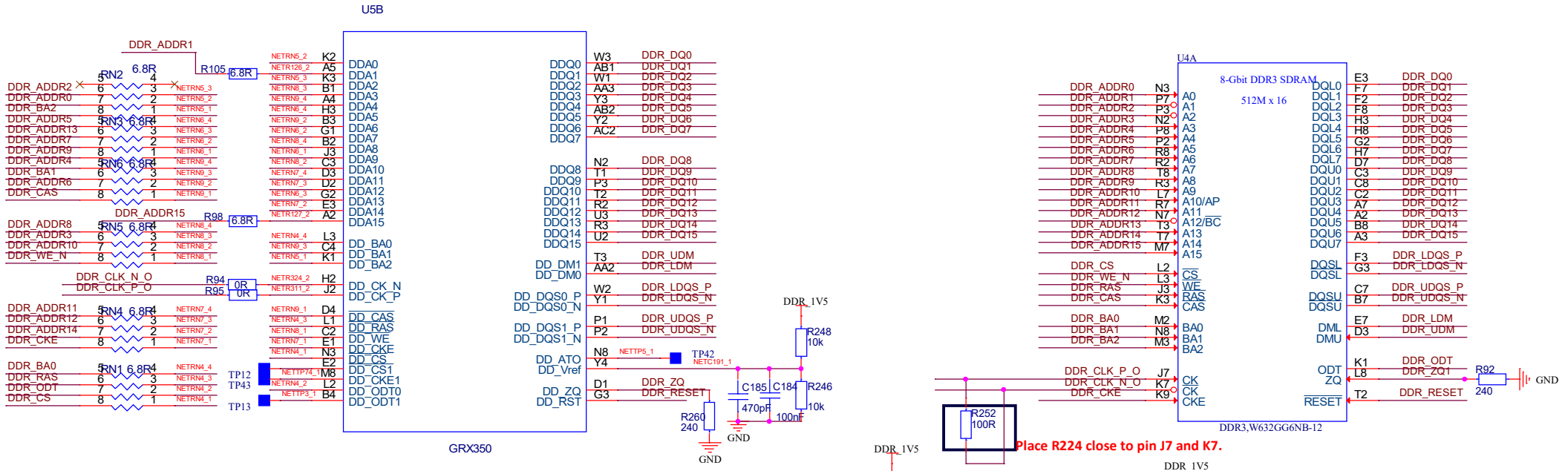
1.Add 24.9 ohm serial resistor on RGMII TX signals (TXCLK, TXCTL, TXD0TXD3) near GRX350

2.50 ohm impedance for RGMII signal routing. Keep the reference plane of RGMII signal continuous.

3.The RGMII RX/TX signals should be routed along with a solid reference GND plane to have precise impedance matching. It will be good to route all the trace in one single layer. If layer interchanged is necessary for trace routing, minimizing via count is absolutely needed. Populate sufficient GND vias to tighten different GND planes nearby the location of layer interchanged.

HEATSINK CLIPS

<OrgName>	DrayTek		
Title	GRX350_NAND_xMII_GPH		
Size: Custom	Document Number: V2135AX		Rev: 6C
Date: Friday, February 11, 2022	Sheet 2 of 26		



Qualified DDR3 List

Etron: EM6GC16EWXD-10H (64Mx16bit, single rank (CS0))

Micron: MT41K128M16JT-125:K (128Mx16bit, single rank (CS0))

Micron: MT41K256M16HA-125 IT:E (256Mx16bit, single rank (CS0))

Winbond: W634GG6LB-12 (256Mx16bit, single rank (CS0))

Etron: EM6GE16EWXC-10H (256Mx16bit, single rank (CS0))

Nanya: NT5CB256M16DP-EK (256Mx16bit, single rank (CS0))

Micron: MT41K512M16HA-125:A (512Mx16bit, single rank (CS0))

1.Place 6.8ohm series termination resistors close to GRX350 for CA group.

2.An external RZQ 240 ohm+/-1% resistor shoudl be connect from the ZQ pin to ground on both GRX350 and DDR device.

3.System DD_VREF and DDR device VREFCA and VREFDQ are separated,divided by 10K ohm +/-1% resistors.

4.55 ohm Single-End and 100 ohm Differential signals impedance control

5.5mils Single-End trace width, trace to trace clearance is 10mils

6.Length Matching
Maximum trace length difference (skew) between DQS and DQS#: ± 4 mils (< 0.6 ps).
Maximum trace length difference (skew) DQ to DQS/ DQS# domain: ± 30 mils (< 10 ps).
Maximum trace length difference (skew) Addr/Cmd to CK/ CK# domain: ± 70 mils (< 25ps).
Maximum trace length difference (skew) DQS/DQS# to CK/ CK# domain: ± 250 mils (< 90ps).

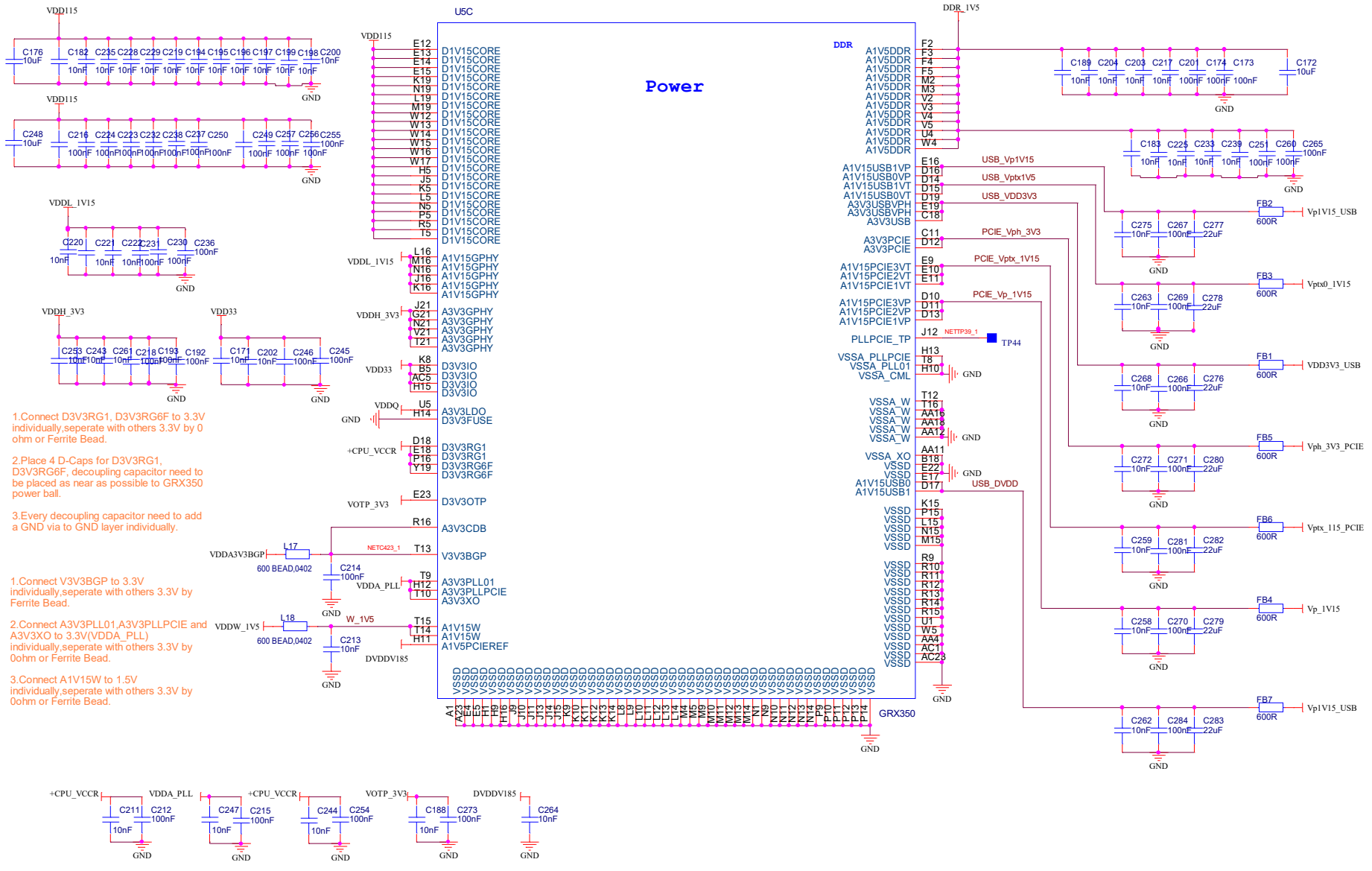
7.Crosstalk control (Note: H is distance from reference layer):
Keep edge-to-edge trace spacing within DQ/DM byte group > 2H
Keep edge-to-edge trace spacing within Cmd/Add/Ctrl > 2H (commonly known as CA)
Keed edge-to-edge trace separation for each group (DQ, DQS/DQS#, CA, CK/CK#) > 3H

8.DDR CLK differential termination 100ohm place at the end on DDR device. as close to CLK pins as possible.

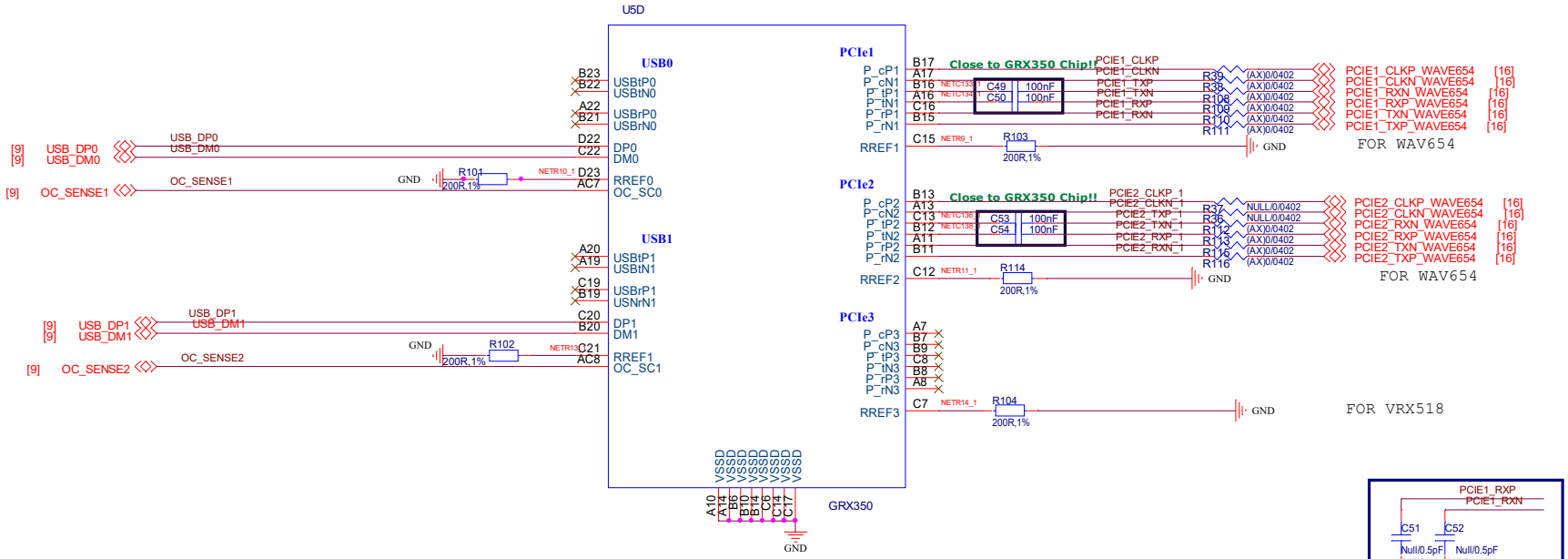
9.Fly-By Topology & VTT Termination recommended for DDR3, if multiple devices are used.

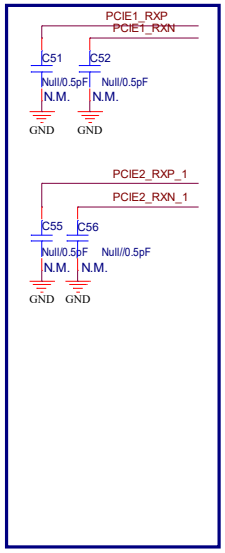
10.Carefully consider layout requirements of DDRn vendor!!!

<OrgName>	DrayTek
Title	GRX350_DDR3_x16
Size	Custom
Document Number	V2135AX
Rev	6C
Date:	Friday, January 28, 2022
Sheet	3 of 26



<OrgName>	DrayTek		
Title	GRX350_Power		
Size: Custom	Document Number: V2135AX		Rev: 6C
Date: Friday, January 28, 2022	Sheet 4 of 26		





1.An external Rref 200 ohm+/-1% resistor should be connect from the USB RREF0, RREF1 pins to ground. Place the Rref resistor close to RREF balls.

2.Place 2 AC coupling capacitors on USB TX pairs , <0.5inch length to GRX350 is recommended.

3.90 ohm characteristic impedance control for USB differential signal routing. Keep the reference plane of signal continuous.

4. Match trace length of differential pairs (_p and _n signal) to given value in appropriate interface specification.

5. Populate sufficient GND vias nearby each PCIE differential pairs to tighten adjacent GND plane with GND layer.

1.An external Rref 200 ohm+/-1% resistor should be connect from the 3 PCIE RREF pins to ground. Place the Rref resistors close to RREF balls.

2.Place 2 AC coupling capacitors on PCIE TX pairs , <0.5inch length to GRX350 is recommended.

3.100 ohm characteristic impedance control for differential signal routing. Keep the reference plane of signal continuous.

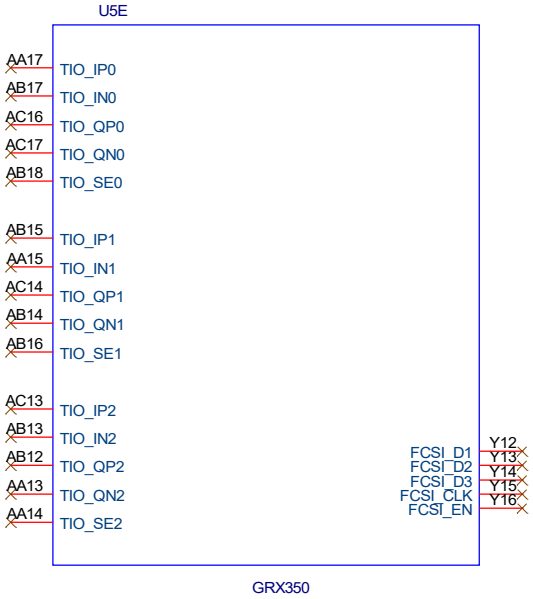
4.In case with >= 2 PCIe differential pairs routing on PCB, a footprint of shielding case to enclose all these differential pairs is highly recommended for the compliance of EN300-328 V1.8.1 standard.

5.0.5pF capacitors to ground on PCIE RX pairs, place them close to GRX350.

6. Match trace length of differential pairs (_p and _n signal) to given value in appropriate interface specification.

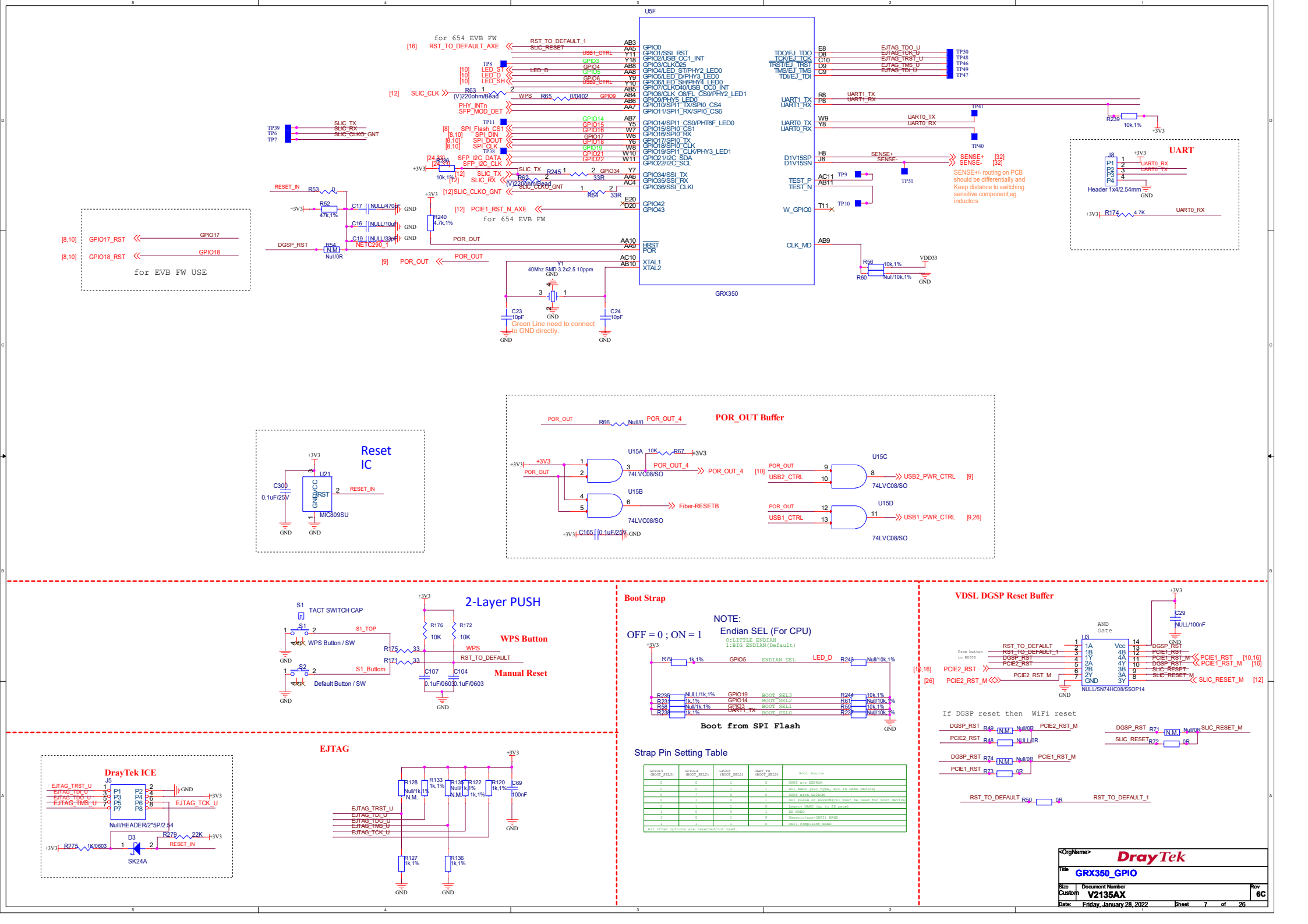
7. Populate sufficient GND vias nearby each PCIE differential pairs to tighten adjacent GND plane with GND layer.

<OrgName>	DrayTek	
Title	GRX350_PCIE_USB	
Size: Custom	Document Number: V2135AX	Rev: 6C
Date: Friday, January 28, 2022	Sheet 5 of 26	



Trace capacitance for BBIO interface must be below 10pF! Recommend the maximum length should be under 3 inch.

<OrgName>	DrayTek	
Title	GRX350_BBIO	
Size: Custom	Document Number: V2135AX	Rev: 6C
Date: Friday, January 28, 2022	Sheet 6 of 26	



GPIO19 (BOOT_SEL3)	GPIO14 (BOOT_SEL2)	GPIO3 (BOOT_SEL1)	UART_TX (BOOT_SEL0)	Boot Source
0	0	1	0	UART w/o EEPROM
0	0	1	1	SPI NAND (SLC type, ECC in NAND device)
0	1	0	0	UART with EEPROM
0	1	0	1	SPI FLASH or EEPROM(CS1 must be used for boot device
0	1	1	0	Legacy NAND (up to 2K page)
1	0	0	1	BE-NAND
1	0	1	0	Generic(non-ONFI) NAND
1	1	1	0	ONFI compliant NAND

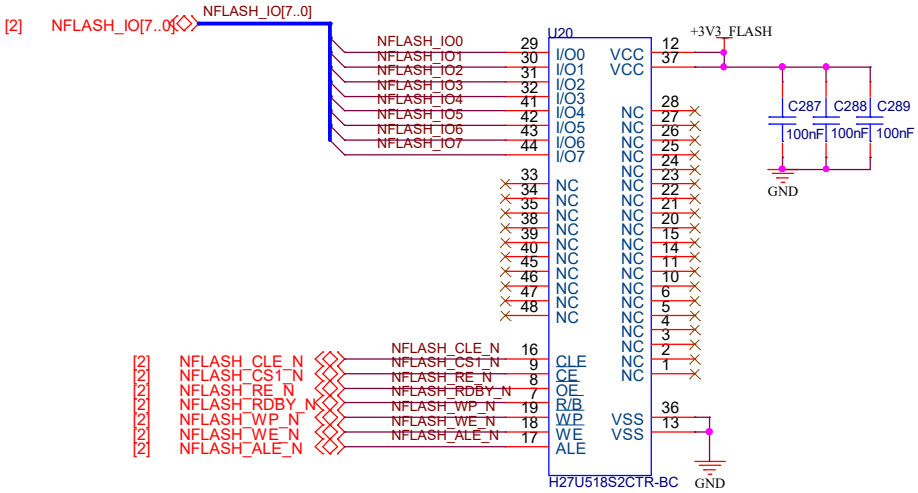
All other options are reserved/not used.

<OrgName> DrayTek

Title: GRX350_GPIO

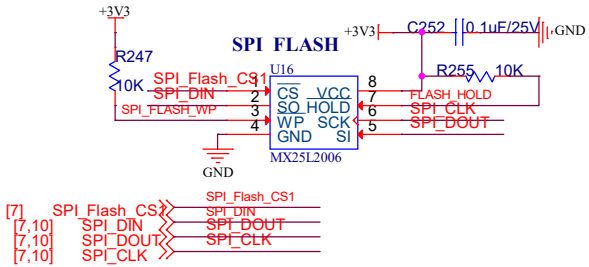
Size: Custom | Document Number: V2135AX | Rev: 6C

Date: Friday, January 28, 2022 | Sheet 7 of 26



Qualified Nand Flash List

Vendor	Model
Hynix	H27uag8, 8k
Hynix	H27u512, 512
Hynix	H27u4g8f2dtr, 2k
Hynix	H27u1g8f2btf, 2k
Samsung	K9F1208, 512
Samsung	K9f1g08u0d, 2k
Samsung	K9g4g08u0b, 2k
Samsung	K9G8G08U0C, 8k
Spansion	S34ml01g100, 2k
Mircon	29f64g08cbaba, 8k
Mircon	29f32g08cbaca, 4k
Infineon	Hyf33ds51280, 512
Toshiba	Th58BVG3S0HTA00, 4k

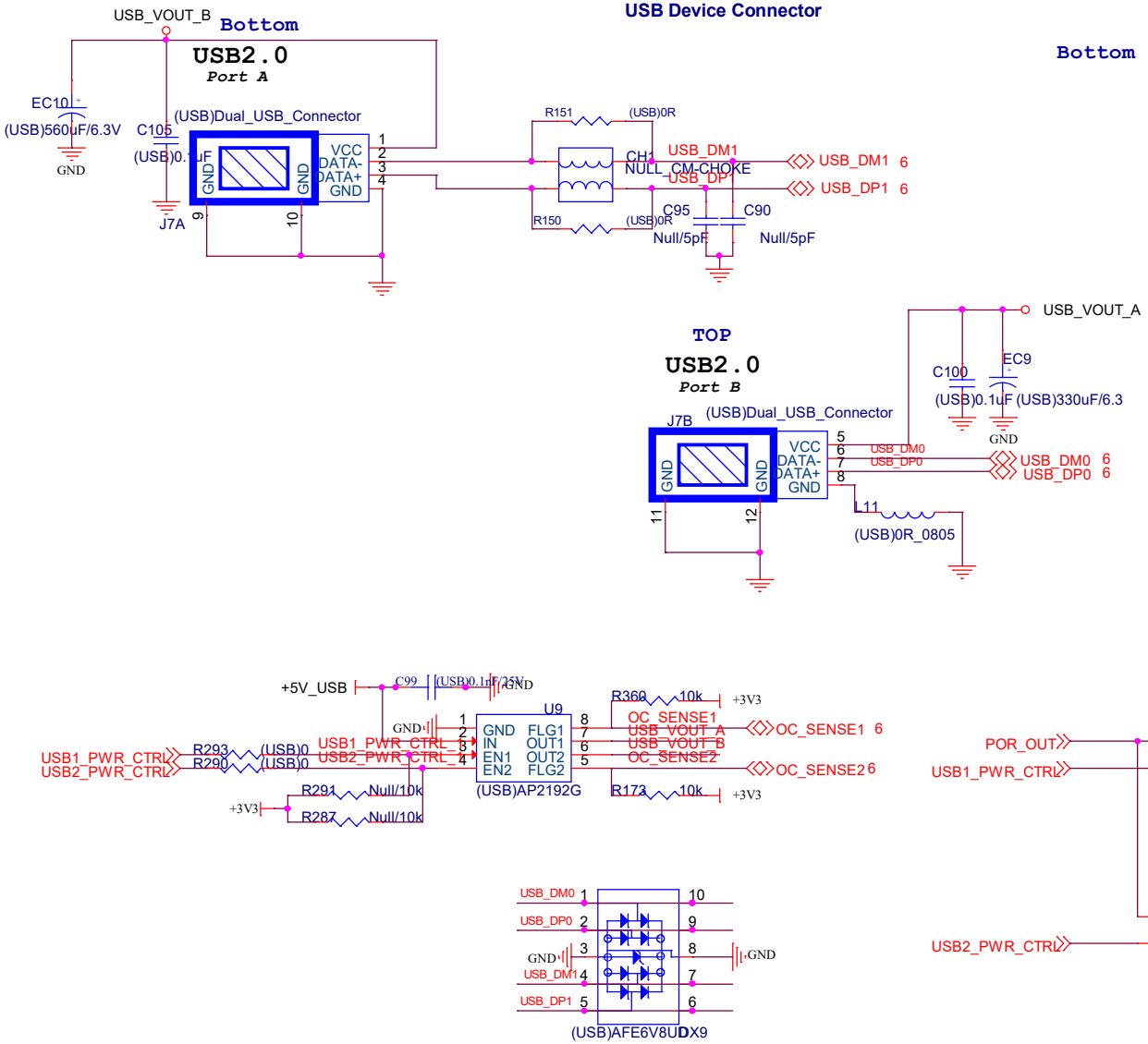


<OrgName>	DrayTek		
Title	NAND_FLASH		
Size: B	Document Number: V2135AX		Rev: 6C
Date: Friday, January 28, 2022	Sheet 8 of 26		

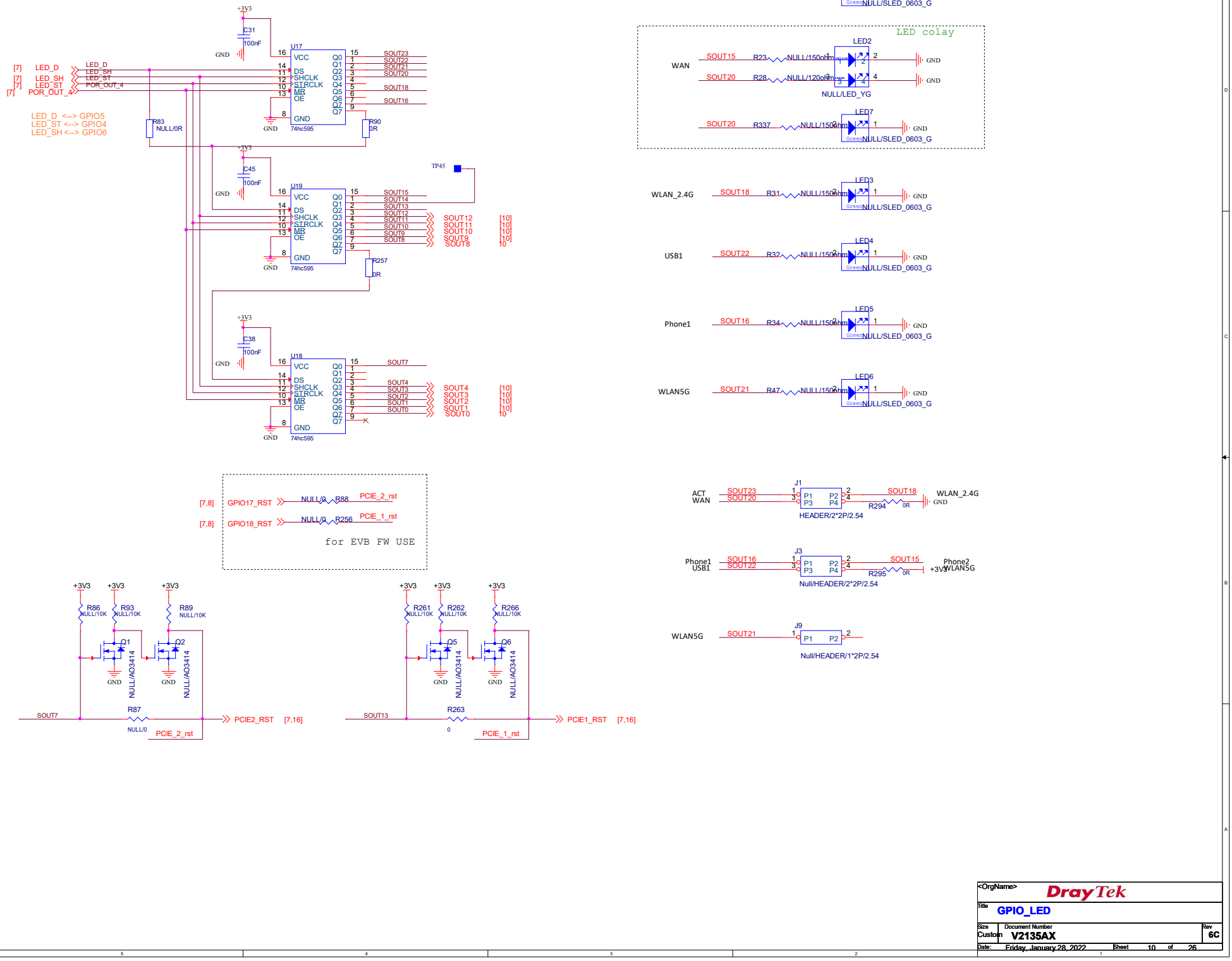
!!Note:
The PCB layout of the differential signal DP and DM should have 90 ohm differential impedance, and keep the trace length below 1 inch if possible.

USB Device Connector

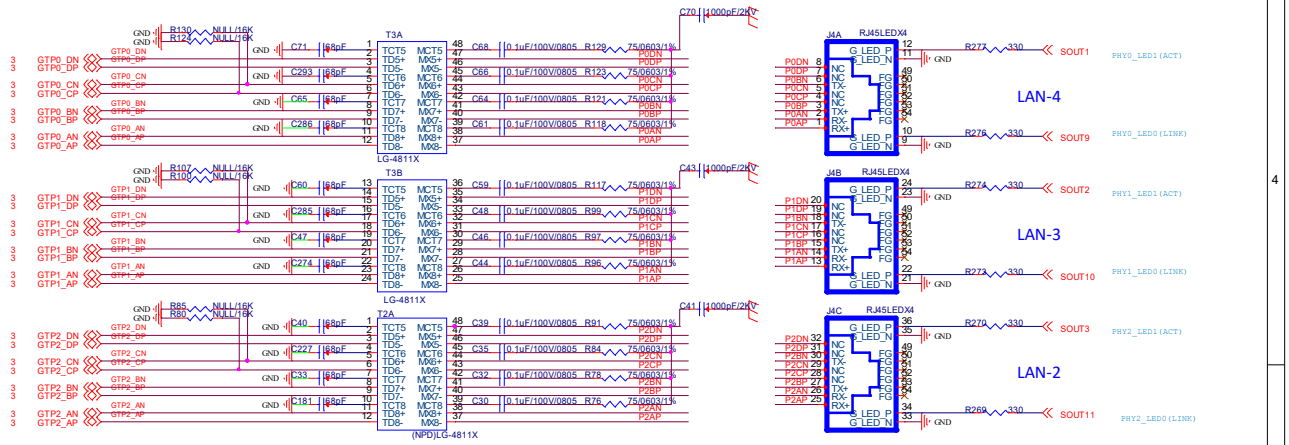
TOP	B
Bottom	A



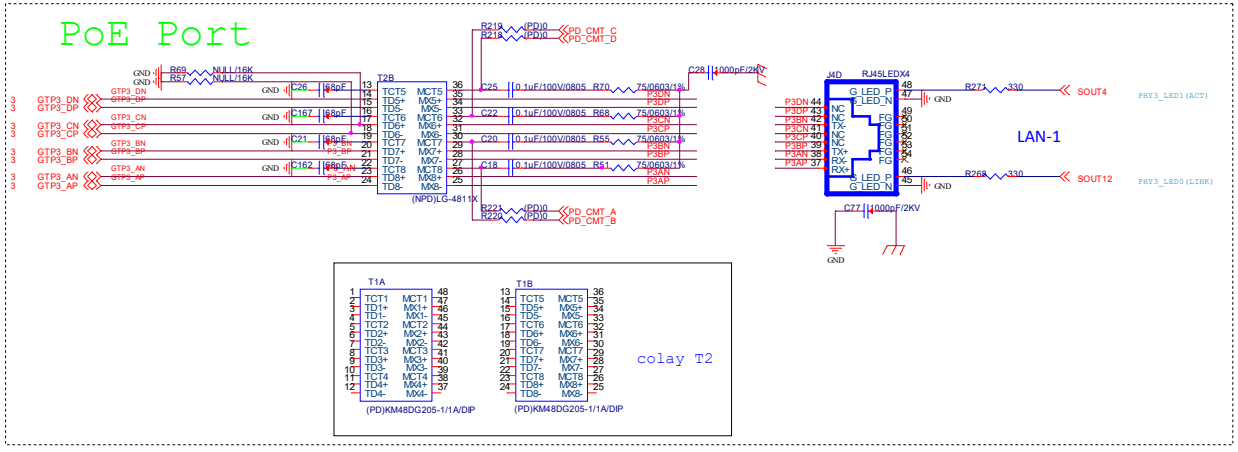
<OrgName>	DrayTek		
Title	USB_Port		
Size B	Document Number V2135AX		Rev 6C
Date: Friday, February 11, 2022	Sheet 08 of 26		

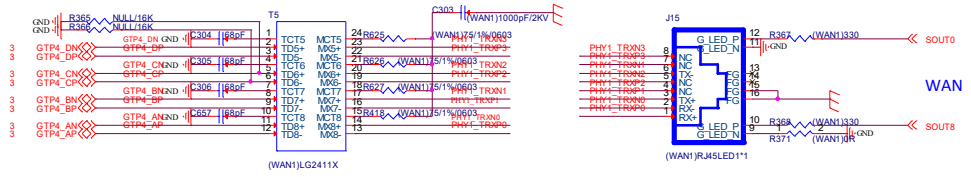


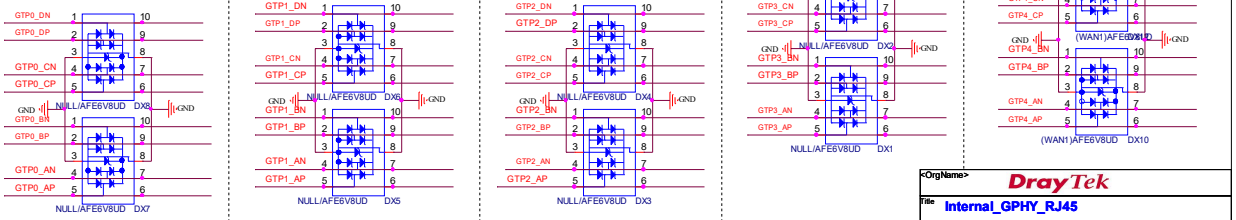
<OrgName>	DrayTek
Title	GPIO_LED
Size	Custom
Document Number	V2135AX
Rev	6C
Date:	Friday, January 28, 2022
Sheet	10 of 26



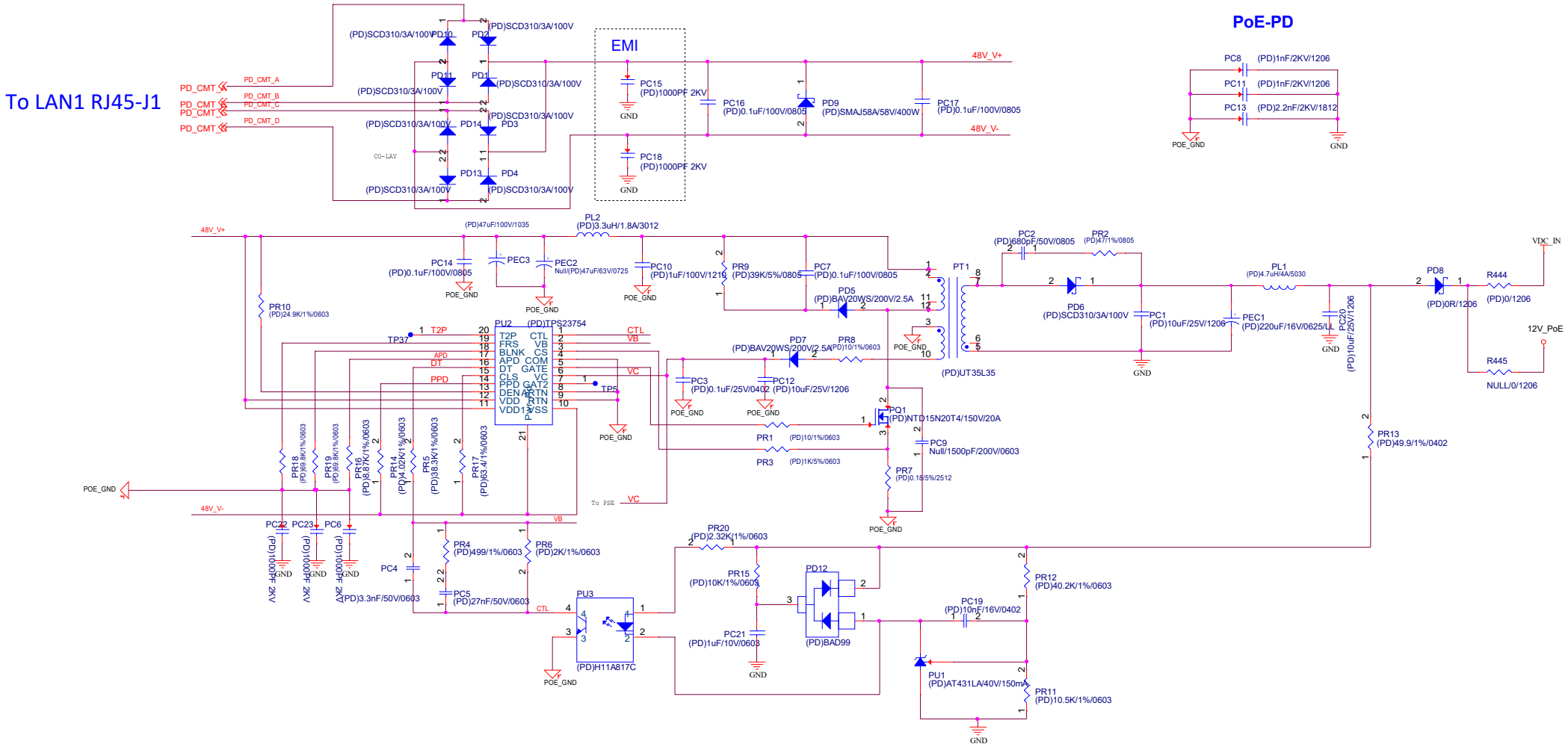
PoE Port



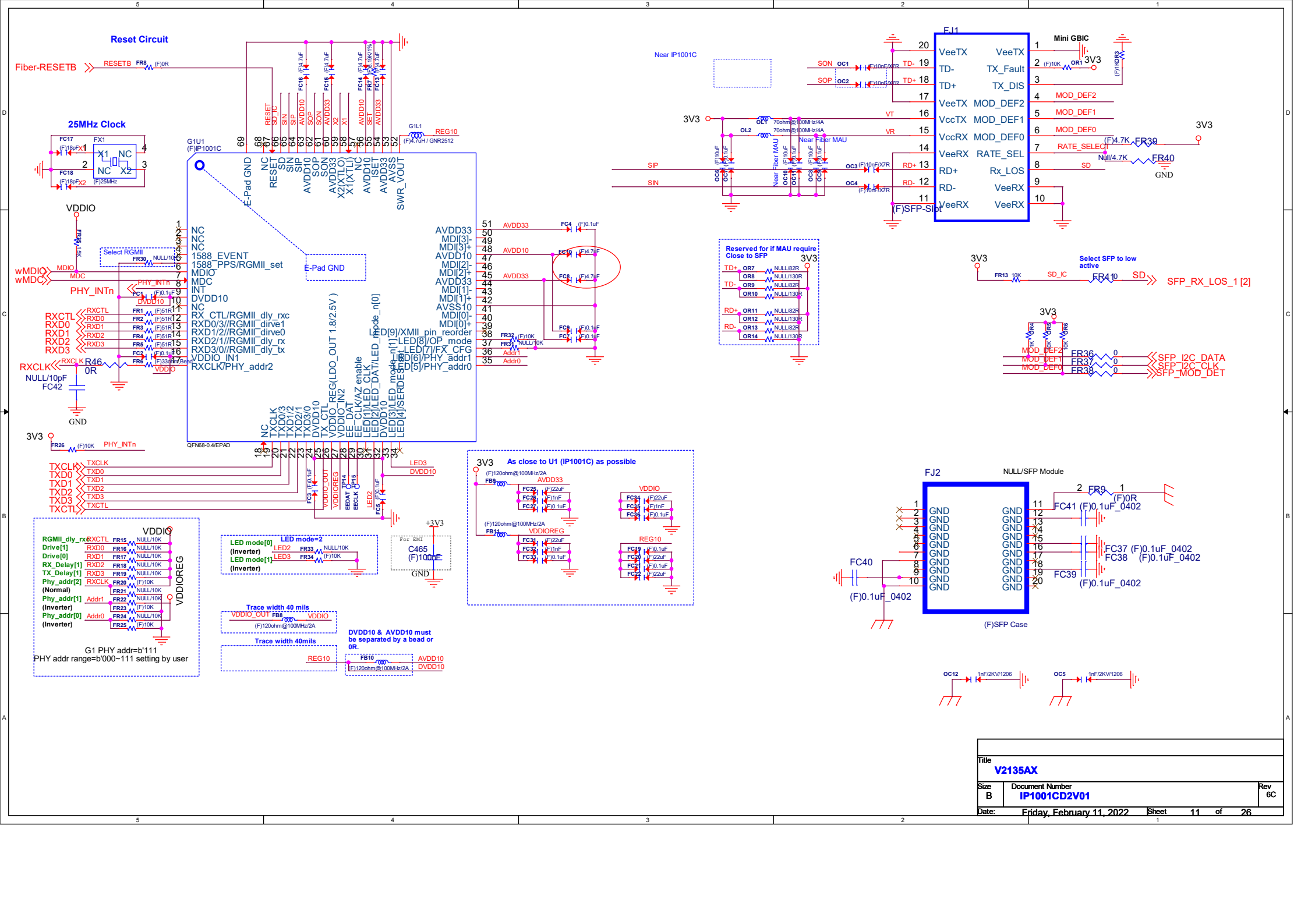




<OrgName>	DrayTek		
Title	Internal_GPHY_RJ45		
Size: Custom	Document Number: V2135AX		Rev: 6C
Date: Friday, January 28, 2022	Sheet 10 of 26		



<OrgName>	DrayTek		
Title	POE PD		
Size	Document Number		Rev
Custom	V2135AX		6C
Date:	Friday, January 28, 2022	Sheet 11 of 26	


Reset Circuit
Fiber-RESETB
RESETB
25MHz Clock
G1U1
(F)IP1001C
E-Pad GND
QFN68-0.4/EPAD
Select RGMII
wMDIO
wMDC
PHY_INTn
RXCTL
RXD0
RXD1
RXD2
RXD3
RXCLK
TXCLK
TXD0
TXD1
TXD2
TXD3
TXCTL
VDDIO
VDDIOREG
G1 PHY addr=b'111
PHY addr range=b'000~111 setting by user
LED mode[0]
(Inverter)
LED mode[1]
(Inverter)
LED mode=2
Trace width 40 mils
Trace width 40mils
DVDD10 & AVDD10 must be separated by a bead or 0R.
Near IP1001C
Near Fiber MAU
Reserved for if MAU require Close to SFP
As close to U1 (IP1001C) as possible
FJ1
Mini GBIC
(F)SFP-Slot
Select SFP to low active
SFP_RX_LOS_1 [2]
SFP_I2C_DATA
SFP_I2C_CLK
SFP_MOD_DET
FJ2
NULL/SFP Module
(F)SFP Case
Title
V2135AX
Size
B
Document Number
IP1001CD2V01
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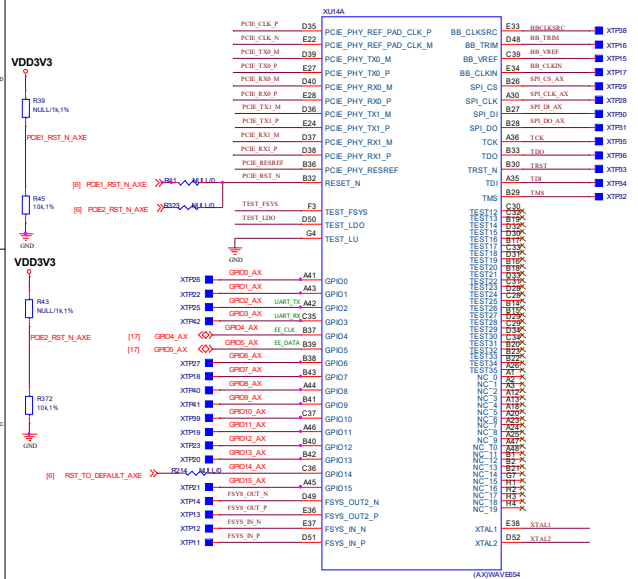
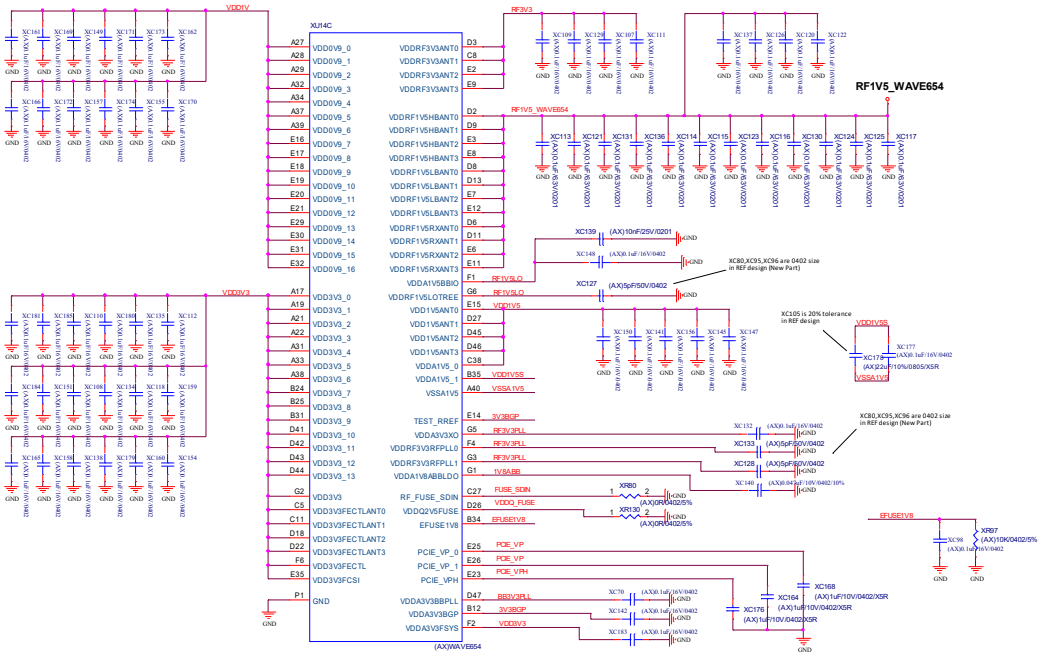
26

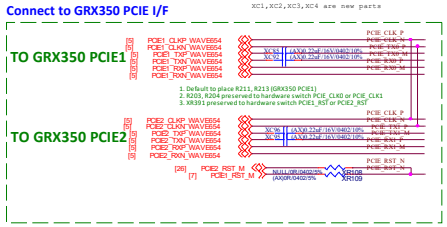
WAVE654 PCIE / GPIO / SPI

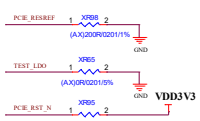


WAVE654 POWER

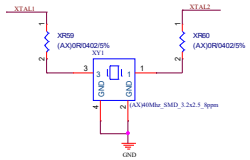


Connect to GRX350 PCIE I/F

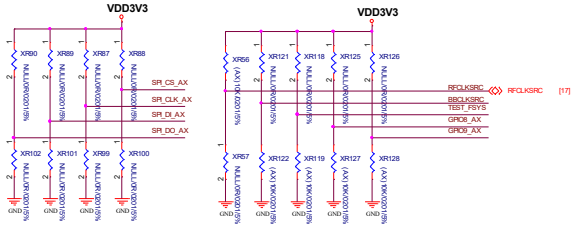




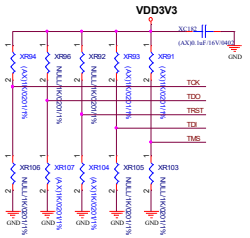
XTAL 40MHz



Boot Strapping



WAV654 Init Strapping



Reserved for GPB654 Refernce Design

SY98004 : Vout=0.6(1+120K/165K)=1.036V
WAV654 Range : 0.72V ~ 1.05V

Table 32 JTAG Signals

Ball No.	Name	Pin Type	Buffer Type	Function
B30	TRST	I	PU	JTAG Reset Notes 1. Low active. 2. If the JTAG interface is not in use, this pin must be connected to V_{SS}.
	EJ_TRST	I	PU	EJTAG Reset
A35	TDI	I	PU	Test Data Input
	EJ_TDI	I		EJTAG Test Data Input
B33	TDO	O	PD	Test Data Output Note: pull down is needed for normal operation.
	EJ_TDO	O		EJTAG Test Data Output
B29	TMS	I	–	Test Mode Select
	EJ_TMS	I		EJTAG Mode Select

Reserved for GPB654 Refernce Design

Reserved for GPB654 Refernce Design

UART CONN

OrgName	DrayTek
Title	WAVE654_POWER_PCIE
Size	D
Document Number	V2135AX
Rev	6C
Date	Friday, January 28, 2022
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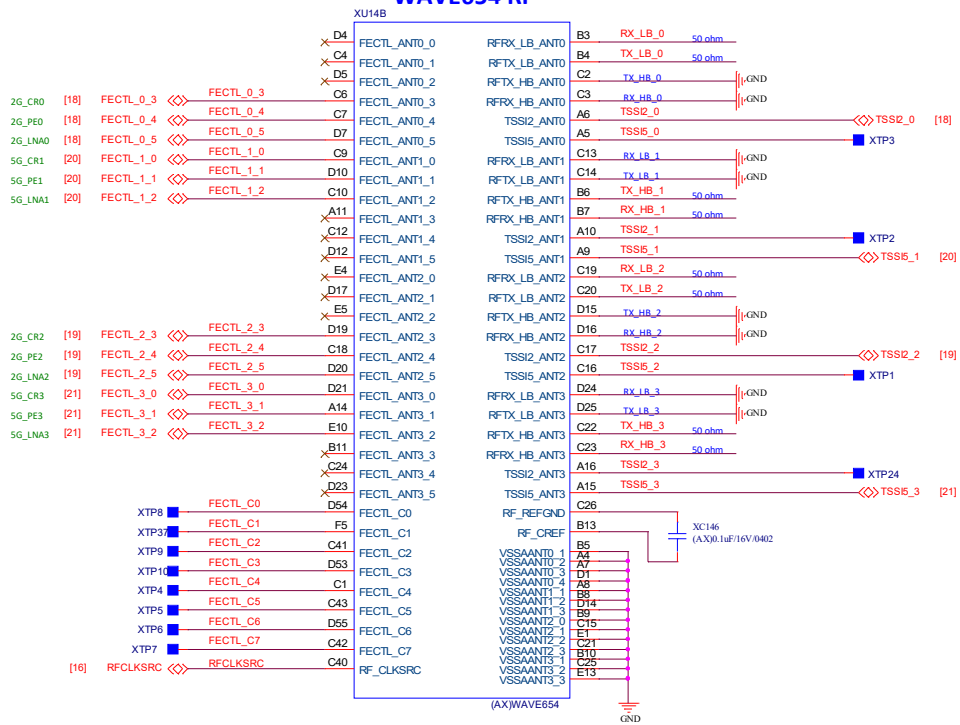
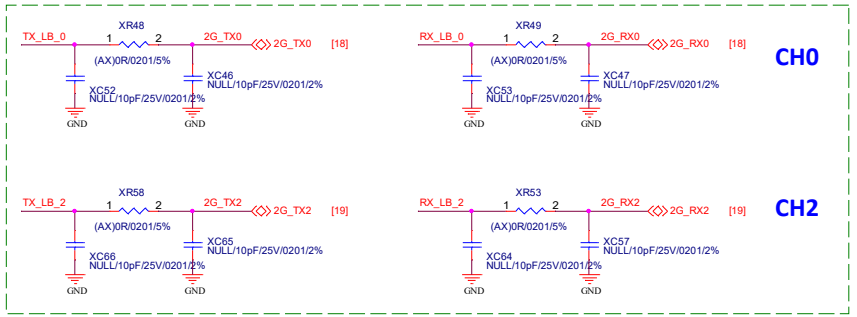
WAVE654 RF



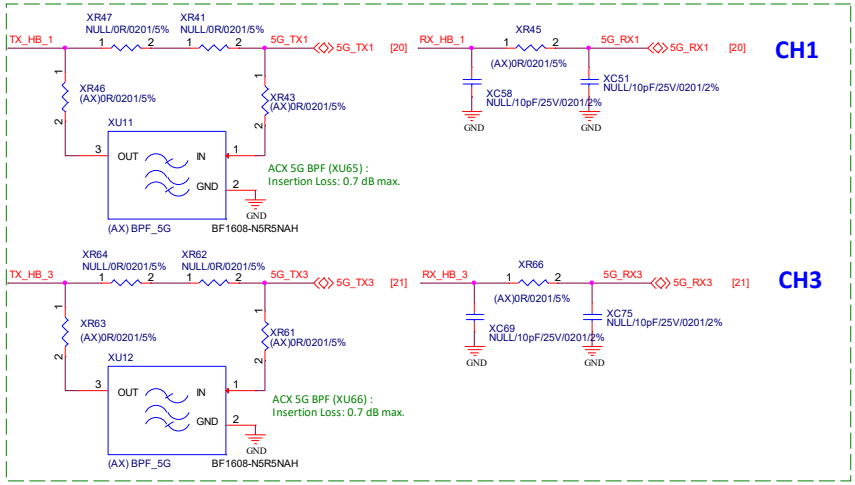
Reserved for GPB654 Refernce Design

PCIE FINGER

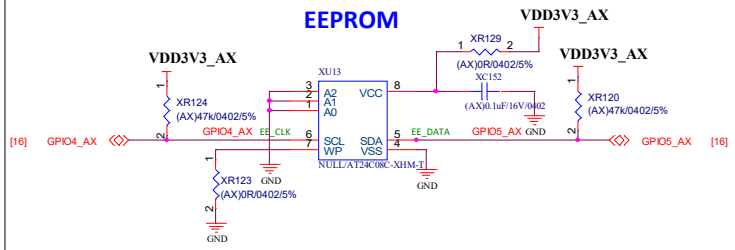
2.4G Front-End



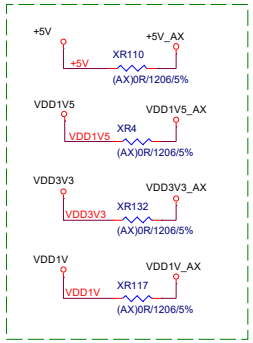
5G Front-End



EEPROM



Connect to main board DCDC



SY98004 : Vout=0.6(1+120K/165K)=1.036V
WAV654 Range : 0.72V ~ 1.05V

<OrgName>	DrayTek	
Title	WAVE654_RF	
Size: Custom	Document Number: V2135AX	Rev: 6C
Date: Friday, January 28, 2022	Sheet 17 of 26	

SKY85331-11 :
Output power: +22 dBm @ 1.8% EVM, HT40, MCS9, 5 V
Output power: +26 dBm @ 3% EVM, HT40, MCS7, 5 V

2.4G FEM CH0

XR90 is new part wihtout Draytek part number

+5V

XR21 (AX)6.8nH/0.6A/0805/5% PA_2G0

XC15 (AX)4.7uF/16V/0603/10%

XC134 is 6.3V voltage in REF design

Layout Notice :
- Each Vcc pin needs to be individually decoupled.
- VCC0, VCC1, VCC2, and VCC3 should NOT be shorted together at the device pins.

Layout Notice :
- Decoupling CAP should be placed before RES

[17] FECTL_0_4 XR28 (AX)0R/0402/5% 2G_PE0 XC37 (AX)1pF/50V/0.05pF/0402

[17] FECTL_0_5 XR22 (AX)0R/0402/5% 2G_LNA0 XC24 (AX)1pF/50V/0.05pF/0402

[17] FECTL_0_3 XR18 (AX)0R/0402/5% 2G_CR0 XC14 (AX)1pF/50V/0.05pF/0402

XC38 (AX)0.1uF/16V/0402

XEU2 SKY85331-11

10	VDD	ANT	17
20	VCC3		
22	VCC2	C1	19
23	VCC1	C0	16
24	VCC0		
BPF_2A0 50 ohm	15 RX_OUT	TX_IN	2
BPF_2B0 50 ohm	13 LNA_IN	LNA_OUT	12
2G_PE0	4 PA_EN	GND1 GND3 GND7 GND9 GND11 GND14 GND18 GND21 PAD	1 3 7 9 11 14 18 21 25
	6 DET		
	5 NU5		
	8 NU8		

(AX)SKY85331-11

XC20 (AX)0.1uF/16V/0402 XC21 (AX)0.1uF/16V/0402 XC22 (AX)0.1uF/16V/0402 XC19 (AX)0.1uF/16V/0402

XC23 NULL/10pF/25V/0201/2% XC16 NULL/10pF/25V/0201/2% XC17 (AX)10pF/25V/0201/2% 50 ohm 2G_ANT0

2G_CR0 2G_LNA0

Layout Notice :
- Control Pin C0, C1 should be shielded by GND with more Vias.

XC29 (AX)10pF/25V/0201/2% 50 ohm 2G_TX0 [17]

XC30 NULL/10pF/25V/0201/2% XL6 NULL/0R/0201/5% XL7 NULL/0R/0201/5% XC35 NULL/10pF/25V/0201/2% XC36 NULL/10pF/25V/0201/2%

Close to XEU2

[17] TSSI2_0 XR30 (AX)0R/0201/5% XR29 (AX)0R/0201/5% XR31 NULL/0R/0201/5% XC40 NULL/10pF/25V/0201/2%

XR98 is designed for RTC7647

BPF (2400-2500MHz)

XU7 NULL/(AX)BPF_2G BF2012-L2R4NAR

XC39 (AX)10pF/25V/0201/2% 2G_RX0 [17]

XR33 0R/0201/5%

ACX 2G BPF (XU30) :
Insertion Loss: 0.9 dB max. (25C)
Insertion Loss: 1.1 dB max. (-40C~85C)

ACX 2G BPF (XU31) :
Insertion Loss: 0.9 dB max. (25C)
Insertion Loss: 1.1 dB max. (-40C~85C)

SAW (For LTE)

Close to XEU2

Co-Layout

BPF_2A0 XR134 NULL/0R/0201/5% XR135 NULL/0R/0201/5% BPF_2B0

XR136 (AX_LTE)1.5nH XR137 (AX_LTE)0R/0201/5%

XL23 NULL/0.5pF/50V/0201 XL24 (AX)0.5pF/50V/0201

XU20 In GND GND Out

XL25 (AX_LTE)5.1nH

XL26 NULL/10nH/0.25A/0201/3% (AX_LTE)SAW_SF14112442A01T

2G_CH0_5G_CH1_DIPLEXER

Co-Layout

2G_ANT0 XR20 (AX)0R/0201/5% XR19 NULL/1.5nH XL4 NULL/0.5pF/50V/0201

XR12 (AX)0R/0201/5% XR13 NULL/0R/0201/5% XL2 (AX)0.5pF/50V/0201

XU3 In GND GND Out

XL3 NULL/5.1nH

XL5 NULL/10nH/0.25A/0201/3% NULL/SAW_SF14112442A01T

[20] 5G_ANT1_DI 5G_ANT1_DI 50 ohm XR9 (AX)0R/0201/5% 50 ohm XR3 (AX)0R/0201/5%

XU1

HI_FREQ	1	
LO_FREQ	3	
COMMON	5	
GND2 GND4 GND6	2 4 6	

(AX)DIPLEXER DP1608-A2455BKH0

XR1 (AX)4.7pF/0201 50 ohm

Close to SMA3

XL1 (AX)0R/0201/5% 2G_5G_A0_IPX XJ1 (AX)IPEX_2G_FEM0

XC2 (AX)0.4pF/50V/0201 XC1 NULL/2.2pF/50V/0201

Walsin SAW Filter (XU71) :
Insertion Loss: 2.2 dB typ. 2.9 dB max. @ 2400 ~ 2484 MHz (-30 ~ +85C)
Pin : 28 dBm @ 2400 ~ 2484 MHz

ACX 2G/5G Diplexer (XU7) :
2G Insertion Loss: 0.6 dB max.
5G Insertion Loss: 0.78 dB max.
2G Isolation: 38 dB min. @ 2400 ~ 2500 MHz
5G Isolation: 38 dB min. @ 4900 ~ 5950 MHz

<OrgName>	DrayTek		
Title	RF_2.4G_FEM_CH0		
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SKY85331-11 :
Output power: +22 dBm @ 1.8% EVM, HT40, MCS9, 5 V
Output power: +26 dBm @ 3% EVM, HT40, MCS7, 5 V

2.4G FEM CH2

XR77 is new part wihtout Draytek part number

+5V
XR54 (AX)6.8nH/0.6A/0805/5%
PA_2G2
XC59 (AX)4.7uF/16V/0603/10%
XC121 is 6.3V voltage in REF design

Layout Notice :
- Decoupling CAP should be placed before RES

[17] FECTL_2_4 — XR55 (AX)0R/0402/5% — 2G_PE2 — XC63 (AX)1pF/50V/0.05pF/0402
[17] FECTL_2_5 — XR39 (AX)0R/0402/5% — 2G_LNA2 — XC41 (AX)1pF/50V/0.05pF/0402
[17] FECTL_2_3 — XR44 (AX)0R/0402/5% — 2G_CR2 — XC48 (AX)1pF/50V/0.05pF/0402

Layout Notice :
- Each Vcc pin needs to be individually decoupled.
- VCC0, VCC1, VCC2, and VCC3 should NOT be shorted together at the device pins.

XC50 (AX)0.1uF/16V/0402 — PA_2G2
XC49 (AX)0.1uF/16V/0402
XC55 (AX)0.1uF/16V/0402
XC54 (AX)0.1uF/16V/0402
XC60 (AX)0.1uF/16V/0402

XEU3 SKY85331-11
10 VDD
20 VCC3
22 VCC2
23 VCC1
24 VCC0
15 RX_OUT — BPF_2A2 50 ohm
13 LNA_IN — BPF_2B2 50 ohm
4 PA_EN — 2G_PE2
6 DET
5 NU5
8 NU8
17 ANT — XC44 NULL/10pF/25V/0201/2% — XC42 NULL/10pF/25V/0201/2% — XC43 (AX)10pF/25V/0201/2% — 50 ohm — 2G_ANT2
19 C1 — 2G_CR2
16 C0 — 2G_LNA2
Layout Notice :
- Control Pin C0, C1 should be shielded by GND with more Vias.
2 TX_IN — XC61 (AX)10pF/25V/0201/2% — 50 ohm — 2G_TX2 — 2G_TX2 [17]
12 LNA_OUT — 50 ohm
GND1 GND3 GND7 GND9 GND11 GND14 GND18 GND21 PAD
(AX)SKY85331-11

XC62 NULL/10pF/25V/0201/2%
XC67 NULL/10pF/25V/0201/2%
XL12 NULL/0R/6201/5%
XL13 NULL/0R/0201/5%
XC68 NULL/10pF/25V/0201/2%

Close to XEU1
[17] TSSI2_2 — XR52 (AX)0R/0201/5% — XR50 (AX)0R/0201/5%
XR51 NULL/0R/0201/5%
XC56 NULL/10pF/25V/0201/2%
XR85 is designed for RTC7647

Close to XEU3
Co-Layout
BPF_2A2 — XR40 NULL/0R/0201/5% — XR139 (AX_LTE)1.5nH — XL27 NULL/0.5pF/50V/0201
XR138 NULL/0R/0201/5% — XR140 (AX_LTE)0R/0201/5% — XL28 (AX)0.5pF/50V/0201
XU21 In GND GND Out — XL29 (AX_LTE)5.1nH
XL30 NULL/10nH/0.25A/0201/3% — (AX_LTE)SAW_SF14112442A01T — BPF_2B2

ACX 2G BPF (XU33) :
Insertion Loss: 0.9 dB max. (25C)
Insertion Loss: 1.1 dB max. (-40C~85C)

BPF (2400-2500MHz)

XC45 (AX)10pF/25V/0201/2%
XU10 IN GND2 GND4 OUT
NULL/(AX)BPF_2G BF2012-L2R4NAR
2G_RX2 — 2G_RX2 [17]
XR42 0R/0201/5%

ACX 2G BPF (XU32) :
Insertion Loss: 0.9 dB max. (25C)
Insertion Loss: 1.1 dB max. (-40C~85C)

SAW (For LTE)

Co-Layout
2G_ANT2 — XR37 (AX)0R/0201/5% — XR38 NULL/1.5nH — XL11 NULL/0.5pF/50V/0201
XR36 (AX)0R/0201/5% — XR35 NULL/0R/0201/5% — XL10 (AX)0.5pF/50V/0201
[21] 5G_ANT3_DI — 5G_ANT3_DI — 50 ohm — XR34 (AX)0R/0201/5% — 50 ohm — XR68 (AX)0R/0201/5%
XU8 In GND GND Out — XL8 NULL/5.1nH — XL9 NULL/10nH/0.25A/0201/3% — NULL/SAW_SF14112442A01T

2G_CH2_5G_CH3_DIPLEXER

XU15 HI_FREQ LO_FREQ COMMON GND2 GND4 GND6
(AX)DIPLEXER DP1608-A2455BKH0
XR71 (AX)4.7pF/0201 — 50 ohm

Close to XJ9
XL14 (AX)0R/0201/5% — 2G_5G_A2_IPX
XC79 (AX)0.4pF/50V/0201
XC86 NULL/2.2pF/50V/0201
XJ2 — (AX)IPEX_ANT2_XJ9

To XJ10

ACX 2G/5G Diplexer (XU7) :
2G Insertion Loss: 0.6 dB max.
5G Insertion Loss: 0.78 dB max.
2G Isolation: 38 dB min. @ 2400 ~ 2500 MHz
5G Isolation: 38 dB min. @ 4900 ~ 5950 MHz

Walsin SAW Filter (XU73) :
Insertion Loss: 2.2 dB typ. 2.9 dB max. @ 2400 ~ 2484 MHz (-30 ~ +85C)
Pin : 28 dBm @ 2400 ~ 2484 MHz

<OrgName>	DrayTek		
Title	RF_2.4G_FEM_CH2		
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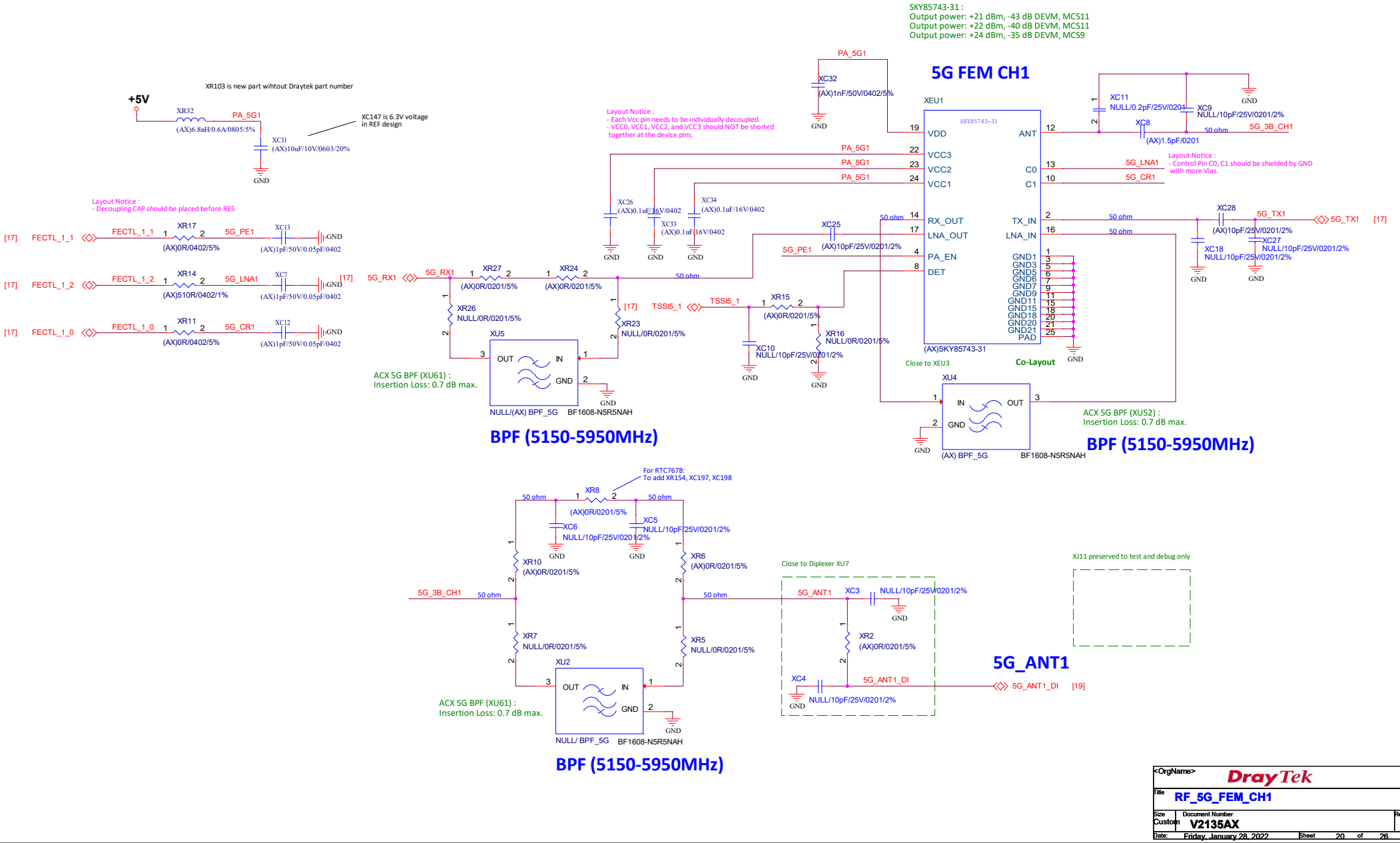
SKY85743-31 :
Output power: +21 dBm, -43 dB DEVM, MCS11
Output power: +22 dBm, -40 dB DEVM, MCS11
Output power: +24 dBm, -35 dB DEVM, MCS9
5G FEM CH1
XR103 is new part wihtout Draytek part number
+5V
XR32
(AX)6.8nH/0.6A/0805/5%
PA_5G1
XC31
(AX)10uF/10V/0603/20%
XC147 is 6.3V voltage in REF design
GND
Layout Notice :
- Decoupling CAP should be placed before RES
[17] FECTL_1_1
FECTL_1_1
XR17
(AX)0R/0402/5%
5G_PE1
XC13
(AX)1pF/50V/0.05pF/0402
[17] FECTL_1_2
FECTL_1_2
XR14
(AX)510R/0402/1%
5G_LNA1
XC7
(AX)1pF/50V/0.05pF/0402
[17]
[17] FECTL_1_0
FECTL_1_0
XR11
(AX)0R/0402/5%
5G_CR1
XC12
(AX)1pF/50V/0.05pF/0402
Layout Notice :
- Each Vcc pin needs to be individually decoupled.
- VCC0, VCC1, VCC2, and VCC3 should NOT be shorted together at the device pins.
PA_5G1
XC32
(AX)1nF/50V/0402/5%
XEU1
SKY85743-31
VDD
VCC3
VCC2
VCC1
RX_OUT
LNA_OUT
PA_EN
DET
ANT
C0
C1
TX_IN
LNA_IN
GND1
GND3
GND5
GND6
GND7
GND9
GND11
GND15
GND18
GND20
GND21
PAD
(AX)SKY85743-31
XC26
(AX)0.1uF/16V/0402
XC33
(AX)0.1uF/16V/0402
XC34
(AX)0.1uF/16V/0402
XC25
(AX)10pF/25V/0201/2%
XC11
NULL/0.2pF/25V/0201
XC9
NULL/10pF/25V/0201/2%
XC8
(AX)1.5pF/0201
50 ohm
5G_3B_CH1
5G_LNA1
5G_CR1
Layout Notice :
- Control Pin C0, C1 should be shielded by GND with more Vias.
XC28
(AX)10pF/25V/0201/2%
XC27
NULL/10pF/25V/0201/2%
XC18
NULL/10pF/25V/0201/2%
5G_TX1
[17]
5G_RX1
XR27
(AX)0R/0201/5%
XR24
(AX)0R/0201/5%
XR26
NULL/0R/0201/5%
XR23
NULL/0R/0201/5%
XU5
OUT
IN
GND
ACX 5G BPF (XU61) :
Insertion Loss: 0.7 dB max.
NULL/(AX) BPF_5G
BF1608-N5R5NAH
BPF (5150-5950MHz)
TSSI5_1
XR15
(AX)0R/0201/5%
XR16
NULL/0R/0201/5%
XC10
NULL/10pF/25V/0201/2%
Close to XEU3
Co-Layout
XU4
ACX 5G BPF (XU52) :
Insertion Loss: 0.7 dB max.
(AX) BPF_5G
BF1608-N5R5NAH
BPF (5150-5950MHz)
For RTC7678:
To add XR154, XC197, XC198
XR8
(AX)0R/0201/5%
XC6
NULL/10pF/25V/0201/2%
XC5
NULL/10pF/25V/0201/2%
XR10
(AX)0R/0201/5%
XR6
(AX)0R/0201/5%
XR7
NULL/0R/0201/5%
XR5
NULL/0R/0201/5%
XU2
ACX 5G BPF (XU61) :
Insertion Loss: 0.7 dB max.
NULL/ BPF_5G
BF1608-N5R5NAH
BPF (5150-5950MHz)
Close to Diplexer XU7
5G_ANT1
XC3
NULL/10pF/25V/0201/2%
XR2
(AX)0R/0201/5%
XC4
NULL/10pF/25V/0201/2%
5G_ANT1_DI
[19]
XJ11 preserved to test and debug only
5G_ANT1
<OrgName>
DrayTek
Title
RF_5G_FEM_CH1
Size
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SKY85743-31 :
Output power: +21 dBm, -43 dB DEVM, MCS11
Output power: +22 dBm, -40 dB DEVM, MCS11
Output power: +24 dBm, -35 dB DEVM, MCS9

XR119 is new part wihtout Draytek part number

+5V
XR84
(AX)6.8nH/0.6A/0805/5%
PA_5G3
XC94
(AX)10uF/10V/0603/20%
GND
XC147 is 6.3V voltage in REF design

Layout Notice :
- Decoupling CAP should be placed before RES

[17] FECTL_3_1 FECTL_3_1 XR69 (AX)0R/0402/5% 5G_PE3 XC71 (AX)1pF/50V/0.05pF/0402 GND
[17] FECTL_3_2 FECTL_3_2 XR81 (AX)510R/0402/1% 5G_LNA3 XC97 (AX)1pF/50V/0.05pF/0402 [17]
[17] FECTL_3_0 FECTL_3_0 XR72 (AX)0R/0402/5% 5G_CR3 XC83 (AX)1pF/50V/0.05pF/0402 GND

5G FEM CH3

PA_5G3 XC91 (AX)1nF/50V/0402/5% GND

Layout Notice :
- Each Vcc pin needs to be individually decoupled.
- VCC0, VCC1, VCC2, and VCC3 should NOT be shorted together at the device pins.

XEU4 SKY85743-31
19 VDD
22 VCC3 PA_5G3
23 VCC2 PA_5G3
24 VCC1 PA_5G3
14 RX_OUT
17 LNA_OUT
4 PA_EN
8 DET
12 ANT
13 C0 5G_LNA3
10 C1 5G_CR3
2 TX_IN
16 LNA_IN
GND1 GND3 GND5 GND6 GND7 GND9 GND11 GND15 GND18 GND20 GND21 PAD
(AX)SKY85743-31

XC90 NULL/3nH/0201
XC88 NULL/10pF/25V/0201/2%
XC89 (AX)1.5pF/50V/0201
50 ohm 5G_3B_CH3

Layout Notice :
- Control Pin C0, C1 should be shielded by GND with more Vias.

XC77 (AX)0.1uF/16V/0402
XC84 (AX)0.1uF/16V/0402
XC78 (AX)0.1uF/16V/0402
XC93 (AX)10pF/25V/0201/2%
5G_PE3
50 ohm

5G_RX3 [17] XR85 (AX)0R/0201/5% XR82 (AX)0R/0201/5% XR86 NULL/0R/0201/5% XR83 NULL/0R/0201/5%
XU18 OUT IN GND
NULL/(AX) BPF_5G BF1608-N5R5NAH
ACX 5G BPF (XU63) :
Insertion Loss: 0.7 dB max.

TSSI5_3 [17] XR70 (AX)0R/0201/5% XR73 NULL/0R/0201/5% XC76 NULL/10pF/25V/0201/2%

Close to XEU4
Co-Layout

50 ohm TX_IN 50 ohm LNA_IN
XC73 (AX)10pF/25V/0201/2% 5G_TX3 5G_TX3 [17]
XC72 NULL/10pF/25V/0201/2% XC74 NULL/10pF/25V/0201/2%

XU17 IN OUT GND
(AX) BPF_5G BF1608-N5R5NAH
ACX 5G BPF (XU54) :
Insertion Loss: 0.7 dB max.

BPF (5150-5950MHz)

BPF (5150-5950MHz)

For RTC7678:
To add XR155, XC199, XC210

5G_3B_CH3 50 ohm XR77 (AX)0R/0201/5% 50 ohm
XC82 NULL/10pF/25V/0201/2% XC81 NULL/10pF/25V/0201/2%
XR79 (AX)0R/0201/5% XR76 (AX)0R/0201/5%
XR78 NULL/0R/0201/5% XR75 NULL/0R/0201/5%
XU16 OUT IN GND
NULL/ BPF_5G BF1608-N5R5NAH
ACX 5G BPF (XU63) :
Insertion Loss: 0.7 dB max.

Close to Diplexer XU6
5G_ANT3 XC87 NULL/10pF/25V/0201/2%
XR74 (AX)0R/0201/5%
XC80 NULL/10pF/25V/0201/2%
5G_ANT3_DI 5G_ANT3_DI [19]

XJ12 preserved to test and debug only

5G_ANT3

<OrgName> DrayTek

Title RF_5G_FEM_CH3

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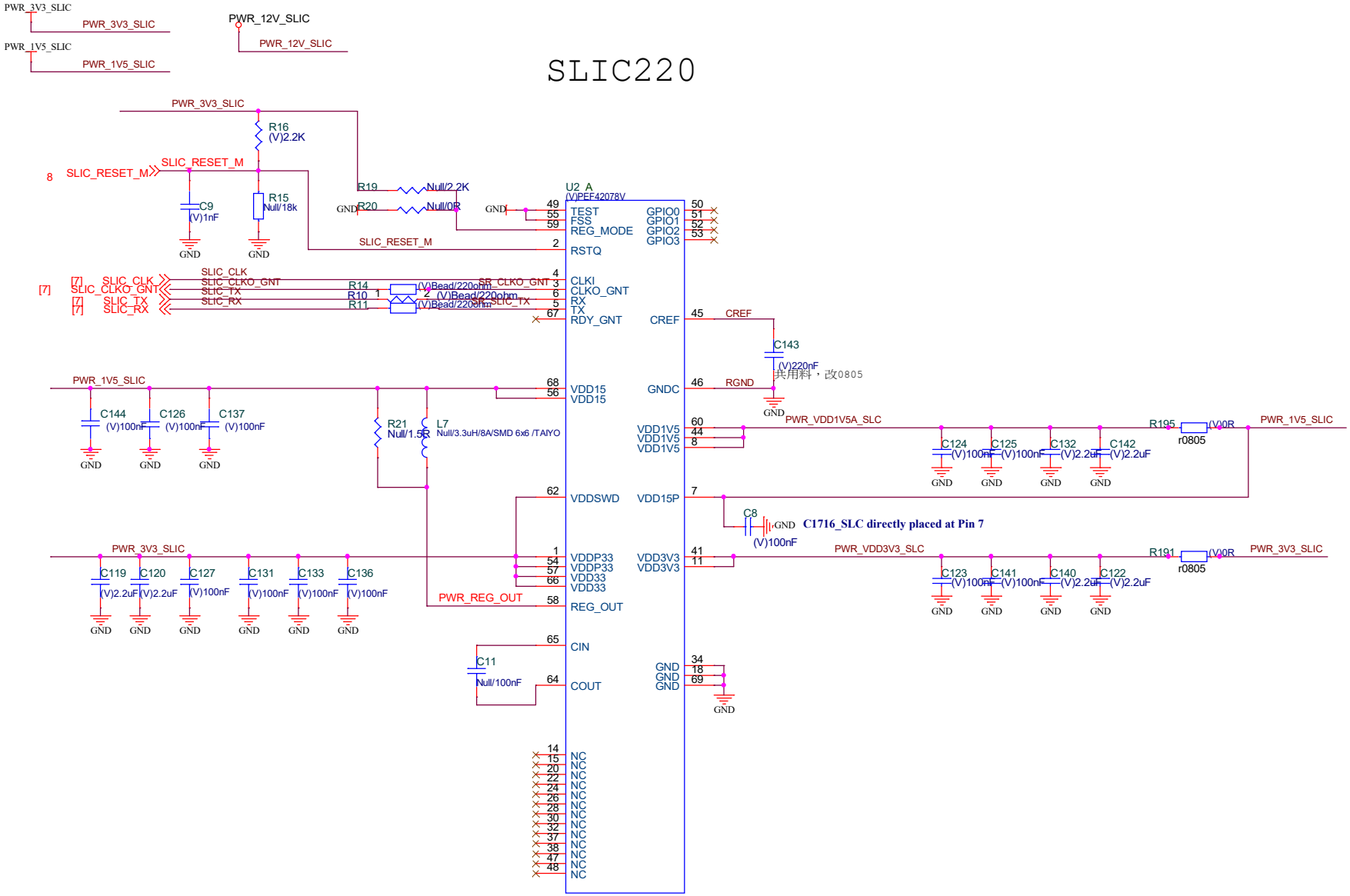

<OrgName>	DrayTek		
Title	XWAYSLIC220_DIGITAL		
Size: Custom	Document Number: V2135AX		Rev: 6C
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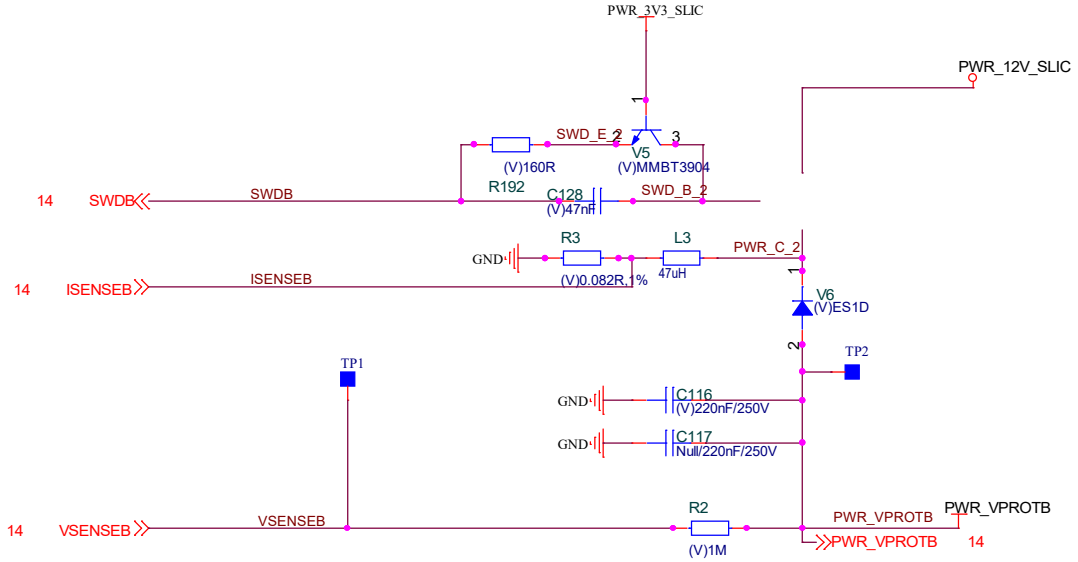
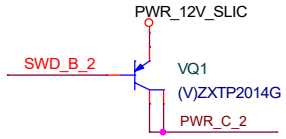
DCDC Type
Dedicated DCDC = T0.2
Combined DCDC = T1.1

Move radiating parts (like switching regulators and coils, voice SLIC/coils,) far away from DSL-AFE. A distance (at least 5cm) between the reiating part and the DSL must be maintain.





Component	Dedicated DCDC	Combined DCDC
R77	0.082R	0.068R
L9	47uH/1.8A	33uH/2.1A
C204	mount	X
C1806	X	mount

<OrgName> DrayTek

Title: U2_PNP_DCDC_T02_V11

Size: Custom | Document Number: V2135AX | Rev: 6C

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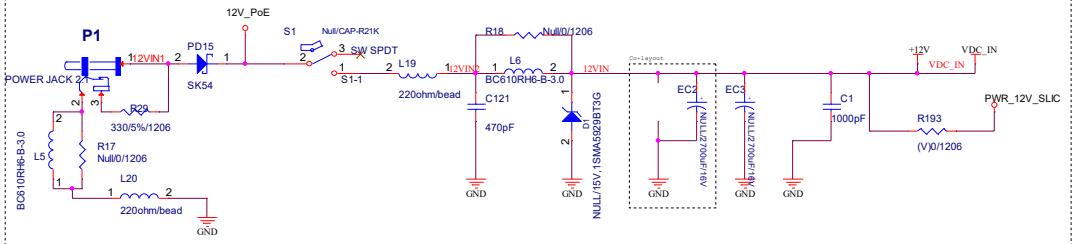
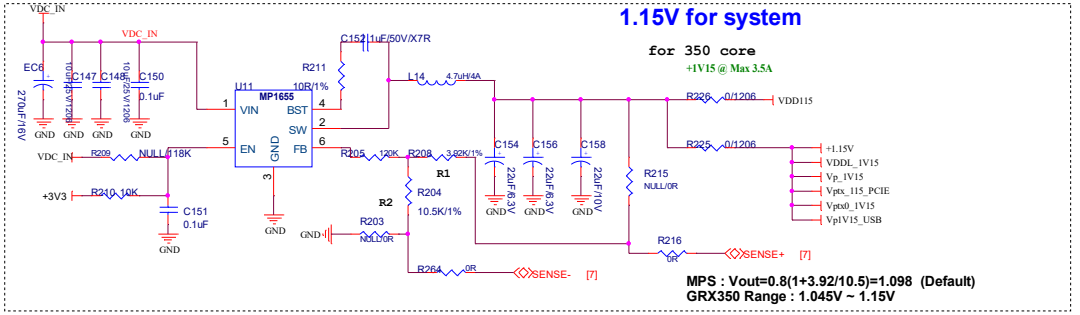
12V DC Power Input



1.15V for system

for 350 core

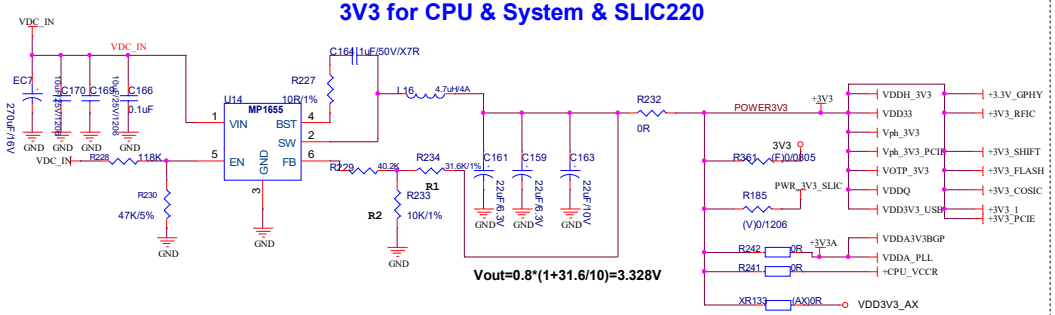
+1V15 @ Max 3.5A



MPS : Vout=0.8(1+3.92/10.5)=1.098 (Default)

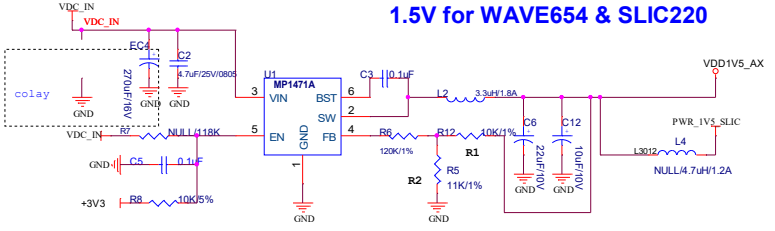
GRX350 Range : 1.045V ~ 1.15V

3V3 for CPU & System & SLIC220



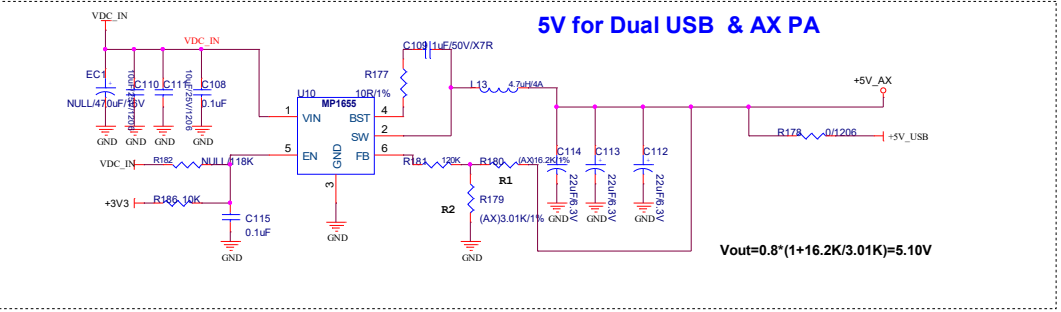
Vout=0.8*(1+31.6/10)=3.328V

1.5V for WAVE654 & SLIC220



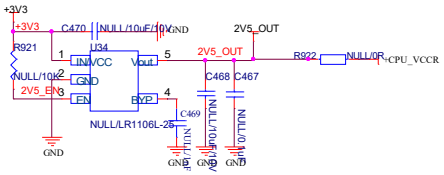
Vout=0.8*(1+10/11)=1.527V

5V for Dual USB & AX PA

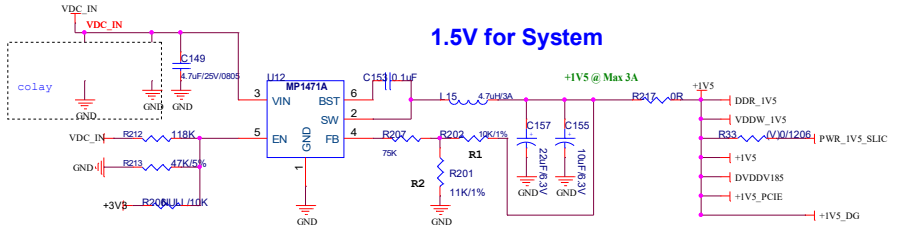


Vout=0.8*(1+16.2K/3.01K)=5.10V

2V5 for PHY



1.5V for System



Vout=0.8(1+10/11)=1.527V

<OrgName>	DrayTek		
Title	POWER		
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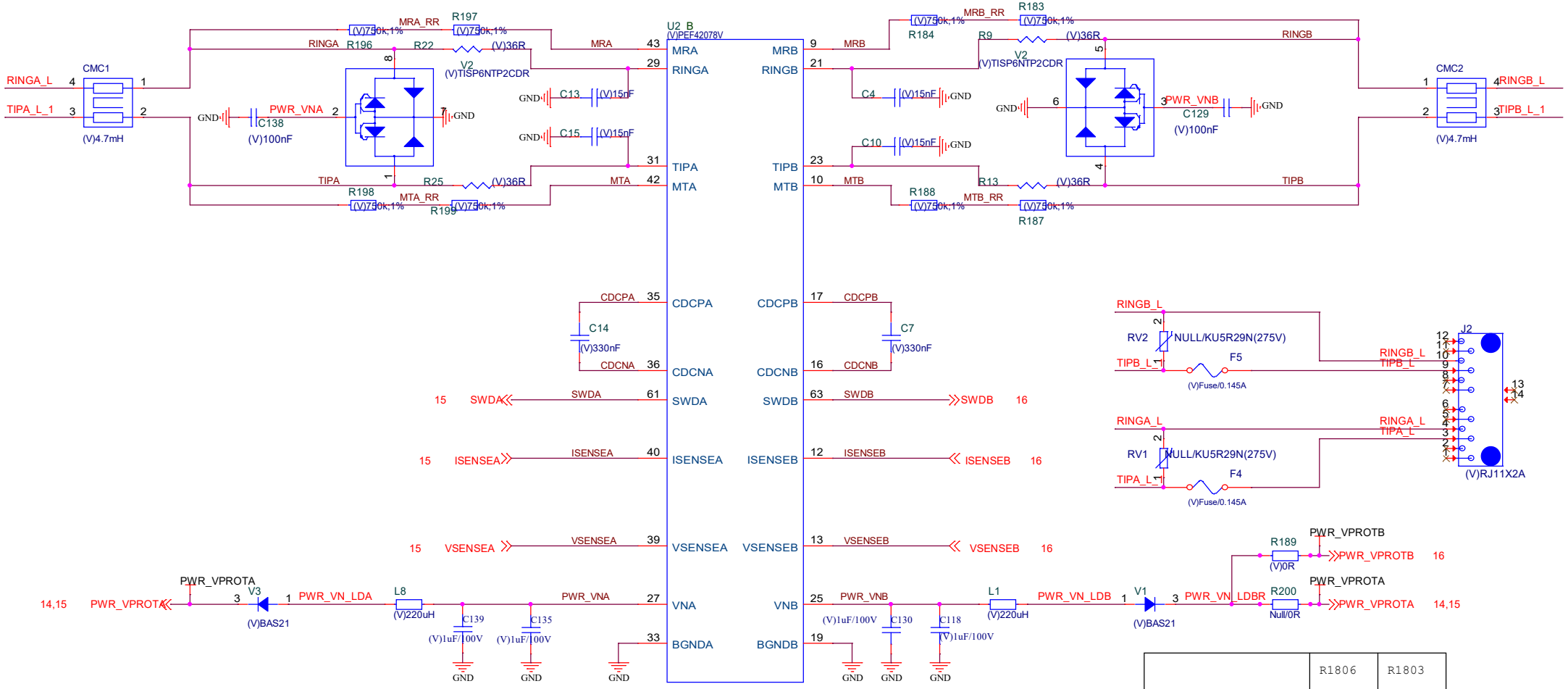
SLIC220



	R1806	R1803
Dedicated DCDC mode	Mounted	X
Combined DCDC mode	X	Mounted

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Title: XWAYSLIC220_ANALOG

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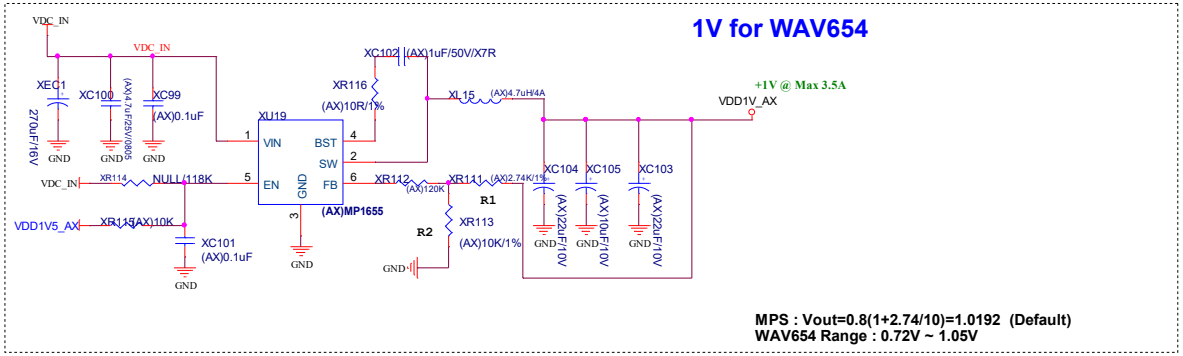

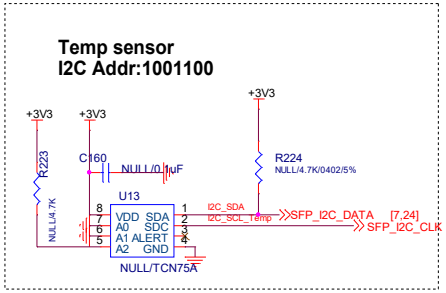

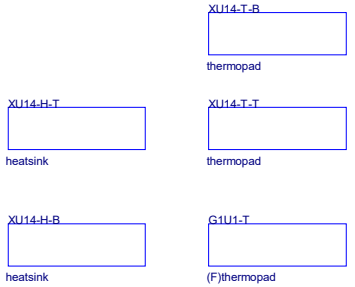

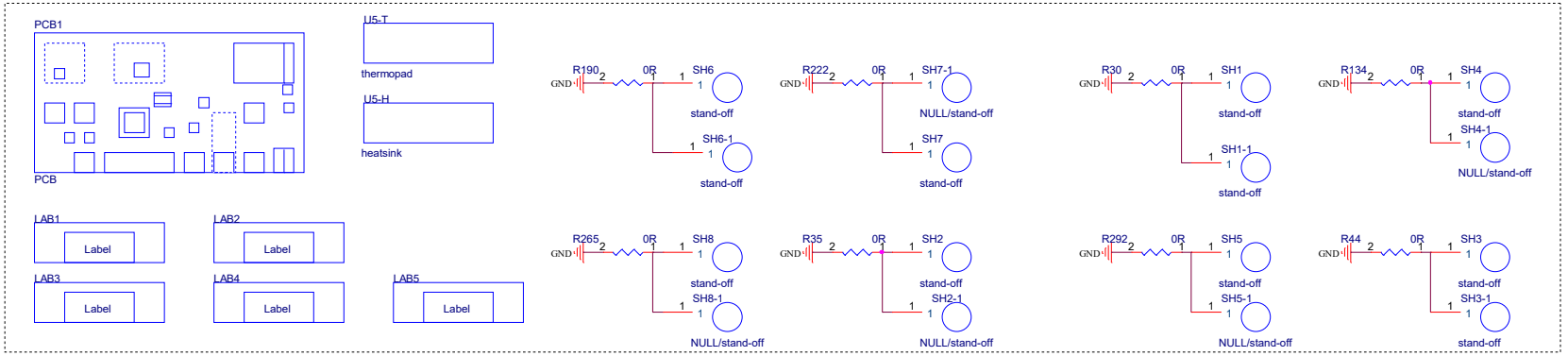

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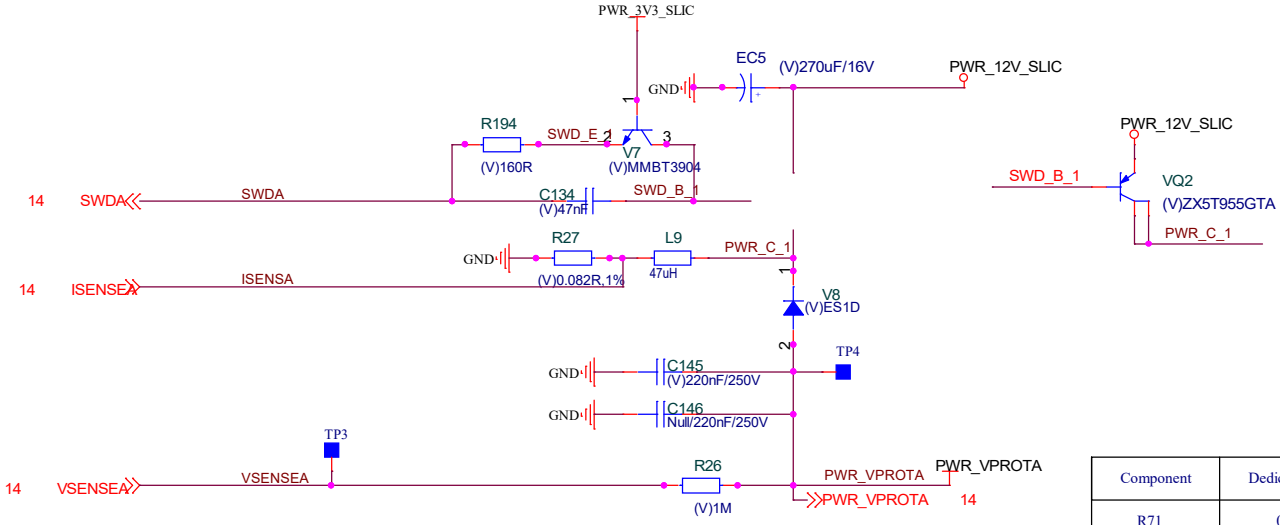
DCDC Type
Dedicated DCDC = T0.2
Combined DCDC = T1.1

Move radiating parts (like switching regulators and coils, voice SLIC/coils,) far away from DSL-AFE. A distance (at least 5cm) between the reiating part and the DSL must be maintain.



Component	Dedicated DCDC	Combined DCDC
R71	0.082R	0.068R
L7	47uH/1.8A	33uH/2.1A
C196	mount	X
C1805	X	mount

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Title: U1_PNP_DCDC_T02_V11

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REVISION HISTORY

Version	Date	List of Modification	Page
V6A	2021-02-02	1. Remove VRX518 circuit 2. Add EWAN circuit 3. Add IP1001 circuit	Ian
	2020-12-10	2.4GHz FEM (152-5331900-00G,SKY85331-11) : 1. Add XU31, XU33 2. Remove XC12, XC13, XC10, XC11 3. Null XR101, XR88, XU30, XU32 4. Place XR137, XR136 5. Remove XR146, XR149, XR142, XR145 5GHz FEM (152-5743900-00G,SKY85743-31) : 1. Add XU51, XU53 for co-layout with XU52, XU54 2. Remove XR117, XR113, XC16, XC17 3. Remove XR118, XR129, XC181, XC182 4. Place XR11, XR12 6. Null XU61, XR10, XR135 7. Place XR139, XR140 8. Null XU63, XR138, XR141	mChen
V6B	2021-06-16	1. Add U20, XR135, XR135, XR136, XR137, XL23, XL24, XL25, XL26 2. Add U21, XR40, XR138, XR139, XR140, XL27, XL28, XL29, XL30 3. PEC3 change footprint EC/1050 4. Add PD15, R444, R445 5. Add J9 6. XC15, XC59 change C0805 7. Add SH4-1	Ian
V6C	2022-01-04	1. Modify EC7 ,EC6 to 270uF. 2. Add U34 curcuit	Ian

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BOM Difference

	V2765ax	V2765Vax							
(VD)	V	V							
(V)	NULL	V							
(5)	V	V							
(PD)	NULL	NULL							
(AX)	V	V							
(NPD)	V	V							
(AX_LTE)	NULL	NULL							

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Title BOM Difference

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