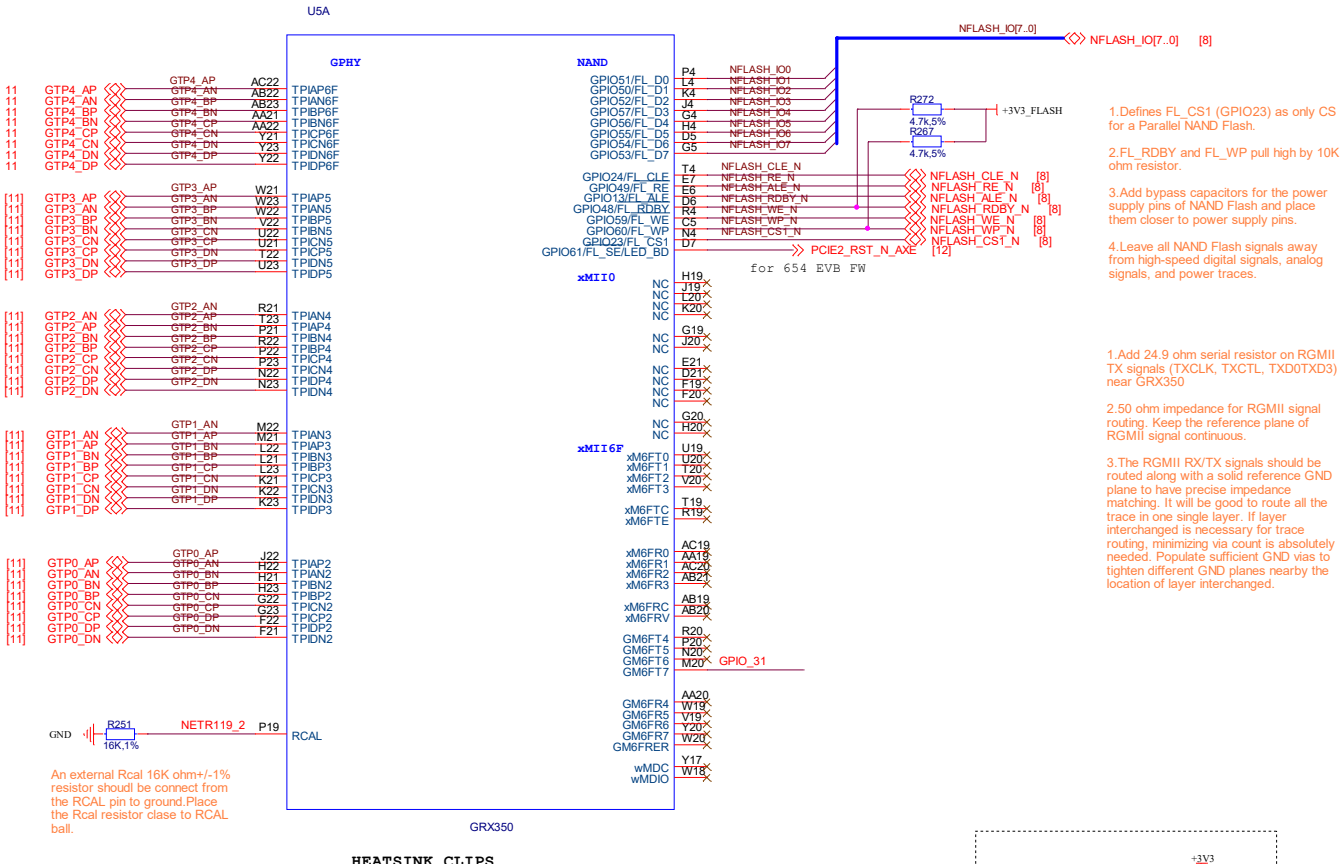
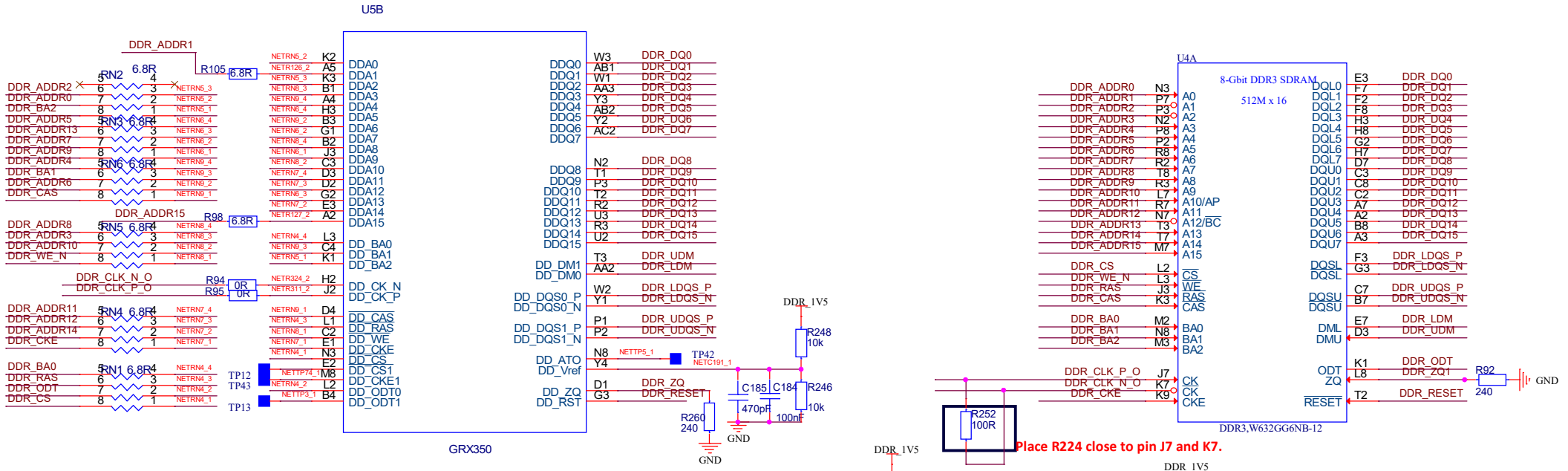


<OrgName>	DrayTek		
Title	GRX350_NAND_xMII_GPH		
Size: Custom	Document Number: V2766AX		Rev: 6B
Date: Thursday, July 21, 2022	Sheet 2 of 34		



Qualified DDR3 List

- Etron: EM6GC16EWXD-10H (64Mx16bit, single rank (CS0))
- Micron: MT41K128M16JT-125:K (128Mx16bit, single rank (CS0))
- Micron: MT41K256M16HA-125 IT:E (256Mx16bit, single rank (CS0))
- Winbond: W634GG6LB-12 (256Mx16bit, single rank (CS0))
- Etron: EM6GE16EWXC-10H (256Mx16bit, single rank (CS0))
- Nanya: NT5CB256M16DP-EK (256Mx16bit, single rank (CS0))
- Micron: MT41K512M16HA-125:A (512Mx16bit, single rank (CS0))

1.Place 6.8ohm series termination resistors close to GRX350 for CA group.

2.An external RZQ 240 ohm+/-1% resistor shoudl be connect from the ZQ pin to ground on both GRX350 and DDR device.

3.System DD_VREF and DDR device VREFCA and VREFDQ are separated,divided by 10K ohm +/-1% resistors.

4.55 ohm Single-End and 100 ohm Differential signals impedance control

5.5mils Single-End trace width, trace to trace clearance is 10mils

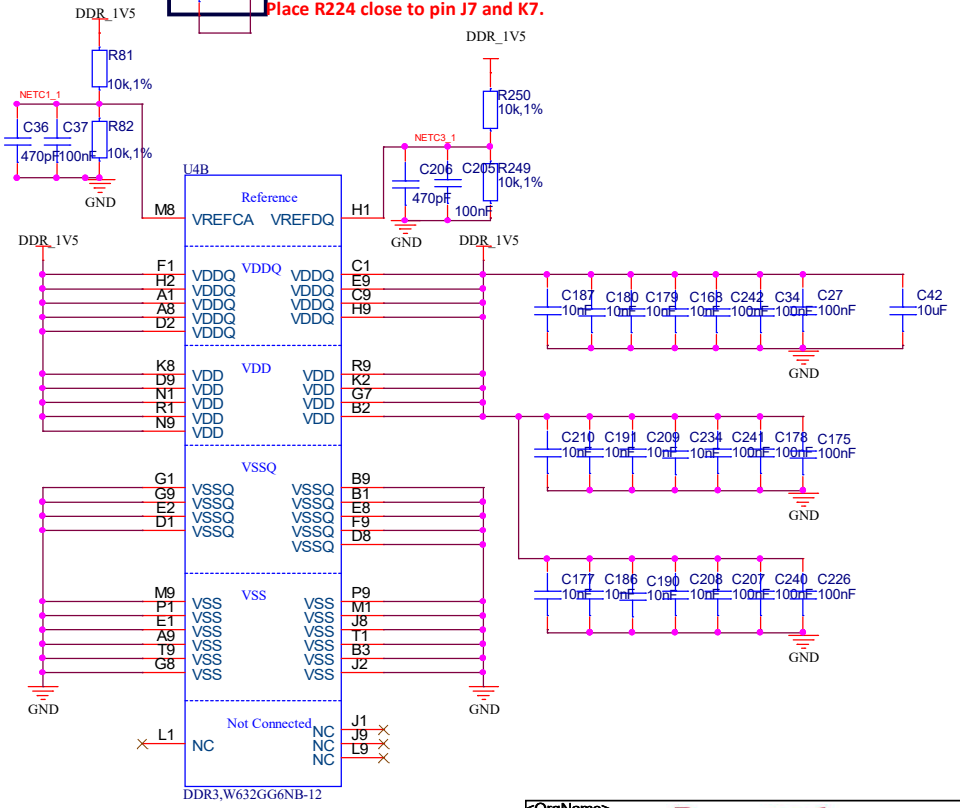
6.Length Matching
Maximum trace length difference (skew) between DQS and DQS#: ± 4 mils (< 0.6 ps).
Maximum trace length difference (skew) DQ to DQS/ DQS# domain: ± 30 mils (< 10 ps).
Maximum trace length difference (skew) Addr/Cmd to CK/ CK# domain: ± 70 mils (< 25ps).
Maximum trace length difference (skew) DQS/DQS# to CK/ CK# domain: ± 250 mils (< 90ps).

7.Crosstalk control (Note: H is distance from reference layer):
Keep edge-to-edge trace spacing within DQ/DM byte group > 2H
Keep edge-to-edge trace spacing within Cmd/Add/Ctrl > 2H (commonly known as CA)
Keed edge-to-edge trace separation for each group (DQ, DQS/DQS#, CA, CK/CK#) > 3H

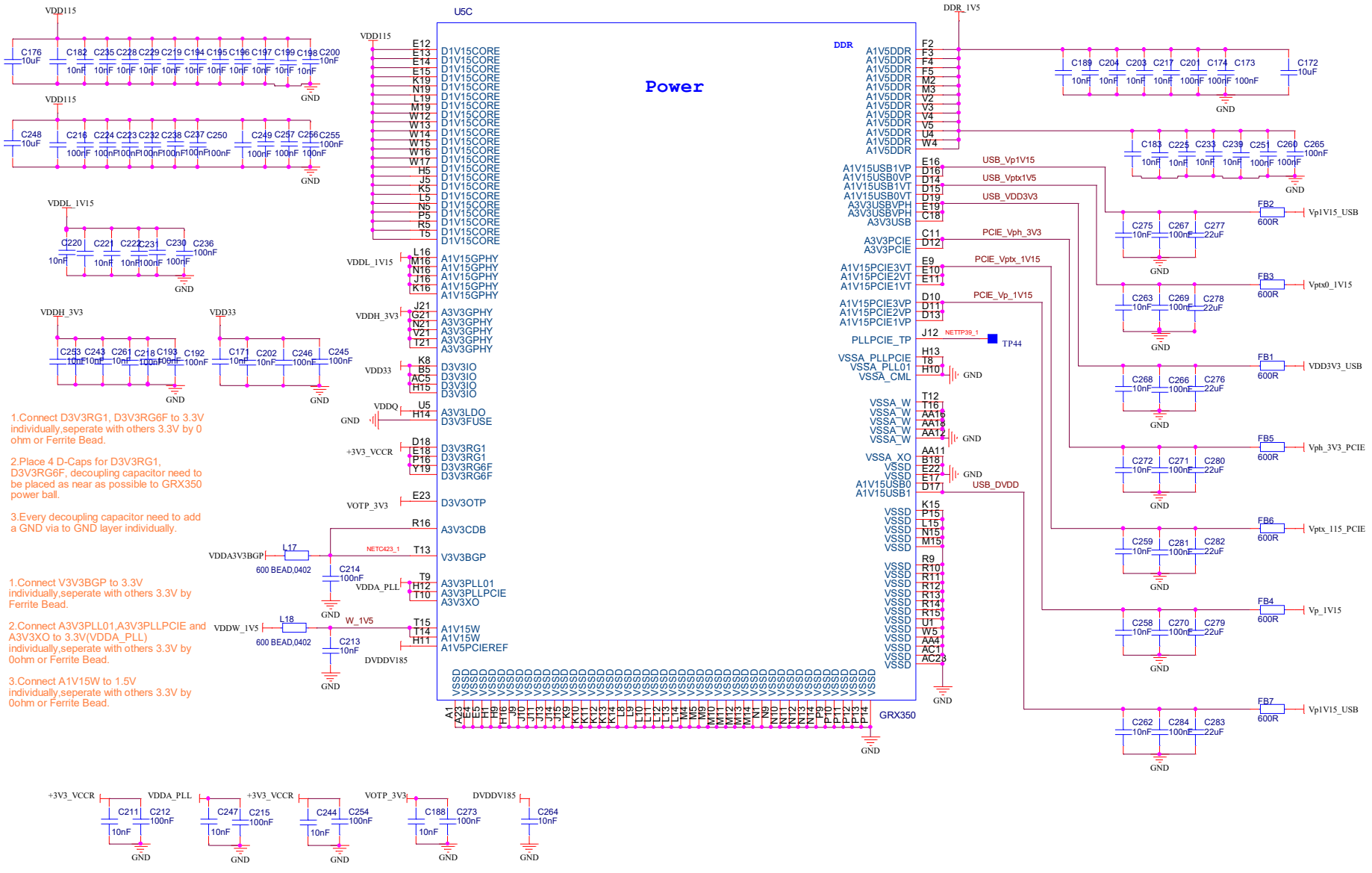
8.DDR CLK differential termination 100ohm place at the end on DDR device. as close to CLK pins as possible.

9.Fly-By Topology & VTT Termination recommended for DDR3, if multiple devices are used.

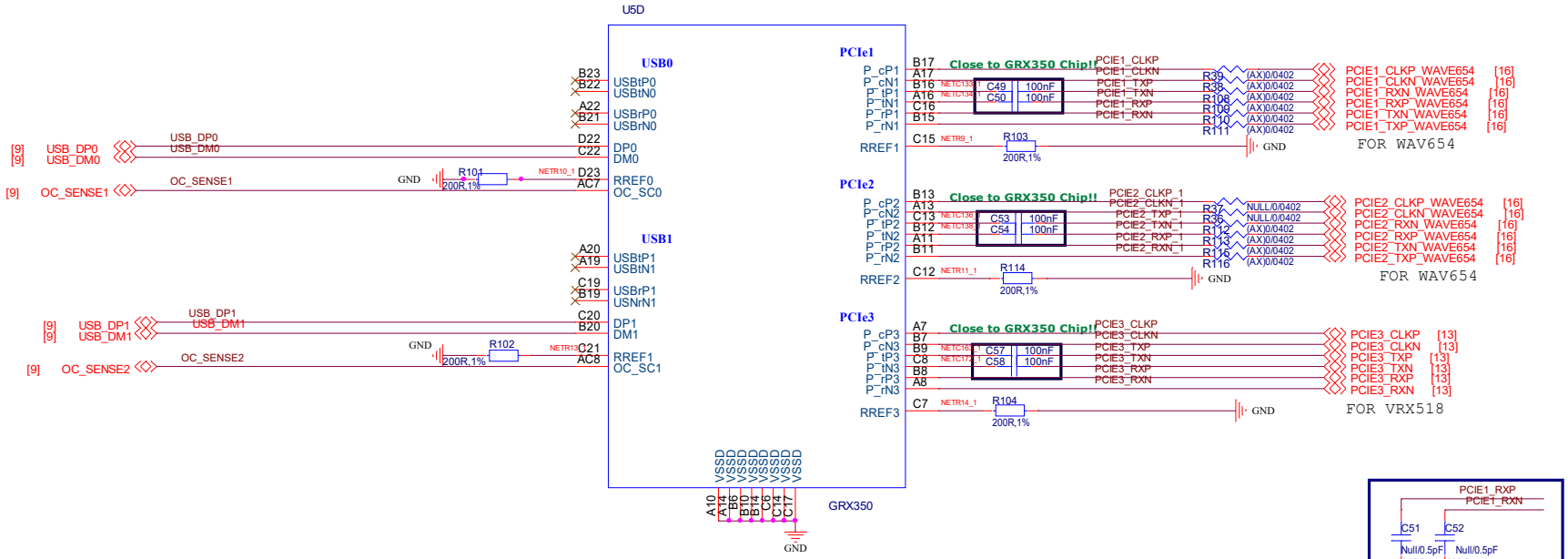
10.Carefully consider layout requirements of DDRn vendor!!!

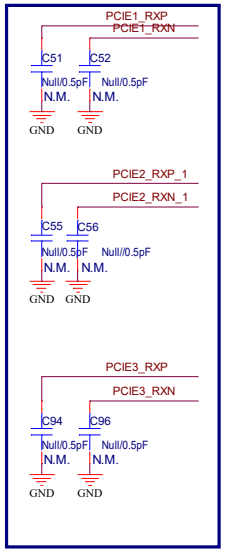


<OrgName>	DrayTek		
Title	GRX350_DDR3_x16		
Size: Custom	Document Number: V2766AX		Rev: 6B
Date: Thursday, July 21, 2022	Sheet 3 of 34		



<OrgName>	DrayTek		
Title	GRX350_Power		
Size: Custom	Document Number: V2766AX		Rev: 6B
Date: Thursday, July 21, 2022	Sheet 4 of 34		





1.An external Rref 200 ohm+/-1% resistor should be connect from the USB RREF0, RREF1 pins to ground. Place the Rref resistor close to RREF balls.

2.Place 2 AC coupling capacitors on USB TX pairs , <0.5inch length to GRX350 is recommended.

3.90 ohm characteristic impedance control for USB differential signal routing. Keep the reference plane of signal continuous.

4. Match trace length of differential pairs (_p and _n signal) to given value in appropriate interface specification.

5. Populate sufficient GND vias nearby each PCIE differential pairs to tighten adjacent GND plane with GND layer.

1.An external Rref 200 ohm+/-1% resistor should be connect from the 3 PCIE RREF pins to ground. Place the Rref resistors close to RREF balls.

2.Place 2 AC coupling capacitors on PCIE TX pairs , <0.5inch length to GRX350 is recommended.

3.100 ohm characteristic impedance control for differential signal routing. Keep the reference plane of signal continuous.

4.In case with >= 2 PCIe differential pairs routing on PCB, a footprint of shielding case to enclose all these differential pairs is highly recommended for the compliance of EN300-328 V1.8.1 standard.

5.0.5pF capacitors to ground on PCIE RX pairs, place them close to GRX350.

6. Match trace length of differential pairs (_p and _n signal) to given value in appropriate interface specification.

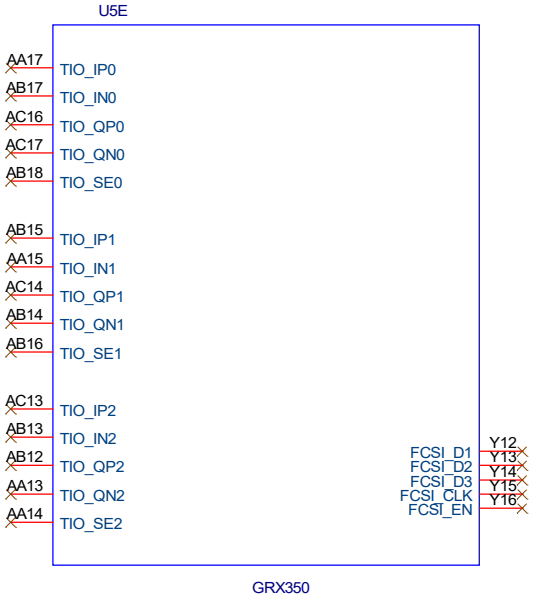
7. Populate sufficient GND vias nearby each PCIE differential pairs to tighten adjacent GND plane with GND layer.

<OrgName> DrayTek

Title: GRX350_PCIE_USB

Size	Document Number	Rev
Custom	V2766AX	6B

Date: Thursday, July 21, 2022 Sheet 5 of 34



Trace capacitance for BBIO interface must be below 10pF! Recommend the maximum length should be under 3 inch.

<OrgName>	DrayTek	
Title	GRX350_BBIO	
Size: Custom	Document Number: V2766AX	Rev: 6B
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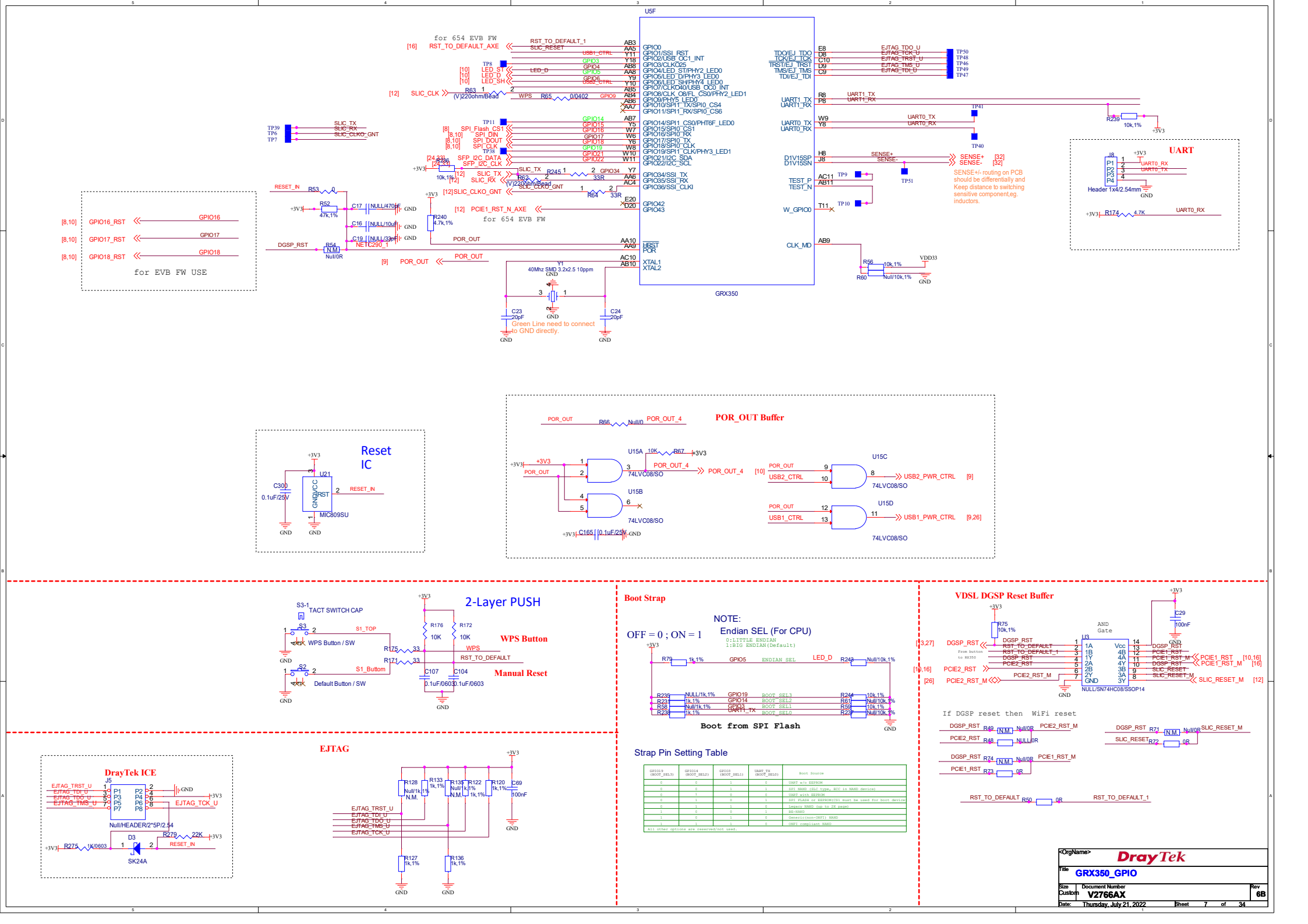
U5F
GRX350
for 654 EVB FW
RST_TO_DEFAULT_AXE
SLIC_RESET
LED_D
LED_ST
LED_D
LED_SH
SLIC_CLK
SLIC_TX
SLIC_RX
SLIC_CLKO_GNT
SPI_Flash_CS1
SPI_DIN
SPI_DOUT
SPI_CLK
SFP_I2C_DATA
SFP_I2C_CLK
PCIE1_RST_N_AXE
POR_OUT
GPIO0
GPIO1/SSI_RST
GPIO2/USB_OC1_INT
GPIO3/CLKO25
GPIO4/LED_ST/PHY2_LED0
GPIO5/LED_D/PHY3_LED0
GPIO6/LED_SH/PHY4_LED0
GPIO7/CLKOUT0/USB_OC0_INT
GPIO8/CLK_O8/FL_CS0/PHY2_LED1
GPIO9/PHY5_LED0
GPIO10/SPI1_TX/SPI0_CS4
GPIO11/SPI1_RX/SPI0_CS6
GPIO14/SPI1_CS0/PHT6F_LED0
GPIO15/SPI0_CS1
GPIO16/SPI0_RX
GPIO17/SPI0_TX
GPIO18/SPI0_CLK
GPIO19/SPI1_CLK/PHY3_LED1
GPIO21/I2C_SDA
GPIO22/I2C_SCL
GPIO34/SSI_TX
GPIO35/SSI_RX
GPIO36/SSI_CLK
GPIO42
GPIO43
HRST
POR
XTAL1
XTAL2
TDO/EJ_TDO
TCK/EJ_TCK
TRST/EJ_TRST
TMS/EJ_TMS
TDI/EJ_TDI
UART1_TX
UART1_RX
UART0_TX
UART0_RX
D1V15SP
D1V15SN
TEST_P
TEST_N
W_GPIO0
CLK_MD
EJTAG_TDO_U
EJTAG_TCK_U
EJTAG_TRST_U
EJTAG_TMS_U
EJTAG_TDI_U
SENSE+
SENSE-
SENSE+/- routing on PCB should be differentially and Keep distance to switching sensitive component,eg. inductors.
UART
Header 1x4/2.54mm
for EVB FW USE
GPIO16_RST
GPIO17_RST
GPIO18_RST
Reset IC
MIC809SU
POR_OUT Buffer
74LVC08/SO
USB2_PWR_CTRL
USB1_PWR_CTRL
2-Layer PUSH
WPS Button
Manual Reset
TACT SWITCH CAP
WPS Button / SW
Default Button / SW
Boot Strap
NOTE:
Endian SEL (For CPU)
OFF = 0 ; ON = 1
0:LITTLE ENDIAN
1:BIG ENDIAN(Default)
Boot from SPI Flash
Strap Pin Setting Table
VDSL DGSP Reset Buffer
AND Gate
NULL/SN74HC08/SSOP14
If DGSP reset then WiFi reset
DrayTek ICE
Null/HEADER/2*5P/2.54
SK24A
EJTAG
Green Line need to connect to GND directly.
<OrgName>
DrayTek
Title
GRX350_GPIO
Size
Custom
Document Number
V2766AX
Rev
6B
Date:
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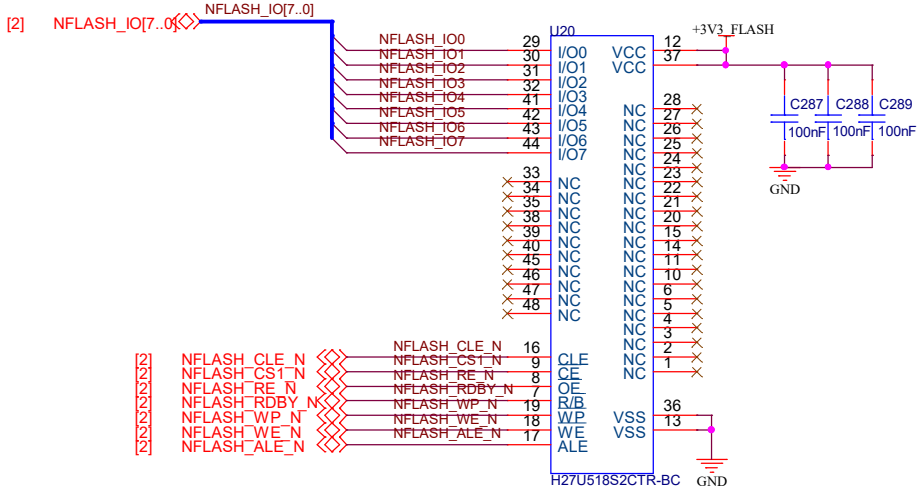
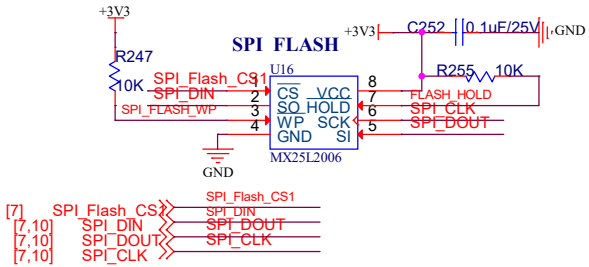


Qualified Nand Flash List

Vendor	Model
Hynix	H27uag8, 8k
Hynix	H27u512, 512
Hynix	H27u4g8f2dtr, 2k
Hynix	H27u1g8f2btf, 2k
Samsung	K9F1208, 512
Samsung	K9f1g08u0d, 2k
Samsung	K9g4g08u0b, 2k
Samsung	K9G8G08U0C, 8k
Spansion	S34ml01g100, 2k
Mircon	29f64g08cbaba, 8k
Mircon	29f32g08cbaca, 4k
Infineon	Hyf33ds51280, 512
Toshiba	Th58BVG3S0HTA00, 4k

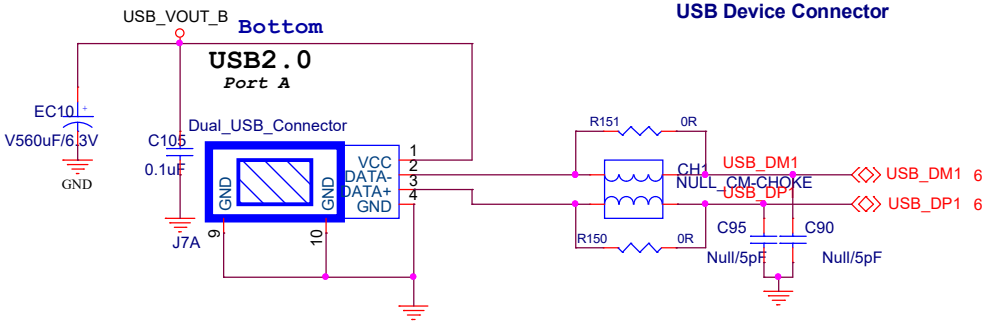


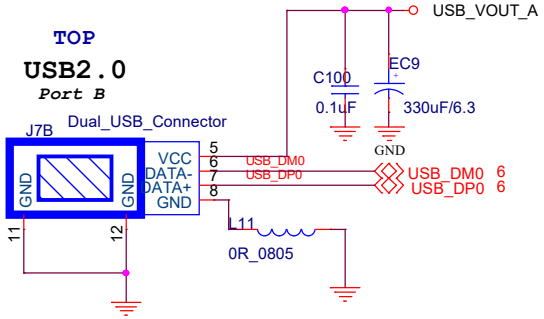
<OrgName>	DrayTek		
Title	NAND_FLASH		
Size B	Document Number V2766AX		Rev 6B
Date: Thursday, July 21, 2022	Sheet 8 of 34		

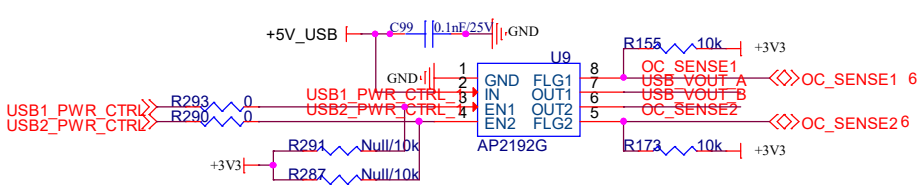
!!Note:
The PCB layout of the differential signal DP and DM should have 90 ohm differential impedance, and keep the trace length below 1 inch if possible.

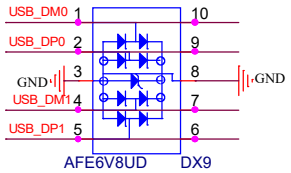
TOP B
Bottom A

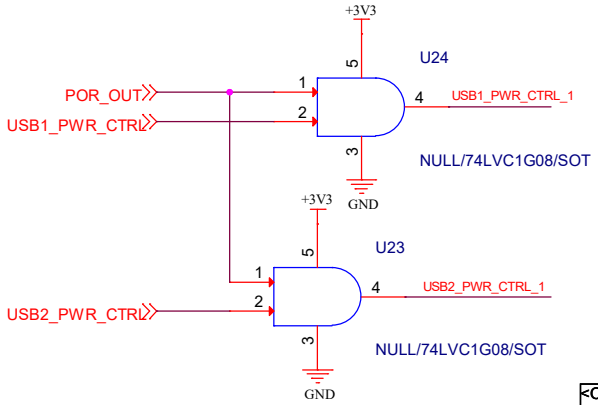
USB Device Connector











<OrgName>	DrayTek
Title	USB_Port
Size: B	Document Number: V2766AX
Rev	6B
Date:	Thursday, July 21, 2022
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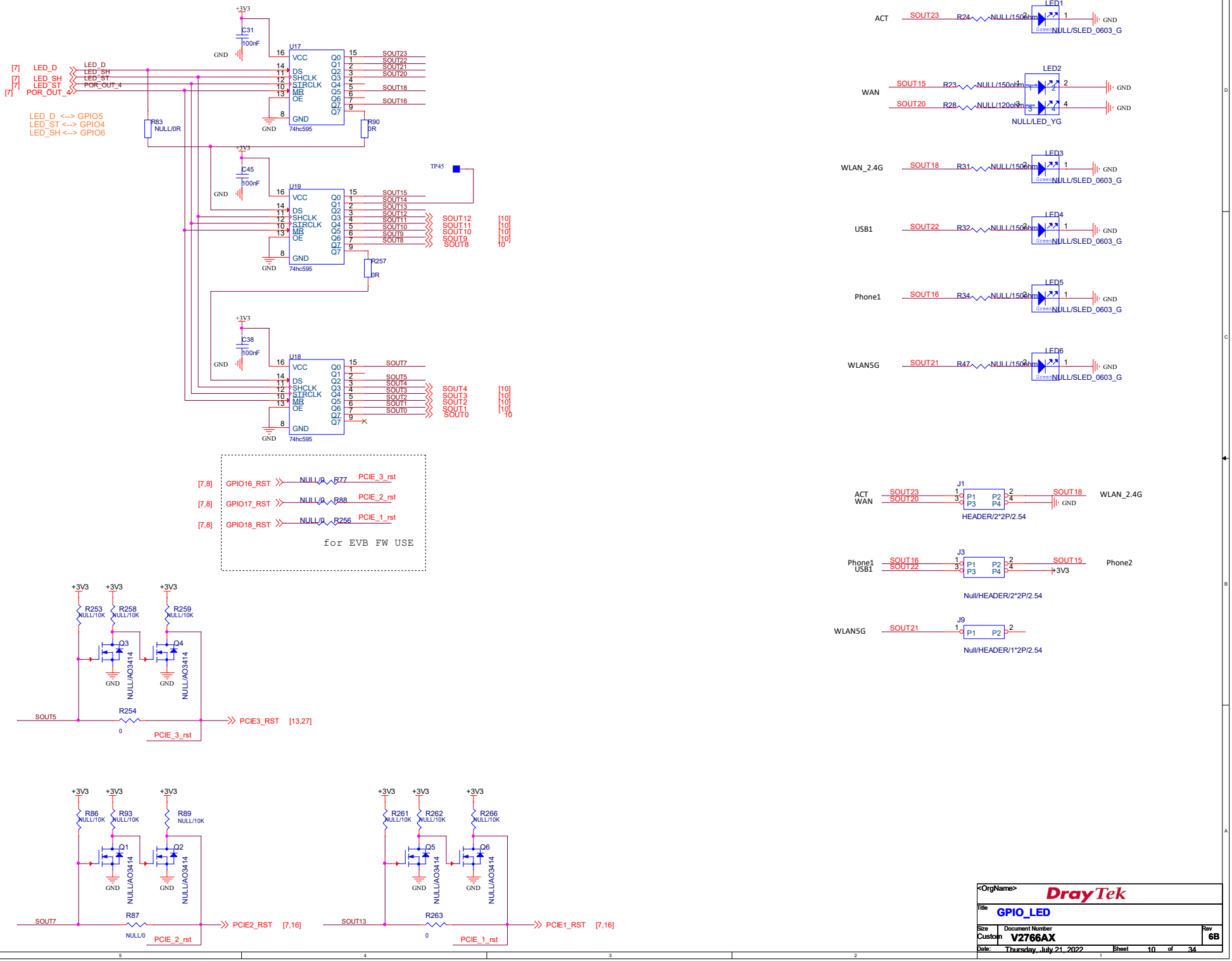
[7] LED_D
[7] LED_SH
[7] LED_ST
[7] POR_OUT_4
LED_D <--> GPIO5
LED_ST <--> GPIO4
LED_SH <--> GPIO6
+3V3
C31
100nF
GND
U17
74hc595
R83 NULL/0R
R90 0R
SOUT23
SOUT22
SOUT21
SOUT20
SOUT18
SOUT16
C45
U19
TP45
R257 0R
SOUT15
SOUT14
SOUT13
SOUT12
SOUT11
SOUT10
SOUT9
SOUT8
C38
U18
SOUT7
SOUT5
SOUT4
SOUT3
SOUT2
SOUT1
SOUT0
[10]
[7,8] GPIO16_RST
[7,8] GPIO17_RST
[7,8] GPIO18_RST
NULL/0
R77 PCIE_3_rst
R88 PCIE_2_rst
R256 PCIE_1_rst
for EVB FW USE
R253 NULL/10K
R258 NULL/10K
R259 NULL/10K
Q3
Q4
NULL/AO3414
R254 0
PCIE_3_rst
PCIE3_RST [13,27]
R86 NULL/10K
R93 NULL/10K
R89 NULL/10K
Q1
Q2
R87 NULL/0
PCIE_2_rst
PCIE2_RST [7,16]
R261 NULL/10K
R262 NULL/10K
R266 NULL/10K
Q5
Q6
R263 0
PCIE_1_rst
PCIE1_RST [7,16]
ACT
WAN
WLAN_2.4G
USB1
Phone1
WLAN5G
LED1
LED2
LED3
LED4
LED5
LED6
R24 NULL/150ohm
R23 NULL/150ohm
R28 NULL/120ohm
R31 NULL/150ohm
R32 NULL/150ohm
R34 NULL/150ohm
R47 NULL/150ohm
NULL/SLED_0603_G
NULL/LED_YG
J1
HEADER/2*2P/2.54
J3
Null/HEADER/2*2P/2.54
J9
Null/HEADER/1*2P/2.54
Phone2
+3V3
<OrgName>
DrayTek
Title
GPIO_LED
Size
Custom
Document Number
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6B
Date:
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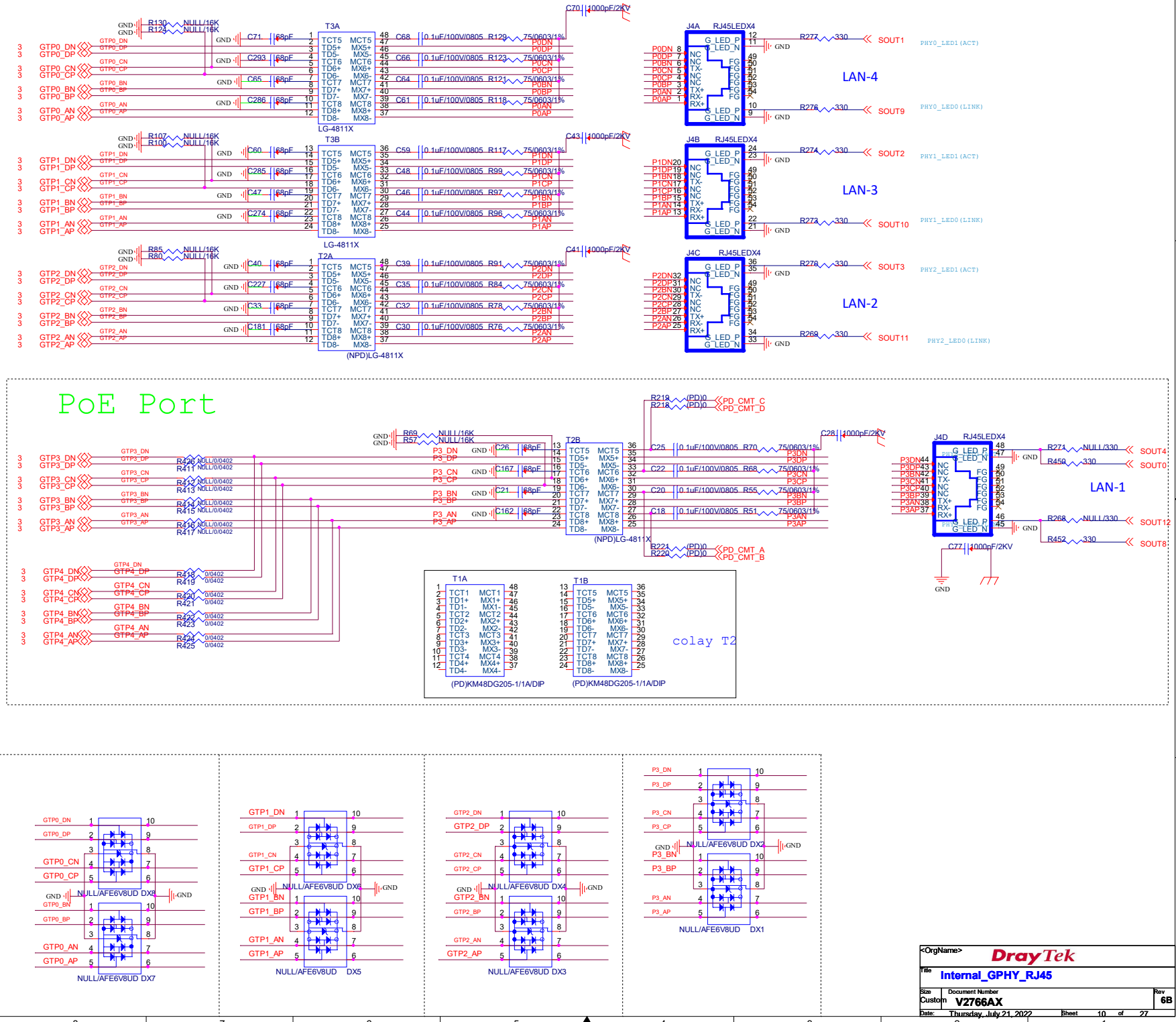

<OrgName>	DrayTek
Title	Internal_GPHY_RJ45
Size	Custom
Document Number	V2766AX
Rev	6B
Date:	Thursday, July 21, 2022
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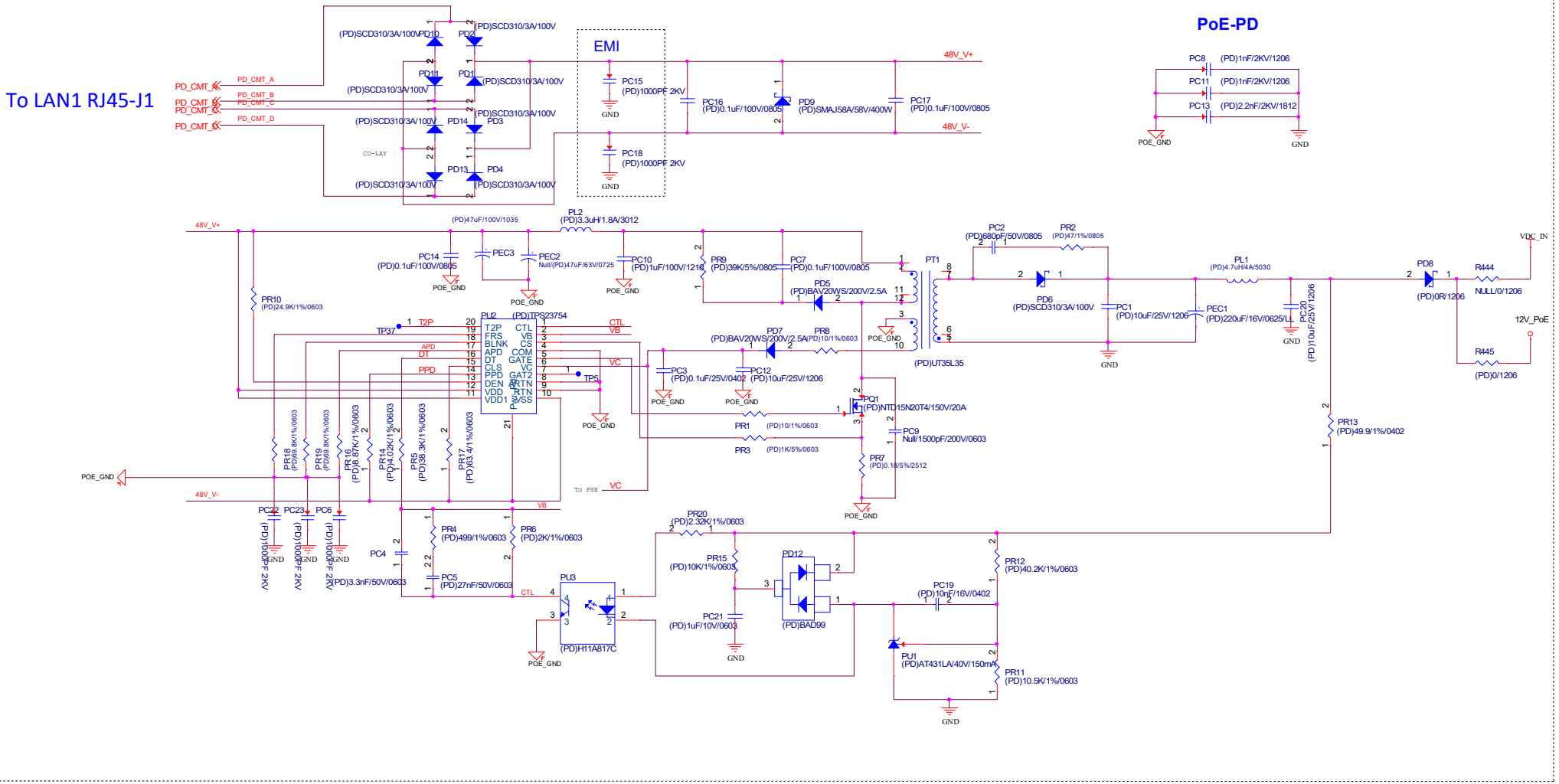

<OrgName>	DrayTek	
Title	POE PD	
Size C	Document Number V2766AX	Rev 6B
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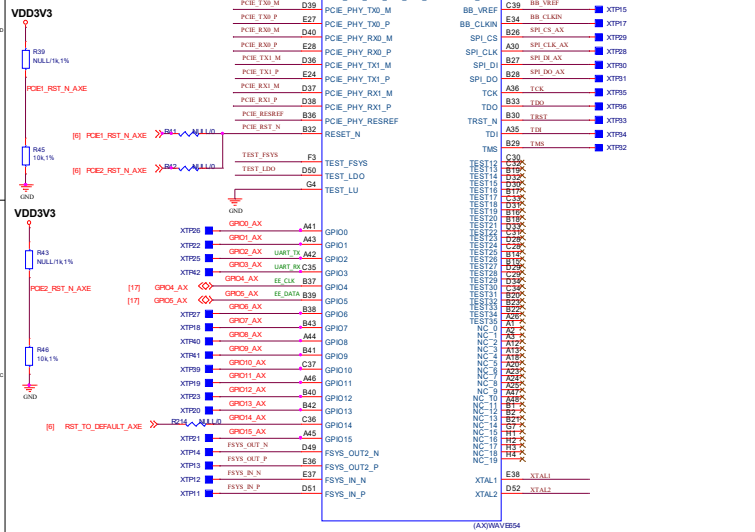
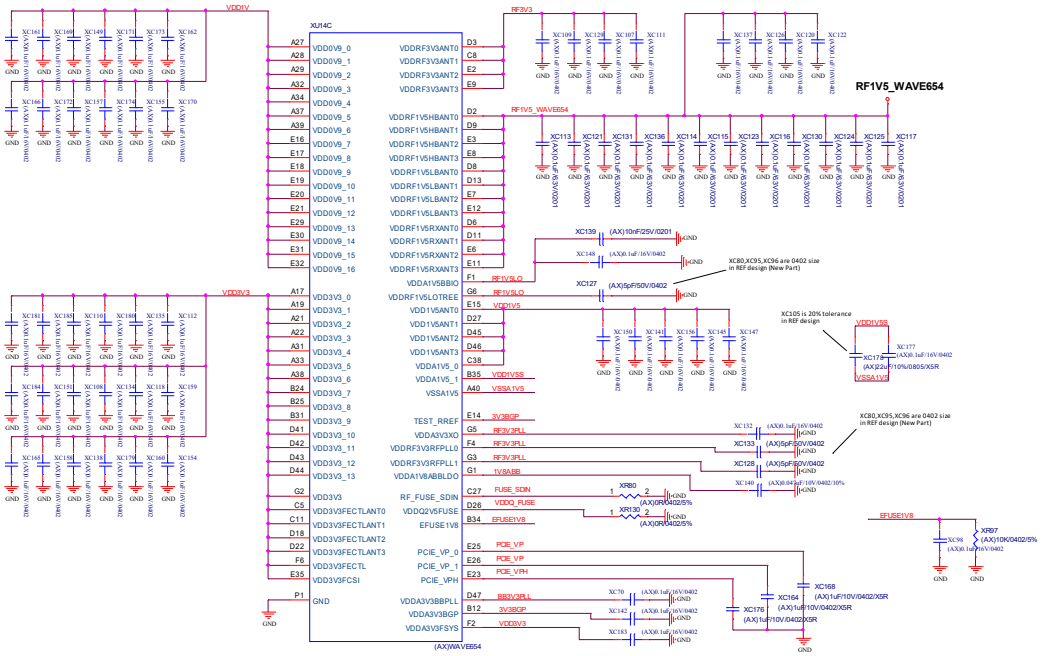
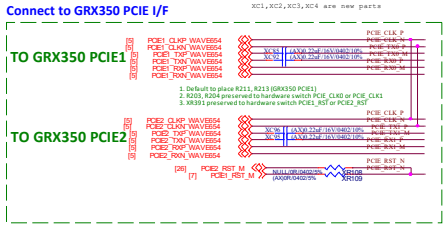
WAVE654 PCIE / GPIO / SPI

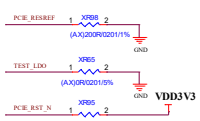


WAVE654 POWER

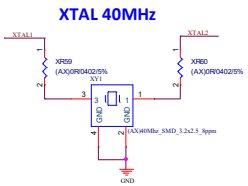


Connect to GRX350 PCIE I/F

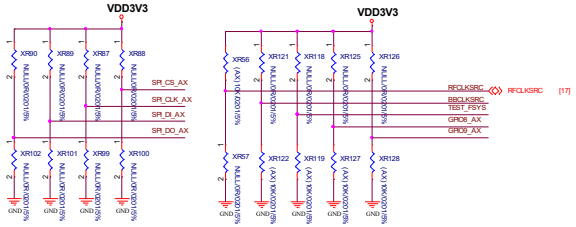




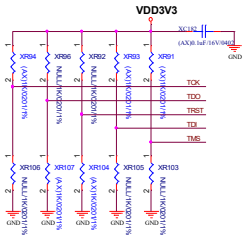
XTAL 40MHz



Boot Strapping



WAV654 Init Strapping



Reserved for GPB654 Refernce Design

SY98004 : Vout=0.6(1+120K/165K)=1.036V
WAV654 Range : 0.72V ~ 1.05V

Table 32 JTAG Signals

Ball No.	Name	Pin Type	Buffer Type	Function
B30	TRST	I	PU	JTAG Reset Notes 1. Low active. 2. If the JTAG interface is not in use, this pin must be connected to V_{SS}.
	EJ_TRST	I	PU	EJTAG Reset
A35	TDI	I	PU	Test Data Input
	EJ_TDI	I		EJTAG Test Data Input
B33	TDO	O	PD	Test Data Output Note: pull down is needed for normal operation.
	EJ_TDO	O		EJTAG Test Data Output
B29	TMS	I	–	Test Mode Select
	EJ_TMS	I		EJTAG Mode Select

Reserved for GPB654 Refernce Design

Reserved for GPB654 Refernce Design

UART CONN

<OrgName>	DrayTek
Title	WAVE654_POWER_PCIE
Size	D
Document Number	V2766AX
Rev	6B
Date	Thursday, July 21, 2022
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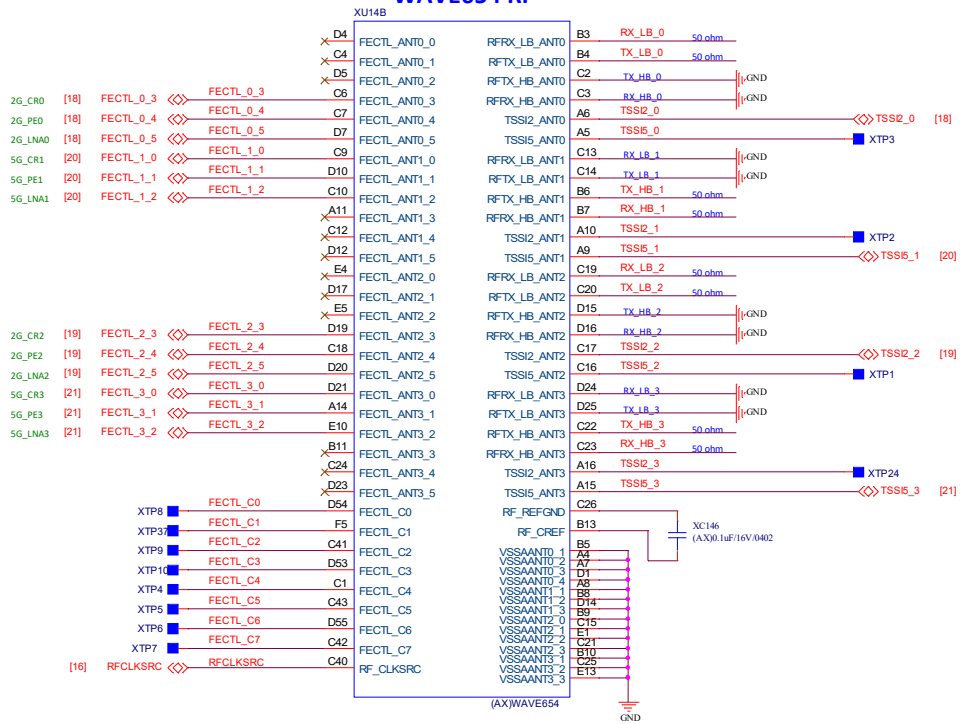
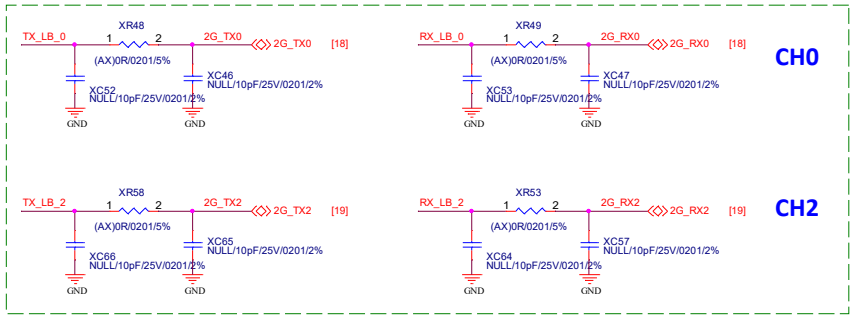
WAVE654 RF



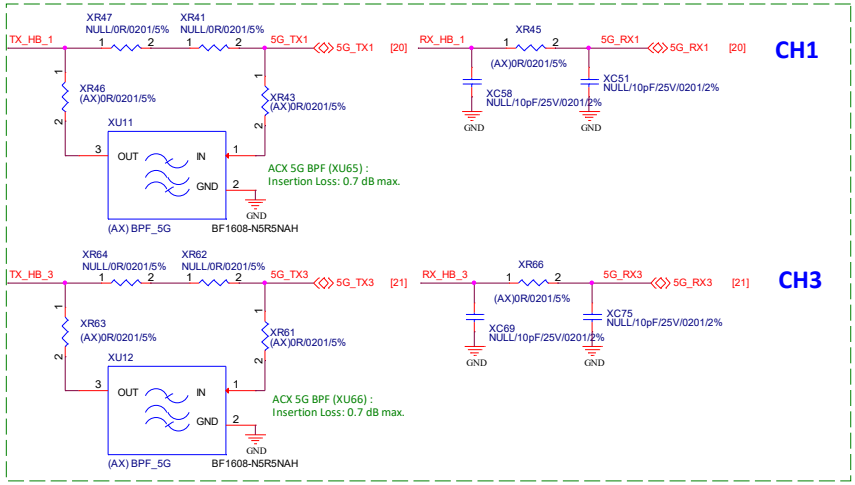
Reserved for GPB654 Refernce Design

PCIE FINGER

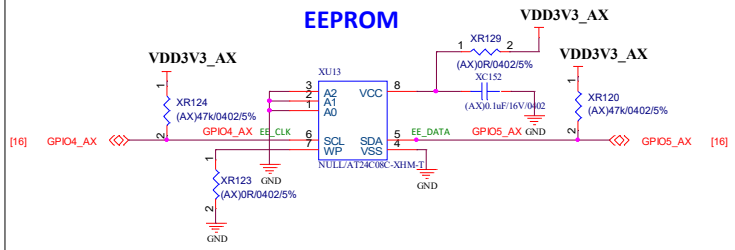
2.4G Front-End



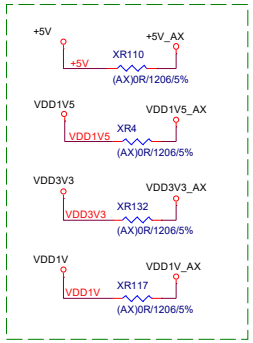
5G Front-End



EEPROM



Connect to main board DCDC



SY98004 : Vout=0.6(1+120K/165K)=1.036V
WAV654 Range : 0.72V ~ 1.05V

<OrgName>	DrayTek	
Title	WAVE654_RF	
Size: Custom	Document Number: V2766AX	Rev: 6B
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SKY85331-11 :
Output power: +22 dBm @ 1.8% EVM, HT40, MCS9, 5 V
Output power: +26 dBm @ 3% EVM, HT40, MCS7, 5 V

2.4G FEM CH0

XR90 is new part wihtout Draytek part number

+5V
XR21 (AX)6.8nH/0.6A/0805/5%
PA_2G0
XC15 (AX)4.7uF/16V/0805/10%
XC134 is 6.3V voltage in REF design
GND

Layout Notice :
- Decoupling CAP should be placed before RES

[17] FECTL_0_4 FECTL_0_4 XR28 2G_PE0 XC37 (AX)0R/0402/5% (AX)1pF/50V/0.05pF/0402
[17] FECTL_0_5 FECTL_0_5 XR22 2G_LNA0 XC24 (AX)0R/0402/5% (AX)1pF/50V/0.05pF/0402
[17] FECTL_0_3 FECTL_0_3 XR18 2G_CR0 XC14 (AX)0R/0402/5% (AX)1pF/50V/0.05pF/0402

Layout Notice :
- Each Vcc pin needs to be individually decoupled.
- VCC0, VCC1, VCC2, and VCC3 should NOT be shorted together at the device pins.

PA_2G0 XC38 (AX)0.1uF/16V/0402 GND

XEU2 SKY85331-11
10 VDD
20 VCC3
22 VCC2
23 VCC1
24 VCC0
15 RX_OUT
13 LNA_IN
4 PA_EN
6 DET
5 NU5
8 NU8
17 ANT
19 C1
16 C0
2 TX_IN
12 LNA_OUT
1 3 7 9 11 14 18 21 25 GND1 GND3 GND7 GND9 GND11 GND14 GND18 GND21 PAD
(AX)SKY85331-11

PA_2G0 XC20 (AX)0.1uF/16V/0402 XC21 (AX)0.1uF/16V/0402
PA_2G0 XC22 (AX)0.1uF/16V/0402 XC19 (AX)0.1uF/16V/0402
BPF_2A0 50 ohm
BPF_2B0 50 ohm
2G_PE0

Close to XEU2
[17] TSSI2_0 TSSI2_0 XR30 (AX)0R/0201/5% XR29 (AX)0R/0201/5% XR31 NULL/0R/0201/5% XC40 NULL/10pF/25V/0201/2%
XR98 is designed for RTC7647

XC23 NULL/10pF/25V/0201/2% XC16 NULL/10pF/25V/0201/2% XC17 (AX)10pF/25V/0201/2% 50 ohm 2G_ANT0
2G_CR0
2G_LNA0
Layout Notice :
- Control Pin C0, C1 should be shielded by GND with more Vias.

XC29 (AX)10pF/25V/0201/2% 50 ohm 2G_TX0 [17]
XC30 NULL/10pF/25V/0201/2%
XC35 NULL/10pF/25V/0201/2%
XC36 NULL/10pF/25V/0201/2%
XL6 NULL/0R/0201/5%
XL7 NULL/0R/0201/5%

BPF (2400-2500MHz)

XC39 (AX)10pF/25V/0201/2%
XU7 IN GND2 GND4 OUT
NULL/(AX)BPF_2G BF2012-L2R4NAR
2G_RX0 [17]
XR33 0R/0201/5%

ACX 2G BPF (XU30) :
Insertion Loss: 0.9 dB max. (25C)
Insertion Loss: 1.1 dB max. (-40C~85C)

SAW (For LTE)

Close to XEU2
Co-Layout
BPF_2A0 XR134 NULL/0R/0201/5% XR135 NULL/0R/0201/5% BPF_2B0
XR136 (AX_LTE)1.5nH (AX_LTE)0R/0201/5% XR137
XL23 NULL/0.5pF/50V/0201 XL24 (AX)0.5pF/50V/0201
XU20 In GNDin GNDout
XL25 (AX_LTE)5.1nH
XL26 NULL/10nH/0.25A/0201/3% (AX_LTE)SAW_SF14112442A01T

Walsin SAW Filter (XU20) :
Insertion Loss: 2.9 dB 20x. @ 2400 ~ 2484 MHz
Pin : 28 dBm @ 2400 ~ 2484 MHz, 20MHz OFDM Signal

2G_CH0_5G_CH1_DIPLEXER

XU1 HI_FREQ LO_FREQ COMMON GND2 GND4 GND6
(AX)DIPLEXER DP1608-A2455BKH0
XR1 (AX)4.7pF/0201

Close to SMA3
XL1 (AX)0R/0201/5%
2G_5G_A0_IPX
XJ1 (AX)IPEX_2G_FEM0
XC2 (AX)0.4pF/50V/0201
XC1 NULL/2.2pF/50V/0201

ACX 2G/5G Diplexer (XU7) :
2G Insertion Loss: 0.6 dB max.
5G Insertion Loss: 0.78 dB max.
2G Isolation: 38 dB min. @ 2400 ~ 2500 MHz
5G Isolation: 38 dB min. @ 4900 ~ 5950 MHz

Co-Layout
2G_ANT0 XR20 (AX)0R/0201/5% XR19 NULL/1.5nH XL4 NULL/0.5pF/50V/0201
XR12 (AX)0R/0201/5% XR13 NULL/0R/0201/5% XL2 (AX)0.5pF/50V/0201
[20] 5G_ANT1_DI 5G_ANT1_DI 50 ohm XR9 (AX)0R/0201/5% 50 ohm XR3 (AX)0R/0201/5%
XU3 In GNDin GNDout
XL3 NULL/5.1nH
XL5 NULL/10nH/0.25A/0201/3% NULL/SAW_SF14112442A01T

Walsin SAW Filter (XU71) :
Insertion Loss: 2.2 dB typ. 2.9 dB max. @ 2400 ~ 2484 MHz (-30 ~ +85C)
Pin : 28 dBm @ 2400 ~ 2484 MHz

<OrgName> DrayTek
Title RF_2.4G_FEM_CH0
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SKY85331-11 :
Output power: +22 dBm @ 1.8% EVM, HT40, MCS9, 5 V
Output power: +26 dBm @ 3% EVM, HT40, MCS7, 5 V

2.4G FEM CH2

XR77 is new part wihtout Draytek part number

+5V

XR54 (AX)6.8nH/0.6A/0805/5%

XC59 (AX)4.7uF/16V/0805/10%

XC121 is 6.3V voltage in REF design

Layout Notice :
- Decoupling CAP should be placed before RES

[17] FECTL_2_4 — XR55 (AX)0R/0402/5% — 2G_PE2 — XC63 (AX)1pF/50V/0.05pF/0402

[17] FECTL_2_5 — XR39 (AX)0R/0402/5% — 2G_LNA2 — XC41 (AX)1pF/50V/0.05pF/0402

[17] FECTL_2_3 — XR44 (AX)0R/0402/5% — 2G_CR2 — XC48 (AX)1pF/50V/0.05pF/0402

Layout Notice :
- Each Vcc pin needs to be individually decoupled.
- VCC0, VCC1, VCC2, and VCC3 should NOT be shorted together at the device pins.

XEU3 SKY85331-11

10	VDD	ANT	17
20	VCC3	C1	19
22	VCC2	C0	16
23	VCC1	TX_IN	2
24	VCC0	LNA_OUT	12
15	RX_OUT	GND1 GND3 GND7 GND9 GND11 GND14 GND18 GND21 PAD	1 3 7 9 11 14 18 21 25
13	LNA_IN		
4	PA_EN		
6	DET		
5	NU5		
8	NU8		

(AX)SKY85331-11

PA_2G2 — XC50 (AX)0.1uF/16V/0402 — GND

XC49 (AX)0.1uF/16V/0402 — XC55 (AX)0.1uF/16V/0402 — XC54 (AX)0.1uF/16V/0402 — XC60 (AX)0.1uF/16V/0402

BPF_2A2 50 ohm — BPF_2B2 50 ohm — 2G_PE2

Close to XEU1

[17] TSSI2_2 — XR52 (AX)0R/0201/5% — XR50 (AX)0R/0201/5% — XR51 NULL/0R/0201/5% — XC56 NULL/10pF/25V/0201/2%

XR85 is designed for RTC7647

XC44 NULL/10pF/25V/0201/2% — XC42 NULL/10pF/25V/0201/2% — XC43 (AX)10pF/25V/0201/2% — 50 ohm — 2G_ANT2

2G_CR2 — 2G_LNA2

Layout Notice :
- Control Pin C0, C1 should be shielded by GND with more Vias.

XC61 (AX)10pF/25V/0201/2% — 50 ohm — 2G_TX2 — 2G_TX2 [17]

XC62 NULL/10pF/25V/0201/2% — XL12 NULL/0R/0201/5% — XL13 NULL/0R/0201/5% — XC67 NULL/10pF/25V/0201/2% — XC68 NULL/10pF/25V/0201/2%

BPF (2400-2500MHz)

XC45 (AX)10pF/25V/0201/2% — XU10 IN / OUT / GND2 / GND4 — 2G_RX2 — 2G_RX2 [17]

NULL/(AX)BPF_2G BF2012-L2R4NAR

XR42 0R/0201/5%

ACX 2G BPF (XU32) :
Insertion Loss: 0.9 dB max. (25C)
Insertion Loss: 1.1 dB max. (-40C~85C)

Close to XEU3

Co-Layout — BPF_2A2 — XR40 NULL/0R/0201/5% — XR139 (AX_LTE)1.5nH — XL27 NULL/0.5pF/50V/0201

Co-Layout — XR138 NULL/0R/0201/5% — XR140 (AX_LTE)0R/0201/5% — BPF_2B2 — XL28 (AX)0.5pF/50V/0201

XU21 In / GND / GND / Out — XL29 (AX_LTE)5.1nH — XL30 NULL/10nH/0.25A/0201/3% — (AX_LTE)SAW_SF14112442A01T

Walsin SAW Filter (XU21) :
Insertion Loss: 2.9 dB 20x. @ 2400 ~ 2484 MHz
Pin : 28 dBm @ 2400 ~ 2484 MHz, 20MHz OFDM Signal

SAW (For LTE)

2G_CH2_5G_CH3_DIPLEXER

XU15

1	HI_FREQ	COMMON	5
3	LO_FREQ		
2 4 6	GND2 GND4 GND6		

(AX)DIPLEXER DP1608-A2455BKH0

XR71 (AX)4.7pF/0201

Close to XJ9

XL14 (AX)0R/0201/5% — 2G_5G_A2_IPX — XJ2 — (AX)IPEX_ANT2_XJ9

XC79 (AX)0.4pF/50V/0201 — XC86 NULL/2.2pF/50V/0201

To XJ10

2G_ANT2 — Co-Layout — XR37 (AX)0R/0201/5% — XR38 NULL/1.5nH — XL11 NULL/0.5pF/50V/0201

Co-Layout — XR36 (AX)0R/0201/5% — XR35 NULL/0R/0201/5% — XL10 (AX)0.5pF/50V/0201

[21] 5G_ANT3_DI — 5G_ANT3_DI — 50 ohm — XR34 (AX)0R/0201/5% — 50 ohm — XR68 (AX)0R/0201/5%

XU8 In / GND / GND / Out — XL8 NULL/5.1nH — XL9 NULL/10nH/0.25A/0201/3% — NULL/SAW_SF14112442A01T

Walsin SAW Filter (XU73) :
Insertion Loss: 2.2 dB typ. 2.9 dB max. @ 2400 ~ 2484 MHz (-30 ~ +85C)
Pin : 28 dBm @ 2400 ~ 2484 MHz

ACX 2G/5G Diplexer (XU7) :
2G Insertion Loss: 0.6 dB max.
5G Insertion Loss: 0.78 dB max.
2G Isolation: 38 dB min. @ 2400 ~ 2500 MHz
5G Isolation: 38 dB min. @ 4900 ~ 5950 MHz

<OrgName>	DrayTek		
Title	RF_2.4G_FEM_CH2		
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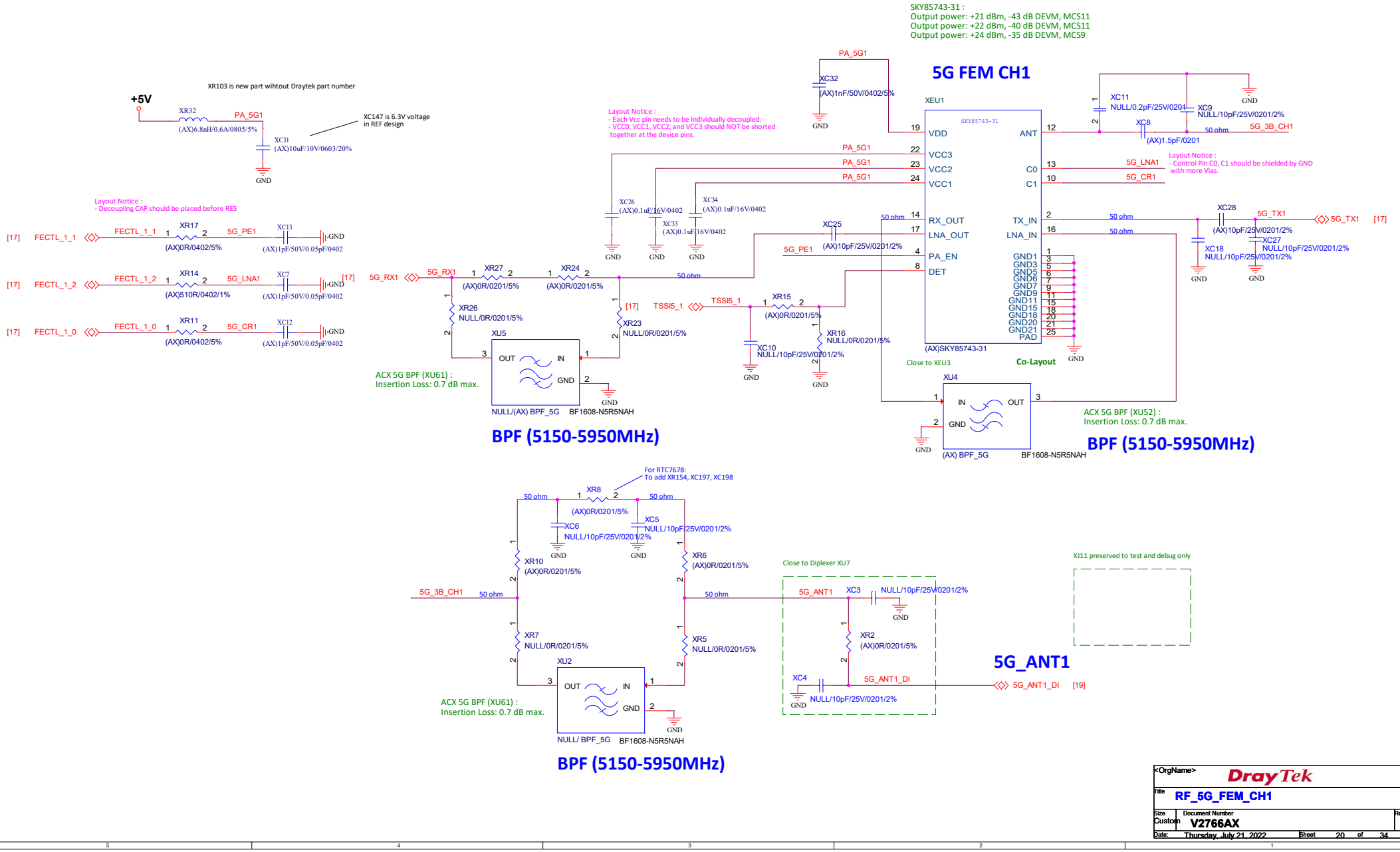
SKY85743-31 :
Output power: +21 dBm, -43 dB DEVM, MCS11
Output power: +22 dBm, -40 dB DEVM, MCS11
Output power: +24 dBm, -35 dB DEVM, MCS9
5G FEM CH1
XR103 is new part wihtout Draytek part number
+5V
XR32
(AX)6.8nH/0.6A/0805/5%
PA_5G1
XC31
(AX)10uF/10V/0603/20%
XC147 is 6.3V voltage in REF design
GND
Layout Notice :
- Decoupling CAP should be placed before RES
[17] FECTL_1_1
FECTL_1_1
XR17
(AX)0R/0402/5%
5G_PE1
XC13
(AX)1pF/50V/0.05pF/0402
[17] FECTL_1_2
FECTL_1_2
XR14
(AX)510R/0402/1%
5G_LNA1
XC7
(AX)1pF/50V/0.05pF/0402
[17] FECTL_1_0
FECTL_1_0
XR11
(AX)0R/0402/5%
5G_CR1
XC12
(AX)1pF/50V/0.05pF/0402
Layout Notice :
- Each Vcc pin needs to be individually decoupled.
- VCC0, VCC1, VCC2, and VCC3 should NOT be shorted together at the device pins.
XEU1
SKY85743-31
VDD
VCC3
VCC2
VCC1
RX_OUT
LNA_OUT
PA_EN
DET
ANT
C0
C1
TX_IN
LNA_IN
GND1 GND3 GND5 GND6 GND7 GND9 GND11 GND15 GND18 GND20 GND21 PAD
(AX)SKY85743-31
Co-Layout
XC32 (AX)1nF/50V/0402/5%
XC26 (AX)0.1uF/16V/0402
XC33 (AX)0.1uF/16V/0402
XC34 (AX)0.1uF/16V/0402
XC11 NULL/0.2pF/25V/0201
XC9 NULL/10pF/25V/0201/2%
XC8 (AX)1.5pF/0201
50 ohm
5G_3B_CH1
5G_LNA1
5G_CR1
Layout Notice :
- Control Pin C0, C1 should be shielded by GND with more Vias.
XC28 (AX)10pF/25V/0201/2%
XC27 NULL/10pF/25V/0201/2%
XC18 NULL/10pF/25V/0201/2%
5G_TX1
[17]
XC25 (AX)10pF/25V/0201/2%
5G_PE1
5G_RX1
XR27 (AX)0R/0201/5%
XR24 (AX)0R/0201/5%
XR26 NULL/0R/0201/5%
XR23 NULL/0R/0201/5%
XU5
OUT
IN
GND
ACX 5G BPF (XU61) :
Insertion Loss: 0.7 dB max.
NULL/(AX) BPF_5G
BF1608-N5R5NAH
BPF (5150-5950MHz)
TSSI5_1
XR15 (AX)0R/0201/5%
XR16 NULL/0R/0201/5%
XC10 NULL/10pF/25V/0201/2%
Close to XEU3
XU4
IN
OUT
GND
(AX) BPF_5G
BF1608-N5R5NAH
ACX 5G BPF (XU52) :
Insertion Loss: 0.7 dB max.
BPF (5150-5950MHz)
For RTC7678:
To add XR154, XC197, XC198
XR8 (AX)0R/0201/5%
XC6 NULL/10pF/25V/0201/2%
XC5 NULL/10pF/25V/0201/2%
XR10 (AX)0R/0201/5%
XR6 (AX)0R/0201/5%
XR7 NULL/0R/0201/5%
XR5 NULL/0R/0201/5%
XU2
ACX 5G BPF (XU61) :
Insertion Loss: 0.7 dB max.
NULL/ BPF_5G
BF1608-N5R5NAH
Close to Diplexer XU7
5G_ANT1
XC3 NULL/10pF/25V/0201/2%
XR2 (AX)0R/0201/5%
XC4 NULL/10pF/25V/0201/2%
5G_ANT1_DI
[19]
XJ11 preserved to test and debug only
5G_ANT1
<OrgName>
DrayTek
Title
RF_5G_FEM_CH1
Size
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SKY85743-31 :
Output power: +21 dBm, -43 dB DEVM, MCS11
Output power: +22 dBm, -40 dB DEVM, MCS11
Output power: +24 dBm, -35 dB DEVM, MCS9

XR119 is new part wihtout Draytek part number

+5V
XR84
(AX)6.8nH/0.6A/0805/5%
PA_5G3
XC94
(AX)10uF/10V/0603/20%
GND
XC147 is 6.3V voltage in REF design

Layout Notice :
- Decoupling CAP should be placed before RES

[17] FECTL_3_1 FECTL_3_1 XR69 (AX)0R/0402/5% 5G_PE3 XC71 (AX)1pF/50V/0.05pF/0402 GND
[17] FECTL_3_2 FECTL_3_2 XR81 (AX)510R/0402/1% 5G_LNA3 XC97 (AX)1pF/50V/0.05pF/0402 [17]
[17] FECTL_3_0 FECTL_3_0 XR72 (AX)0R/0402/5% 5G_CR3 XC83 (AX)1pF/50V/0.05pF/0402 GND

5G FEM CH3

PA_5G3
XC91
(AX)1nF/50V/0402/5%
GND

Layout Notice :
- Each Vcc pin needs to be individually decoupled.
- VCC0, VCC1, VCC2, and VCC3 should NOT be shorted together at the device pins.

XEU4
SKY85743-31
19 VDD
22 VCC3
23 VCC2
24 VCC1
14 RX_OUT
17 LNA_OUT
4 PA_EN
8 DET
12 ANT
13 C0
10 C1
2 TX_IN
16 LNA_IN
GND1 GND3 GND5 GND6 GND7 GND9 GND11 GND15 GND18 GND20 GND21 PAD
(AX)SKY85743-31

XC90 NULL/3nH/0201
XC88 NULL/10pF/25V/0201/2%
XC89 (AX)1.5pF/50V/0201
50 ohm
5G_3B_CH3

5G_LNA3
5G_CR3
Layout Notice :
- Control Pin C0, C1 should be shielded by GND with more Vias.

XC77 (AX)0.1uF/16V/0402
XC84 (AX)0.1uF/16V/0402
XC78 (AX)0.1uF/16V/0402

XC93 (AX)10pF/25V/0201/2%
5G_PE3
50 ohm

XC73 (AX)10pF/25V/0201/2%
5G_TX3
5G_TX3 [17]
XC72 NULL/10pF/25V/0201/2%
XC74 NULL/10pF/25V/0201/2%

5G_RX3 5G_RX3 XR85 (AX)0R/0201/5% XR82 (AX)0R/0201/5%
XR86 NULL/0R/0201/5%
XR83 NULL/0R/0201/5%
[17] TSSI5_3 TSSI5_3 XR70 (AX)0R/0201/5%
XR73 NULL/0R/0201/5%
XC76 NULL/10pF/25V/0201/2%

XU18
OUT IN GND
NULL/(AX) BPF_5G BF1608-N5R5NAH

ACX 5G BPF (XU63) :
Insertion Loss: 0.7 dB max.

Close to XEU4
Co-Layout

XU17
IN OUT GND
(AX) BPF_5G BF1608-N5R5NAH

ACX 5G BPF (XU54) :
Insertion Loss: 0.7 dB max.

BPF (5150-5950MHz)

BPF (5150-5950MHz)

For RTC7678:
To add XR155, XC199, XC210

50 ohm XR77 (AX)0R/0201/5% 50 ohm
XC82 NULL/10pF/25V/0201/2%
XC81 NULL/10pF/25V/0201/2%
XR79 (AX)0R/0201/5%
XR76 (AX)0R/0201/5%
5G_3B_CH3 50 ohm 50 ohm
XR78 NULL/0R/0201/5%
XR75 NULL/0R/0201/5%

XU16
OUT IN GND
NULL/ BPF_5G BF1608-N5R5NAH

ACX 5G BPF (XU63) :
Insertion Loss: 0.7 dB max.

Close to Diplexer XU6
5G_ANT3 XC87 NULL/10pF/25V/0201/2%
XR74 (AX)0R/0201/5%
XC80 NULL/10pF/25V/0201/2%
5G_ANT3_DI
5G_ANT3_DI [19]

XJ12 preserved to test and debug only

5G_ANT3

<OrgName> DrayTek
Title RF_5G_FEM_CH3
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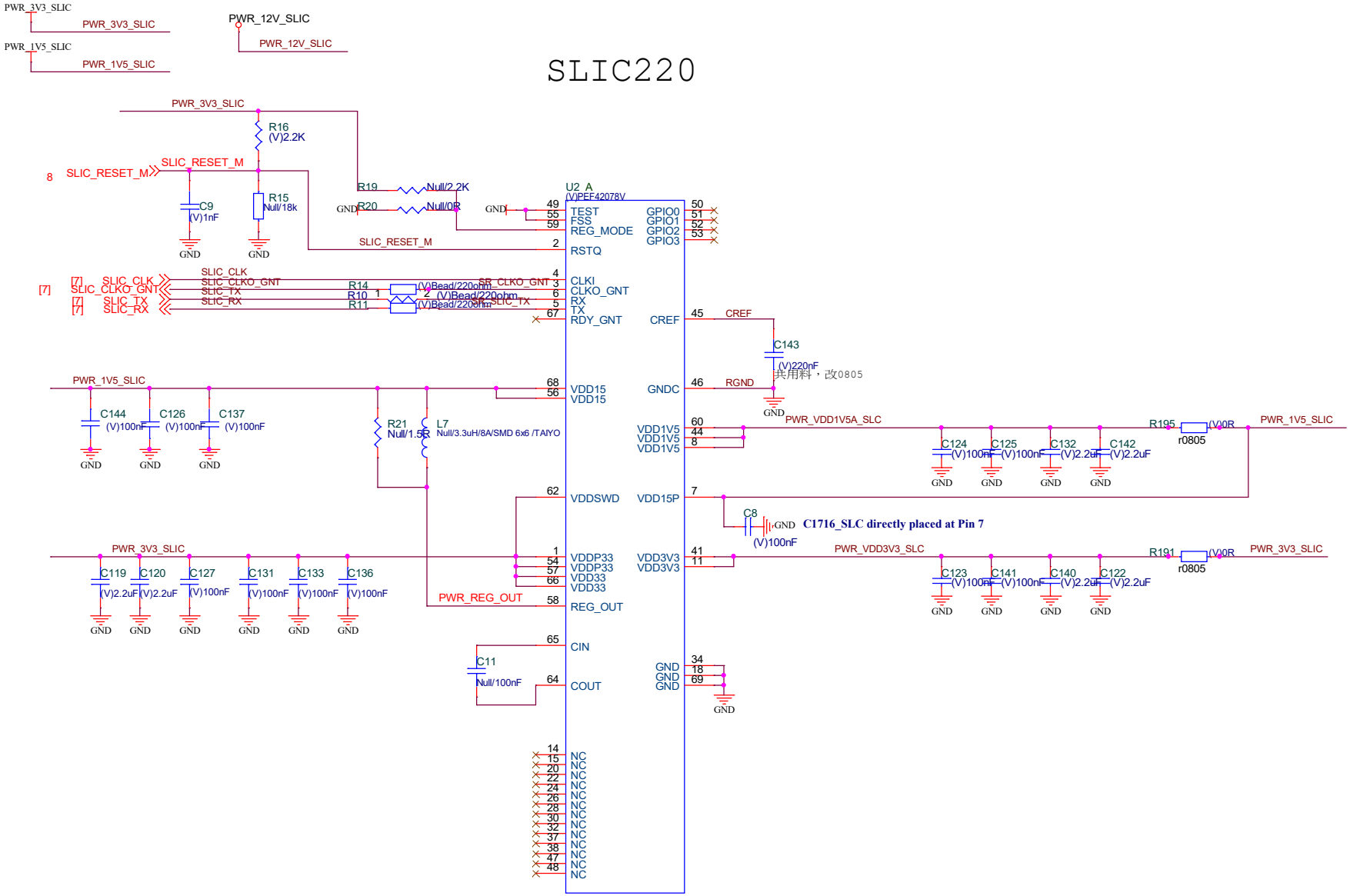

<OrgName>	DrayTek		
Title	XWAYSLIC220_DIGITAL		
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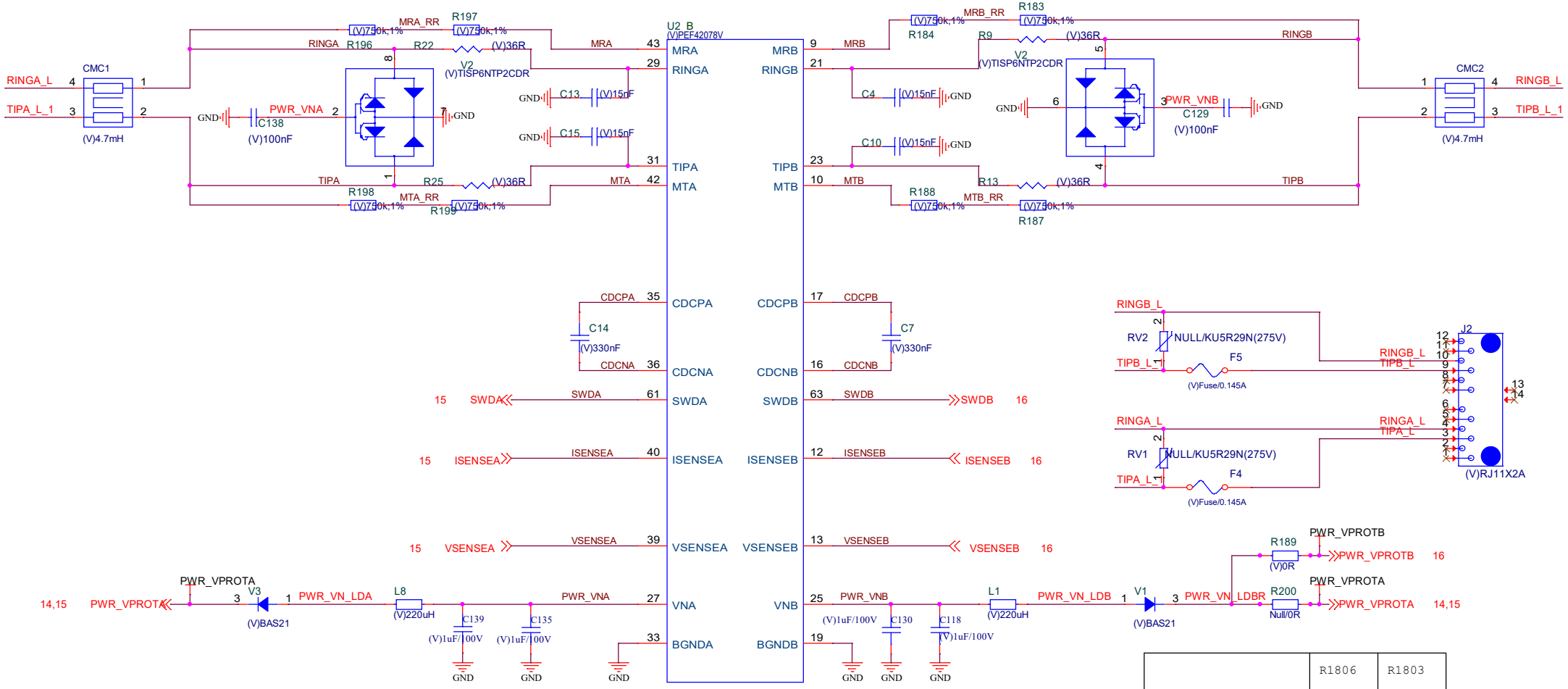
SLIC220



	R1806	R1803
Dedicated DCDC mode	Mounted	X
Combined DCDC mode	X	Mounted

<OrgName> DrayTek

Title: XWAYSLIC220_ANALOG

Size: Custom | Document Number: V2766AX | Rev: 6B

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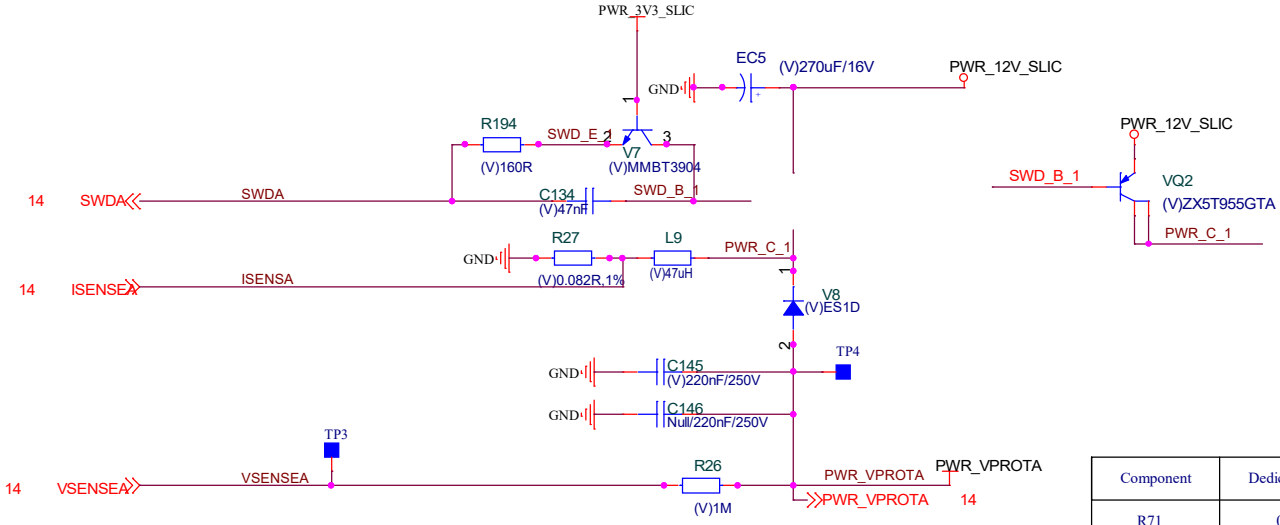
DCDC Type
Dedicated DCDC = T0.2
Combined DCDC = T1.1

Move radiating parts (like switching regulators and coils, voice SLIC/coils,) far away from DSL-AFE. A distance (at least 5cm) between the reiating part and the DSL must be maintain.



Component	Dedicated DCDC	Combined DCDC
R71	0.082R	0.068R
L7	47uH/1.8A	33uH/2.1A
C196	mount	X
C1805	X	mount

<OrgName> DrayTek

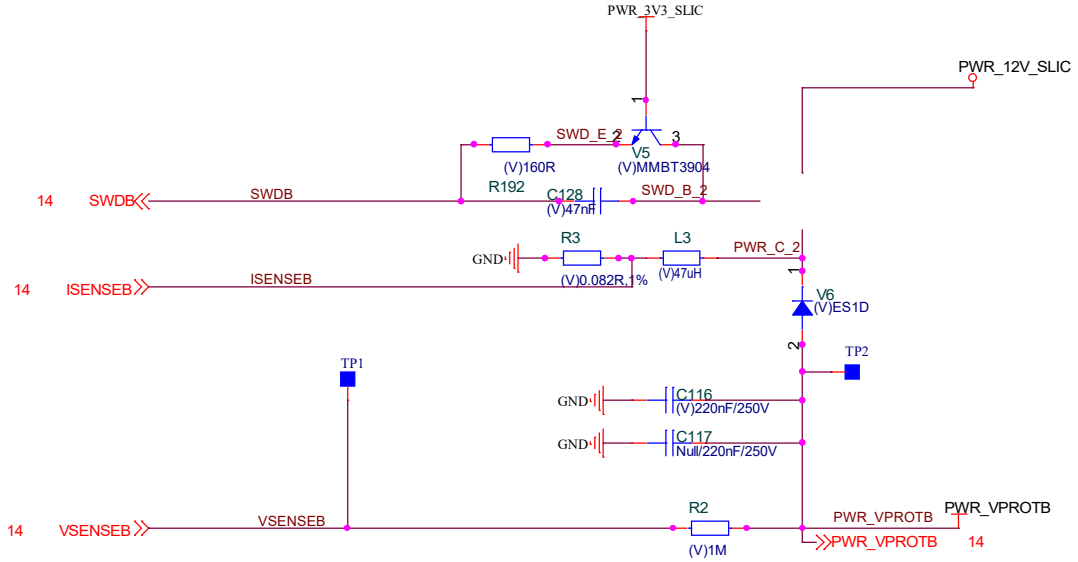
Title: U1_PNP_DCDC_T02_V11

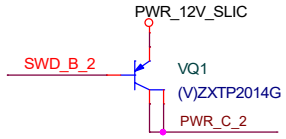
Size: Custom | Document Number: V2766AX | Rev: 6B

Date: Thursday, July 21, 2022 | Sheet 24 of 27

DCDC Type
Dedicated DCDC = T0.2
Combined DCDC = T1.1

Move radiating parts (like switching regulators and coils, voice SLIC/coils,) far away from DSL-AFE. A distance (at least 5cm) between the reiating part and the DSL must be maintain.





Component	Dedicated DCDC	Combined DCDC
R77	0.082R	0.068R
L9	47uH/1.8A	33uH/2.1A
C204	mount	X
C1806	X	mount

<OrgName> DrayTek

Title: U2_PNP_DCDC_T02_V11

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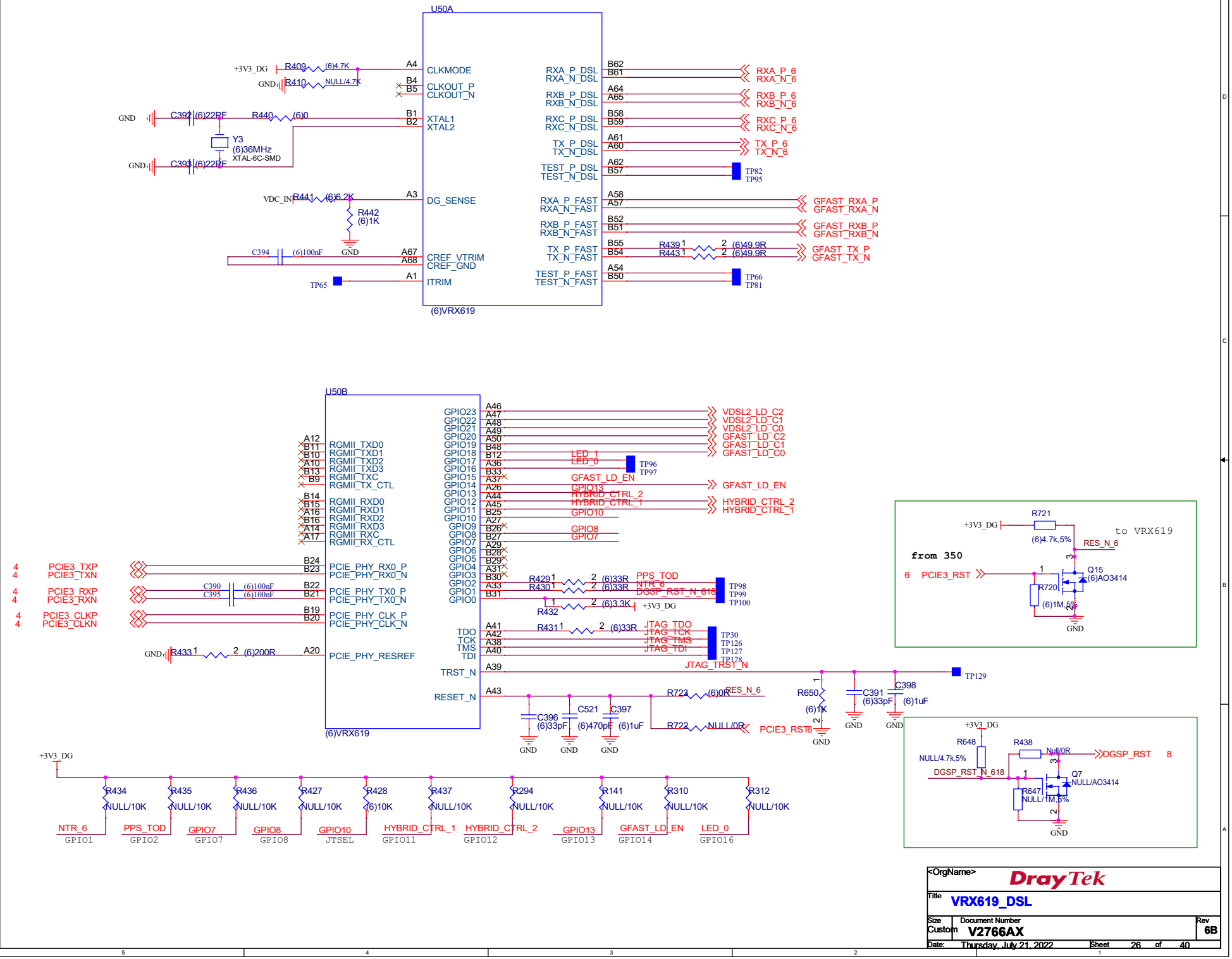
U50A
CLKMODE
CLKOUT_P
CLKOUT_N
XTAL1
XTAL2
DG_SENSE
CREF_VTRIM
CREF_GND
ITRIM
(6)VRX619
RXA_P_DSL
RXA_N_DSL
RXB_P_DSL
RXB_N_DSL
RXC_P_DSL
RXC_N_DSL
TX_P_DSL
TX_N_DSL
TEST_P_DSL
TEST_N_DSL
RXA_P_FAST
RXA_N_FAST
RXB_P_FAST
RXB_N_FAST
TX_P_FAST
TX_N_FAST
TEST_P_FAST
TEST_N_FAST
U50B
RGMII_TXD0
RGMII_TXD1
RGMII_TXD2
RGMII_TXD3
RGMII_TXC
RGMII_TX_CTL
RGMII_RXD0
RGMII_RXD1
RGMII_RXD2
RGMII_RXD3
RGMII_RXC
RGMII_RX_CTL
PCIE_PHY_RX0_P
PCIE_PHY_RX0_N
PCIE_PHY_TX0_P
PCIE_PHY_TX0_N
PCIE_PHY_CLK_P
PCIE_PHY_CLK_N
PCIE_PHY_RESREF
GPIO23
GPIO22
GPIO21
GPIO20
GPIO19
GPIO18
GPIO17
GPIO16
GPIO15
GPIO14
GPIO13
GPIO12
GPIO11
GPIO10
GPIO9
GPIO8
GPIO7
GPIO6
GPIO5
GPIO4
GPIO3
GPIO2
GPIO1
GPIO0
TDO
TCK
TMS
TDI
TRST_N
RESET_N
VDSL2_LD_C2
VDSL2_LD_C1
VDSL2_LD_C0
GFAST_LD_C2
GFAST_LD_C1
GFAST_LD_C0
GFAST_LD_EN
HYBRID_CTRL_2
HYBRID_CTRL_1
PPS_TOD
NTR_6
DGSP_RST_N_618
JTAG_TDO
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TRST_N
RES_N_6
PCIE3_RST
to VRX619
from 350
Q15
(6)AO3414
Q7
NULL/AO3414
DGSP_RST
NTR_6
PPS_TOD
GPIO7
GPIO8
GPIO10
HYBRID_CTRL_1
HYBRID_CTRL_2
GPIO13
GFAST_LD_EN
LED_0
GPIO1
GPIO2
GPIO7
GPIO8
JTSEL
GPIO11
GPIO12
GPIO13
GPIO14
GPIO16
<OrgName>
DrayTek
Title
VRX619_DSL
Size
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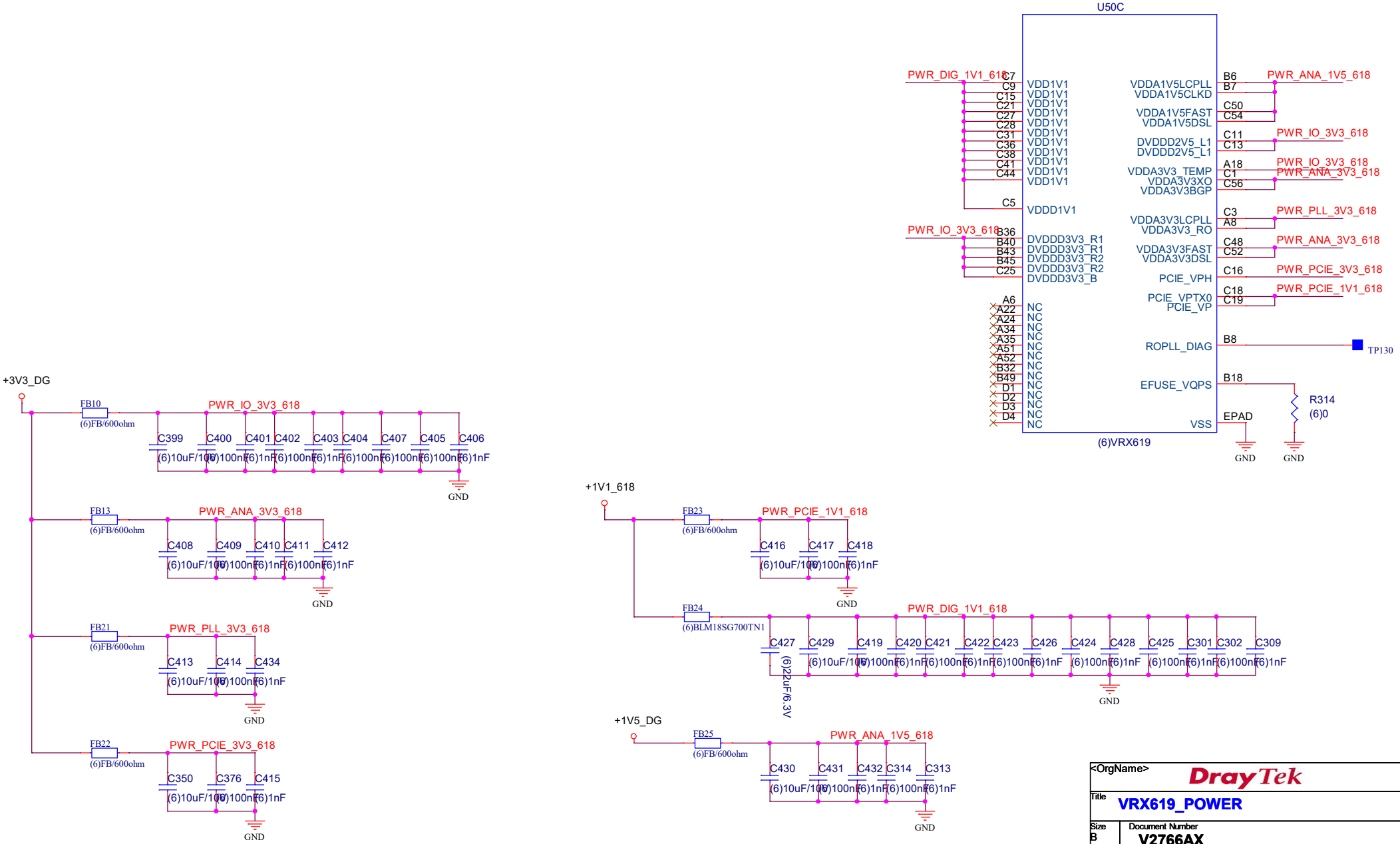

<OrgName>	DrayTek	
Title	VRX619_POWER	
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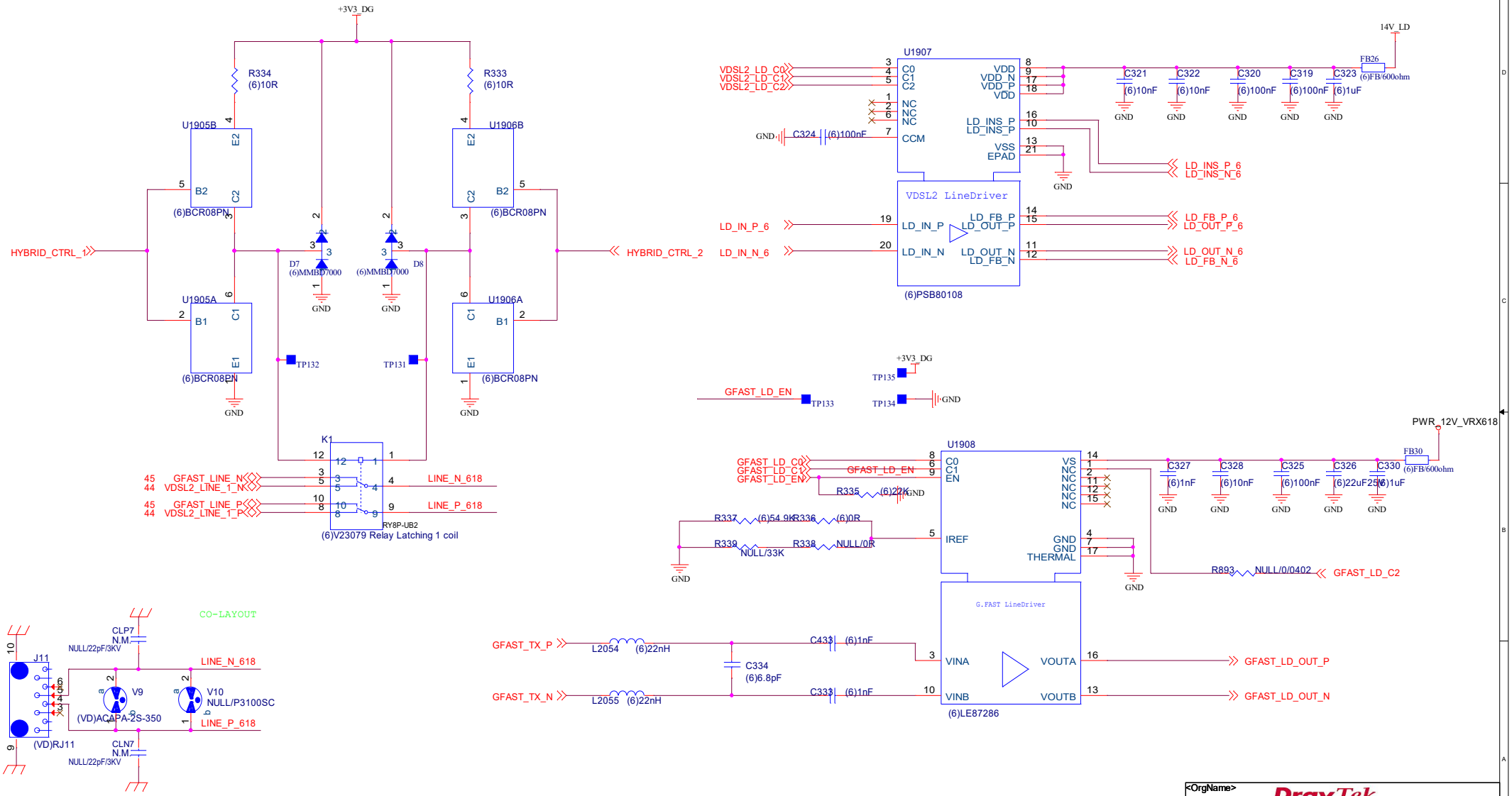

<OrgName> DrayTek

Title: VRX619_Relay_Line driver

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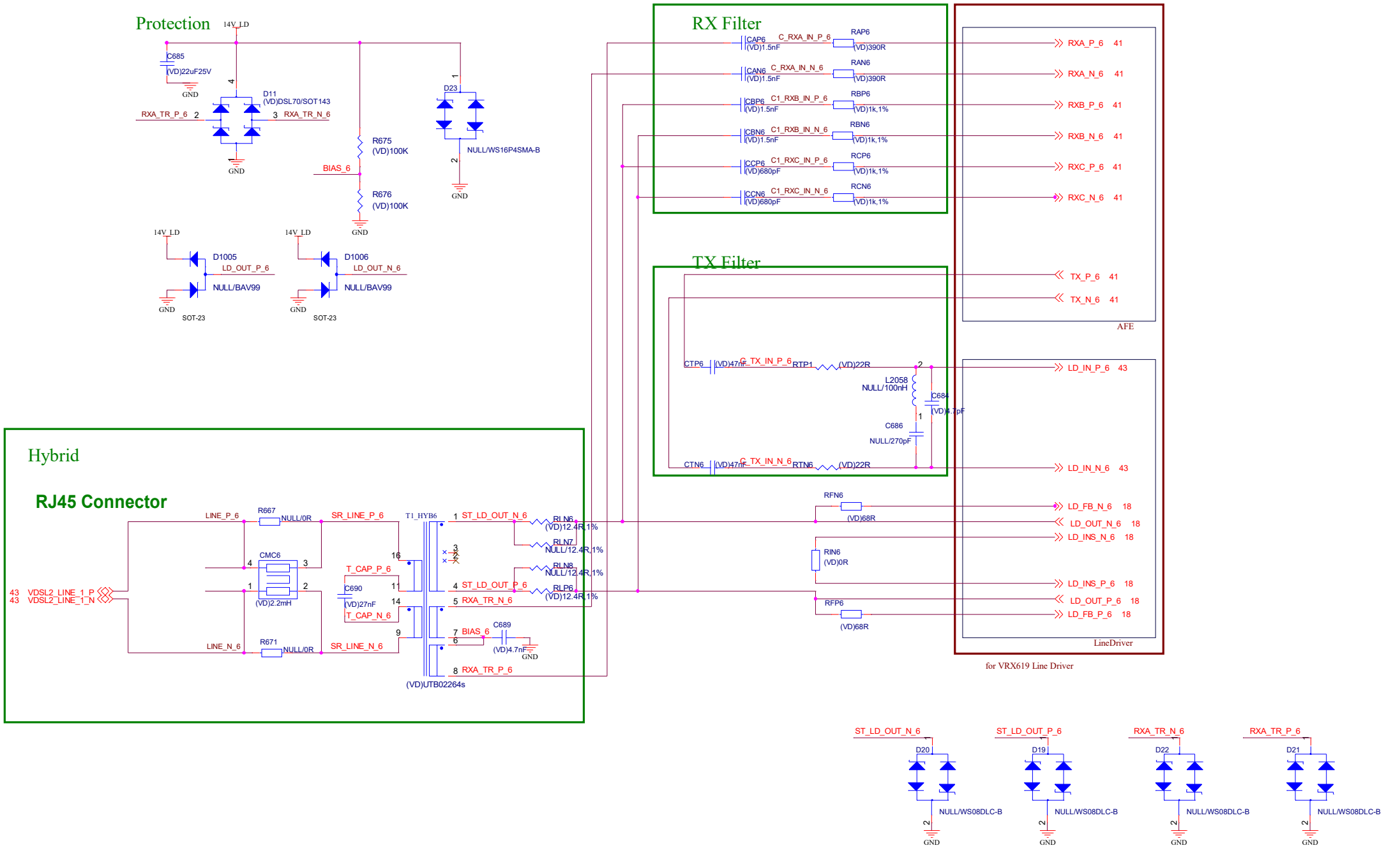
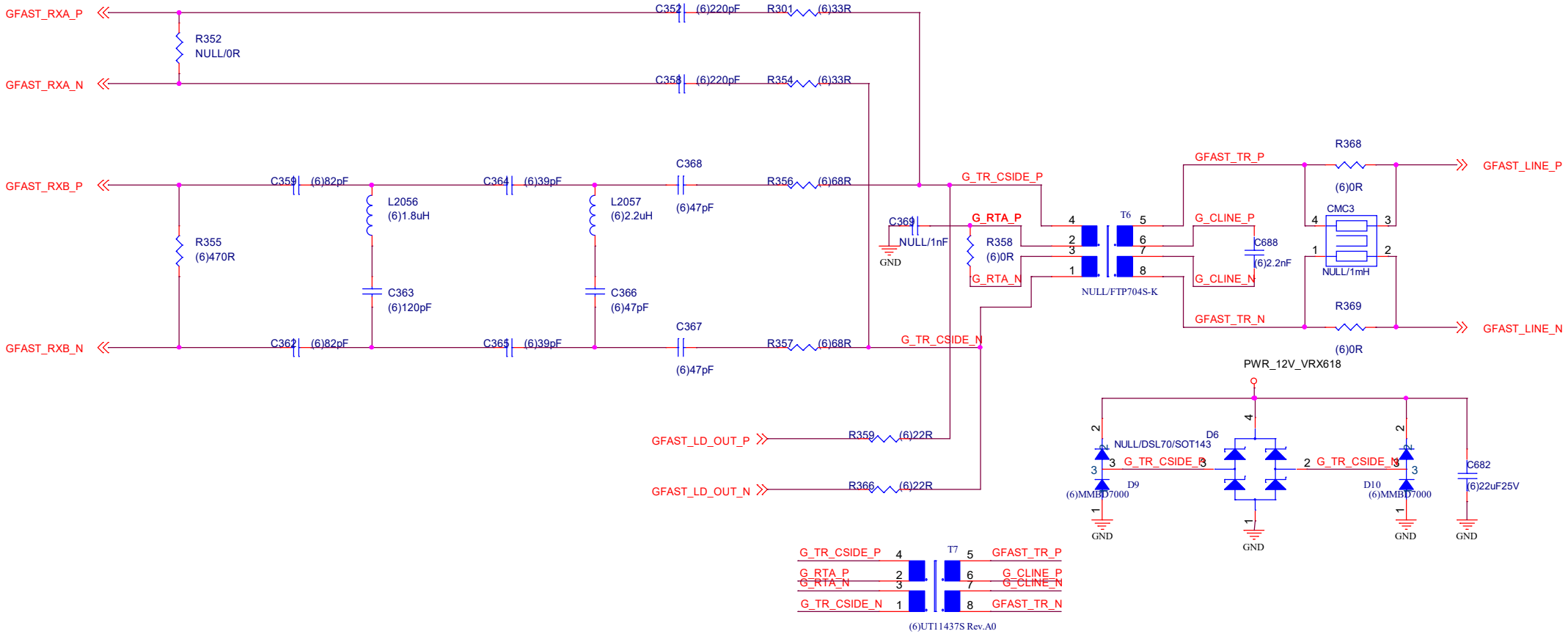


<OrgName>	DrayTek		
Title	VRX619_VDSL2_Hybrid		
Size: Custom	Document Number: V2766AX		Rev: 6B
Date: Thursday, July 21, 2022	Sheet 29 of 40		



<OrgName>	DrayTek		
Title	VRX619_GFAST_Hybrid		
Size: Custom	Document Number: V2766AX		Rev: 6B
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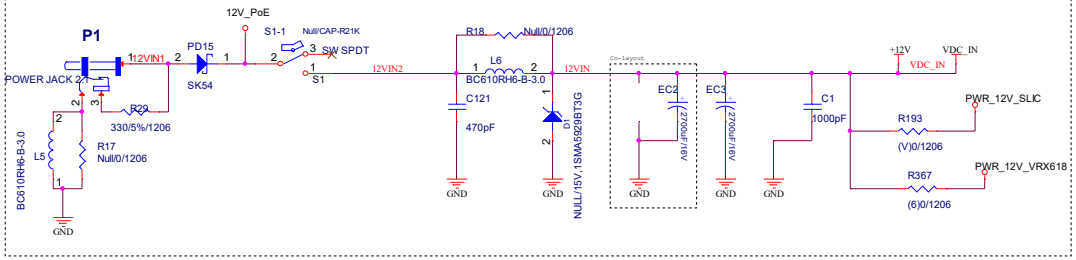
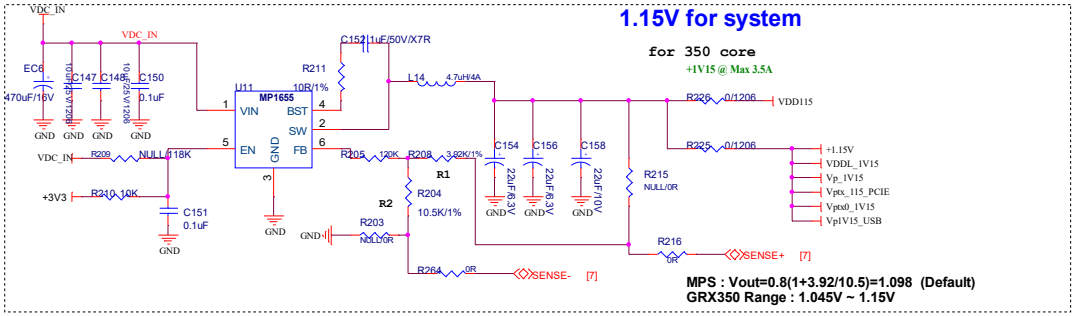
12V DC Power Input



1.15V for system

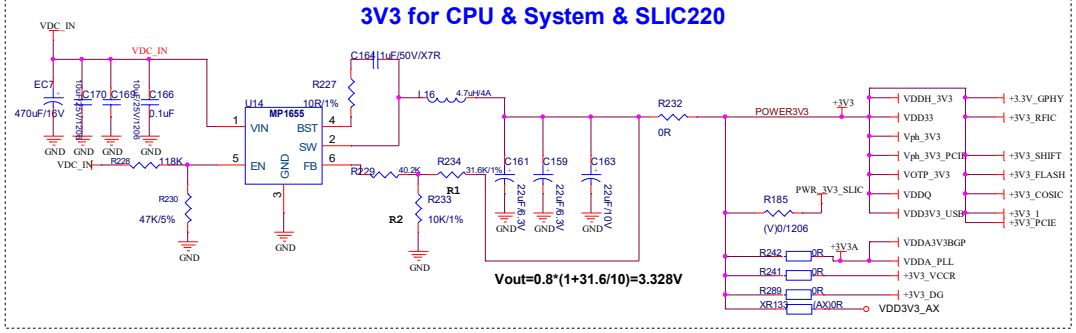
for 350 core

+1V15 @ Max 3.5A



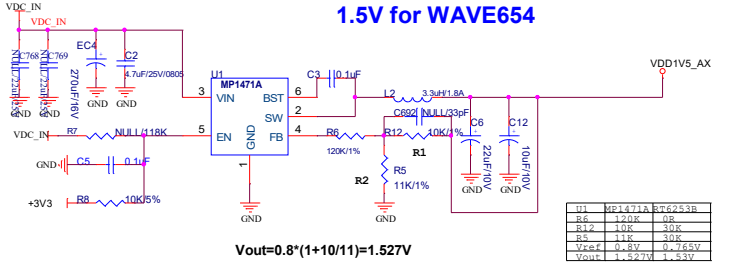
MPS : Vout=0.8(1+3.92/10.5)=1.098 (Default)
GRX350 Range : 1.045V ~ 1.15V

3V3 for CPU & System & SLIC220



Vout=0.8*(1+31.6/10)=3.328V

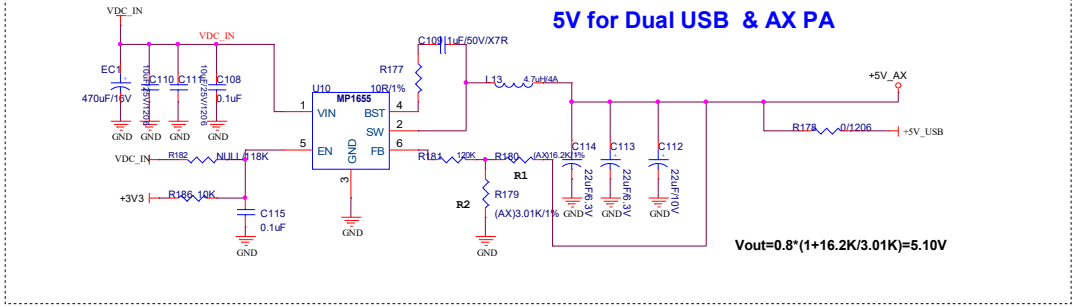
1.5V for WAVE654



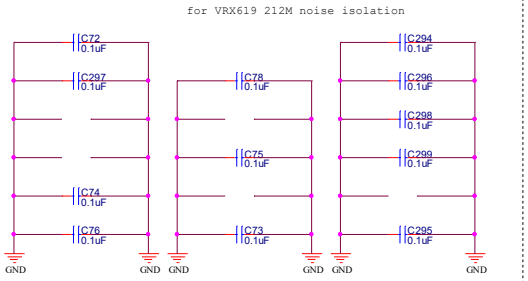
U1	MP1471A	RT6253B
R6	120K	0R
R12	10K	30K
R5	11K	30K
Vref	0.8V	0.765V
Vout	1.527V	1.53V

Vout=0.8*(1+10/11)=1.527V

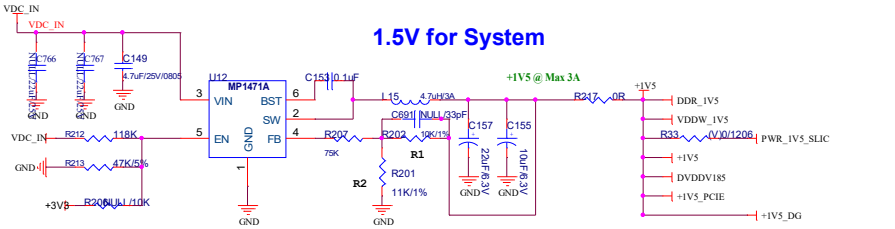
5V for Dual USB & AX PA



Vout=0.8*(1+16.2K/3.01K)=5.10V



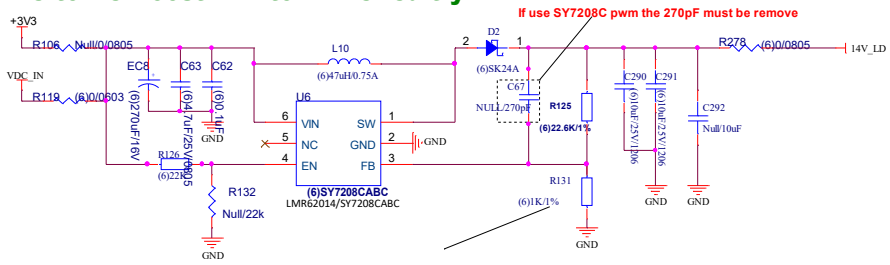
1.5V for System



U12	MP1471A	RT6253B
R207	75K	0R
R202	10K	30K
R201	11K	30K
Vref	0.8V	0.765V
Vout	1.527V	1.53V

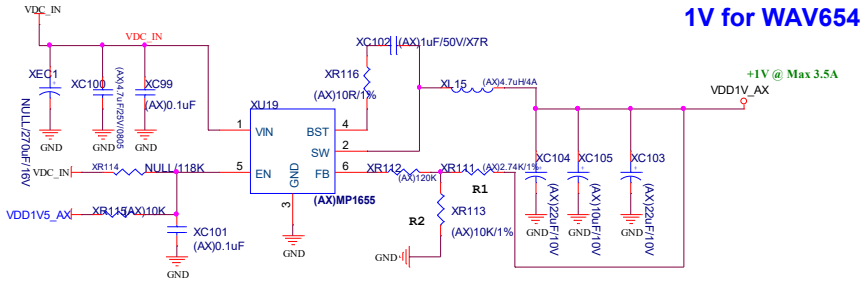
Vout=0.8(1+10/11)=1.527V

DC to DC Boost 12V to 14V circuitry



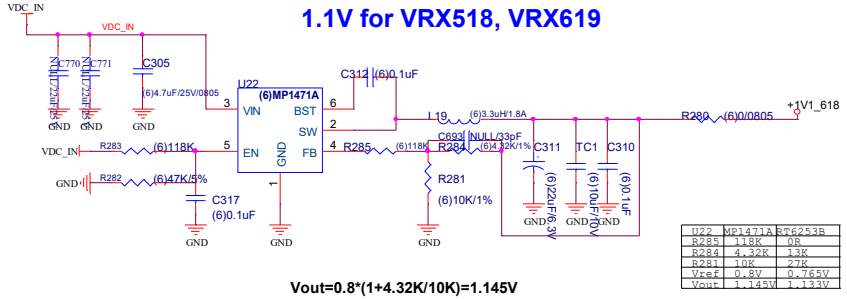
Silergy SY7208C Vout=0.6*(1+22.6/1)=14.16V

1V for WAV654



MPS : Vout=0.8(1+2.74/10)=1.0192 (Default)
WAV654 Range : 0.72V ~ 1.05V

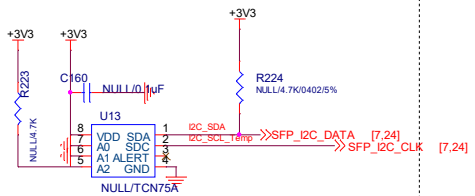
1.1V for VRX518, VRX619

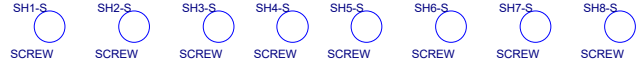


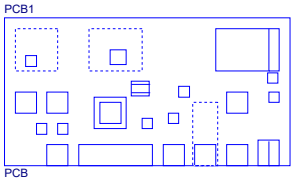
U22	MP1471A	RT6253B
R285	118K	0R
R284	4.32K	13K
R281	10K	27K
Vref	0.8V	0.765V
Vout	1.145V	1.133V

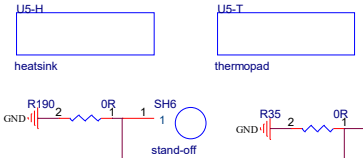
Vout=0.8*(1+4.32K/10K)=1.145V

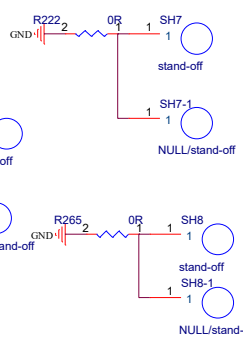
Temp sensor
I2C Addr:1001100

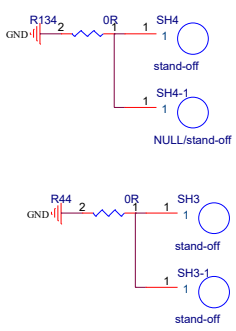


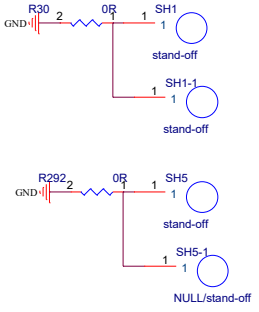


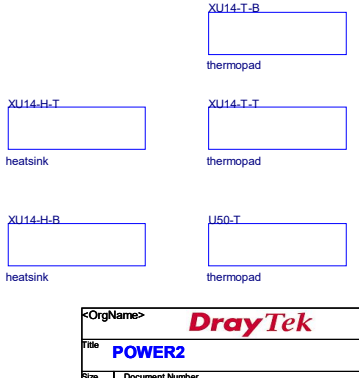












<OrgName>	DrayTek	
Title	POWER2	
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REVISION HISTORY

Version	Date	List of Modification	Page
	2020-12-01		Ian
V0A	2020-12-10	2.4GHz FEM (152-5331900-00G,SKY85331-11) : 1. Add XU31, XU33 2. Remove XC12, XC13, XC10, XC11 3. Null XR101, XR88, XU30, XU32 4. Place XR137, XR136 5. Remove XR146, XR149, XR142, XR145 5GHz FEM (152-5743900-00G,SKY85743-31) : 1. Add XU51, XU53 for co-layout with XU52, XU54 2. Remove XR117, XR113, XC16, XC17 3. Remove XR118, XR129, XC181, XC182 4. Place XR11, XR12 6. Null XU61, XR10, XR135 7. Place XR139, XR140 8. Null XU63, XR138, XR141	mChen
V6B	2021-5-28	1. Change VRX619 circuit 2. Add J9 3. colay internal PHY 4	Ian
V6C	2022-02-24	1.C326,C682,C685 colay C1206	Ian
V6D	2022-07-18	1.Add C766, C767, C691, C768, C769, C692, C770, C771, C693	Ian

<OrgName> DrayTek

Title History

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BOM Difference

	V2765ax	V2765Vax							
(VD)	V	V							
(V)	NULL	V							
(5)	V	V							
(PD)	NULL	NULL							
(AX)	V	V							
(NPD)	V	V							
(AX_LTE)	NULL	NULL							

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Title: BOM Difference

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