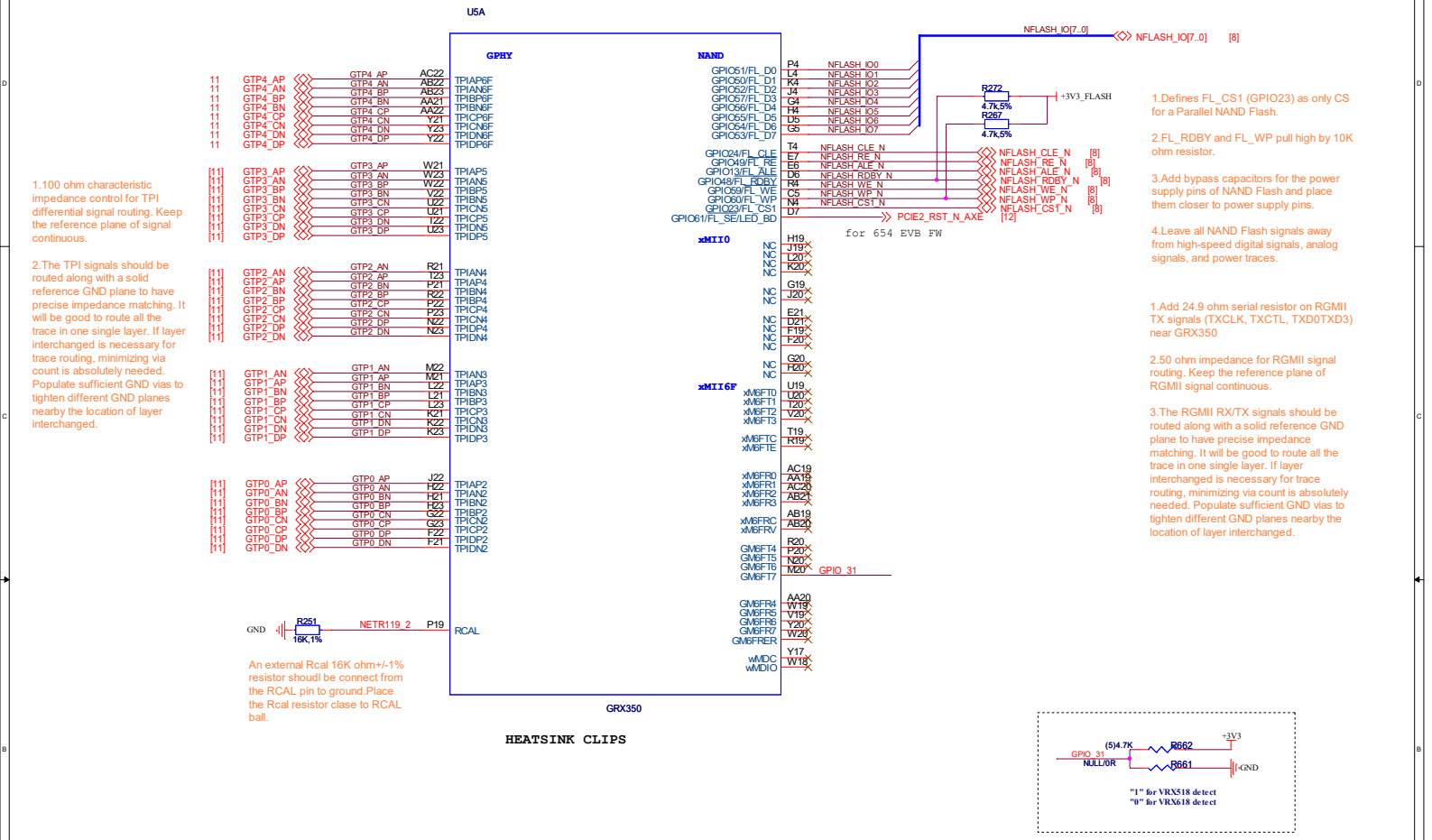


1.100 ohm characteristic impedance control for TPI differential signal routing. Keep the reference plane of signal continuous.

2.The TPI signals should be routed along with a solid reference GND plane to have precise impedance matching. It will be good to route all the trace in one single layer. If layer interchanged is necessary for trace routing, minimizing via count is absolutely needed. Populate sufficient GND vias to tighten different GND planes nearby the location of layer interchanged.

An external Rcal 16K ohm+/-1% resistor shoudl be connect from the RCAL pin to ground.Place the Rcal resistor clase to RCAL ball.

1.Defines FL_CS1 (GPIO23) as only CS for a Parallel NAND Flash.

2.FL_RDBY and FL_WP pull high by 10K ohm resistor.

3.Add bypass capacitors for the power supply pins of NAND Flash and place them closer to power supply pins.

4.Leave all NAND Flash signals away from high-speed digital signals, analog signals, and power traces.

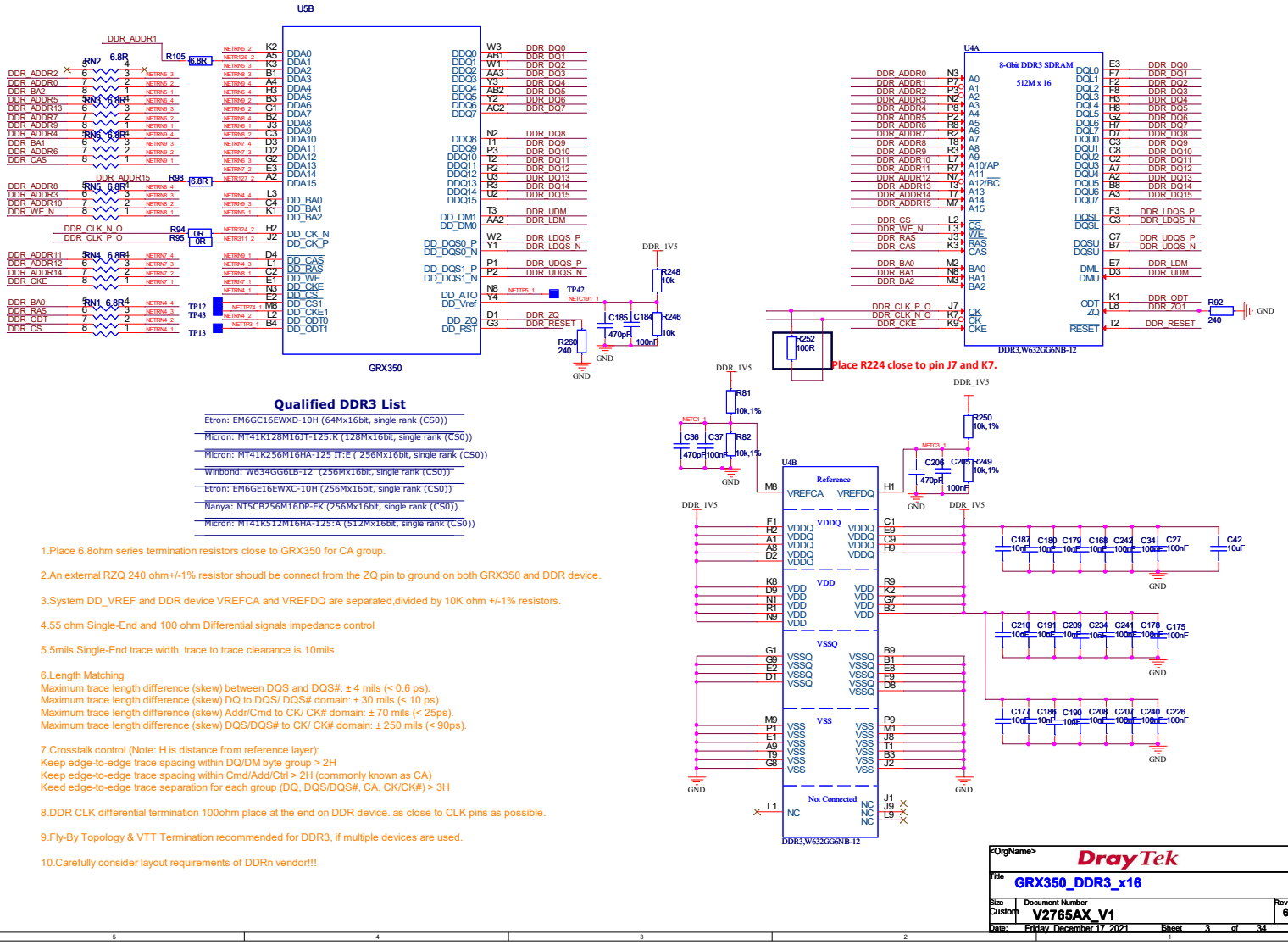
1.Add 24.9 ohm serial resistor on RGMII TX signals (TXCLK, TXCTL, TXD0TXD3) near GRX350

2.50 ohm impedance for RGMII signal routing. Keep the reference plane of RGMII signal continuous.

3.The RGMII RX/TX signals should be routed along with a solid reference GND plane to have precise impedance matching. It will be good to route all the trace in one single layer. If layer interchanged is necessary for trace routing, minimizing via count is absolutely needed. Populate sufficient GND vias to tighten different GND planes nearby the location of layer interchanged.

HEATSINK CLIPS

<OrgName>	DrayTek		
Title	GRX350_NAND_xMII_GPH		
Size: Custom	Document Number: V2765AX_V1		Rev: 6B
Date: Friday, December 17, 2021	Sheet 2 of 34		



1.Place 6.8ohm series termination resistors close to GRX350 for CA group.

2.An external RZQ 240 ohm+/-1% resistor shoudl be connect from the ZQ pin to ground on both GRX350 and DDR device.

3.System DD_VREF and DDR device VREFCA and VREFDQ are separated,divided by 10K ohm +/-1% resistors.

4.55 ohm Single-End and 100 ohm Differential signals impedance control

5.5mils Single-End trace width, trace to trace clearance is 10mils

6.Length Matching
Maximum trace length difference (skew) between DQS and DQS#: ± 4 mils (< 0.6 ps).
Maximum trace length difference (skew) DQ to DQS/ DQS# domain: ± 30 mils (< 10 ps).
Maximum trace length difference (skew) Addr/Cmd to CK/ CK# domain: ± 70 mils (< 25ps).
Maximum trace length difference (skew) DQS/DQS# to CK/ CK# domain: ± 250 mils (< 90ps).

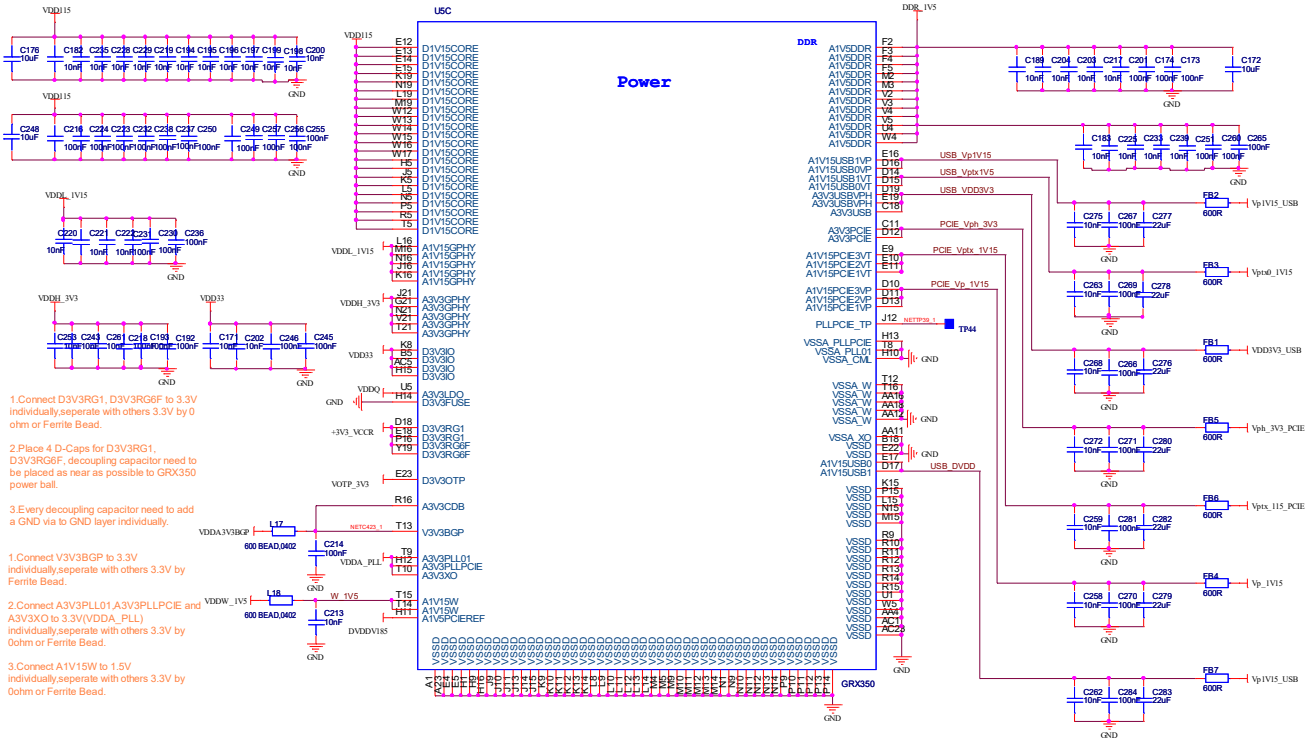
7.Crosstalk control (Note: H is distance from reference layer):
Keep edge-to-edge trace spacing within DQ/DM byte group > 2H
Keep edge-to-edge trace spacing within Cmd/Add/Ctrl > 2H (commonly known as CA)
Keed edge-to-edge trace separation for each group (DQ, DQS/DQS#, CA, CK/CK#) > 3H

8.DDR CLK differential termination 100ohm place at the end on DDR device. as close to CLK pins as possible.

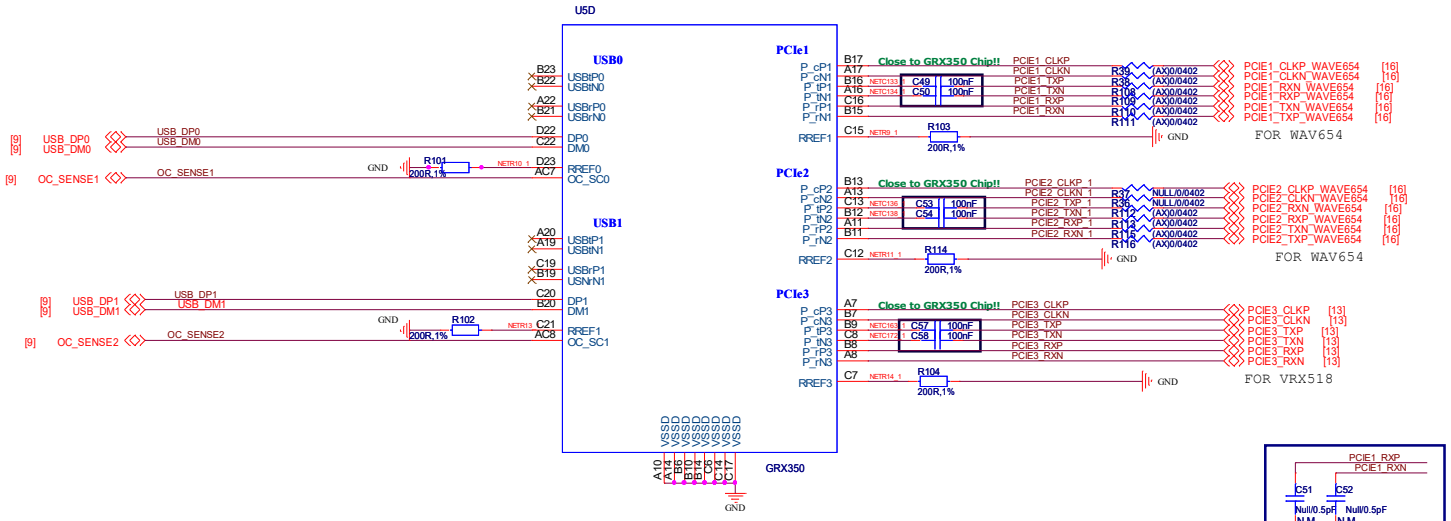
9.Fly-By Topology & VTT Termination recommended for DDR3, if multiple devices are used.

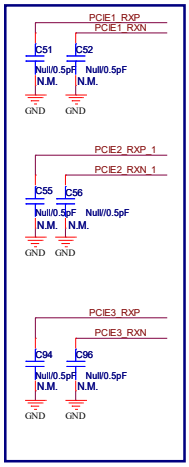
10.Carefully consider layout requirements of DDRn vendor!!!

<OrgName>	DrayTek	
Title	GRX350_DDR3_x16	
Size: Custom	Document Number: V2765AX_V1	Rev: 6B
Date: Friday, December 17, 2021	Sheet 3 of 34	



<OrgName>	DrayTek		
Title	GRX350_Power		
Size: Custom	Document Number: V2765AX_V1		Rev: 6B
Date: Friday, December 17, 2021	Sheet 4 of 34		





1.An external Rref 200 ohm+/-1% resistor should be connect from the USB RREF0, RREF1 pins to ground. Place the Rref resistor close to RREF balls.

2.Place 2 AC coupling capacitors on USB TX pairs , <0.5inch length to GRX350 is recommended.

3.90 ohm characteristic impedance control for USB differential signal routing. Keep the reference plane of signal continuous.

4. Match trace length of differential pairs (_p and _n signal) to given value in appropriate interface specification.

5. Populate sufficient GND vias nearby each PCIE differential pairs to tighten adjacent GND plane with GND layer.

1.An external Rref 200 ohm+/-1% resistor should be connect from the 3 PCIE RREF pins to ground. Place the Rref resistors close to RREF balls.

2.Place 2 AC coupling capacitors on PCIE TX pairs , <0.5inch length to GRX350 is recommended.

3.100 ohm characteristic impedance control for differential signal routing. Keep the reference plane of signal continuous.

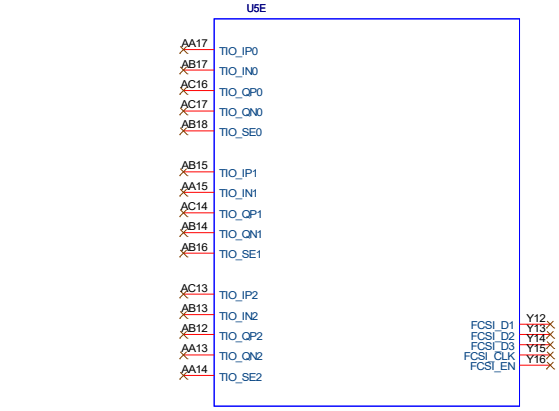
4.In case with >= 2 PCIe differential pairs routing on PCB, a footprint of shielding case to enclose all these differential pairs is highly recommended for the compliance of EN300-328 V1.8.1 standard.

5.0.5pF capacitors to ground on PCIE RX pairs, place them close to GRX350.

6. Match trace length of differential pairs (_p and _n signal) to given value in appropriate interface specification.

7. Populate sufficient GND vias nearby each PCIE differential pairs to tighten adjacent GND plane with GND layer.

<OrgName>	DrayTek	
Title	GRX350_PCIE_USB	
Size: Custom	Document Number: V2765AX_V1	Rev: 6B
Date: Friday, December 17, 2021	Sheet 5 of 34	



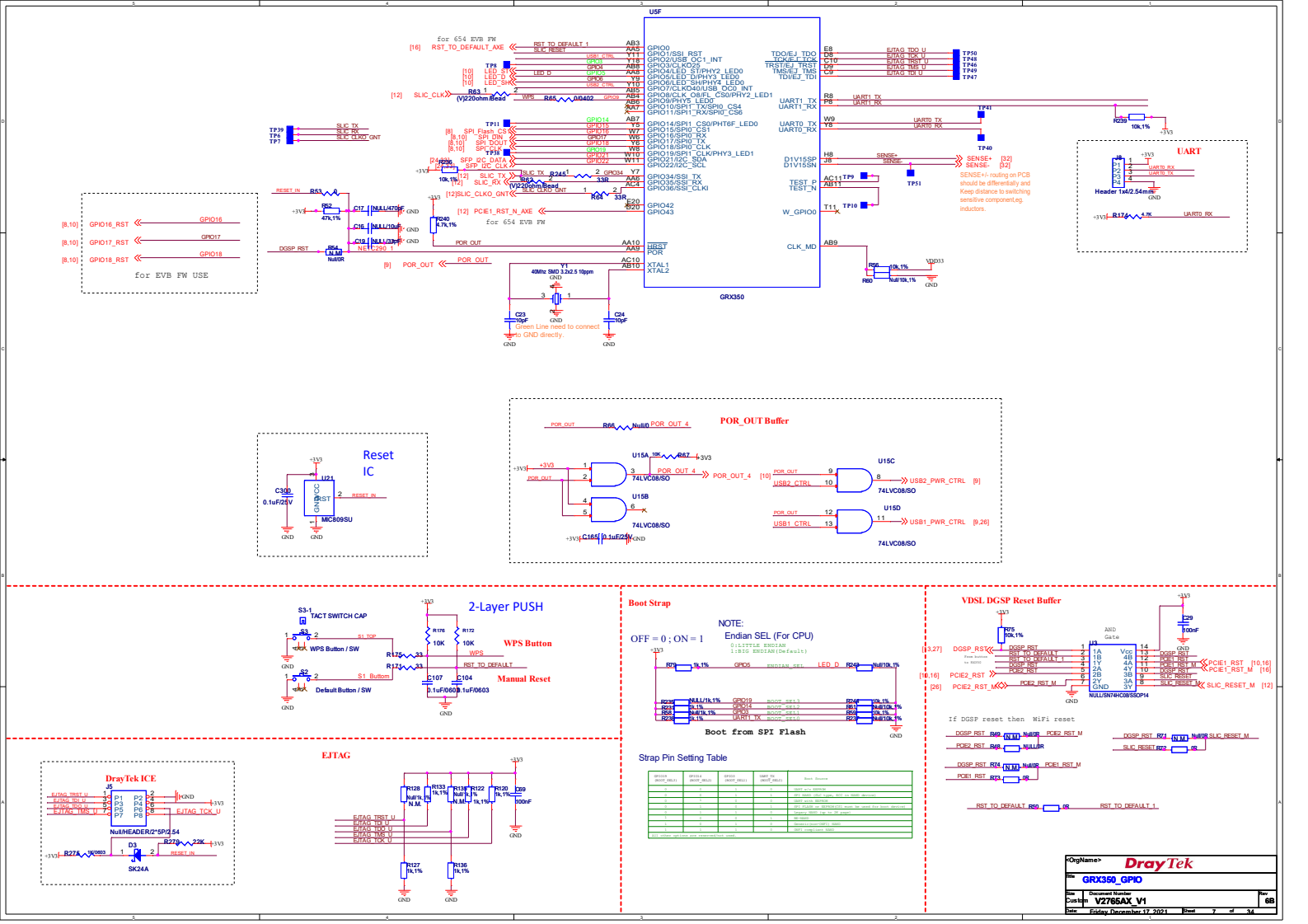
Trace capacitance for BBIO interface must be below 10pF! Recommend the maximum length should be under 3 inch.

<OrgName> DrayTek

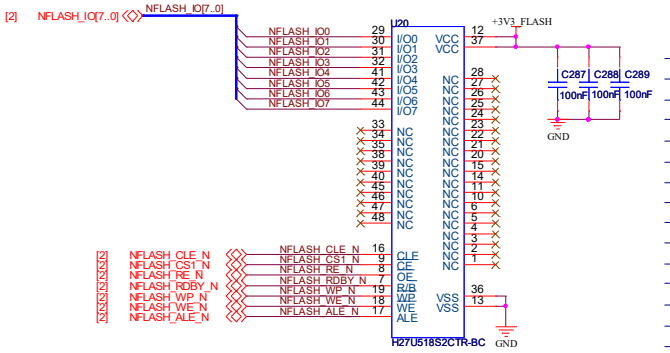
Title: GRX350_BBIO

Size: Custom | Document Number: V2765AX_V1 | Rev: 6B

Date: Friday, December 17, 2021 | Sheet 6 of 34

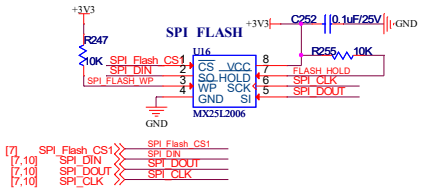


<OrgName>	DrayTek	
Title	GRX350_GPIO	
Size: Custom	Document Number: V2765AX_V1	Rev: 6B
Date: Friday, December 17, 2021	Sheet 7 of 34	



Qualified Nand Flash List

Vendor	Model
Hynix	H27uag8, 8k
Hynix	H27u512, 512
Hynix	H27u4g8f2dtr, 2k
Hynix	H27u1g8f2btf, 2k
Samsung	K9F1208, 512
Samsung	K9f1g08u0d, 2k
Samsung	K9g4g08u0b, 2k
Samsung	K9G8G08U0C, 8k
Spansion	S34ml01g100, 2k
Mircon	29f-4g08cbaba, 8k
Mircon	29f32g08cbaca, 4k
Infineon	Hyf33ds51280, 512
Toshiba	Th58BVG3S0HTA00, 4k



<OrgName> DrayTek

Title: NAND_FLASH

Size	Document Number	Rev
B	V2765AX_V1	6B

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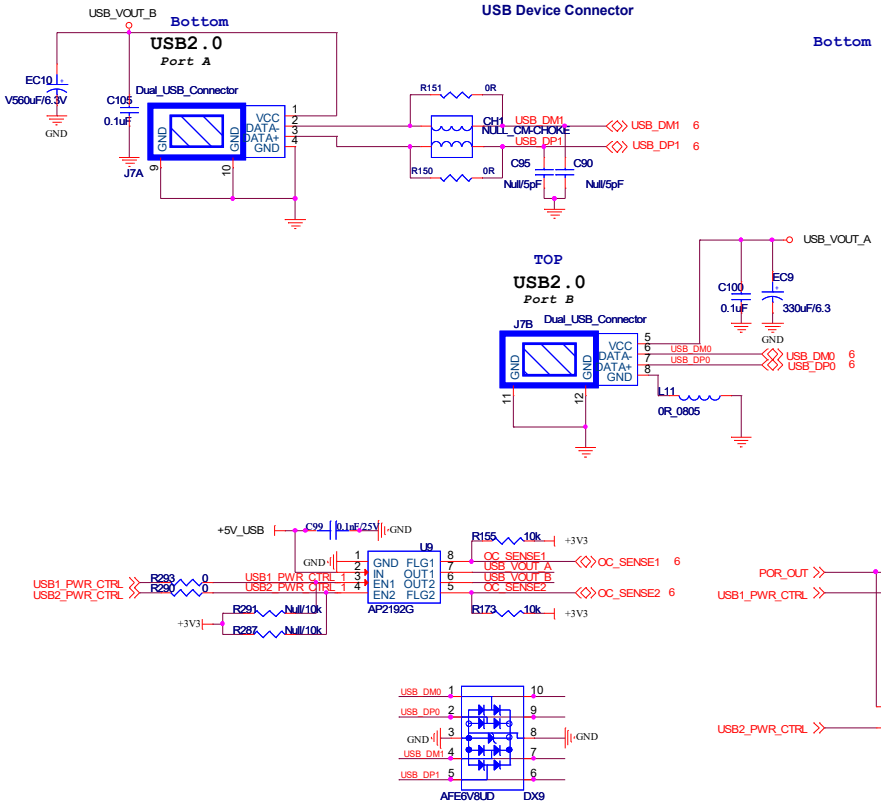
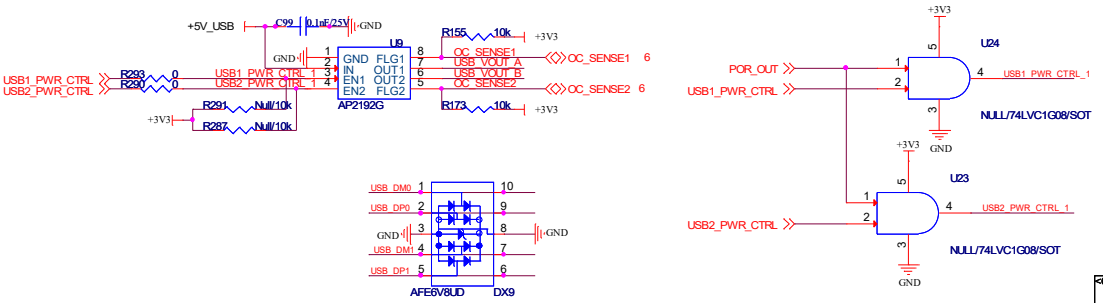
!!Note:
The PCB layout of the differential signal DP and DM should have 90 ohm differential impedance, and keep the trace length below 1 inch if possible.

TOP B
Bottom A

USB Device Connector



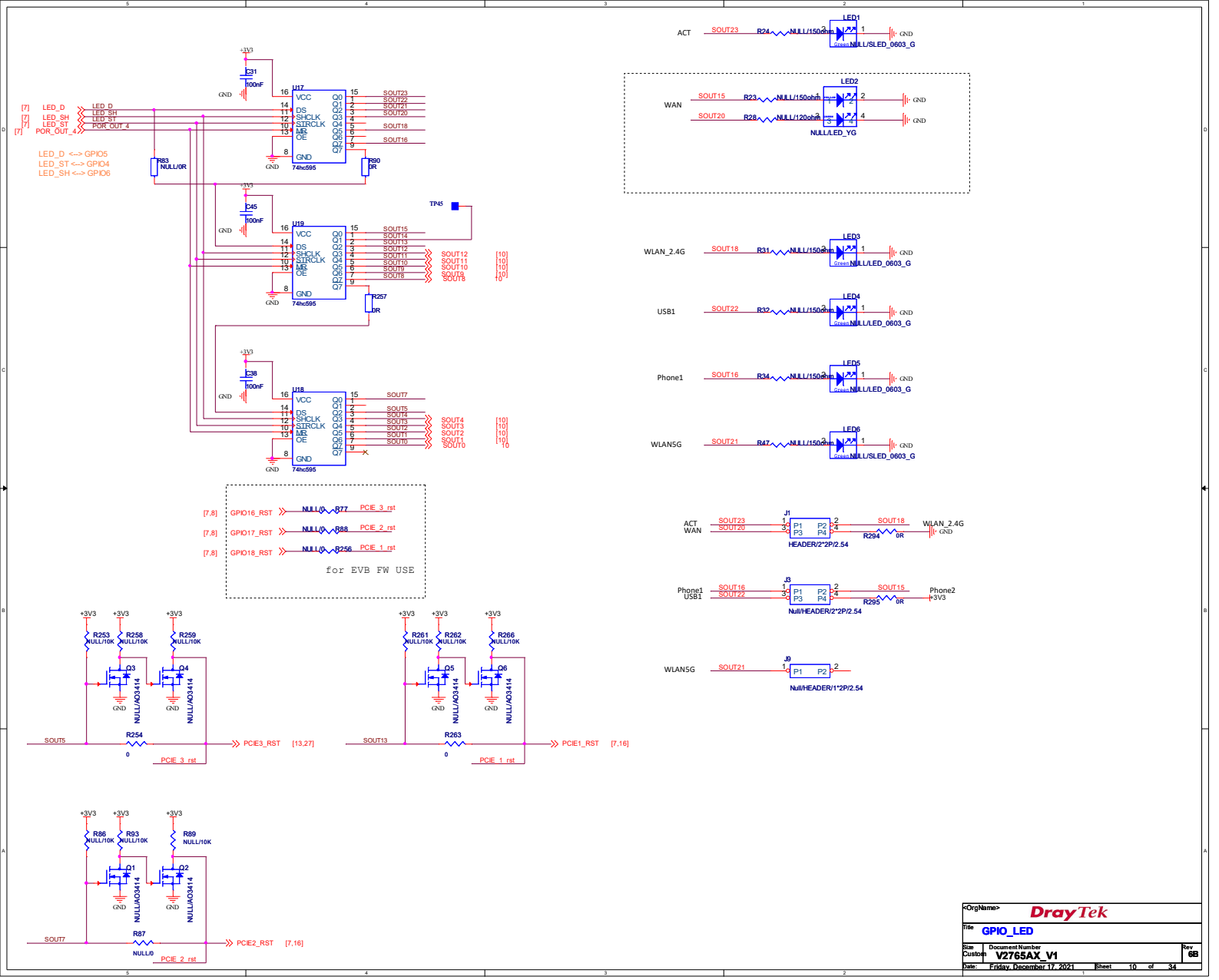


<OrgName> DrayTek

Title: USB_Port

Size: B | Document Number: V2765AX_V1 | Rev: 6B

Date: Friday, December 17, 2021 | Sheet 08 of 27



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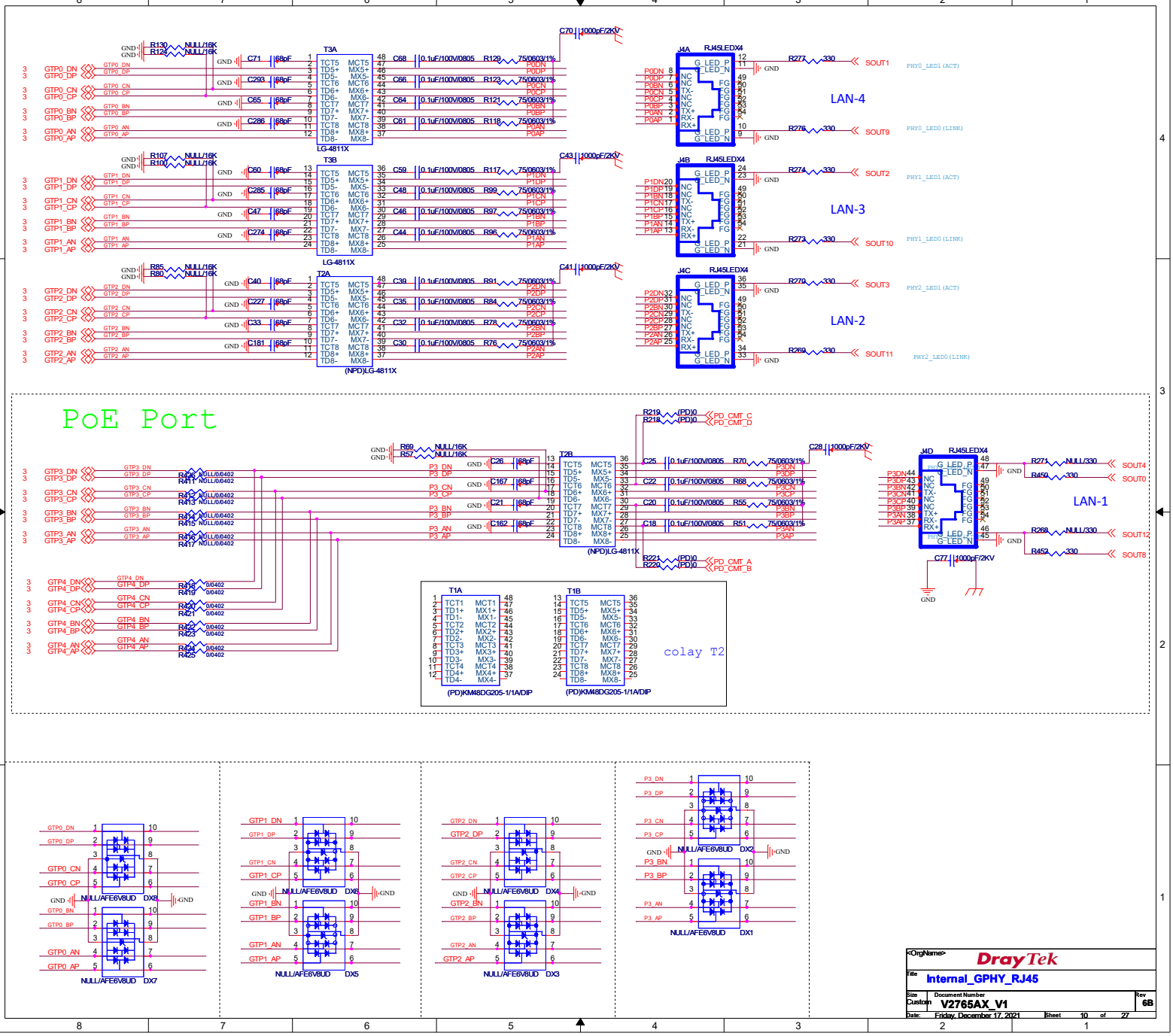
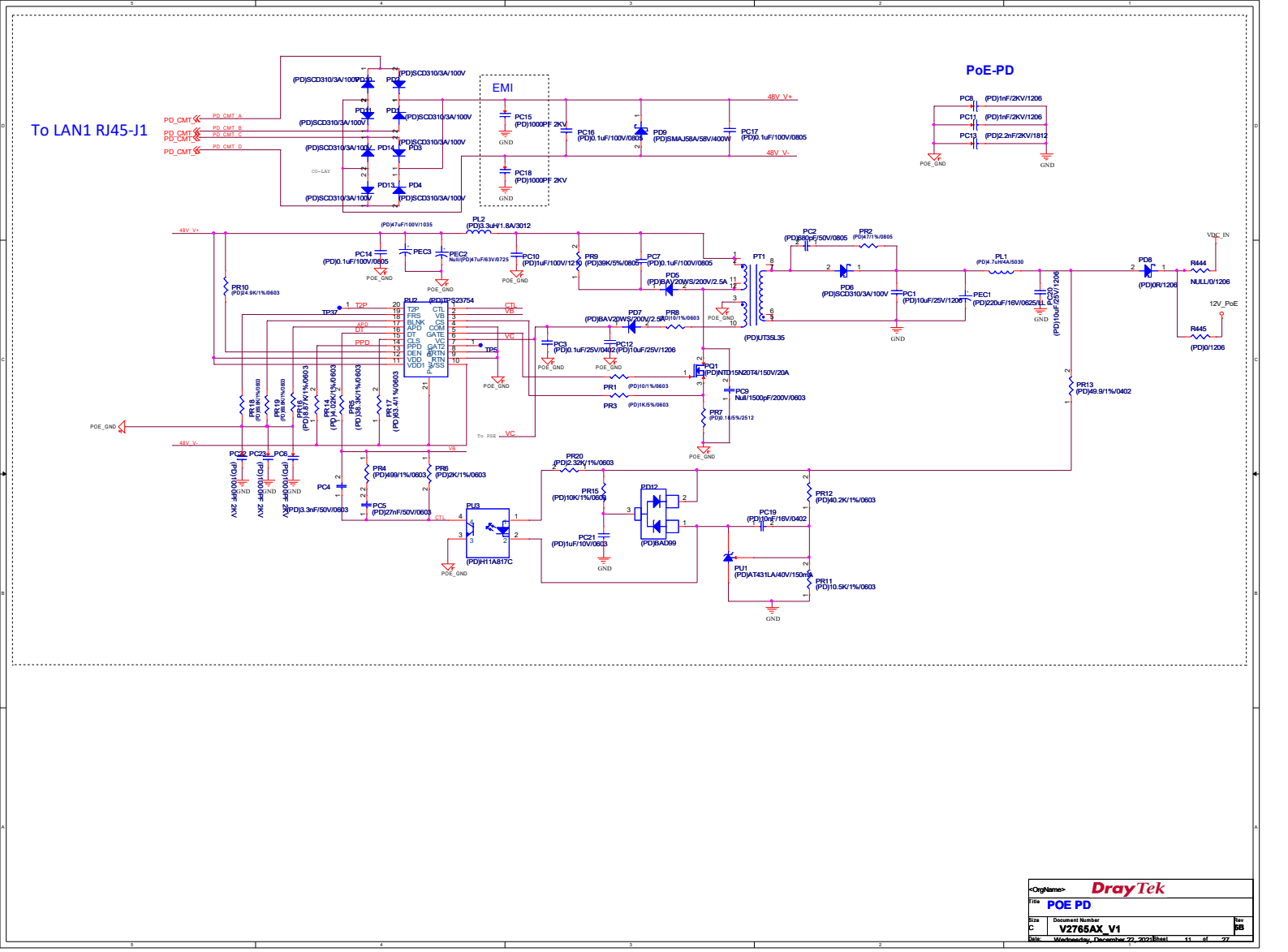
Title	GPIO_LED
Size: Custom	Document Number: V2765AX_V1
Rev	6B
Date: Friday, December 17, 2021	Sheet 10 of 34



<OrgName>	DrayTek
Title	Internal_GPHY_RJ45
Size / Document Number	Custom / V2765AX_V1
Rev	6B
Date: Friday, December 17, 2021	Sheet 10 of 27


To LAN1 RJ45-J1
PoE-PD
EMI
PD_CMT_A
PD_CMT_B
PD_CMT_C
PD_CMT_D
48V_V+
48V_V-
POE_GND
GND
VDC_IN
12V_PoE
TPS23754
PT1
PU1
PU3
PD12
PQ1
PL2
PL1
PC1
PC2
PC8
PC11
PC13
PC14
PC15
PC16
PC17
PC18
PC19
PC20
PC21
PC22
PC23
PC6
PEC1
PEC2
PEC3
PD1
PD2
PD3
PD4
PD5
PD6
PD7
PD8
PD9
PR1
PR2
PR3
PR4
PR5
PR6
PR7
PR8
PR9
PR10
PR11
PR12
PR13
PR14
PR15
PR16
PR17
PR18
PR19
PR20
R444
R445
TP37
T2P
APD
DT
PPD
VC
VB
CTL
TPS
To PSE
CO-LAY
(PD)SCD310/3A/100V
(PD)1nF/2KV/1206
(PD)2.2nF/2KV/1812
(PD)1000PF 2KV
(PD)0.1uF/100V/0805
(PD)SMAJ58A/58V/400W
(PD)0.1uF/100V/0805
(PD)47uF/100V/1035
(PD)3.3uH/1.8A/3012
(PD)0.1uF/100V/0805
(PD)1uF/100V/1210
(PD)39K/5%/0805
(PD)0.1uF/100V/0805
(PD)BAV20WS/200V/2.5A
(PD)BAV20WS/200V/2.5A
(PD)UT3SL35
(PD)68nF/50V/0805
(PD)47R/1%/0805
(PD)SCD310/3A/100V
(PD)10uF/25V/1206
(PD)x.7uH/4A/5030
(PD)220uF/16V/0625/LL
(PD)10uF/25V/1206
(PD)0R/1206
NULL/0/1206
(PD)0/1206
(PD)0.1uF/25V/0402
(PD)10uF/25V/1206
(PD)NTD15N20T4/150V/20A
Null/1500pF/200V/0603
(PD)10/1%/0603
(PD)1K/5%/0603
(PD)0.1R/5%/2512
(PD)49.9/1%/0402
(PD)2.32K/1%/0603
(PD)10K/1%/0603
(PD)1uF/10V/0603
(PD)BAD99
(PD)10nF/16V/0402
(PD)AT431LA/40V/150mA
(PD)10.5K/1%/0603
(PD)40.2K/1%/0603
(PD)H11A817C
(PD)24.9K/1%/0603
(PD)499/1%/0603
(PD)2K/1%/0603
(PD)3.3nF/50V/0603
(PD)4.02K/1%/0603
(PD)38.3K/1%/0603
(PD)8.41K/1%/0603
(PD)47K/1%/0603
(PD)100uF/100V
(PD)470uF/25V
(PD)470uF/16V
<OrgName>
DrayTek
Title
POE PD
Size
C
Document Number
V2765AX_V1
Rev
5B
Date:
Wednesday, December 22, 2021
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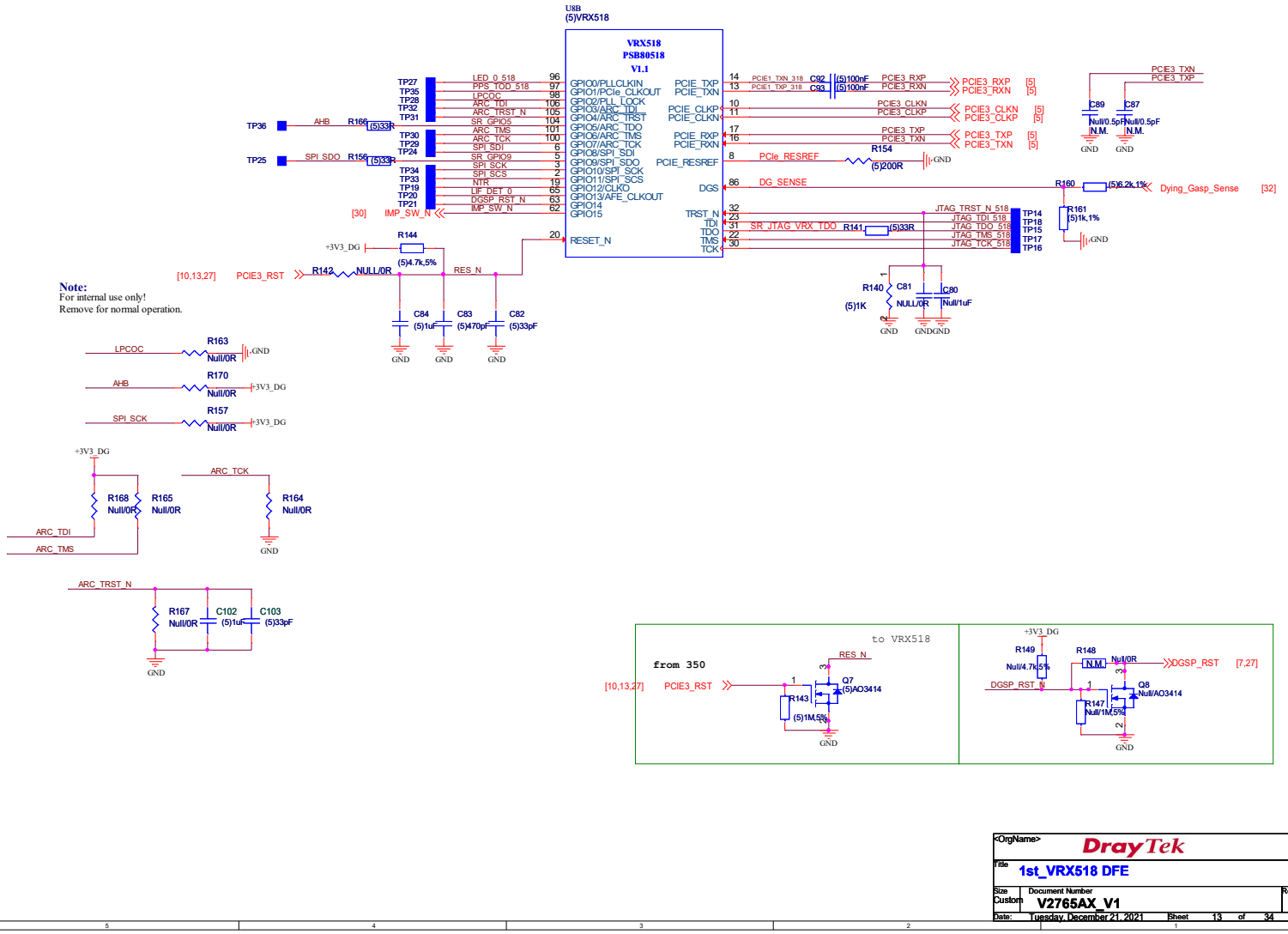
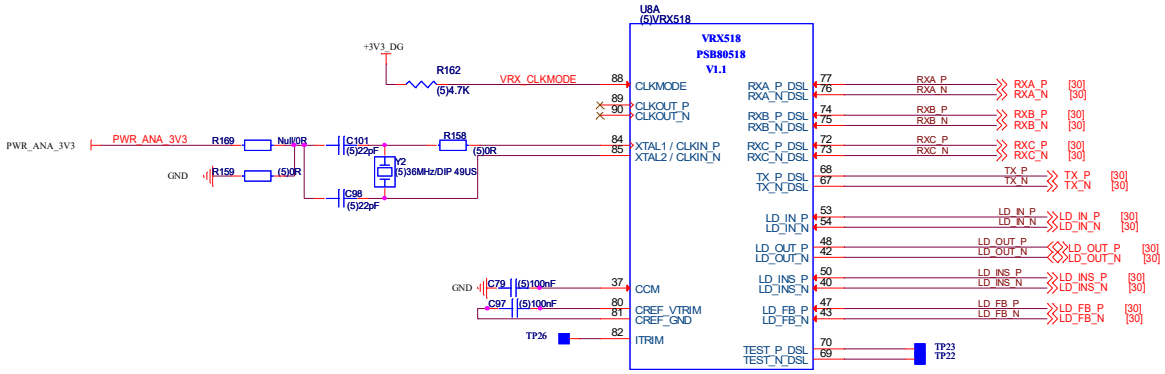


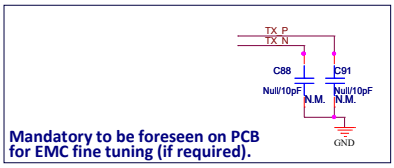
<OrgName> DrayTek

Title: 1st_VRX518 DFE

Size	Document Number	Rev
Custom	V2765AX_V1	6B

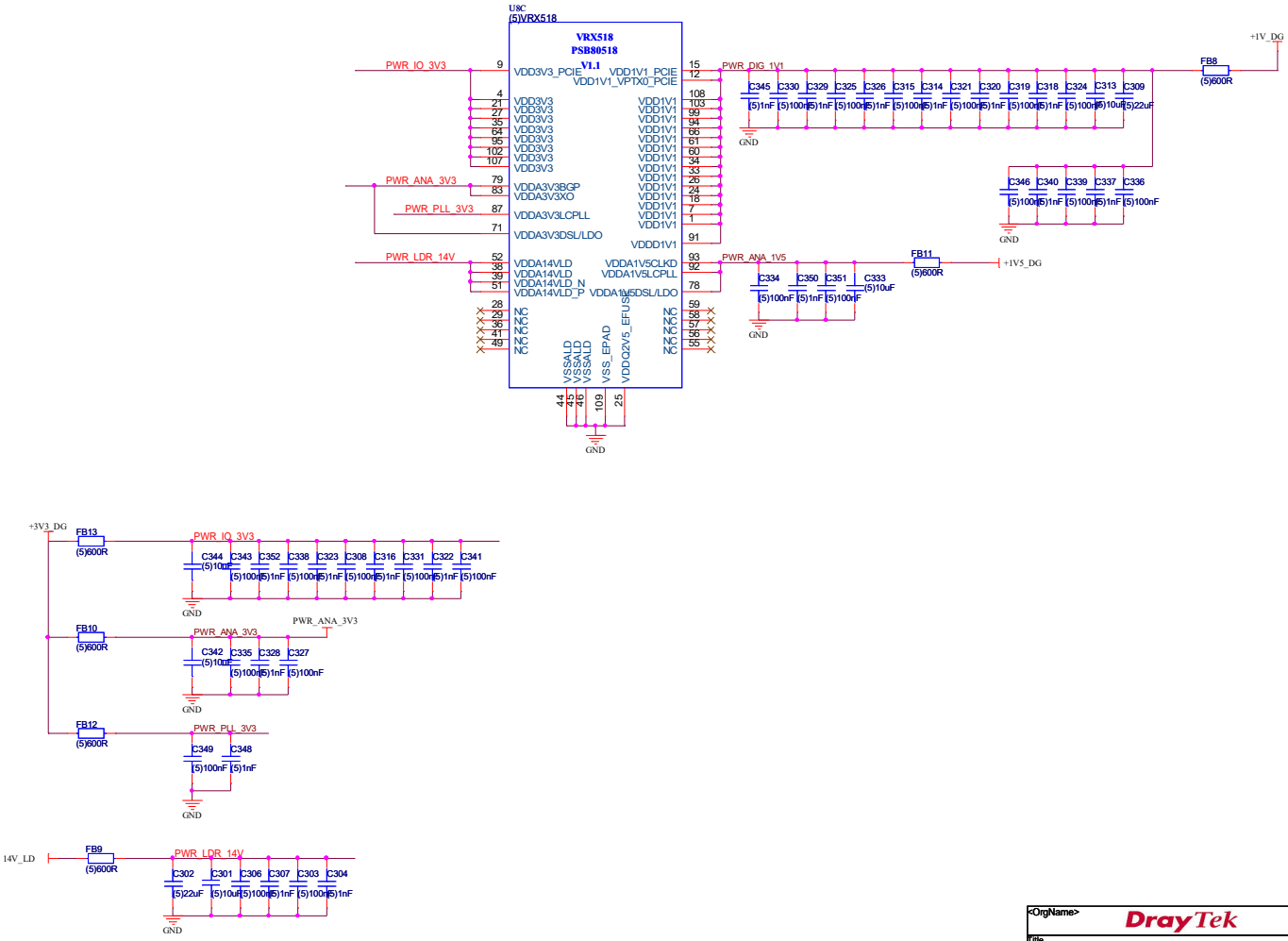
Date: Tuesday, December 21, 2021 Sheet 13 of 34



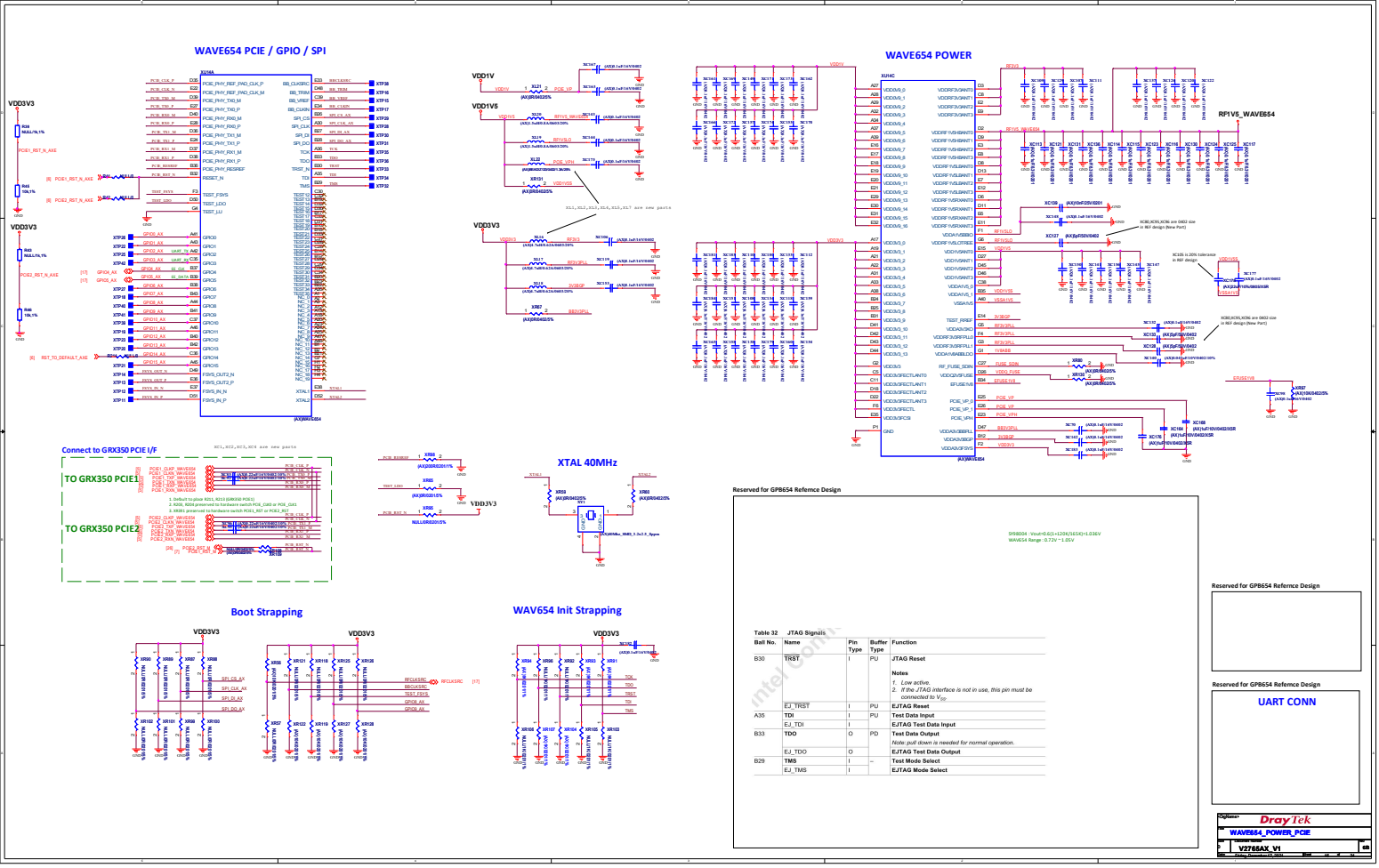


Place protection (SMBD7000 is only valid for xRX300, for xRX200-family we the need DSL70) close to transformer and connect it by 1mm track width.

<OrgName>	DrayTek	
Title: 1st_VRX518 AFE		
Size: Custom	Document Number: V2765AX_V1	Rev: 6B
Date: Friday, December 17, 2021	Sheet 14 of 34	



<OrgName>	DrayTek		
Title	1st_VRX518 power		
Size: Custom	Document Number: V2765AX_V1		Rev: 6B
Date: Friday, December 17, 2021	Sheet 15 of 34		



Reserved for GP8654 Refernce Design

Table 32 JTAG Signals

Ball No.	Name	Pin Type	Buffer Type	Function
B30	TRST	I	PU	**JTAG Reset**
				Notes 1. *Low active.* 2. *If the JTAG interface is not in use, this pin must be connected to V_{SS}.*
	EJ_TRST	I	PU	**EJTAG Reset**
A35	TDI	I	PU	**Test Data Input**
	EJ_TDI	I		**EJTAG Test Data Input**
B33	TDO	O	PD	**Test Data Output** *Note: pull down is needed for normal operation.*
	EJ_TDO	O		**EJTAG Test Data Output**
B29	TMS	I	–	**Test Mode Select**
	EJ_TMS	I		**EJTAG Mode Select**

Reserved for GP8654 Refernce Design

Reserved for GP8654 Refernce Design

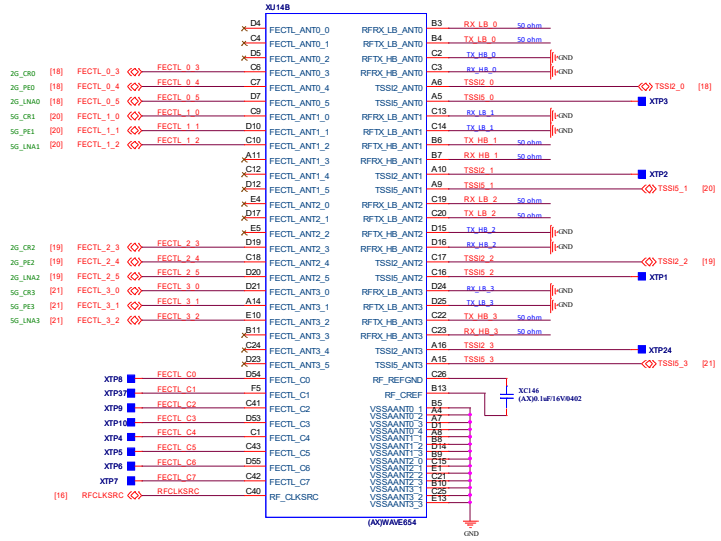
UART CONN

Digitaler DrayTek

WAVE654_POWER_PCIE

V2765AX_V1

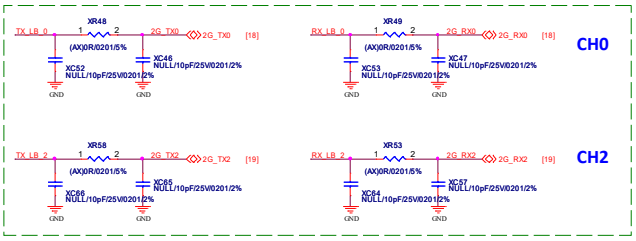
WAVE654 RF



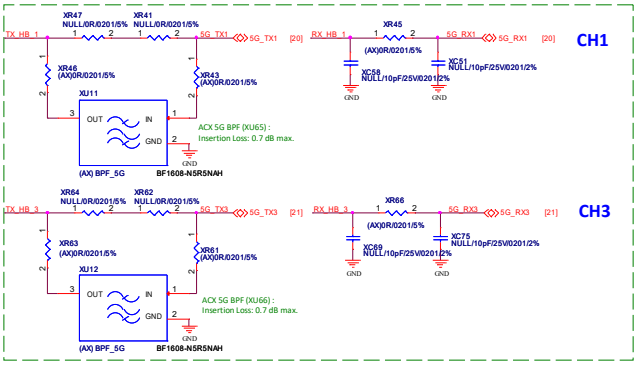
Reserved for GPB654 Refernce Design

PCIE FINGER

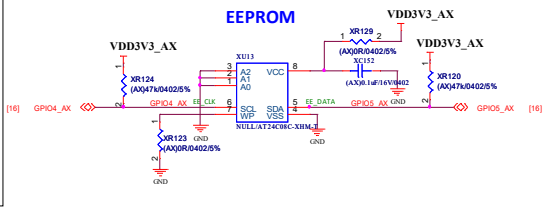
2.4G Front-End



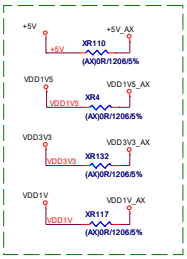
5G Front-End



EEPROM

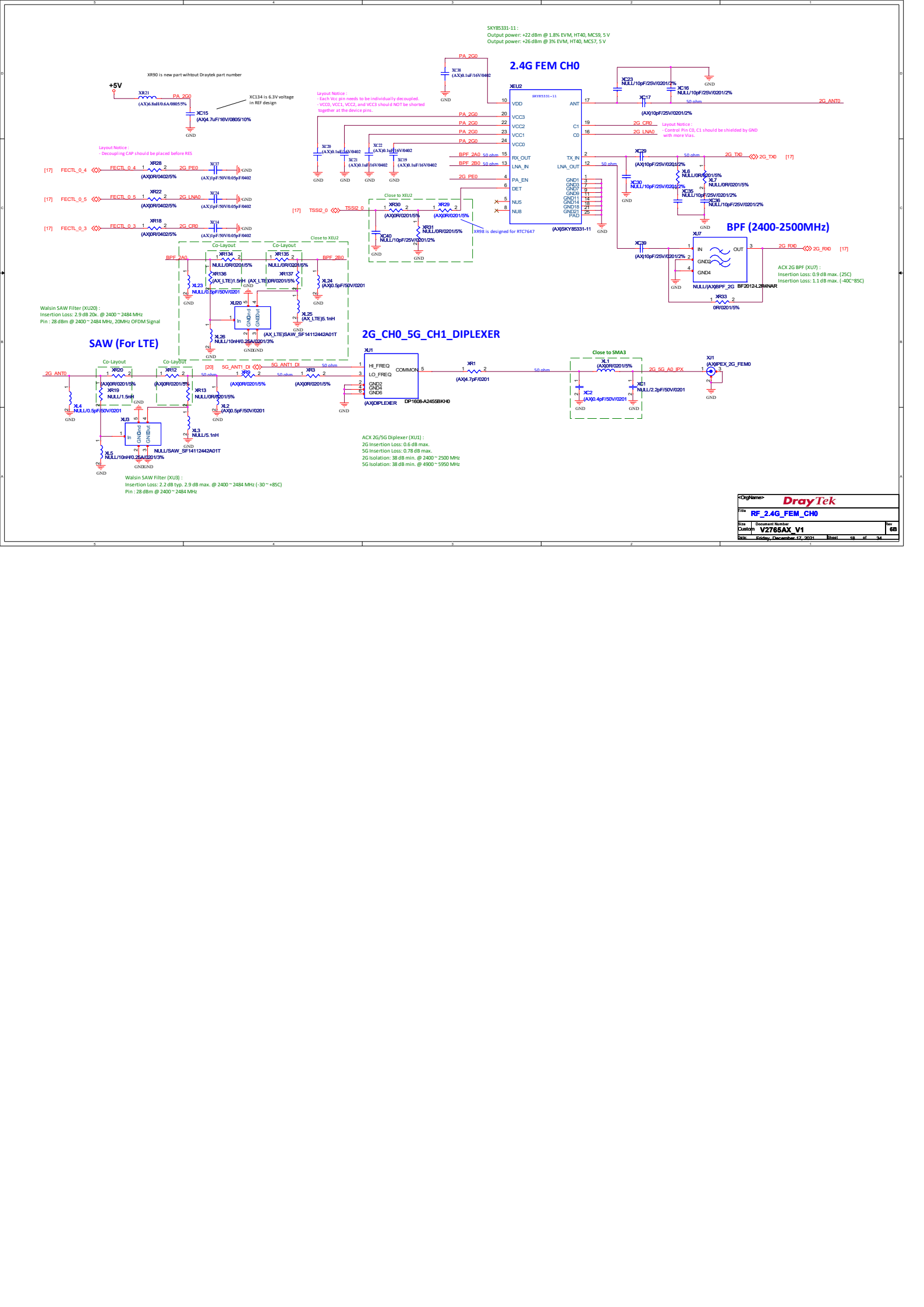


Connect to main board DCDC



SY98004 : Vout=0.6(1+120K/165K)=1.036V
WAV654 Range : 0.72V ~ 1.05V

<OrgName>	DrayTek	
Title	WAVE654_RF	
Size: Custom	Document Number: V2765AX_V1	Rev: 6B
Date: Friday, December 17, 2021	Sheet 17 of 34	


SKY85331-11 :
Output power: +22 dBm @ 1.8% EVM, HT40, MCS9, 5 V
Output power: +26 dBm @ 3% EVM, HT40, MCS7, 5 V
2.4G FEM CH0
XR90 is new part wihtout Draytek part number
+5V
XC134 is 6.3V voltage in REF design
Layout Notice :
- Each Vcc pin needs to be individually decoupled.
- VCC0, VCC1, VCC2, and VCC3 should NOT be shorted together at the device pins.
Layout Notice :
- Decoupling CAP should be placed before RES
Layout Notice :
- Control Pin C0, C1 should be shielded by GND with more Vias.
Close to XEU2
XRR98 is designed for RTC7647
BPF (2400-2500MHz)
ACX 2G BPF (XU7) :
Insertion Loss: 0.9 dB max. (25C)
Insertion Loss: 1.1 dB max. (-40C~85C)
Walsin SAW Filter (XU20) :
Insertion Loss: 2.9 dB 20x. @ 2400 ~ 2484 MHz
Pin : 28 dBm @ 2400 ~ 2484 MHz, 20MHz OFDM Signal
SAW (For LTE)
2G_CH0_5G_CH1_DIPLEXER
Close to SMA3
ACX 2G/5G Diplexer (XU1) :
2G Insertion Loss: 0.6 dB max.
5G Insertion Loss: 0.78 dB max.
2G Isolation: 38 dB min. @ 2400 ~ 2500 MHz
5G Isolation: 38 dB min. @ 4900 ~ 5950 MHz
Walsin SAW Filter (XU3) :
Insertion Loss: 2.2 dB typ. 2.9 dB max. @ 2400 ~ 2484 MHz (-30 ~ +85C)
Pin : 28 dBm @ 2400 ~ 2484 MHz
<OrgName>
DrayTek
File
RF_2.4G_FEM_CH0
Size
Custom
Document Number
V2765AX_V1
Rev
6B
Date:
Friday, December 17, 2021
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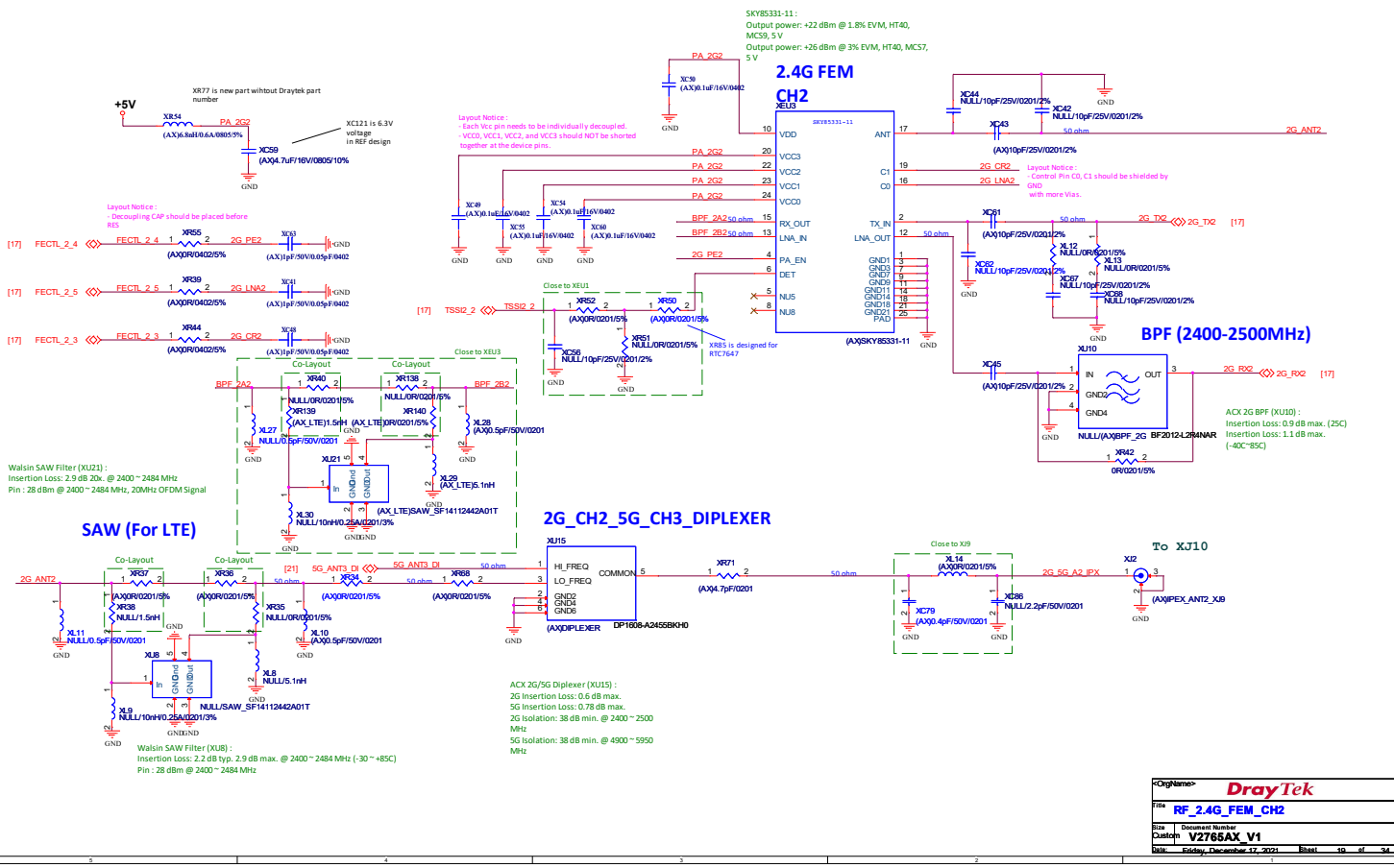
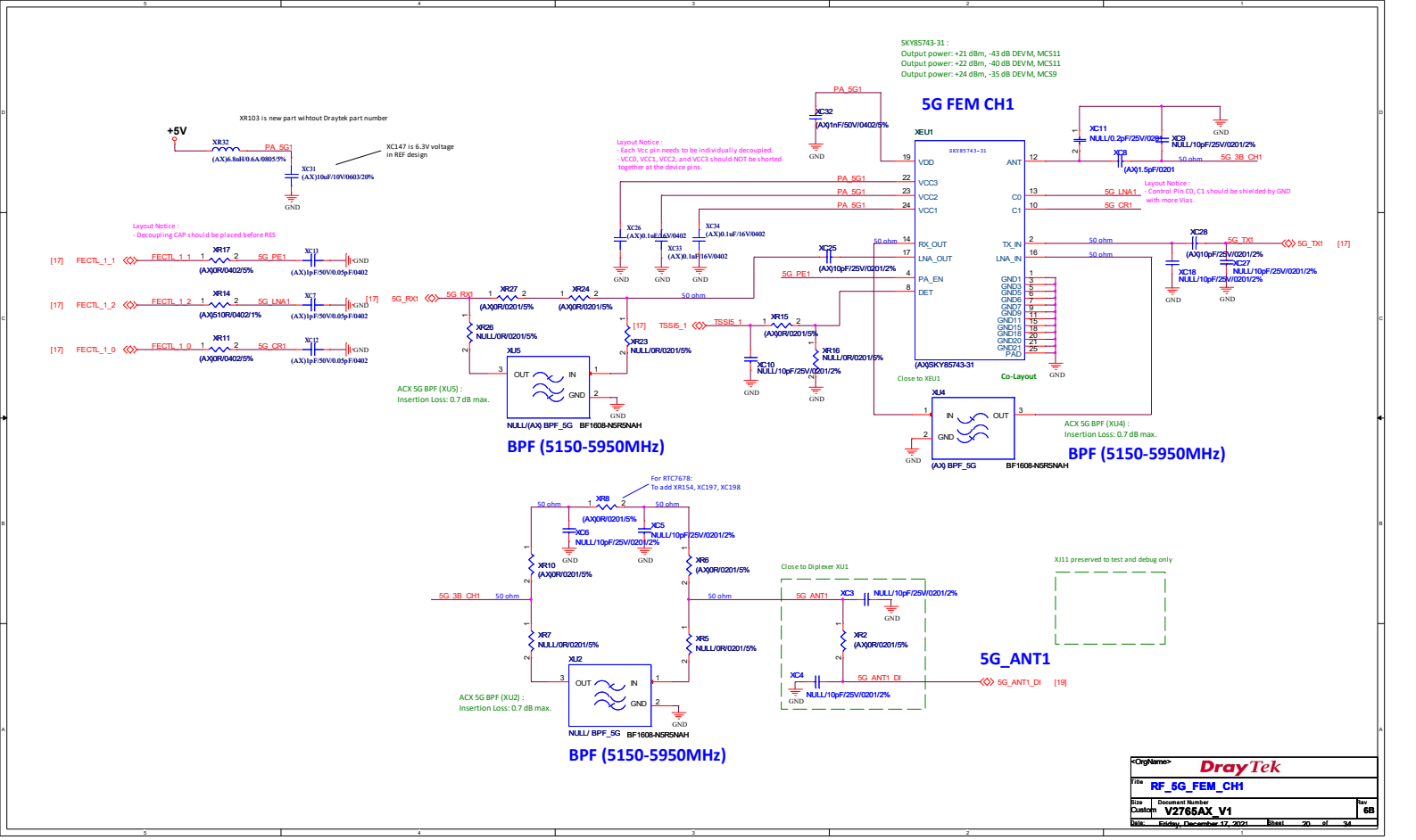
of
34


SKY85331-11 :
Output power: +22 dBm @ 1.8% EVM, HT40, MCS9, 5 V
Output power: +26 dBm @ 3% EVM, HT40, MCS7, 5 V
2.4G FEM CH2
XR77 is new part wihtout Draytek part number
+5V
XR54 (AX)6.8nH/0.6A/0805/5%
XC121 is 6.3V voltage in REF design
XC59 (AX)4.7uF/16V/0805/10%
Layout Notice : - Decoupling CAP should be placed before RES
Layout Notice : - Each Vcc pin needs to be individually decoupled. - VCC0, VCC1, VCC2, and VCC3 should NOT be shorted together at the device pins.
XC49 (AX)0.1uF/16V/0402
XC55 (AX)0.1uF/16V/0402
XC54 (AX)0.1uF/16V/0402
XC60 (AX)0.1uF/16V/0402
XC50 (AX)0.1uF/16V/0402
XU3 SKY85331-11
VDD VCC3 VCC2 VCC1 VCC0 RX_OUT LNA_IN PA_EN DET NU5 NU8 ANT C1 C0 TX_IN LNA_OUT GND1 GND3 GND7 GND9 GND11 GND14 GND18 GND21 PAD
(AX)SKY85331-11
XC44 NULL/10pF/25V/0201/2%
XC42 NULL/10pF/25V/0201/2%
XC43 (AX)10pF/25V/0201/2%
2G_ANT2
Layout Notice : - Control Pin C0, C1 should be shielded by GND with more Vias.
2G_CR2
2G_LNA2
XC61 (AX)10pF/25V/0201/2%
XC62 NULL/10pF/25V/0201/2%
XC67 NULL/10pF/25V/0201/2%
XC68 NULL/10pF/25V/0201/2%
XL12 NULL/0R/0201/5%
XL13 NULL/0R/0201/5%
2G_TX2
[17] FECTL_2_4 FECTL_2_5 FECTL_2_3
XR55 XR39 XR44 (AX)0R/0402/5%
XC63 XC61 XC58 (AX)1pF/50V/0.05pF/0402
2G_PE2
2G_LNA2
2G_CR2
PA_2G2
BPF_2A2 50 ohm
BPF_2B2 50 ohm
Close to XEU1
[17] TSSI2_2
XR52 XR59 (AX)0R/0201/5%
XC56 NULL/10pF/25V/0201/2%
XR51 NULL/0R/0201/5%
XR85 is designed for RTC7647
BPF (2400-2500MHz)
XU10 IN OUT GND2 GND4
NULL/(AX)BPF_2G BF2012-L2R4NAR
XC45 (AX)10pF/25V/0201/2%
2G_RX2
XR42 0R/0201/5%
ACX 2G BPF (XU10) : Insertion Loss: 0.9 dB max. (25C) Insertion Loss: 1.1 dB max. (-40C~85C)
Close to XEU3
Co-Layout
BPF_2A2
BPF_2B2
XR40 XR138 XR139 XR140 NULL/0R/0201/5%
(AX_LTE)1.5nH (AX_LTE)0R/0201/5%
XL27 XL28 NULL/0.5pF/50V/0201 (AX)0.5pF/50V/0201
XL21 XL29 (AX_LTE)5.1nH
XL30 NULL/10nH/0.25A/0201/3%
(AX_LTE)SAW_SF14112442A01T
Walsin SAW Filter (XU21) : Insertion Loss: 2.9 dB 20x. @ 2400 ~ 2484 MHz Pin : 28 dBm @ 2400 ~ 2484 MHz
SAW (For LTE)
2G_CH2_5G_CH3_DIPLEXER
XU15 HI_FREQ LO_FREQ COMMON GND2 GND4 GND6
(AX)DIPLEXER DP1608-A2455BKH0
XR71 (AX)4.7pF/0201
Close to XJ9
XL14 (AX)0R/0201/5%
XC79 (AX)0.4pF/50V/0201
XC86 NULL/2.2pF/50V/0201
2G_5G_A2_IPX
XJ2 (AX)IPEX_ANT2_XJ9
To XJ10
2G_ANT2
[21] 5G_ANT3_DI
XR37 XR38 XR36 XR35 XR34 XR68 (AX)0R/0201/5%
NULL/1.5nH NULL/0R/0201/5%
XL11 XL10 NULL/0.5pF/50V/0201 (AX)0.5pF/50V/0201
XL8 XL9 NULL/5.1nH NULL/10nH/0.25A/0201/3%
NULL/SAW_SF14112442A01T
Walsin SAW Filter (XU8) : Insertion Loss: 2.2 dB typ. 2.9 dB max. @ 2400 ~ 2484 MHz (-30 ~ +85C) Pin : 28 dBm @ 2400 ~ 2484 MHz
ACX 2G/5G Diplexer (XU15) : 2G Insertion Loss: 0.6 dB max. 5G Insertion Loss: 0.78 dB max. 2G Isolation: 38 dB min. @ 2400 ~ 2500 MHz 5G Isolation: 38 dB min. @ 4900 ~ 5950 MHz
<OrgName> DrayTek
File RF_2.4G_FEM_CH2
Size Custom Document Number V2765AX_V1 Rev 6B
Date: Friday, December 17, 2021 Sheet 19 of 34


SKY85743-31 :
Output power: +21 dBm, -43 dB DEVM, MCS11
Output power: +22 dBm, -40 dB DEVM, MCS11
Output power: +24 dBm, -35 dB DEVM, MCS9
5G FEM CH1
XR103 is new part wihtout Draytek part number
+5V
XC147 is 6.3V voltage in REF design
Layout Notice :
- Decoupling CAP should be placed before RES
Layout Notice :
- Each Vcc pin needs to be individually decoupled.
- VCC0, VCC1, VCC2, and VCC3 should NOT be shorted together at the device pins.
Layout Notice :
- Control Pin C0, C1 should be shielded by GND with more Vias.
Close to XEU1
Co-Layout
ACX 5G BPF (XU5) :
Insertion Loss: 0.7 dB max.
BPF (5150-5950MHz)
ACX 5G BPF (XU4) :
Insertion Loss: 0.7 dB max.
BPF (5150-5950MHz)
For RTC7678:
To add XR154, XC197, XC198
Close to Diplexer XU1
XJ11 preserved to test and debug only
5G_ANT1
ACX 5G BPF (XU2) :
Insertion Loss: 0.7 dB max.
BPF (5150-5950MHz)
<OrgName>
DrayTek
File RF_5G_FEM_CH1
Size Custom
Document Number V2765AX_V1
Rev 6B
Date: Friday, December 17, 2021
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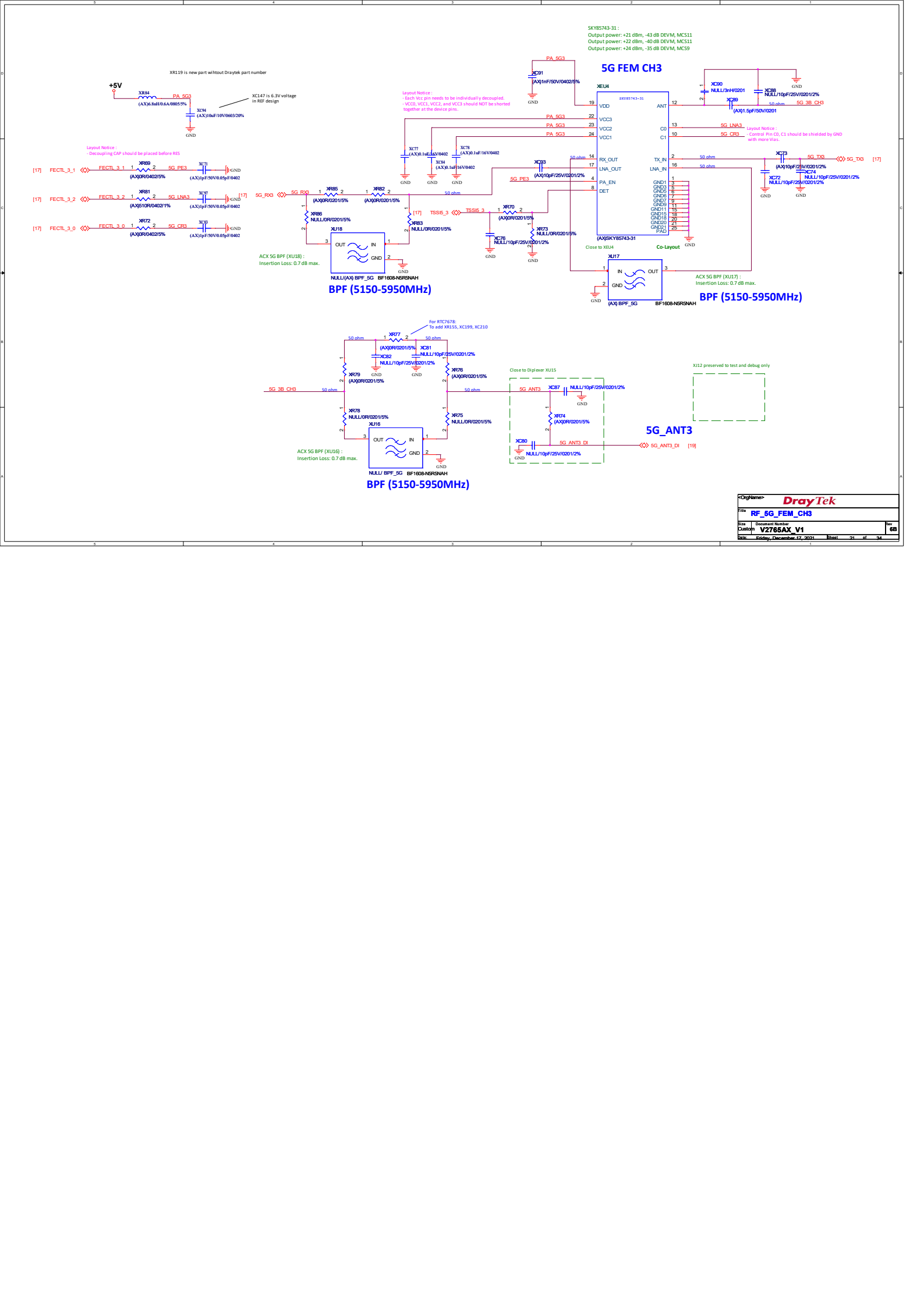
SKY85743-31 :
Output power: +21 dBm, -43 dB DEVM, MCS11
Output power: +22 dBm, -40 dB DEVM, MCS11
Output power: +24 dBm, -35 dB DEVM, MCS9
5G FEM CH3
XR119 is new part wihtout Draytek part number
+5V
XR84
(AX)6.8nH/0.6A/0805/5%
PA_5G3
XC94
(AX)10uF/10V/0603/20%
XC147 is 6.3V voltage in REF design
GND
Layout Notice :
- Decoupling CAP should be placed before RES
[17] FECTL_3_1
FECTL_3_1
XR89
(AX)0R/0402/5%
5G_PE3
XC71
(AX)1pF/50V/0.05pF/0402
[17] FECTL_3_2
FECTL_3_2
XR81
(AX)510R/0402/1%
5G_LNA3
XC97
(AX)1pF/50V/0.05pF/0402
[17] FECTL_3_0
FECTL_3_0
XR72
(AX)0R/0402/5%
5G_CR3
XC93
(AX)1pF/50V/0.05pF/0402
Layout Notice :
- Each Vcc pin needs to be individually decoupled.
- VCC0, VCC1, VCC2, and VCC3 should NOT be shorted together at the device pins.
XC91
(AX)1nF/50V/0402/5%
XEU4
SKY85743-31
VDD
VCC3
VCC2
VCC1
RX_OUT
LNA_OUT
PA_EN
DET
ANT
C0
C1
TX_IN
LNA_IN
GND1
GND3
GND5
GND6
GND7
GND9
GND11
GND15
GND18
GND20
GND21
PAD
(AX)SKY85743-31
Close to XEU4
Co-Layout
XC77
(AX)0.1nF/16V/0402
XC78
(AX)0.1nF/16V/0402
XC84
(AX)0.1nF/16V/0402
XC90
NULL/3nH/0201
XC88
NULL/10pF/25V/0201/2%
XC89
(AX)1.5pF/50V/0201
5G_3B_CH3
5G_LNA3
5G_CR3
Layout Notice :
- Control Pin C0, C1 should be shielded by GND with more Vias.
XC73
(AX)10pF/25V/0201/2%
5G_TX3
XC72
NULL/10pF/25V/0201/2%
XC74
NULL/10pF/25V/0201/2%
5G_PE3
XC93
(AX)10pF/25V/0201/2%
5G_RX3
XR85
(AX)0R/0201/5%
XR82
(AX)0R/0201/5%
XR86
NULL/0R/0201/5%
XR83
NULL/0R/0201/5%
XU18
OUT
IN
GND
ACX 5G BPF (XU18) :
Insertion Loss: 0.7 dB max.
NULL/(AX) BPF_5G BF1608-N5R5NAH
BPF (5150-5950MHz)
TSSI5_3
XR70
(AX)0R/0201/5%
XR73
NULL/0R/0201/5%
XC76
NULL/10pF/25V/0201/2%
XU17
(AX) BPF_5G
BF1608-N5R5NAH
ACX 5G BPF (XU17) :
Insertion Loss: 0.7 dB max.
BPF (5150-5950MHz)
For RTC7678:
To add XR155, XC199, XC210
XR77
(AX)0R/0201/5%
XC81
NULL/10pF/25V/0201/2%
XC82
NULL/10pF/25V/0201/2%
XR79
(AX)0R/0201/5%
XR76
(AX)0R/0201/5%
XR78
NULL/0R/0201/5%
XR75
NULL/0R/0201/5%
XU16
NULL/ BPF_5G BF1608-N5R5NAH
ACX 5G BPF (XU16) :
Insertion Loss: 0.7 dB max.
BPF (5150-5950MHz)
Close to Diplexer XU15
5G_ANT3
XC87
NULL/10pF/25V/0201/2%
XR74
(AX)0R/0201/5%
XC80
NULL/10pF/25V/0201/2%
5G_ANT3_DI
[19]
XJ12 preserved to test and debug only
5G_ANT3
<OrgName>
DrayTek
File
RF_5G_FEM_CH3
Size
Custom
Document Number
V2765AX_V1
Rev
6B
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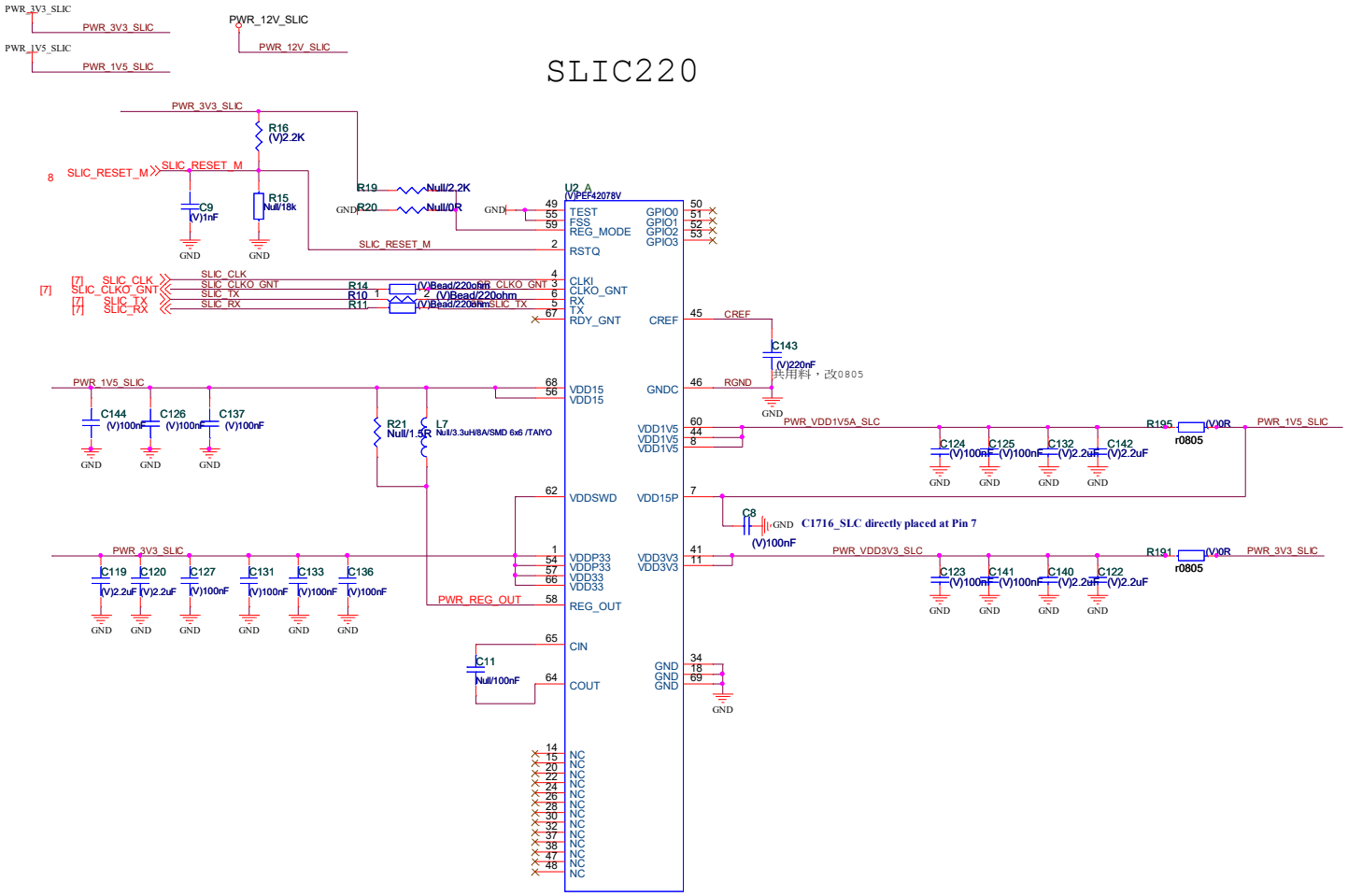
34



<OrgName>	DrayTek	
Title	XWAYSLIC220_DIGITAL	
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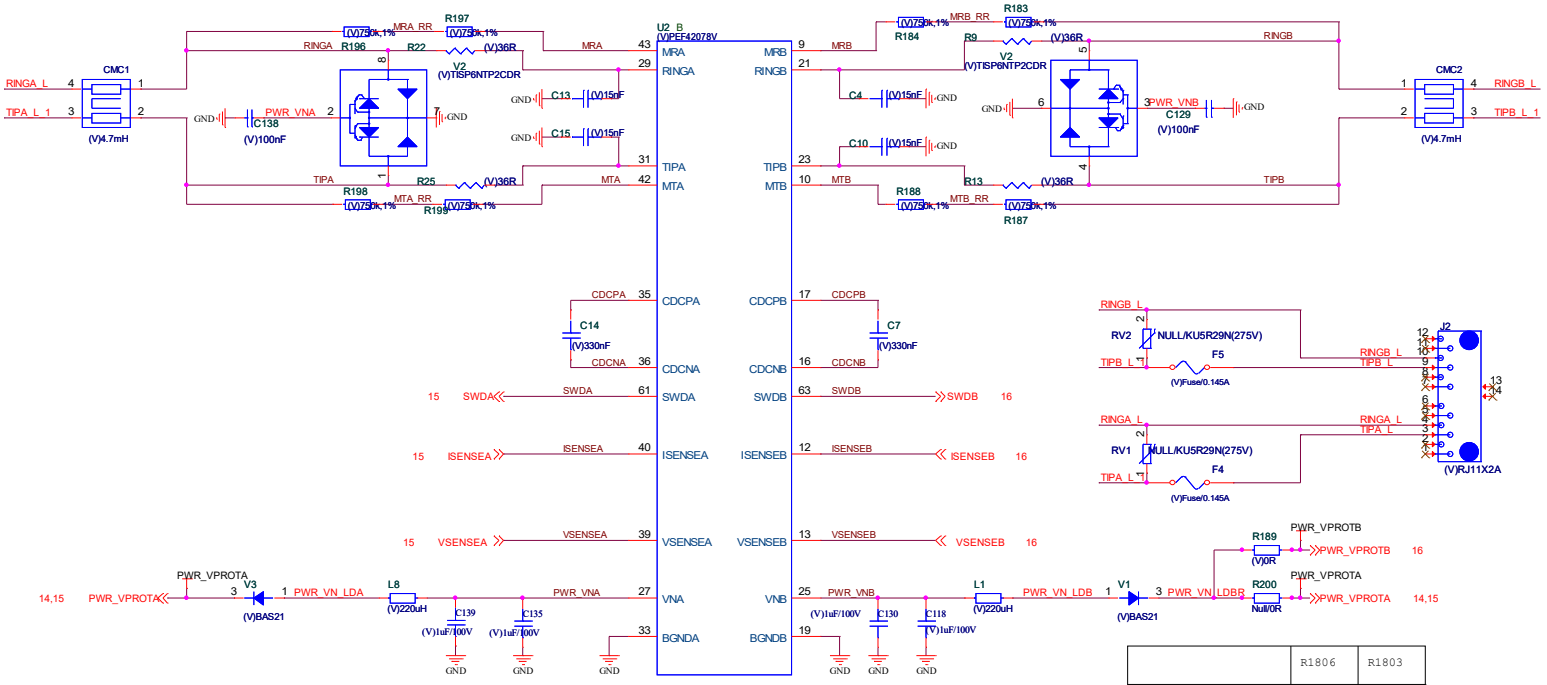
SLIC220



	R1806	R1803
Dedicated DCDC mode	Mounted	X
Combined DCDC mode	X	Mounted

<OrgName> DrayTek

Title: XWAYSLIC220_ANALOG

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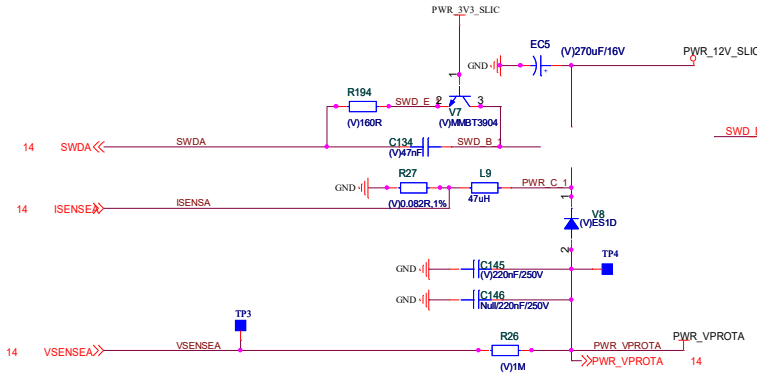
Date: Friday, December 17, 2021 | Sheet 23 of 27

DCDC Type

Dedicated DCDC = T0.2
Combined DCDC = T1.1

Move radiating parts (like switching regulators and coils, voice SLIC/coils,) far away from DSL-AFE. A distance (at least 5cm) between the reiating part and the DSL must be maintain.



Component	Dedicated DCDC	Combined DCDC
R71	0.082R	0.068R
L7	47uH/1.8A	33uH/2.1A
C196	mount	X
C1805	X	mount

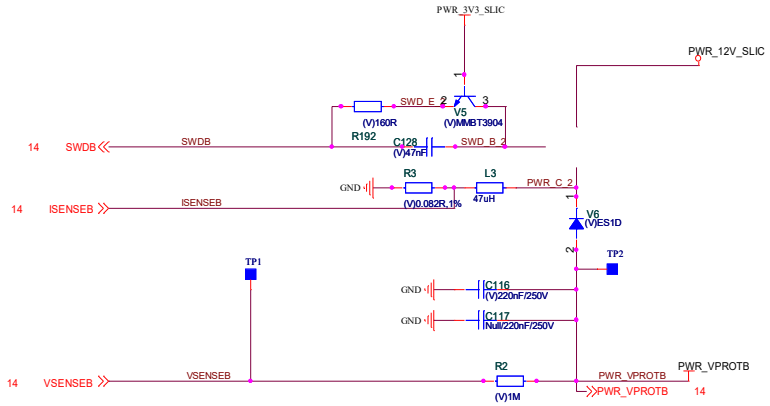
<OrgName> DrayTek		
Title: U1_PNP_DCDC_T02_V11		
Size: Custom	Document Number: V2765AX_V1	Rev: 6B
Date: Friday, December 17, 2021	Sheet 24 of 27	

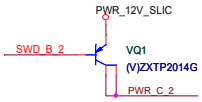
DCDC Type

Dedicated DCDC = T0.2

Combined DCDC = T1.1

Move radiating parts (like switching regulators and coils, voice SLIC/coils,) far away from DSL-AFE. A distance (at least 5cm) between the relating part and the DSL must be maintain.





Component	Dedicated DCDC	Combined DCDC
R77	0.082R	0.068R
L9	47uH/1.8A	33uH/2.1A
C204	mount	X
C1806	X	mount

<OrgName> DrayTek

Title: U2_PNP_DCDC_T02_V11

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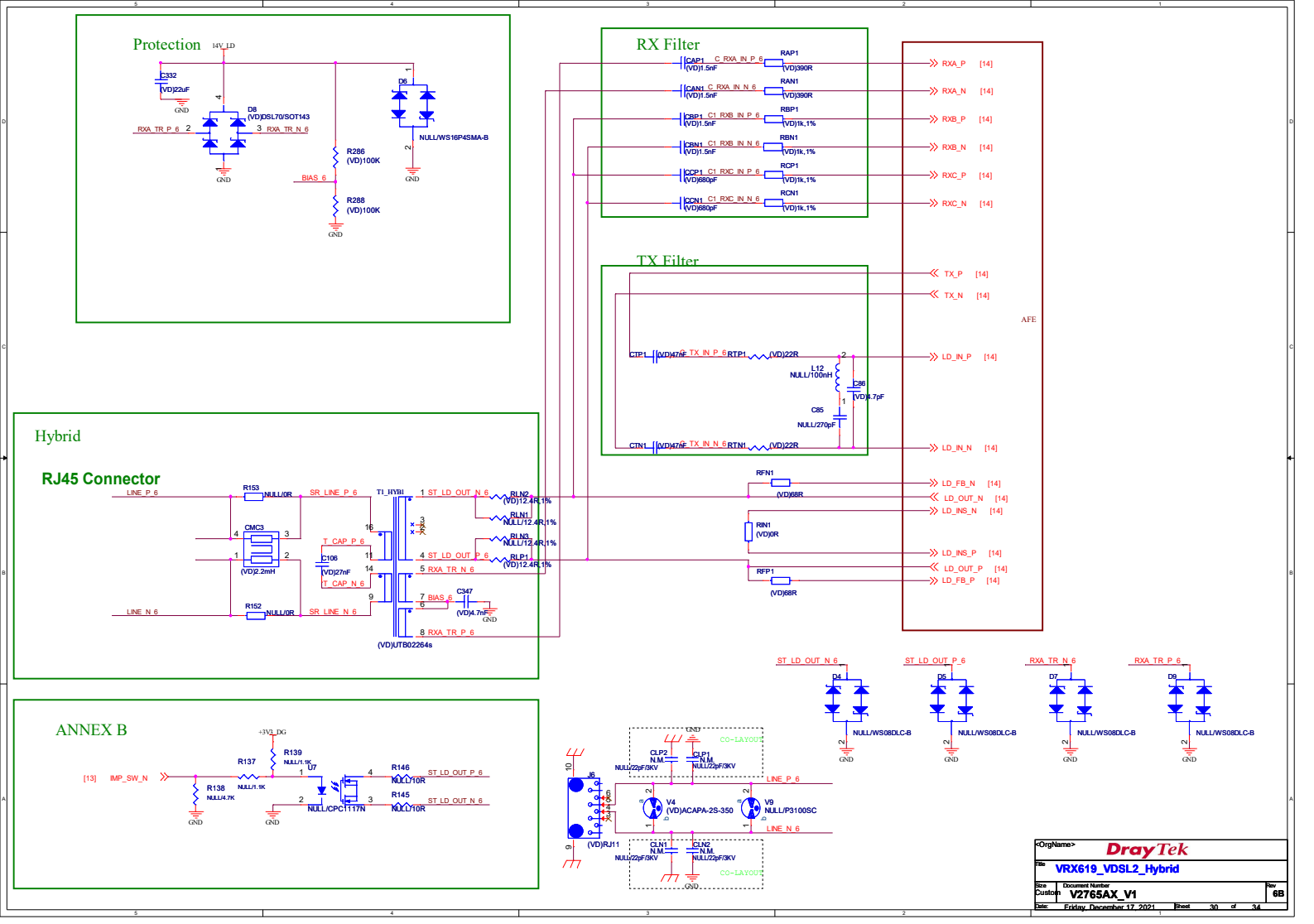

<OrgName> DrayTek

Title: VRX619_VDSL2_Hybrid

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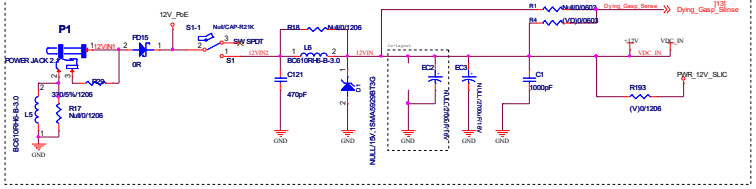
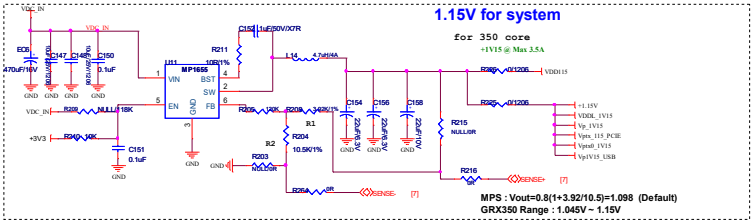
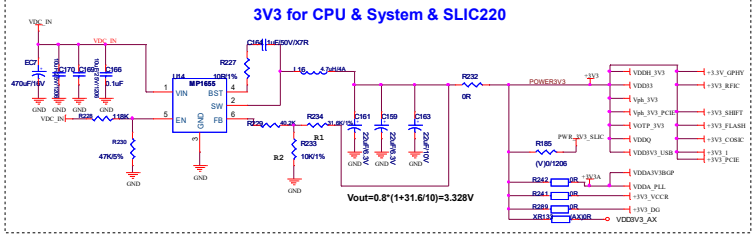
12V DC Power Input



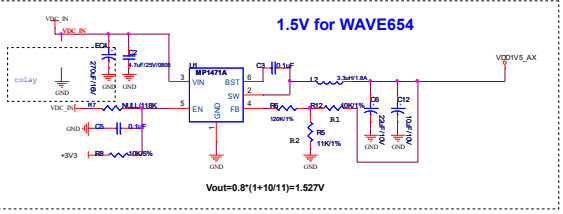
1.15V for system



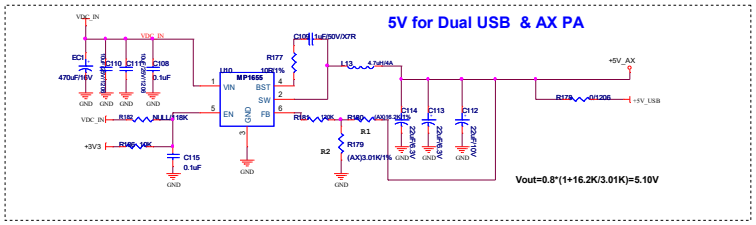
3V3 for CPU & System & SLIC220

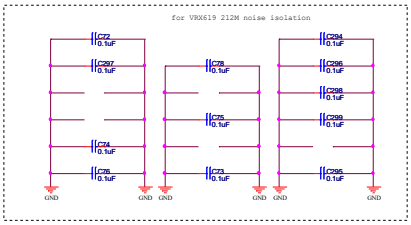


1.5V for WAVE654

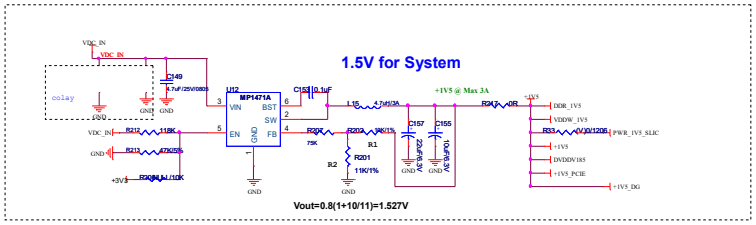


5V for Dual USB & AX PA

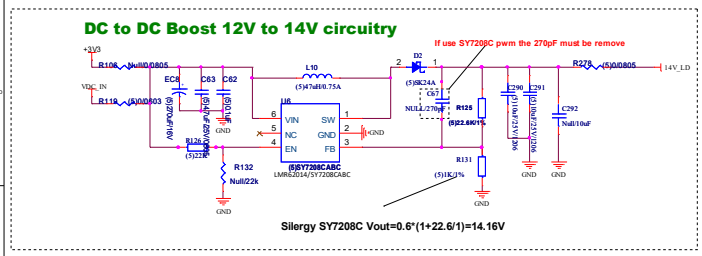


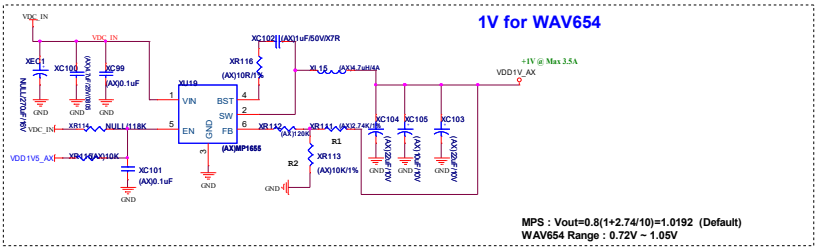


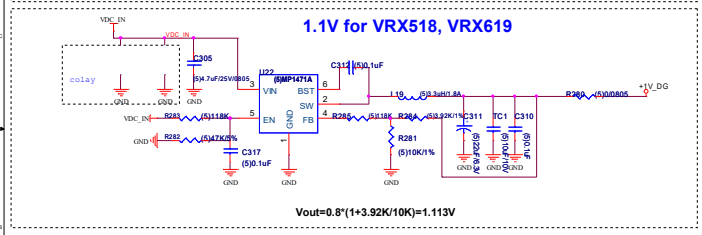
1.5V for System

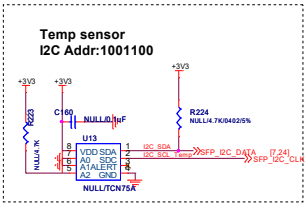


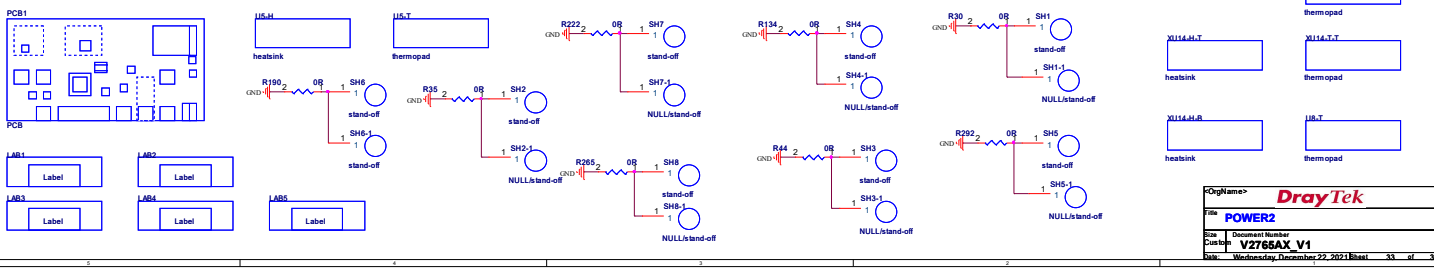
<OrgName>	DrayTek		
Title	POWER		
Size	Document Number		Rev
Custom	V2765AX_V1		0S
Date:	Monday, December 20, 2021	Sheet 32 of 34	

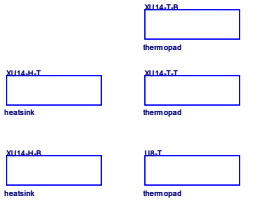











heatsink
thermopad

REVISION HISTORY

Version	Date	List of Modification	Page
	2020-12-01		Ian
V0A	2020-12-10	2.4GHz FEM (152-5331900-00G,SKY85331-11) : 1. Add XU31, XU33 2. Remove XC12, XC13, XC10, XC11 3. Null XR101, XR88, XU30, XU32 4. Place XR137, XR136 5. Remove XR146, XR149, XR142, XR145 5GHz FEM (152-5743900-00G,SKY85743-31) : 1. Add XU51, XU53 for co-layout with XU52, XU54 2. Remove XR117, XR113, XC16, XC17 3. Remove XR118, XR129, XC181, XC182 4. Place XR11, XR12 6. Null XU61, XR10, XR135 7. Place XR139, XR140 8. Null XU63, XR138, XR141	mChen
V6B	2021-11-26	1. C332,C302 change to C1206 2. colay INT_GPHY-TP6F circuit 3. NULL XC90; XC89 change 1.5PF; XR1,XR71 change 4.7pF 4. add J9, PD15, R445, R444 5. XC15,XC59 change to C0805 6. J6 change to 8 pin RJ45	Ian

BOM Difference

	V2765ax	V2765Vax							
(VD)	V	V							
(V)	NULL	V							
(5)	V	V							
(PD)	NULL	NULL							
(AX)	V	V							
(NPD)	V	V							
(AX_LTE)	NULL	NULL							

<OrgName> DrayTek

Title: BOM Difference

Size: B | Document Number: V2765AX_V1 | Rev: 6B

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