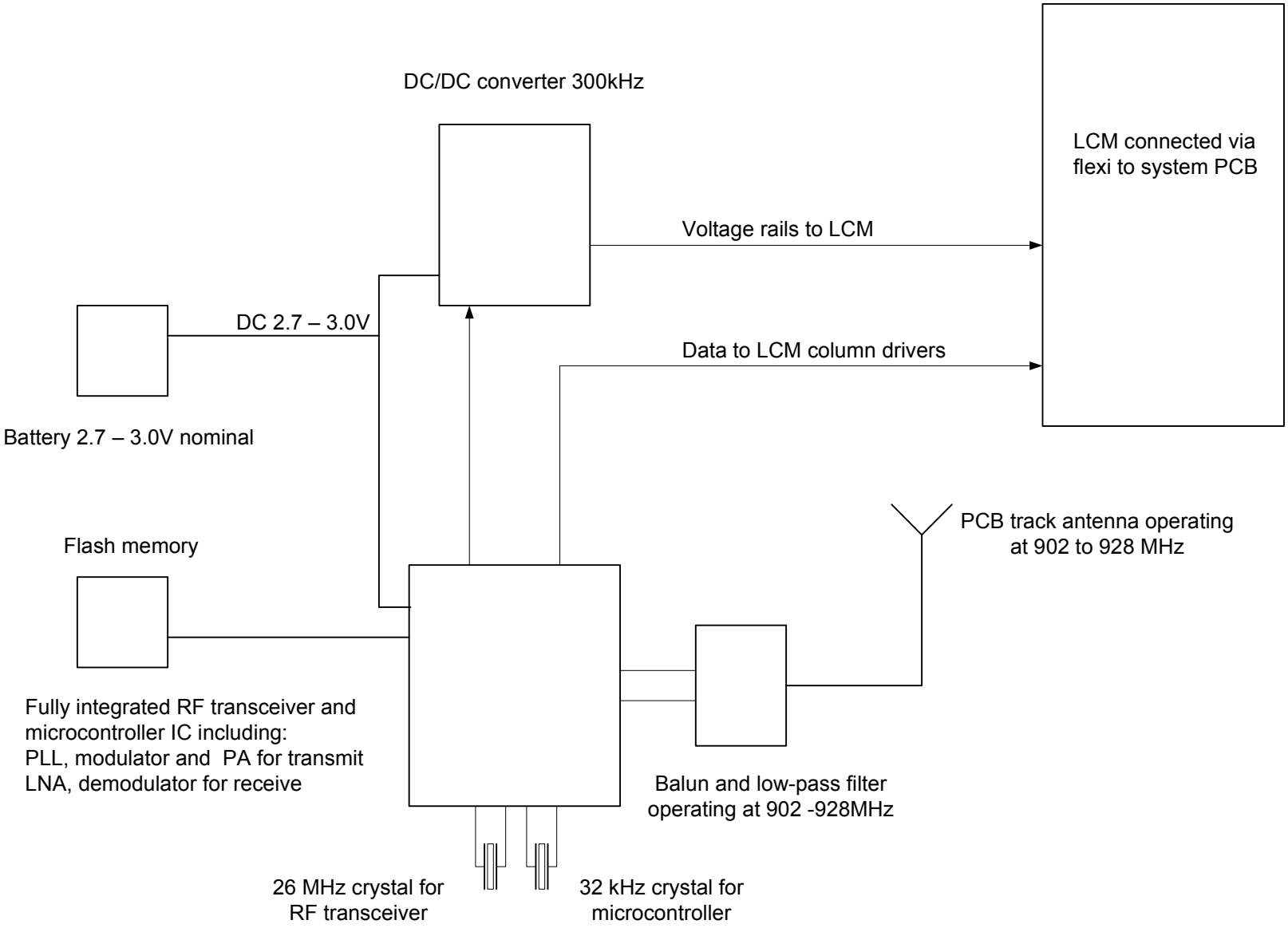
EPOP 900 BLOCK DIAGRAM



EPOP 500 DESCRIPTION

The RF transceiver implements bidirectional RF communications with a remote unit under the control of the integrated microcontroller. The microcontroller timing is derived from the 32kHz crystal.

A 26 MHz crystal forms the fundamental clock which is multiplied up by the PLL (phased locked loop) to a pre-programmed carrier centre frequency in the range 902.5 to 927.5 (902 to 928 MHz band boundaries).

In transmit mode the internal GFSK modulator generates a modulated carrier which is amplified by the integrated power amplifier (PA) with differential output. The Power amplifier output is fed to a balun which converts the signal to a single ended form and a low pass filter ensures that harmonics are attenuated to below the limiting values as specified in the relevant standard. The filtered RF output is fed to the PCB track antenna.

In receive mode, the received signal from the antenna is fed via the low pass filter and balun into the low noise amplifier (LNA) where it is amplified and demodulated. Received data is stored in internal memory or optionally fed to the off-chip flash memory.

The LCM is updated by the integrated microcontroller retrieving image data from the flash memory and forwarding it to the LCM data register. The DC/DC converter running at 300kHz generates suitable bias voltages which in combination with the Image data temporarily buffered in the data register cause the image on the LCM to be updated a line at a time in accordance with the binary pattern in the buffered data.