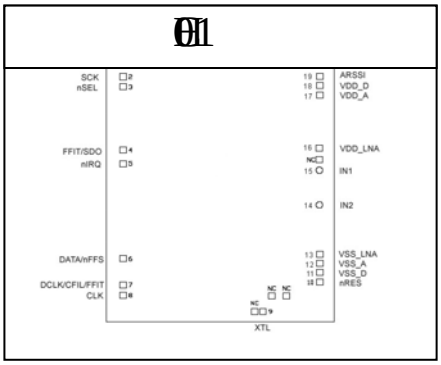
Universal ISM Band FSK Receiver

DESCRIPTION:



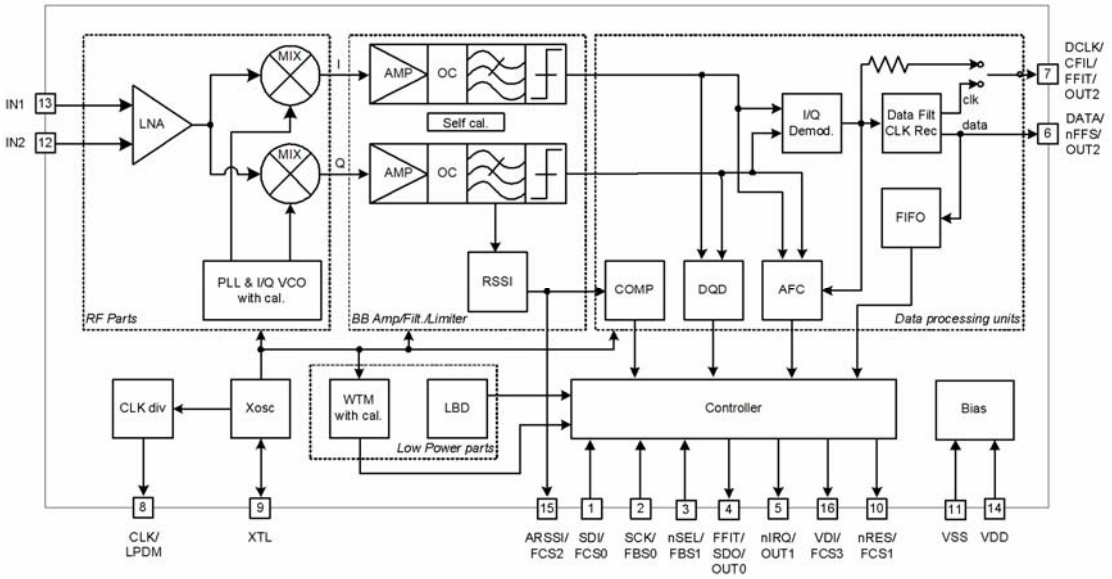
HC01 is a single chip, low power, multi-channel FSK receiver designed for use in applications requiring FCC or ETSI conformance for unlicensed use in the 315, 433, 868, and 915 MHz bands. Used in conjunction with HC's FSK transmitters, the HC01 is a flexible, low cost, and highly integrated solution that does not require production alignments. All required RF functions are integrated. Only an external crystal and bypass filtering are needed for operation.

The HC01 has a completely integrated PLL for easy RF design, and its rapid settling time allows for fast frequency hopping, bypassing multi-path fading, and interference to achieve robust wireless links. The PLL's high resolution allows the usage of multiple channels in any of the bands. The baseband bandwidth (BW) is programmable to accommodate various deviation, data rate, and crystal tolerance requirements. The receiver employs the Zero-IF approach with I/Q demodulation, therefore no external components (except crystal and decoupling) are needed in a typical application. The HC01 is a complete analog RX and baseband receiver including a multi-band PLL synthesizer with an LNA, I/Q down converter mixers, baseband filters and amplifiers, and I/Q demodulator.

The chip dramatically reduces the load on the microcontroller with integrated digital data processing: data filtering, clock recovery, data pattern recognition and integrated FIFO. The automatic frequency control (AFC) feature allows using a low accuracy (low cost) crystal. To minimize the system cost, the chip can provide a clock signal for the microcontroller, avoiding the need for two crystals.

For low power applications, the device supports low duty-cycle operation based on the internal wake-up timer.

BLOCK DIAGRAM



FEATURES:

Fully integrated (low BOM, easy design-in)
No alignment required in production
Fast settling, programmable, high-resolution PLL
Fast frequency hopping capability
High bit rate (up to 115.2 kbps in digital mode and 256 kbps in analog mode)
Direct differential antenna input
Programmable baseband bandwidth (67 to 400 kHz)
Analog and digital RSSI outputs
Automatic frequency control (AFC)
Data quality detection (DQD)
Internal data filtering and clock recovery
RX pattern recognition
SPI compatible serial control interface
Clock and reset signals for microcontroller
16 bit RX data FIFO
Low power duty-cycle mode (less than 0.5 mA average supply current)
Standard 10 MHz crystal reference
Wake-up timer
Low battery detector
2.2 to 5.4 V supply voltage
Low power consumption (~9 mA in low bands)
Low standby current (0.3 µA)

TYPICAL APPLICATIONS

Remote control
Home security and alarm
Wireless keyboard/mouse and other PC peripherals
Toy control
Remote keyless entry
Tire pressure monitoring
Telemetry
Personal/patient data logging
Remote automatic meter reading

DETAILED DESCRIPTION

General

The HC01 FSK receiver is the counterpart of the Hc's FSK transmitter. It covers the unlicensed frequency bands at 315, 433, 868, and 915 MHz. The device facilitates compliance with FCC and ETSI requirements.

The programmable PLL synthesizer determines the operating frequency, while preserving accuracy based on the on-chip crystal-controlled reference oscillator. The PLL's high resolution allows for the use of multiple channels in any of the bands.

The receiver employs the Zero-IF approach with I/Q demodulation, allowing the use of a minimal number of external components in a typical application. The HC01 consists of a fully integrated multi-band PLL synthesizer, an LNA with switchable gain, I/Q down converter mixers, baseband filters and amplifiers, and an I/Q demodulator followed by a data filter.

The HC VCO in the PLL performs automatic calibration, which requires only a few microseconds. Calibration always occurs when the synthesizer begins. If temperature or supply voltage changes significantly, VCO recalibration can be invoked easily. Recalibration can be initiated at any time by switching the synthesizer off and back on again.

LNA

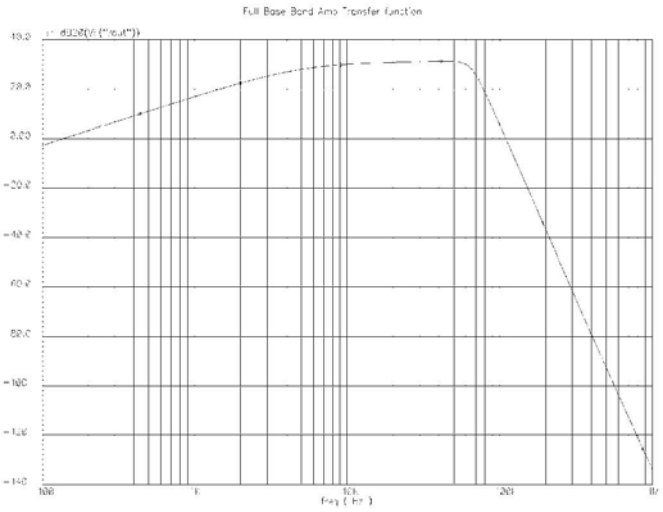
The LNA has 250 Ohm input impedance, which works well with the recommended antennas.

If the RF input of the chip is connected to 50 Ohm devices, an external matching circuit is required to provide the correct matching and to minimize the noise figure of the receiver.

The LNA gain (and linearity) can be selected (0, –6, –14, –20 dB relative to the highest gain) according to RF signal strength. This is useful in an environment with strong interferers.

Baseband Filters

The receiver bandwidth is selectable by programming the bandwidth (BW) of the baseband filters. This allows setting up the receiver according to the characteristics of the signal to be received. An appropriate bandwidth can be selected to accommodate various FSK deviation, data rate, and crystal tolerance requirements. The filter structure is a 7-th order Butterworth low-pass with 40 dB suppression at 2*BW frequency. Offset cancellation is accomplished by using a high-pass filter with a cut-off frequency below 7 kHz.



Data Filtering and Clock Recovery

The output data filtering can be completed by an external capacitor or by using digital filtering according to the final application.

Analog operation:

The filter is an RC type low-pass filter and a Schmitt-trigger (St). The resistor (10k) and the St is integrated on the chip. An (external) capacitor can be chosen according to the actual bit-rate. In this mode the receiver can handle up to 256 kbps data rate.

Digital operation:

The data filter is a digital realization of an analog RC filter followed by a comparator with hysteresis. In this mode there is a clock recovery circuit (CR), which can provide synchronized clock to the data. With this clock the received data can fill the RX Data FIFO. The CR has three operation modes: fast, slow, and automatic. In slow mode, its noise immunity is very high, but it has slower settling time and requires more accurate data timing than in fast mode. In automatic mode the CR automatically changes between fast and slow modes. The CR starts in fast mode, then automatically switches to slow mode after locking.

(Only the data filter and the clock recovery use the bit-rate clock. Therefore, in analog mode, there is no need for setting the correct bit-rate.)

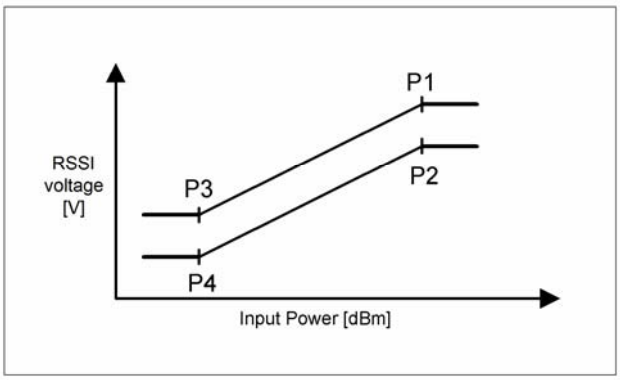
Data Validity Blocks

RSSI

A digital RSSI output is provided to monitor the input signal level. It goes high if the received signal strength exceeds a given preprogrammed level. An analog RSSI signal is also available. The RSSI settling time depends on the filter capacitor used.

P1	-65 dBm	1300 mV
P2	-65 dBm	1000 mV
P3	-100 dBm	600 mV
P4	-100 dBm	300 mV

Voltage on ARRSI pin vs. Input RF power



DQD

The Data Quality Detector monitors the I/Q output of the baseband amplifier chain by counting the consecutive correct 0->1, 1->0 transitions. The DQD output indicates the quality of the signal to be demodulated. Using this method it is possible to "forecast" the probability of BER degradation. The programmable DQD parameter defines the threshold for signaling the good/bad data quality by the digital one-bit DQD output. In cases when the deviation is close to the bit rate, there should be four transitions during a single one bit period in the I/Q signals. As the bit rate decreases in comparison to the deviation, more and more transitions will happen during a bit period.

AFC

By using an integrated Automatic Frequency Control (AFC) feature, the receiver can synchronize its local oscillator to the received signal, allowing the use of:

- inexpensive, low accuracy crystals
- narrower receiver bandwidth (i.e. increased sensitivity)
- higher data rate

Crystal Oscillator

The chip has a single-pin crystal oscillator circuit, which provides a 10 MHz reference signal for the PLL. To reduce external parts and simplify design, the crystal load capacitor is internal and programmable. Guidelines for selecting the appropriate crystal can be found later in this datasheet. The receiver can supply the clock signal for the microcontroller, so accurate timing is possible without the need for a second crystal.

When the microcontroller turns the crystal oscillator off by clearing the appropriate bit using the Configuration Setting Command, the chip provides a fixed number (128) of further clock pulses (“clock tail”) for the microcontroller to let it go to idle or sleep mode.

Low Battery Voltage Detector

The low battery detector circuit monitors the supply voltage and generates an interrupt if it falls below a programmable threshold level.

Wake-Up Timer

The wake-up timer has very low current consumption (1.5 μA typical) and can be programmed from 1 ms to several days with an accuracy of ±5%.

It calibrates itself to the crystal oscillator at every startup, and then at every 30 seconds. When the crystal oscillator is switched off, the calibration circuit switches it back on only long enough for a quick calibration (a few milliseconds) to facilitate accurate wake-up timing.

Event Handling

In order to minimize current consumption, the receiver supports the sleep mode. Active mode can be initiated by several wake-up events (wake-up timer timeout, low supply voltage detection, on-chip FIFO filled up or receiving a request through the serial interface).

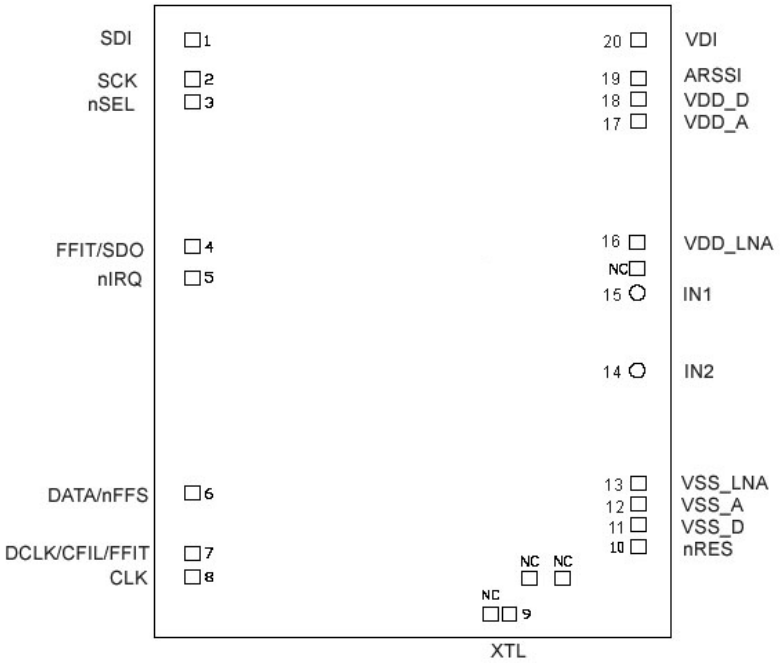
If any wake-up event occurs, the wake-up logic generates an interrupt signal which can be used to wake up the microcontroller, effectively reducing the period the microcontroller has to be active. The cause of the interrupt can be read out from the receiver by the microcontroller through the SDO pin.

Interface and Controller

An SPI compatible serial interface lets the user select the frequency band, center frequency of the synthesizer, and the bandwidth of the baseband signal path. Division ratio for the microcontroller clock, wake-up timer period, and low supply voltage detector threshold are also programmable. Any of these auxiliary functions can be disabled when not needed. All parameters are set to default after power-on; the programmed values are retained during sleep mode. The interface supports the read-out of a status register, providing detailed information about the status of the receiver and the received data. It is also possible to store the received data bits into the 16bit RX FIFO register and read them out in a buffered mode. FIFO mode can be enabled through the SPI compatible interface by setting the fe bit to 1 in the Output and FIFO Mode Command.

PACKAGE PIN DEFINITIONS

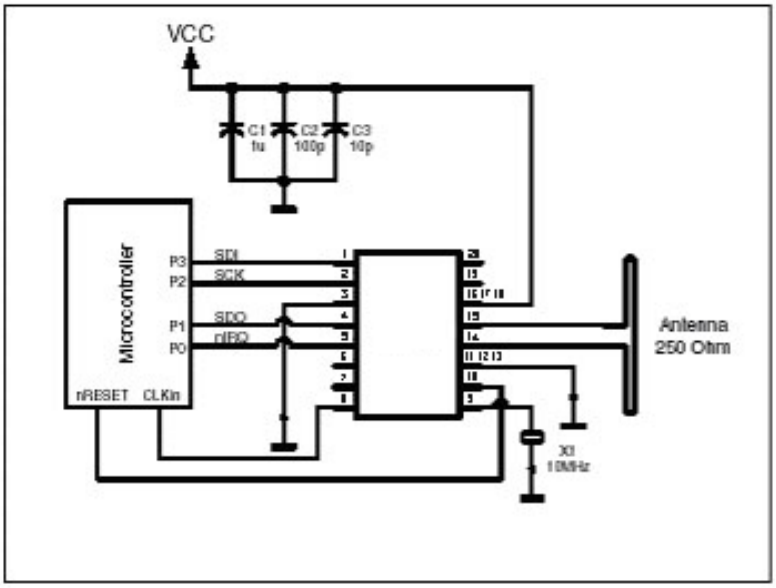
Pin type key: D=digital, A=analog, S=supply, I=input, O=output, IO=input/output



Pin	Name	Type	Function
1	SDI	DI	Data input of serial control interface
2	SCK	DI	Clock input of serial control interface
3	nSEL	DI	Chip select input of three-wire control interface (active low)
4	FFIT/SD	DO	FIFO IT (active low) or serial data out for Status Read Command. Tristate with bushold cell if nSEL=H
5	nIRQ	DO	Interrupt request output, (active low)
6	DATA	DO	Received data output (FIFO not used)
	nFFS	DI	FIFO select input
7	DCLK	DO	Received data clock output (Digital filter used, FIFO not used)
	CFIL	AIO	External data filter capacitor connection (Analog filter used)
	FFIT	DO	FIFO IT (active high) FIFO empty function can be achieved when FIFO IT level is set to one
8	CLK	DO	Clock output for the microcontroller
9	XTL/REF	AIO	Crystal connection (other terminal of crystal to VSS) / External reference input
10	nRES	DO	Reset output (active low)
11	VSS_D	S	Digital VSS(connect to VSS)
12	VSS_A	S	Analog VSS(connect to VSS)
13	VSS_LN	S	LNA VSS(connect to VSS)
14	IN2	AI	RF differential signal input
15	IN1	AI	RF differential signal input

16	VDD_LN	S	Positive supply voltage
17	VDD _A	S	Analog VDD(connect to VDD)
18	VDD_D	S	Digital VDD(connect to VDD)
19	ARSSI	AO	Analog RSSI output
20	VDI	DO	Valid Data Indicator output

Typical Application



GENERAL DEVICE SPECIFICATION

All voltages are referenced to V_{ss}, the potential on the ground reference pin VSS.

Absolute Maximum Ratings (non-operating)

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	-0.5	6.0	V
V_{in}	Voltage on any pin	-0.5	V_{dd}+0.5	V
I_{in}	Input current into any pin except VDD and VSS	-25	25	mA
ESD	Electrostatic discharge with human body model		1000	V
T_{st}	Storage temperature	-55	125	℃

Recommended Operating Range

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	2.2	5.4	V
Top	Ambient operating temperature	-40	85	℃

ELECTRICAL SPECIFICATION

(Min/max values are valid over the whole recommended operating range, typ conditions: T_{op} = 27 ℃; V_{dd} = 2.7 V)

DC Characteristics

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
I_{dd}	Supply current	315 and 433 MHz bands 868 MHz band 915 MHz band		9 10.5 12	11 12.5 14	mA
I_{pd}	Standby current	All blocks disabled		0.3		µA
I_{lb}	Low battery voltage detector current consumption			0.5		µA
I_{wt}	Wake-up timer current consumption (Note 1)			1.5		µA
I_x	Idle current	Crystal oscillator and base-band parts are ON		3.0	3.5	mA
V_{lb}	Low battery detect threshold	Programmable in 0.1 V steps	2.2		5.3	V
V_{lba}	Low battery detection accuracy			75		mV
V_{il}	Digital input low level				$0.3*V_{dd}$	V
V_{ih}	Digital input high level		$0.7*V_{dd}$			V
I_{il}	Digital input current	V_{il} = 0 V	-1		1	µA
I_{ih}	Digital input current	$V_{ih} = V_{dd}$, V_{dd} = 5.4 V	-1		1	µA
V_{ol}	Digital output low level	I_{ol} = 2 mA			0.4	V
V_{oh}	Digital output high level	I_{oh} = -2 mA	V_{dd}-0.4			V

Note: Using the internal wake-up timer and counter reduces the overall current consumption, which should permit approximately 6 months operation from a 1500mAh battery.

AC Characteristics

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f_{LO}	Receiver frequency	315 MHz band, 2.5 kHz resolution	310.24		319.75	MHz
		433 MHz band, 2.5 kHz resolution	430.24		439.75	
		868 MHz band, 5.0 kHz resolution	860.48		879.51	
		915 MHz band, 7.5 kHz resolution	900.72		929.27	
BW	Receiver bandwidth	mode 0	60	67	75	kHz
		mode 1	120	134	150	
		mode 2	180	200	225	
		mode 3	240	270	300	
		mode 4	300	350	375	
		mode 5	360	400	450	
BR	FSK bit rate	With internal digital filters			115.2	kbps
BRA	FSK bit rate	With analog filter			256	kbps
P_{min}	Receiver Sensitivity	BER 10^{-3}, BW=67 kHz, BR=1.2 kbps (Note 1)		-109	-100	dBm
AFC_{range}	AFC locking range	δf_{FSK}: FSK deviation in the received signal		$0.8*\delta f_{FSK}$		
$IIP3_{inh}$	Input IP3	In band interferers in high bands		-21		dBm
$IIP3_{outh}$	Input IP3	Out of band interferers $f-f_{LO}$ > 4MHz		-18		dBm
$IIP3_{inl}$	IIP3 (LNA –6 dB gain)	In band interferers in low		-15		dBm

		bands				
$IIP3_{outl}$	IIP3 (LNA –6 dB gain)	Out of band interferers $f-f_{LO}$ > 4MHz		-12		dBm
CCR	Co-channel rejection	BER=10^{-2} with continuous wave interferer in the channel		-7		dB
ACS	Adjacent channel selectivity	BER=10^{-2} with continuous wave interferer in the adjacent channel, mode 0, channels at 134 kHz, BR=9.6 kbps, δf_{FSK}=30 kHz		23		dB
P_{max}	Maximum input power	LNA: high gain	0			dBm
R_{in}	RF input impedance real part (differential) (Note 2)	LNA gain (0, -14 dB) LNA gain (-6, -20 dB)		250 500		Ohm
C_{in}	RF input capacitance			1		pF
RS_a	RSSI accuracy			+/-5		dB
RSr	RSSI range			46		dB
C_{ARSSI}	Filter capacitance for ARSSI		1			nF
RS_{step}	RSSI programmable level steps			6		dB
RS_{resp}	DRSSI response time	Until the RSSI output goes high after the input signal exceeds the pre-programmed limit. CARRSI=5nF		500		µs

Note 1: See the BER diagrams in the measurement results section for detailed information.

Note 2: See matching circuit parameters and antenna design guide for information.

AC Characteristics (continued)

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f_{ref}	PLL reference frequency	(Note 3)	8	10	12	MHz
f_{res}	PLL frequency resolution	Depends on selected bands	2.5		7.5	kHz
t_{lock}	PLL lock time	Frequency error < 1kHz after 10 MHz step		20		us
$t_{st, P}$	PLL startup time	With running crystal oscillator			250	us
C_{xl}	Crystal load capacitance, see crystal selection guide	Programmable in 0.5 pF steps, tolerance +/-10%	8.5		16	pF
t_{POR}	Internal POR pulse width (Note4)	After V_{dd} has reached 90% of final value		50	100	ms
t_{sx}	Crystal oscillator startup time	Crystal ESR < 100 Ohms			5	ms
t_{PBt}	Wake-up timer clock period	Calibrated every 30 seconds	0.96		1.08	ms
$t_{wake-up}$	Programmable wake-up time		1		$5*10^{11}$	ms
$C_{in, D}$	Digital input capacitance				2	pF
$t_{r, f}$	Digital output rise/fall time	15 pF pure capacitive load			10	ns

Note 3: Using other than a 10 MHz crystal is not recommended because the crystal referred timing and frequency parameters will change accordingly.

Note 4: During this period, commands are not accepted by the chip.

CONTROL INTERFACE

Commands to the receiver are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. The number of bits sent is an integer multiple of 8. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g. bit 15 for a 16-bit command). Bits having no influence (don't care) are indicated with X. The Power On Reset (POR) circuit sets default values in all control registers.

The receiver will generate an interrupt request (IRQ) for the microcontroller on the following events:

- Supply voltage below the preprogrammed value is detected (LBD)
- Wake-up timer timeout (WK-UP)
- FIFO received the preprogrammed amount of bits (FFIT)
- FIFO overflow (FFOV)

FFIT and FFOV are applicable only when the FIFO is enabled. To find out why the nIRQ was issued, the status bits should be read out.

Timing Specification

Symbol	Parameter	Minimum Value [ns]
t_{CH}	Clock high time	25
t_{CL}	Clock low time	25
t_{SS}	Select setup time (nSEL falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nSEL rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{OD}	Data delay time	10

Timing Diagram