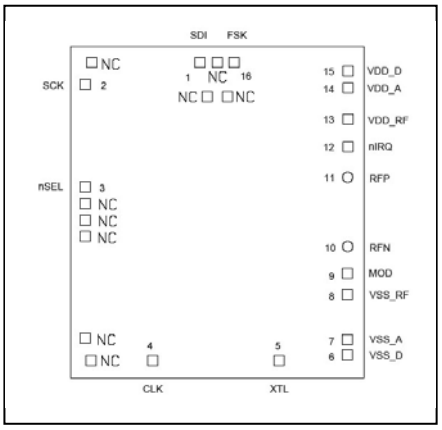
HC02 Universal ISM Band FSK Transmitter

DESCRIPTION

HC02



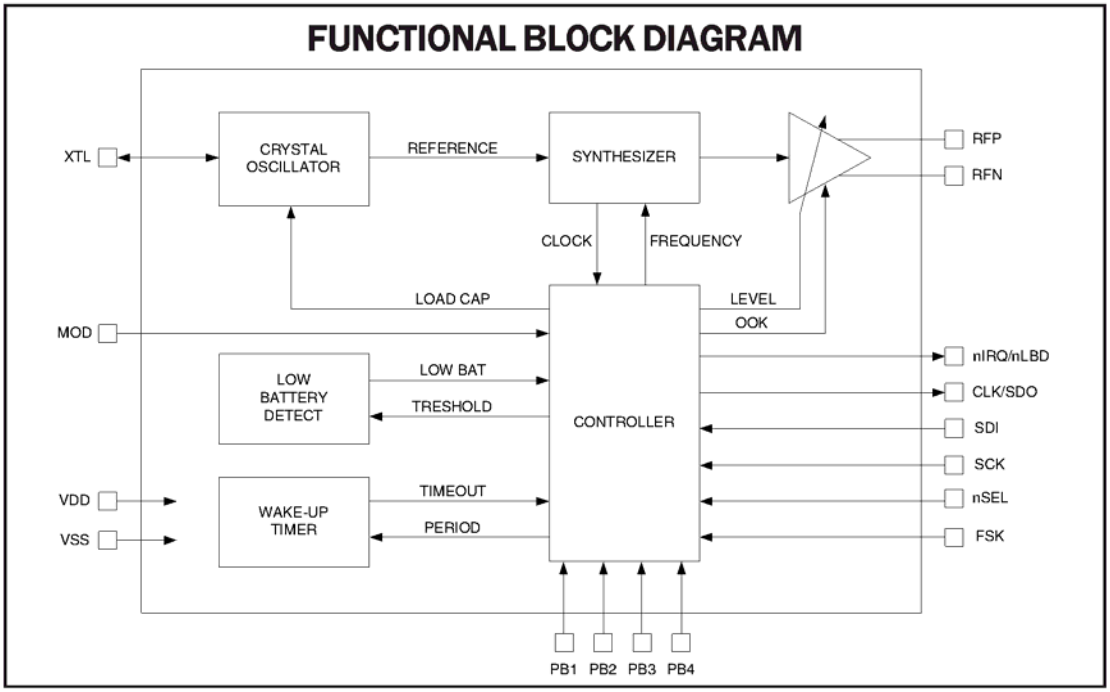
HC02 is a single chip, low power, multi-channel FSK transmitter designed for use in applications requiring FCC or ETSI conformance for unlicensed use in the 433, 868, and 915 MHz bands. Used in conjunction with HC01, HC's FSK receiver, the HC02 transmitter produces a flexible, low cost, and highly integrated solution that does not require production alignments. All required RF functions are integrated. Only an external crystal and bypass filtering are needed for operation. The HC02 offering a higher output power and an improved phase noise characteristic.

The HC02 features a completely integrated PLL for easy RF design, and its rapid settling time allows for fast frequency hopping, bypassing multipath fading and interference to achieve robust wireless links. In addition, highly stable and accurate FSK modulation is accomplished by direct closed-loop modulation with bit rates up to 115.2 kbps. The PLL's high resolution allows the use of multiple channels in any of the bands.

The integrated power amplifier of the transmitter has an open-collector differential output that directly drive a loop antenna with programmable output level. No additional matching network is required. An automatic antenna tuning circuit is built in to avoid costly trimming procedures and de-tuning due to the "hand effect".

For low-power applications, the device supports automatic activation from sleep mode. Active mode can be initiated by several wake-up events (on-chip timer timeout, low supply voltage detection).

FUNCTIONAL BLOCK DIAGRAM



FEATURES

- Fully integrated (low BOM, easy design-in)
- No alignment required in production
- Fast settling, programmable, high-resolution PLL
- Fast frequency hopping capability
- Stable and accurate FSK modulation with programmable deviation
- Programmable PLL loop bandwidth
- Direct loop antenna drive
- Automatic antenna tuning circuit
- Programmable output power level
- SPI bus for applications with microcontroller
- Clock output for microcontroller
- Integrated programmable crystal load capacitor
- Multiple event handling options for wake-up activation
- Wake-up timer
- Low battery detection
- 2.2V to 5.4V supply voltage
- Low power consumption
- Low standby current (0.3 μA)
- Transmit bit synchronization

TYPICAL APPLICATIONS

- Remote control
- Home security and alarm
- Wireless keyboard/mouse and other PC peripherals
- Toy control
- Remote keyless entry
- Tire pressure monitoring
- Telemetry
- Personal/patient data logging
- Remote automatic meter reading

DETAILED FEATURE-LEVEL DESCRIPTION

The HC02 FSK transmitter is designed to cover the unlicensed frequency bands at 433, 868, and 915 MHz. The device facilitates compliance with FCC and ETSI requirements.

PLL

The programmable PLL synthesizer determines the operating frequency, while preserving accuracy based on the on-chip crystal-controlled reference oscillator. The PLL's high resolution allows the usage of multiple channels in any of the bands. The FSK deviation is selectable (from 30 to 210 kHz with 30 kHz increments) to accommodate various bandwidth, data rate and crystal tolerance requirements, and it is also highly accurate due to the direct closed-loop modulation of the PLL. The transmitted digital data can be sent asynchronously through the FSK pin or over the control interface using the appropriate command.

HC Power Amplifier (PA)

The power amplifier has an open-collector differential output and can directly drive a loop antenna with a programmable output power level. An automatic antenna tuning circuit is built in to avoid costly trimming procedures and the so-called "hand effect."

Crystal Oscillator

The chip has a single-pin crystal oscillator circuit, which provides a 10 MHz reference signal for the PLL. To reduce external parts and simplify design, the crystal load capacitor is internal and programmable. Guidelines for selecting the appropriate crystal can be found later in this datasheet.

The transmitters can supply the clock signal for the microcontroller, so accurate timing is possible without the need for a second crystal. When the chip receives a Sleep Command from the microcontroller and turns itself off, it provides several further clock pulses ("clock tail") for the microcontroller to be able to go to idle or sleep mode. The length of the clock tail is programmable.

Low Battery Voltage Detector

The low battery voltage detector circuit monitors the supply voltage and generates an interrupt if it falls below a programmable threshold level.

Wake-Up Timer

The wake-up timer has very low current consumption (1.5 uA typical) and can be programmed from 1 ms to several days with an accuracy of ±5%.

It calibrates itself to the crystal oscillator at every startup, and then every 30 seconds. When the oscillator is switched off, the calibration circuit switches on the crystal oscillator only long enough for a quick calibration (a few milliseconds) to facilitate accurate wake-up timing.

Event Handling

In order to minimize current consumption, the device supports sleep mode. Active mode can be initiated by several wake-up events: timeout of wake-up timer, detection of low supply voltage or through the serial interface.

If any wake-up event occurs, the wake-up logic generates an interrupt, which can be used to wake

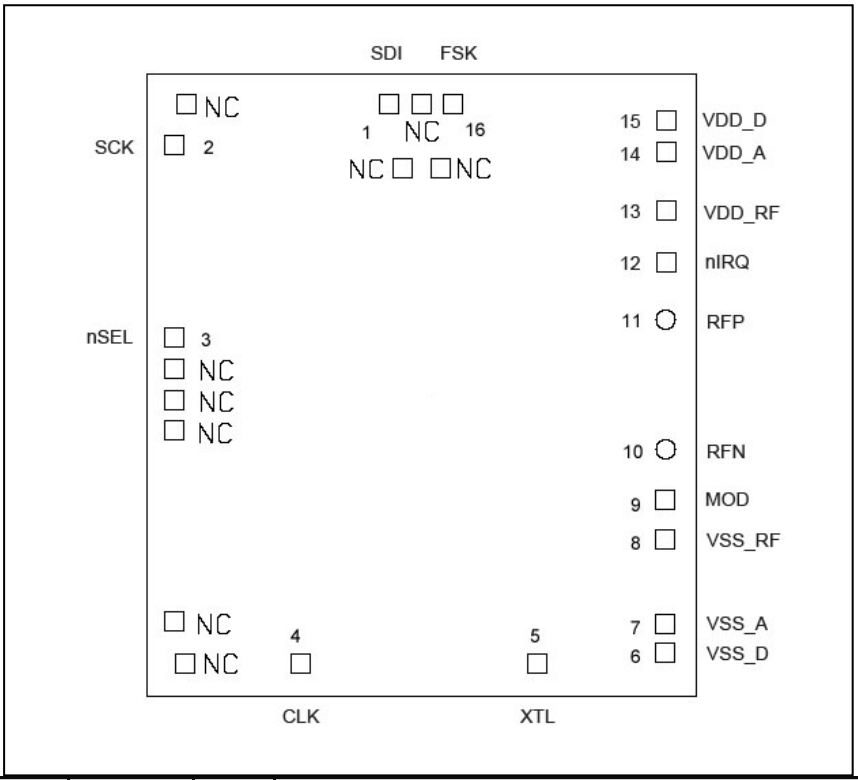
up the microcontroller, effectively reducing the period the microcontroller has to be active. The cause of the interrupt can be read out from the transmitters by the microcontroller through the nIRQ pin.

Interface

An SPI compatible serial interface lets the user select the operating frequency band and center frequency of the synthesizer, polarity and deviation of FSK modulation, and output power level. Division ratio for the microcontroller clock, wake-up timer period, and low battery detector threshold are also programmable. Any of these auxiliary functions can be disabled when not needed. All parameters are set to default after power-on; the programmed values are retained during sleep mode.

PACKAGE PIN DEFINITIONS

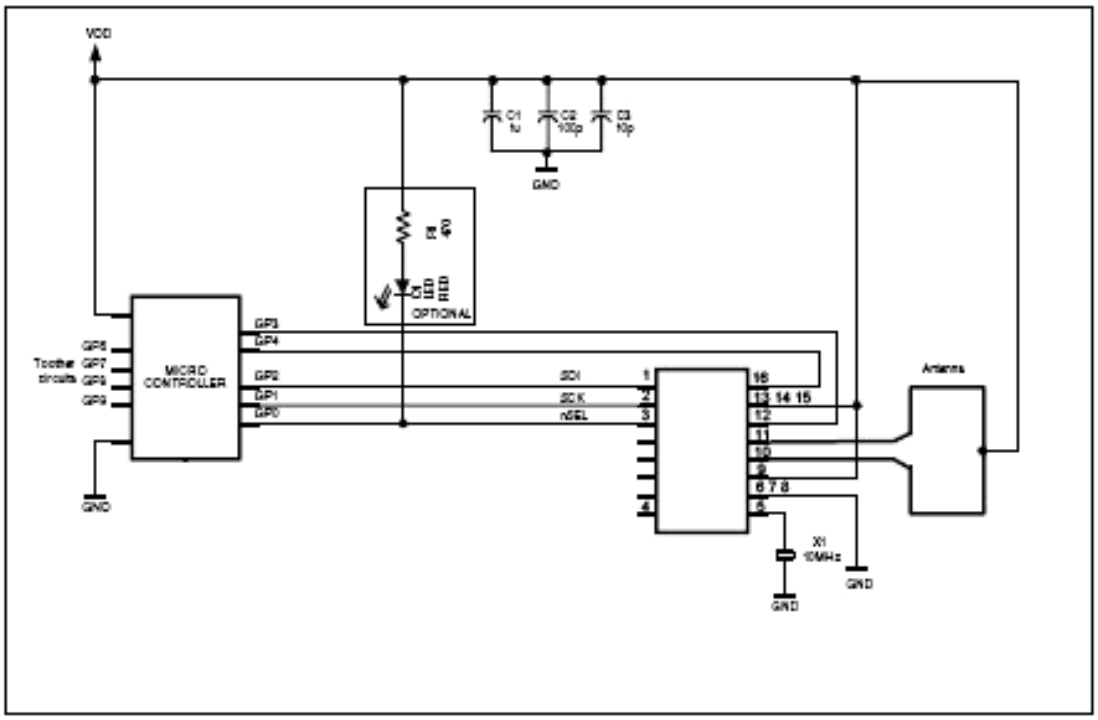
Pin type key: D=digital, A=analog, S=supply, I=input, O=output, IO=input/output



PinP	Name	Type	Function
1	SDI	DI	Data input of serial control interface
2	SCK	DI	Clock input of serial control interface
3	nSEL	DI	Chip select input of serial control interface (active low)
4	CLK	DO	Microcontroller clock (1 MHz-10 MHz)
5	XTL	AIO	Crystal connection (other terminal of crystal to VSS)
6	VSS_D	S	Digital VSS(Connect to VSS)
7	VSS_A	S	Analog VSS(Connect to VSS)
8	VSS_RF	S	RF VSS(Connect to VSS)

9	MOD	DI	Connect to logic high
10	RFN	AO	Power amplifier output (open collector)
11	RFP	AO	Power amplifier output (open collector)
12	nIRQ	DO	Interrupt request output for microcontroller (active low) and status read output
13	VDD_RF	S	RF VDD(Connect to VDD)
14	VDD_A	S	Analog VDD(Connect to VDD)
15	VDD_D	S	Digital VDD(Connect to VDD)
16	FSK	DI	Serial data input for FSK modulation

Typical application



GENERAL DEVICE SPECIFICATION

All voltages are referenced to V_{ss}, the potential on the ground reference pin VSS.

Absolute Maximum Ratings (non-operating)

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	-0.5	6.0	V
V_{in}	Voltage on any pin except open collector outputs	-0.5	V_{dd}+0.5	V
V_{oc}	Voltage on open collector outputs	-0.5	6.0	V
I_{in}	Input current into any pin except VDD and VSS	-25	25	mA
ESD	Electrostatic discharge with human body model		1000	V
T_{st}	Storage temperature	-55	125	℃

Recommended Operating Range

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	2.2	5.4	V
V_{oc}	Voltage on open collector outputs (Max 6.0 V)	V_{dd} - 1	V_{dd} + 1	V
T_{op}	Ambient operating temperature	-40	85	℃

ELECTRICAL SPECIFICATION

(Min/max values are valid over the whole recommended operating range, typ conditions:
T_{op} =27℃;V_{dd} =V_{oc}=2.7V)

DC Characteristics

Symbol	Parameter		Conditions/Notes	Min	Typ	Max	Units
$I_{dd\_TX\_0}$	Supply current (TX mode, Pout =0dBm)	433 MHz band 868 MHz band 915 MHz band	Active state with 0dBm output power		12 14 15		mA
$I_{dd\_TX\_PMAX}$	Supply current (TX mode, Pout =P_{max})	433 MHz band 868 MHz band 915 MHz band	Active state with maximum output power		21 23 24		mA
I_{pd}	Standby current in sleep mode (Note 1)		All blocks disabled		0.3		μA
I_{wt}	Wake-up timer current consumption				1.5		μA
I_{lb}	Low battery detector current consumption				0.5		μA
I_x	Idle current		Only crystal oscillator is on		1.5		mA

V_{lba}	Low battery detection accuracy			75		mV
V_{lb}	Low battery detector threshold	Programmable in 0.1 V steps	2.2		5.3	V
V_{il}	Digital input low level				$0.3*V_{dd}$	V
V_{ih}	Digital input high level		$0.7*V_{dd}$			V
I_{il}	Digital input current	V_{il} = 0 V	-1		1	µA
I_{ih}	Digital input current	$V_{ih} = V_{dd}$, V_{dd} = 5.4 V	-1		1	µA
V_{ol}	Digital output low level	I_{ol} = 2 mA			0.4	V
V_{oh}	Digital output high level	I_{oh} = -2 mA	V_{dd}-0.4			V

AC Characteristic

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f_{ref}	PLL reference frequency	Crystal operation mode is parallel (Note 2)	9	10	11	MHz
f_o		433MHz band, 2.5kHz resolution 868MHz band, 5.0kHz resolution 915MHz band, 7.5kHz resolution	430.24 860.48 900.72		439.75 879.51 929.27	MHz
t_{lock}	PLL lock time	Frequency error < 10 kHz after 10 MHz step, POR default PLL setting(Note 7)		20		µs
t_{sp}	PLL startup time	After turning on from idle mode, with crystal oscillator already stable, POR default PLL setting (Note 7)			250	µs
I_{OUT}	Open collector output current (Note 3)	At all bands	0.5		6	mA
P_{maxL}	Available output power (433MHz band)	With opt. antenna impedance (Note 4)		8		dBm
P_{maxH}	Available output power (868 and 915 MHz band)	With opt. antenna impedance (Note 4)		6		dBm
P_{out}	Typical output power	Selectable in 3 dB steps (Note 3)	P_{max}-21		P_{max}	dBm
P_{sp}	Spurious emission	At max power with loop antenna (Note 5)			-50	dBc

C_o	Output capacitance (set by the automatic antenna tuning circuit)	At low bands At high bands	1.5 1.6	2.3 2.2	2.8 3.1	pF
Q_o	Quality factor of the output capacitance		16	18	22	pF
L_{out}	Output phase noise	100 kHz from carrier 1 MHz from carrier (Note 7)		-85 -105		dBc/Hz
BR_{FSK}	FSK bit rate	(Note 7)			115.2	kbps
df_{fsk}	FSK frequency deviation	Programmable in 30 kHz steps	30		210	kHz
C_{xl}	Crystal load capacitance See Crystal Selection Guidelines	Programmable in 0.5 pF steps, tolerance +/-10%	8.5		16	pF
t_{POR}	Internal POR timeout (Note 6)	After V_{dd} has reached 90% of final value			50	ms
t_{sx}	Crystal oscillator startup time	Crystal ESR < 100 Ohms		1.5	5	ms
t_{PBt}	Wake-up timer clock period	Calibrated every 30 seconds	0.95		1.05	ms
$t_{wake-up}$	Programmable wake-up time		1		$5 *10^{11}$	ms
$C_{in, D}$	Digital input capacitance				2	pF
$t_{r, f}$	Digital output rise/fall time	15 pF pure capacitive load			10	ns

Note 1: Using a CR2032 battery (225 mAh capacity), the expected battery life is greater than 2 years using a 60-second wake-up period for sending 50 byte packets in length at 19.2 kbps with +6 dBm output power in the 915 MHz band.

Note 2: Using anything but a 10 MHz crystal is allowed but not recommended because all crystal-referred timing and frequency parameters will change accordingly.

Note 3: Adjustable in 8 steps.

Note 4: Optimal antenna admittance/impedance for the HC02:

	Yantenna [S]	Zantenna [Ohm]	Lantenna [nH]
434 MHz	1.3E-3 - j6.3E-3	31 + j152	58.00
868 MHz	1.35E-3 - j1.2E-2	9 + j82	15.20
915 MHz	1.45E-3 - j1.3E-2	8.7 + j77	13.60

Note 5: With selective resonant antennas .

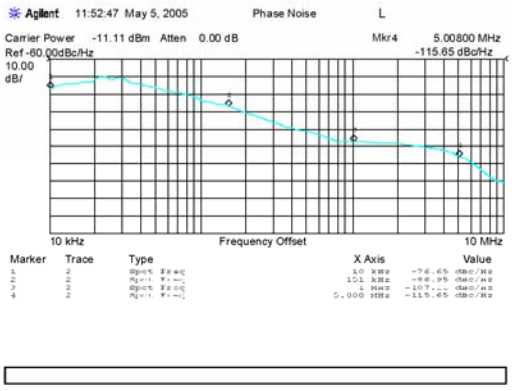
Note 6: During this period, no commands are accepted by the chip.

Note 7: The maximum FSK bitrate and the Output phase noise are dependent on the actual setting of the PLL Setting Command.

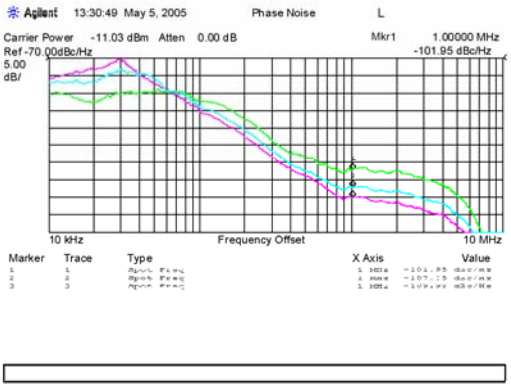
TYPICAL PERFORMANCE DATA (HC02)

Phase noise measurements in the 868 MHz ISM band

50% Charge pump current setting
(Ref. level: -60 dBc/Hz, 10 dB/div)



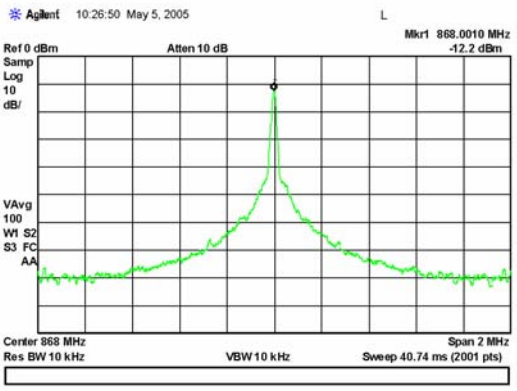
100, 50, 33% Charge pump current settings
(Ref. level: -70 dBc/Hz, 5 dB/div)



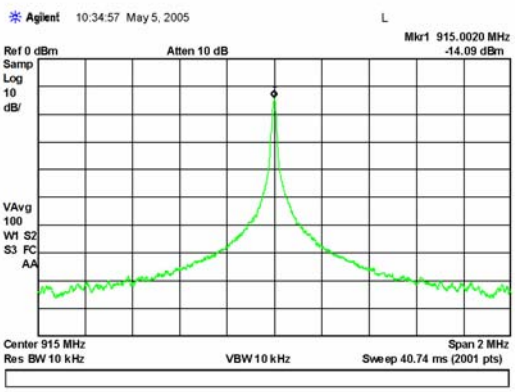
Unmodulated RF Spectrum

The output spectrum is measured at different frequencies. The output is loaded with 50 Ohms through a matching network.

At 868 MHz

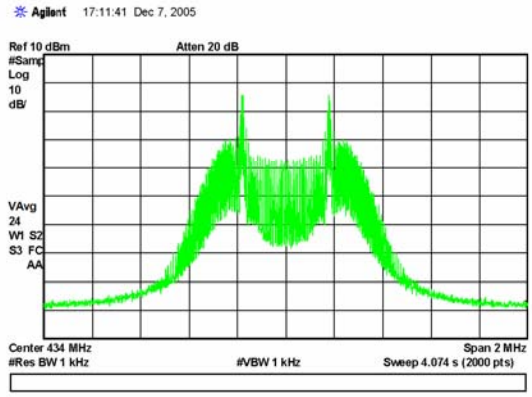


At 915 MHz

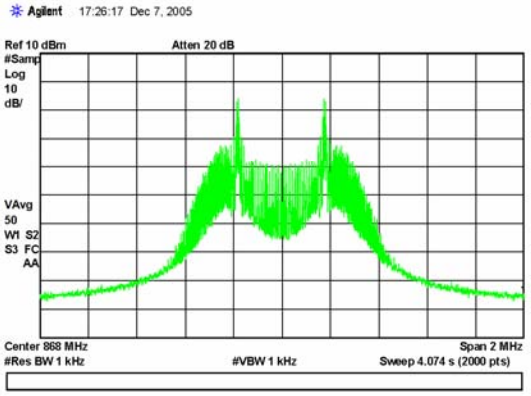


Modulated RF Spectrum

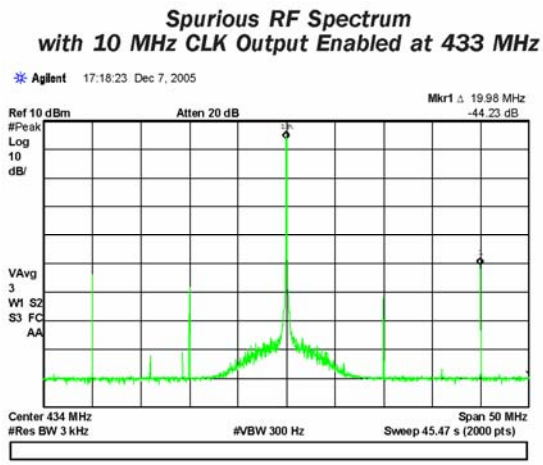
At 433 MHz with
180 kHz Deviation at 9.6 kbps

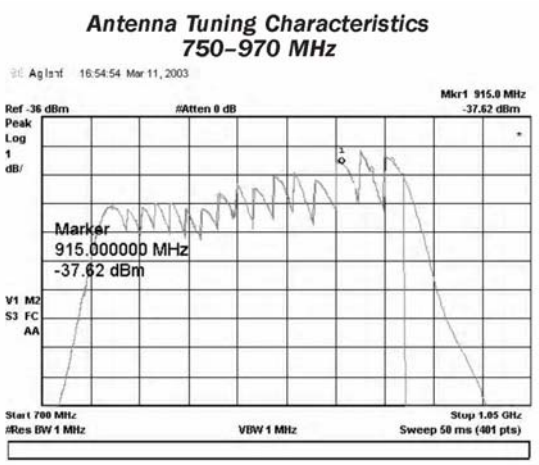


At 868 MHz with
180 kHz Deviation at 9.6 kbps



Other Important Characteristics





The antenna tuning characteristics was recorded in “max-hold” state of the spectrum analyzer. During the measurement, the transmitters were forced to change frequencies by forcing an external reference signal to the XTL pin. While the carrier was changing the antenna tuning circuit switched trough all the available states of the tuning circuit. The graph clearly demonstrates that while the complete output circuit had about a 40 MHz bandwidth, the tuning allows operating in a 220 MHz band. In other words the tuning circuit can compensate for 25% variation in the resonant frequency due to any process or manufacturing spread.

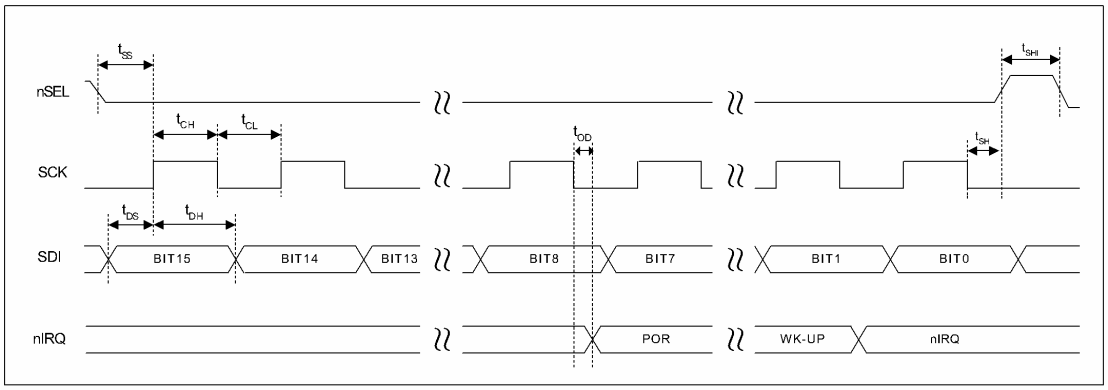
CONTROL INTERFACE

Commands to the transmitters are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. The number of bits sent is an integer multiple of 8. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g. bit 15 for a 16-bit command). Bits having no influence (don’t care) are indicated with X. The Power On Reset (POR) circuit sets default values in all control and command registers.

Timing Specification

Symbol	Parameter	Minimum Value [ns]
t_{CH}	Clock high time	25
t_{CL}	Clock low time	25
t_{SS}	Select setup time (nSEL falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nSEL rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{OD}	Data delay time	10

Timing Diagram

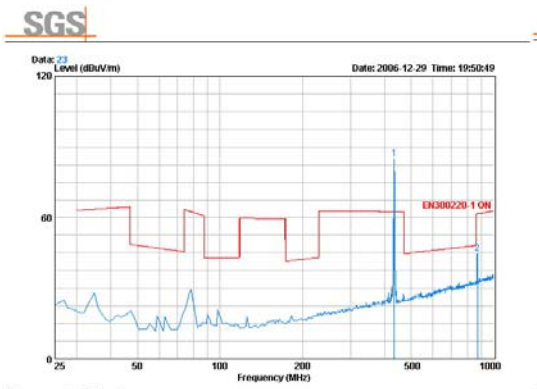


Control Commands

	Control Command	Related Parameters/Functions
1	Configuration Setting Command	Frequency band, microcontroller clock output, crystal load capacitance, frequency deviation
2	Power Management Command	Crystal oscillator, synthesizer, power amplifier, low battery detector, wake-up timer, clock output buffer
3	Frequency Setting Command	Carrier frequency
4	Data Rate Command	Bit rate
5	Power Setting Command	Nominal output power, OOK mode
6	Low Battery Detector Command	Low battery threshold limit
7	Sleep Command	Length of the clock tail after power down
8	Wake-Up Timer Command	Wake-up time period
9	Data Transmit Command	Data transmission
10	Status Register Command	Transmitter status read
11	PLL Setting Command	PLL bandwidth can be modified by this command

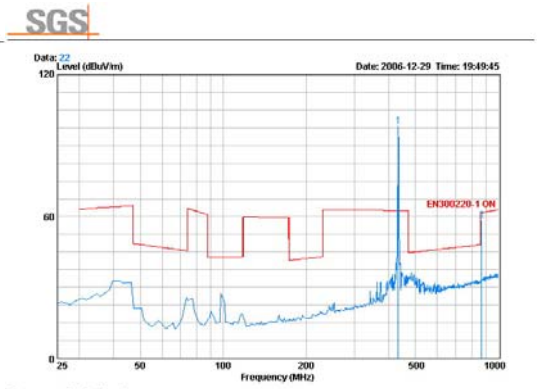
Note: In the following tables the POR column shows the default values of the command registers after power-on.

SGS Reports



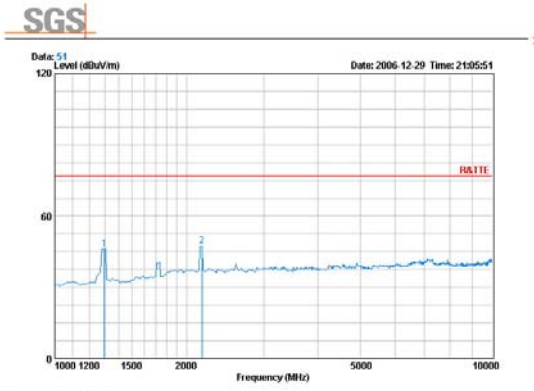
Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 HORIZONTAL
EUT : #A

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	432.550	2.34	16.56	27.52	93.56	84.94	62.55	22.39
2	672.275	3.50	22.93	26.57	44.93	44.80	61.61	-16.82



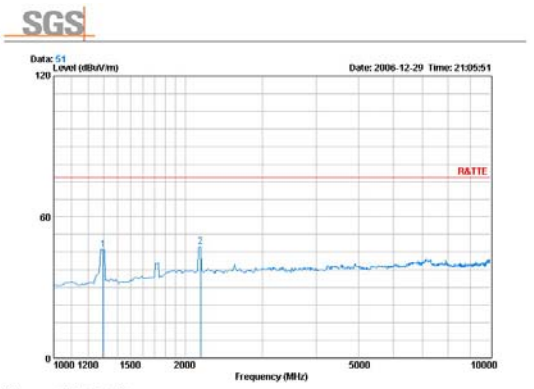
Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 VERTICAL
EUT : #A

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	432.550	2.34	16.56	27.52	106.57	97.95	62.55	35.41
2	868.375	3.48	22.85	26.58	58.53	58.28	61.57	-3.29



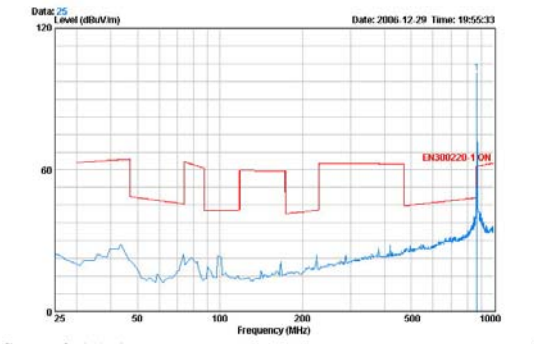
Site : 3m-chamber site
Condition : R&TTE 3m 3117 VERTICAL
EUT : #A

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1	1297.000	1.28	27.66	44.76	61.95	46.13	77.00	-30.87
2 @	2170.000	1.84	32.11	44.70	58.10	47.35	77.00	-29.65



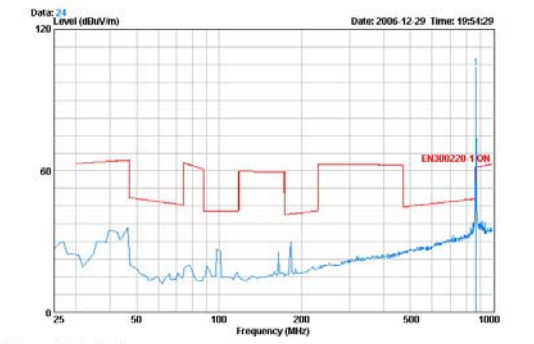
Site : 3m-chamber site
Condition : R&TTE 3m 3117 VERTICAL
EUT : #A

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1	1297.000	1.28	27.66	44.76	61.95	46.13	77.00	-30.87
2 @	2170.000	1.84	32.11	44.70	58.10	47.35	77.00	-29.65



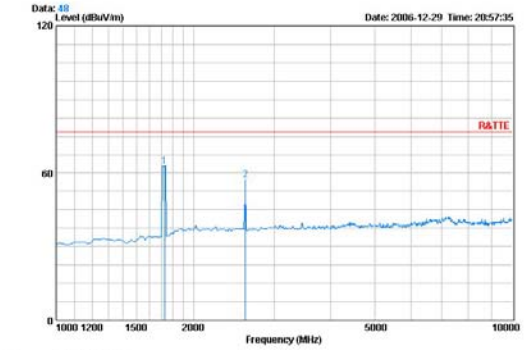
Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 HORIZONTAL
EUT : #C

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	868.375	3.48	22.85	26.58	101.34	101.08	61.57	39.51



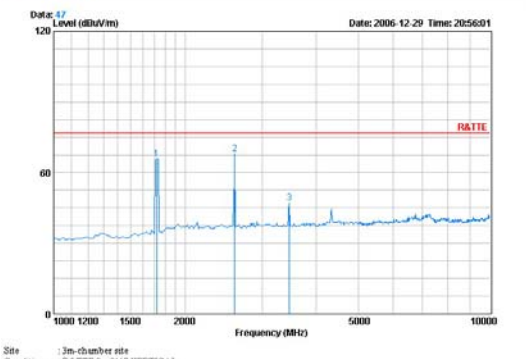
Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 VERTICAL
EUT : #C

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	868.375	3.48	22.85	26.58	103.75	103.49	61.57	41.92



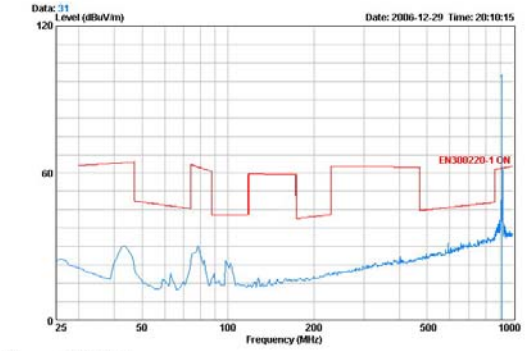
Site : 3m-chamber site
Condition : R&TTE 3m 3117 HORIZONTAL
EUT : #C

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	1729.000	1.59	29.86	44.70	76.11	62.86	77.00	-14.14
2	2602.000	2.04	32.54	44.80	67.38	57.16	77.00	-19.84



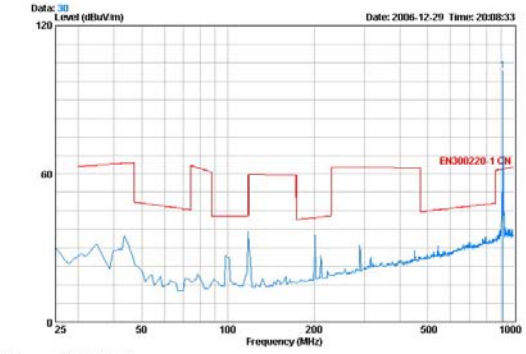
Site : 3m-chamber site
Condition : R&TTE 3m 3117 VERTICAL
EUT : #C

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1	1720.000	1.59	29.82	44.70	78.87	65.58	77.00	-11.42
2 @	2602.000	2.04	32.54	44.80	70.13	67.91	77.00	-9.09
3	3466.000	2.35	33.21	45.01	56.47	47.02	77.00	-29.98



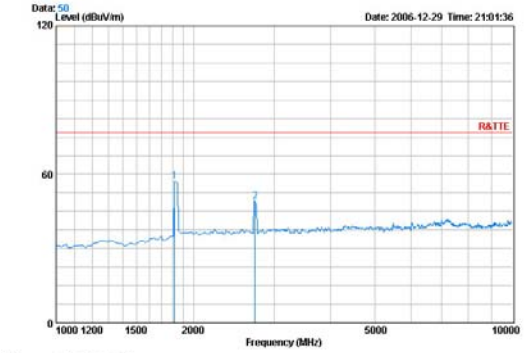
Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 HORIZONTAL
EUT : #E

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	914.200	3.62	23.26	26.43	95.64	96.09	62.05	34.04



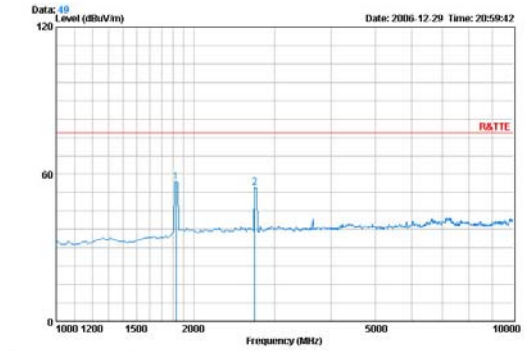
Site : 3m-chamber site
Condition : EN300220-1 ON 3m 0042673 VERTICAL
EUT : #E

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	914.200	3.62	23.26	26.43	101.18	101.63	62.05	39.57



Site : 3m-chamber site
Condition : R&TTE 3m 3117 HORIZONTAL
EUT : #E

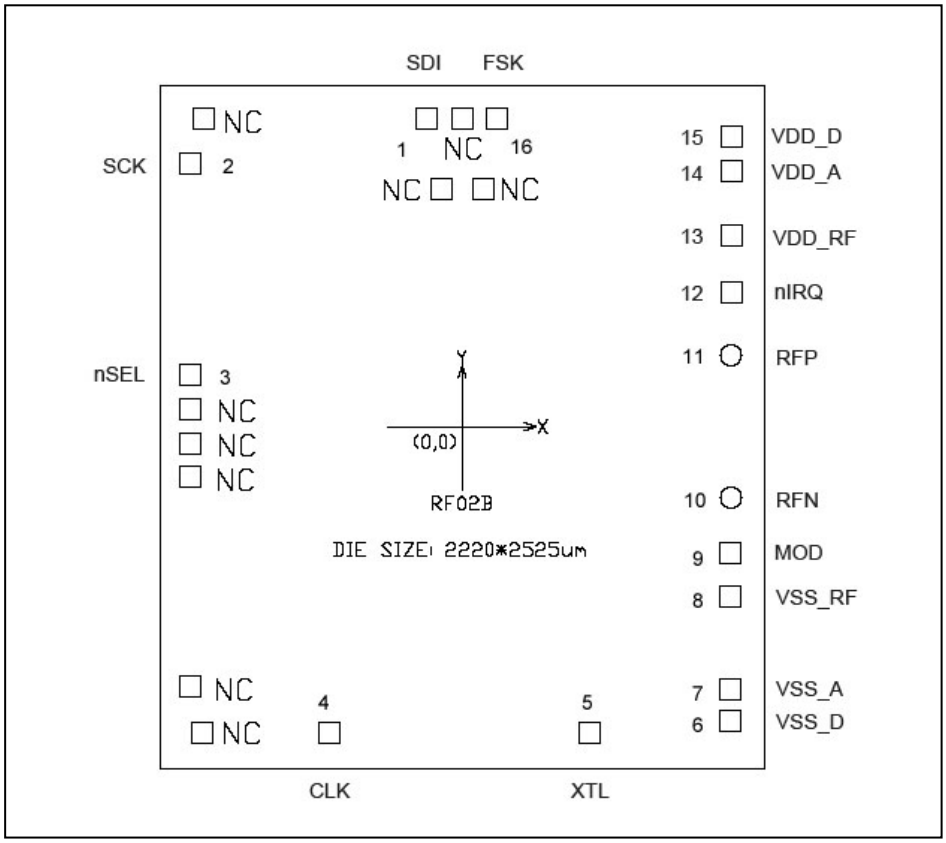
	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	1819.000	1.65	30.61	44.69	69.51	57.09	77.00	-19.91
2	2728.000	2.09	32.82	44.84	58.95	49.03	77.00	-27.97



Site : 3m-chamber site
Condition : R&TTE 3m 3117 VERTICAL
EUT : #E

	Freq	Cable Loss	Antenna Factor	Preamp Factor	Read Level	Level	Limit Line	Over Limit
	MHz	dB	dB/m	dB	dBuV	dBuV/m	dBuV/m	dB
1 @	1620.000	1.66	30.70	44.60	69.20	56.87	77.00	-20.13
2	2719.000	2.09	32.01	44.03	64.43	54.49	77.00	-22.51

HC02 BONDING DIAGRAM



Pad Opening: 85um square, except 76um octagon pads (AN1, AN2)

Die Size: 2220 X 2525 um